KS0718

81 COM / 104 SEG DRIVER & CONTROLLER FOR STN LCD

August. 1999.

Ver. 1.4

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KS0718 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Nov.1998
0.1	Modify syntax errors Append n-line inversion wave form to figure 11 on page 19. Modify figure 12 on page 20	Dec.1998
1.0	Change the number of COM/SEG (85COM / 100SEG -> 81COM / 104SEG) Modify PAD location	Mar.1999
1.1	Append PAD center coordinates to table 1, 2 on page 4, 5 Append referential instruction setup flow on page 48 to 51	Apr.1999
1.2	Change bumped PAD size (modify figure 2 and table 1 on page 3) Change the PAD Center Coordinates of COM39 and COMS1. (modify table 2 on page 4) Change LCD power supply voltage (modify V_{OUT} and V_0 voltage on page1, 52, 53, 54, 55)	May.1999
1.3	Modify Set partial display duty ratio (refer to page 32) Modify N-line Inversion Register “2 to 32” -> “3 to 33” (refer to page 41) Change Consumption Current “2mA” -> “2uA”, “10mA” -> “10uA” (refer to page 47) Add Partial Duty Changing “Waiting for Discharging the LCD Power Levels (refer to figure 39)	Jun.1999
1.4	Fix the TBD Value of DC/AC Characteristics.	Aug.1999

CONTENTS

INTRODUCTION

The KS0718 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 81 common and 104 segment driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 89 x 104 bits. It provides a highly flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

– 81 common outputs / 104 segment outputs

Applicable Duty Ratios

Programmable duty ratio	Applicable LCD bias	Maximum display area
1/9 to 1/81	1/4 to 1/11	81 × 104

– Various partial display
– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 89 x 104 = 9,256 bits
– Bit data "1": a dot of display is illuminated.
– Bit data "0": a dot of display is not illuminated.

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

On-chip Low Power Analog Circuit

– On-chip oscillator circuit
– Voltage converter (x3, x4, x5 or x6)
– Voltage regulator (temperature coefficient: -0.05%/°C or external input)
– On-chip electronic contrast control function (64 steps)
– Voltage follower (LCD bias: 1/4 to 1/11)

Operating Voltage Range

– Supply voltage (V_{DD}): 2.4 to 5.5 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low power Consumption

– 150 μA Max. (V_{DD} = 3V, x5 boosting, V0 = 12V, internal power supply on and display OFF)
– 15 μA Max. (during power save [standby] mode)

Package Type

– Gold bumped chip or TCP

BLOCK DIAGRAM

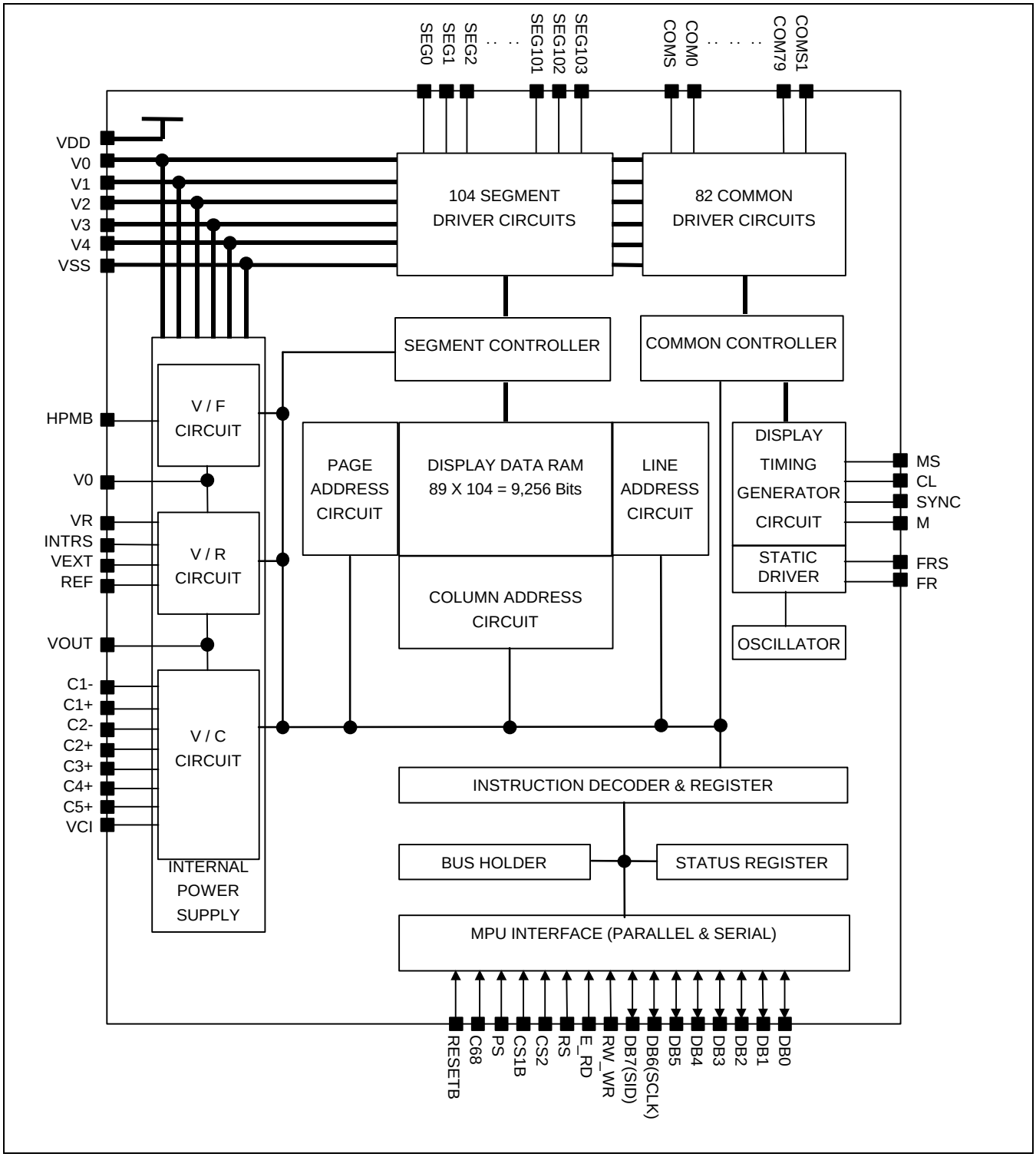


Figure 1. Block Diagram

PAD CONFIGURATION

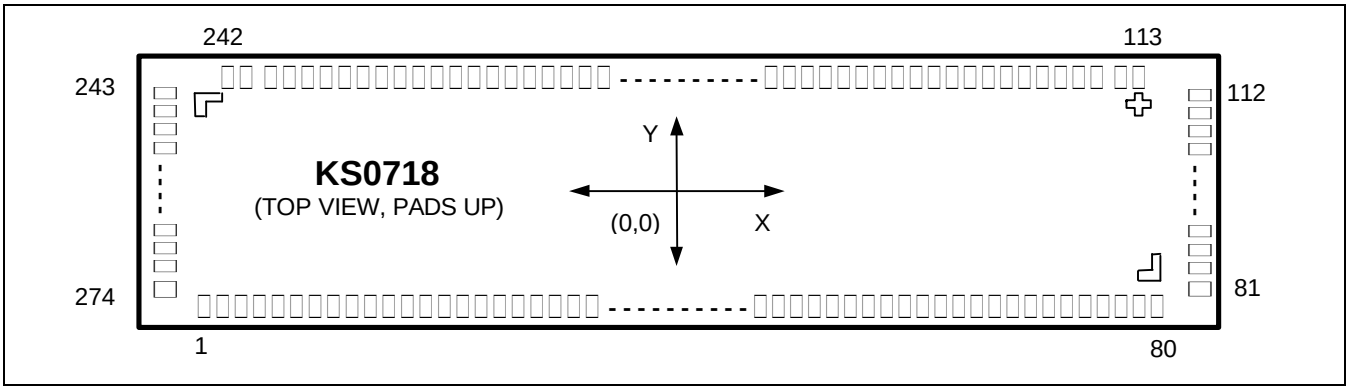
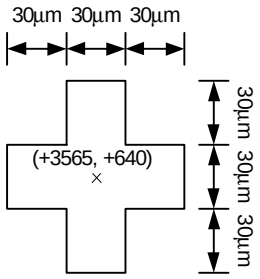


Figure 2. KS0718 Chip Configuration

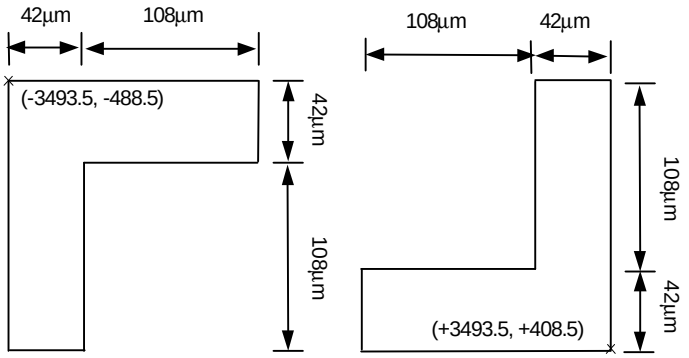
Table 1. KS0718 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	8350	2380	µm
Pad pitch	1 to 80	90		
	82 to 110	60		
	115 to 240			
	245 to 273			
	81	80		
	111 to 114			
	241 to 244			
	274			
Bumped pad size (Max.)	1 to 80	54	112	
	81	110	80	
	82 to 110	110	40	
	111 to 112	110	60	
	113 to 114	60	110	
	115 to 240	40	110	
	241 to 242	60	110	
	243 to 244	110	60	
	245 to 273	110	40	
	274	110	80	
Bumped pad height	All pad	14 (Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate



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PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	FRS	-3555	-1066	51	C3+	945	-1066	101	COM19	4028	190
2	FR	-3465	-1066	52	C3+	1035	-1066	102	COM18	4028	250
3	TEST1	-3375	-1066	53	C1-	1125	-1066	103	COM17	4028	310
4	TEST2	-3285	-1066	54	C1-	1215	-1066	104	COM16	4028	370
5	TEST3	-3195	-1066	55	C1+	1305	-1066	105	COM15	4028	430
6	CL	-3105	-1066	56	C1+	1395	-1066	106	COM14	4028	490
7	M	-3015	-1066	57	C2+	1485	-1066	107	COM13	4028	550
8	SYNC	-2925	-1066	58	C2+	1575	-1066	108	COM12	4028	610
9	VSS	-2835	-1066	59	C2-	1665	-1066	109	COM11	4028	670
10	HPMB	-2745	-1066	60	C2-	1755	-1066	110	COM10	4028	730
11	MS	-2655	-1066	61	C4+	1845	-1066	111	DUMMY	4028	810
12	VDD	-2565	-1066	62	C4+	1935	-1066	112	DUMMY	4028	890
13	PS	-2475	-1066	63	VSS	2025	-1066	113	DUMMY	3910	1043
14	C68	-2385	-1066	64	REF	2115	-1066	114	DUMMY	3830	1043
15	VSS	-2295	-1066	65	VEXT	2205	-1066	115	COM9	3750	1043
16	CS1B	-2205	-1066	66	VDD	2295	-1066	116	COM8	3690	1043
17	CS2	-2115	-1066	67	INTRS	2385	-1066	117	COM7	3630	1043
18	VDD	-2025	-1066	68	VSS	2475	-1066	118	COM6	3570	1043
19	RESETB	-1935	-1066	69	V4	2565	-1066	119	COM5	3510	1043
20	RS	-1845	-1066	70	V4	2655	-1066	120	COM4	3450	1043
21	VSS	-1755	-1066	71	V3	2745	-1066	121	COM3	3390	1043
22	RW_WR	-1665	-1066	72	V3	2835	-1066	122	COM2	3330	1043
23	E_RD	-1575	-1066	73	V2	2925	-1066	123	COM1	3270	1043
24	VDD	-1485	-1066	74	V2	3015	-1066	124	COM0	3210	1043
25	DB0	-1395	-1066	75	V1	3105	-1066	125	COMS	3150	1043
26	DB1	-1305	-1066	76	V1	3195	-1066	126	SEG0	3090	1043
27	DB2	-1215	-1066	77	V0	3285	-1066	127	SEG1	3030	1043
28	DB3	-1125	-1066	78	V0	3375	-1066	128	SEG2	2970	1043
29	DB4	-1035	-1066	79	VR	3465	-1066	129	SEG3	2910	1043
30	DB5	-945	-1066	80	VR	3555	-1066	130	SEG4	2850	1043
31	DB6	-855	-1066	81	COM39	4028	-1030	131	SEG5	2790	1043
32	DB7	-765	-1066	82	COM38	4028	-950	132	SEG6	2730	1043
33	VDD	-675	-1066	83	COM37	4028	-890	133	SEG7	2670	1043
34	VDD	-585	-1066	84	COM36	4028	-830	134	SEG8	2610	1043
35	VDD	-495	-1066	85	COM35	4028	-770	135	SEG9	2550	1043
36	VDD	-405	-1066	86	COM34	4028	-710	136	SEG10	2490	1043
37	VDD	-315	-1066	87	COM33	4028	-650	137	SEG11	2430	1043
38	VCI	-225	-1066	88	COM32	4028	-590	138	SEG12	2370	1043
39	VCI	-135	-1066	89	COM31	4028	-530	139	SEG13	2310	1043
40	VSS	-45	-1066	90	COM30	4028	-470	140	SEG14	2250	1043
41	VSS	45	-1066	91	COM29	4028	-410	141	SEG15	2190	1043
42	VSS	135	-1066	92	COM28	4028	-350	142	SEG16	2130	1043
43	VSS	225	-1066	93	COM27	4028	-290	143	SEG17	2070	1043
44	VSS	315	-1066	94	COM26	4028	-230	144	SEG18	2010	1043
45	VOUT	405	-1066	95	COM25	4028	-170	145	SEG19	1950	1043
46	VOUT	495	-1066	96	COM24	4028	-110	146	SEG20	1890	1043
47	VOUT	585	-1066	97	COM23	4028	-50	147	SEG21	1830	1043
48	VOUT	675	-1066	98	COM22	4028	10	148	SEG22	1770	1043
49	C5+	765	-1066	99	COM21	4028	70	149	SEG23	1710	1043
50	C5+	855	-1066	100	COM20	4028	130	150	SEG24	1650	1043

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
151	SEG25	1590	1043	201	SEG75	-1410	1043	251	COM57	-4028	370
152	SEG26	1530	1043	202	SEG76	-1470	1043	252	COM58	-4028	310
153	SEG27	1470	1043	203	SEG77	-1530	1043	253	COM59	-4028	250
154	SEG28	1410	1043	204	SEG78	-1590	1043	254	COM60	-4028	190
155	SEG29	1350	1043	205	SEG79	-1650	1043	255	COM61	-4028	130
156	SEG30	1290	1043	206	SEG80	-1710	1043	256	COM62	-4028	70
157	SEG31	1230	1043	207	SEG81	-1770	1043	257	COM63	-4028	10
158	SEG32	1170	1043	208	SEG82	-1830	1043	258	COM64	-4028	-50
159	SEG33	1110	1043	209	SEG83	-1890	1043	259	COM65	-4028	-110
160	SEG34	1050	1043	210	SEG84	-1950	1043	260	COM66	-4028	-170
161	SEG35	990	1043	211	SEG85	-2010	1043	261	COM67	-4028	-230
162	SEG36	930	1043	212	SEG86	-2070	1043	262	COM68	-4028	-290
163	SEG37	870	1043	213	SEG87	-2130	1043	263	COM69	-4028	-350
164	SEG38	810	1043	214	SEG88	-2190	1043	264	COM70	-4028	-410
165	SEG39	750	1043	215	SEG89	-2250	1043	265	COM71	-4028	-470
166	SEG40	690	1043	216	SEG90	-2310	1043	266	COM72	-4028	-530
167	SEG41	630	1043	217	SEG91	-2370	1043	267	COM73	-4028	-590
168	SEG42	570	1043	218	SEG92	-2430	1043	268	COM74	-4028	-650
169	SEG43	510	1043	219	SEG93	-2490	1043	269	COM75	-4028	-710
170	SEG44	450	1043	220	SEG94	-2550	1043	270	COM76	-4028	-770
171	SEG45	390	1043	221	SEG95	-2610	1043	271	COM77	-4028	-830
172	SEG46	330	1043	222	SEG96	-2670	1043	272	COM78	-4028	-890
173	SEG47	270	1043	223	SEG97	-2730	1043	273	COM79	-4028	-950
174	SEG48	210	1043	224	SEG98	-2790	1043	274	COMS1	-4028	-1030
175	SEG49	150	1043	225	SEG99	-2850	1043				
176	SEG50	90	1043	226	SEG100	-2910	1043				
177	SEG51	30	1043	227	SEG101	-2970	1043				
178	SEG52	-30	1043	228	SEG102	-3030	1043				
179	SEG53	-90	1043	229	SEG103	-3090	1043				
180	SEG54	-150	1043	230	COM40	-3150	1043				
181	SEG55	-210	1043	231	COM41	-3210	1043				
182	SEG56	-270	1043	232	COM42	-3270	1043				
183	SEG57	-330	1043	233	COM43	-3330	1043				
184	SEG58	-390	1043	234	COM44	-3390	1043				
185	SEG59	-450	1043	235	COM45	-3450	1043				
186	SEG60	-510	1043	236	COM46	-3510	1043				
187	SEG61	-570	1043	237	COM47	-3570	1043				
188	SEG62	-630	1043	238	COM48	-3630	1043				
189	SEG63	-690	1043	239	COM49	-3690	1043				
190	SEG64	-750	1043	240	COM50	-3750	1043				
191	SEG65	-810	1043	241	DUMMY	-3830	1043				
192	SEG66	-870	1043	242	DUMMY	-3910	1043				
193	SEG67	-930	1043	243	DUMMY	-4028	890				
194	SEG68	-990	1043	244	DUMMY	-4028	810				
195	SEG69	-1050	1043	245	COM51	-4028	730				
196	SEG70	-1110	1043	246	COM52	-4028	670				
197	SEG71	-1170	1043	247	COM53	-4028	610				
198	SEG72	-1230	1043	248	COM54	-4028	550				
199	SEG73	-1290	1043	249	COM55	-4028	490				
200	SEG74	-1350	1043	250	COM56	-4028	430				

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PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="5">Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td colspan="5">Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td colspan="5">Ground</td></tr>
<tr><td rowspan="4">V0
V1
V2
V3
V4</td><td rowspan="4">I/O</td><td colspan="5">LCD driver supplies voltages
The voltage determined by LCD pixel is impedance converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</td></tr>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
<tr><td colspan="5">NOTE: N = 4 to 11</td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pins

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
C4+	O	Capacitor 4 positive connection pin for voltage converter
C5+	O	Capacitor 5 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin
VCI	I	Voltage converter input voltage pin Voltages should have the following relationship: VDD ≤ VCI ≤ V0
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = "L")
REF	I	Selects the external VREF voltage via VEXT pin – REF = "L": using the external VREF – REF = "H": using the internal VREF
VEXT	I	Externally input reference voltage (VREF) for the internal voltage regulator It is valid only when REF is "L".

SYSTEM CONTROL

Table 5. System Control Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>Master / slave operations select pin
– MS = "H": master operation
– MS = "L": slave operation
The following table depends on the MS status.
<table>
<tr><td rowspan="2">MS</td><td colspan="2">Internal analog circuits</td><td colspan="3">Display timing signals</td></tr>
<tr><td>Oscillator</td><td>Power supply</td><td>CL</td><td>SYNC</td><td>M</td></tr>
<tr><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the KS0718 is used in master/slave mode (Multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Display sync input / output pin
When the KS0718 is used in master/slave mode (Multi-chip), the SYNC pins must be connected each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signals input / output pin
When the KS0718 is used in master/slave mode (Multi-chip), the M pins must be connected each other.</td></tr>
<tr><td>FR</td><td>O</td><td>Static driver common output pin
This pin is used together with the FRS pin.</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the FR pin.</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistors select pin
This pin selects the resistors for adjusting V0 voltage level.
– INTRS = "H": use the internal resistors
– INTRS = "L": use the external resistors
VR pin and external resistive divider control V0 voltage.</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power control pin of the power supplies circuit for LCD driver
– HPMB = "L": high power mode
– HPMB = "H": normal mode
This pin is valid in master operation.</td></tr>
<tr><td>TEST1
to
TEST3</td><td>I</td><td>Test pins
Don’t use these pins.</td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset the input pin
When RESETB is "L", initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td>Parallel/Serial data input select input
<table>
<tr><td>PS</td><td>Interface Mode</td><td>Data/ Instruction</td><td>Data</td><td>Read / Write</td><td>Serial Clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>RS</td><td>SID(DB7)</td><td>Write only</td><td>SCLK(DB6)</td></tr>
</table>
</td></tr>
<tr><td>*NOTE: When PS is "L", DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either "H" or "L".</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor interface select input pin
– C68 = "H": 6800-series MPU interface
– C68 = "L": 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="4">RW_WR</td><td rowspan="4">I</td><td>Read / Write execution control pin
<table>
<tr><td>C68</td><td>MPU Type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read/Write control input pin
– RW = "H": read
– RW = "L": write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table>
</td></tr>
<tr><td></td></tr>
</table>

Table 6 (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
– RW = "H": When E is "H", DB0 to DB7 are in an output status.
– RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is "L", DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 7. LCD Driver Outputs Pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG103</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM79</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">Vss</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS
(COMS1)</td><td>O</td><td colspan="4">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

NOTE: **DUMMY – These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The KS0718 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

KS0718 has three types of interface with an MPU, which are one serial and two parallel interface. This parallel or serial interface is determined by PS pin as shown in table 8

Table 8. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*×: Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in Table 9. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in table 10.

Table 9. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS = "L")

When the KS0718 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

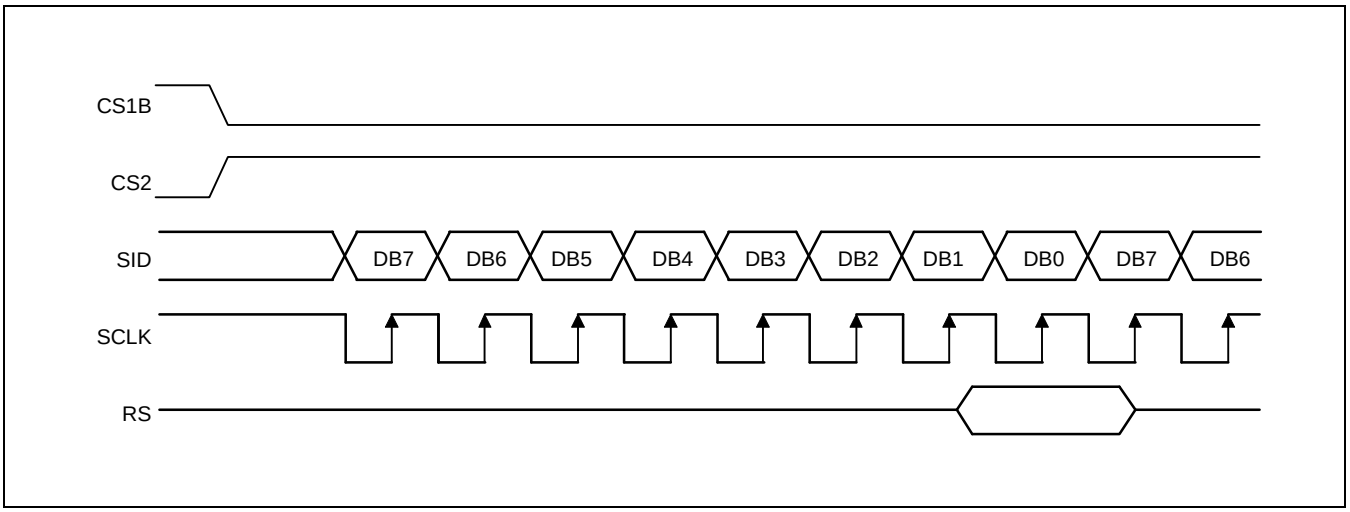

Figure 3. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the KS0718 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The KS0718 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

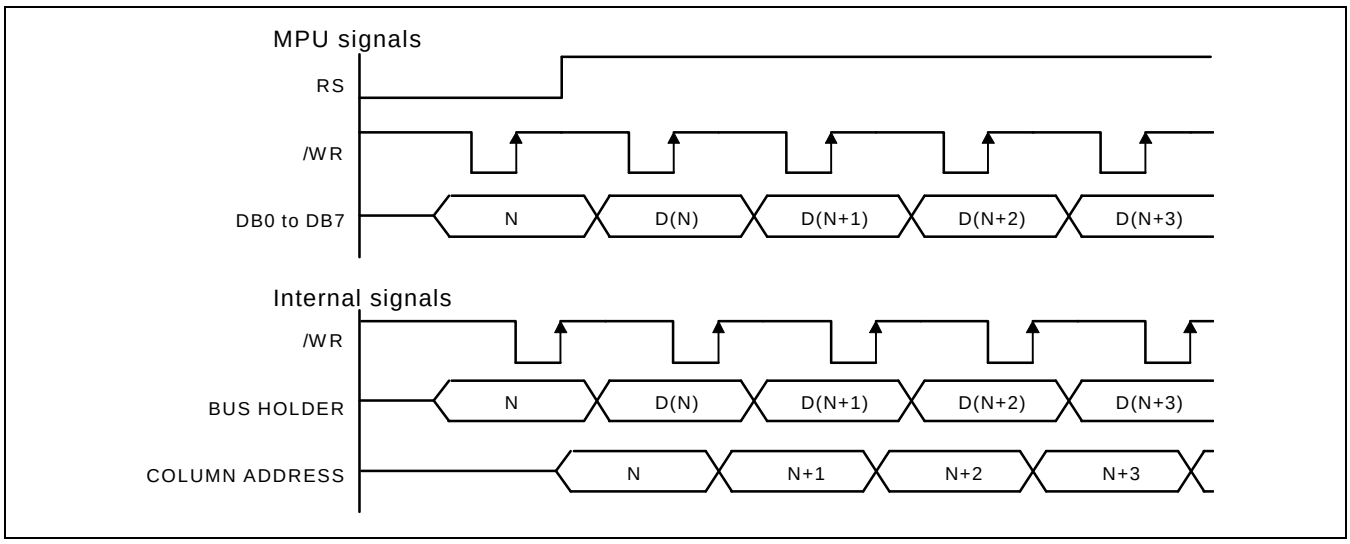

Figure 4. Write Timing

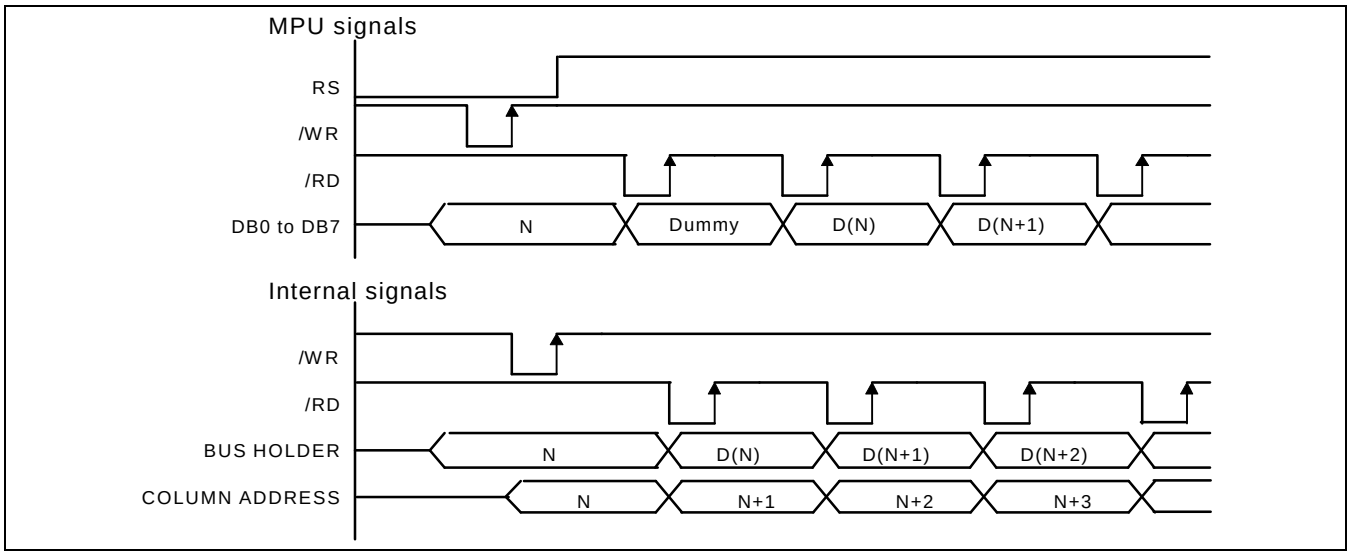

Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 89-row by 104-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 89 rows are divided into 11 pages of 8 lines and the 12th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

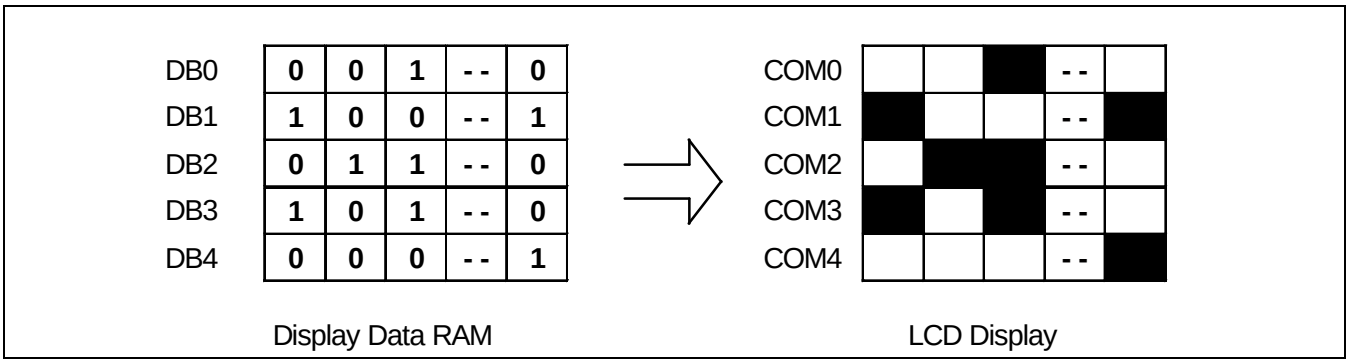

Figure 6. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 11 (DB3, DB1 and DB0 are "H", DB2 is "L") is a special RAM area for the icons and display data DB0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8 & figure 9. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 104-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column address circuit has a 7-bit preset counter that provides column address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 7-bit [Y6:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not incremented and locked if a non-existing address above 67H. It is unlocked if a Column Address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC Select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following figure 7.

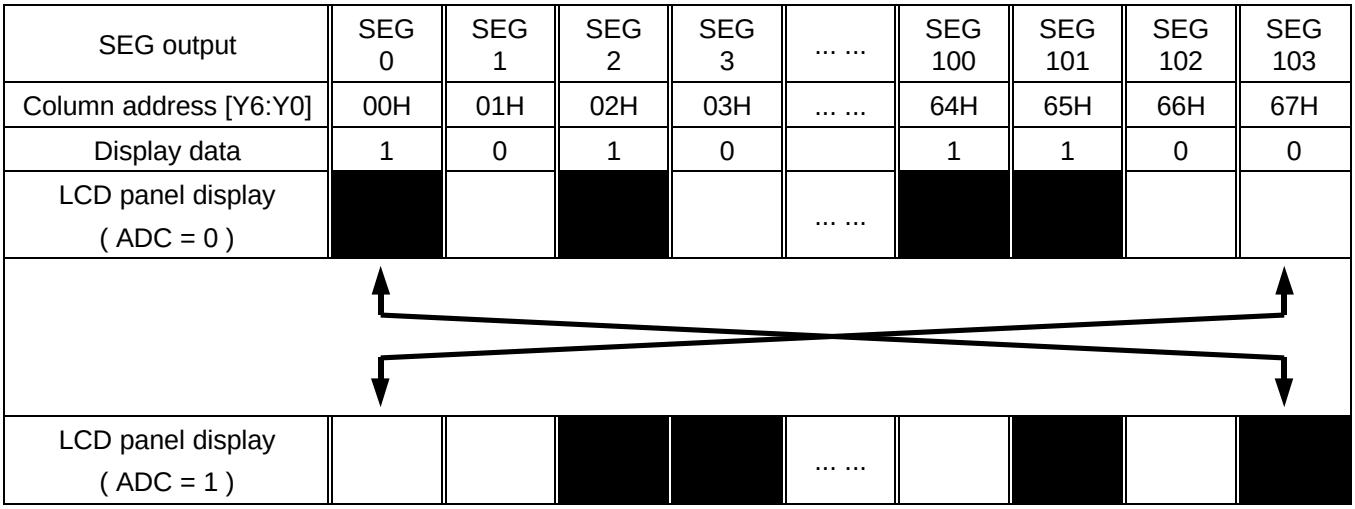

Figure 7. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the Display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

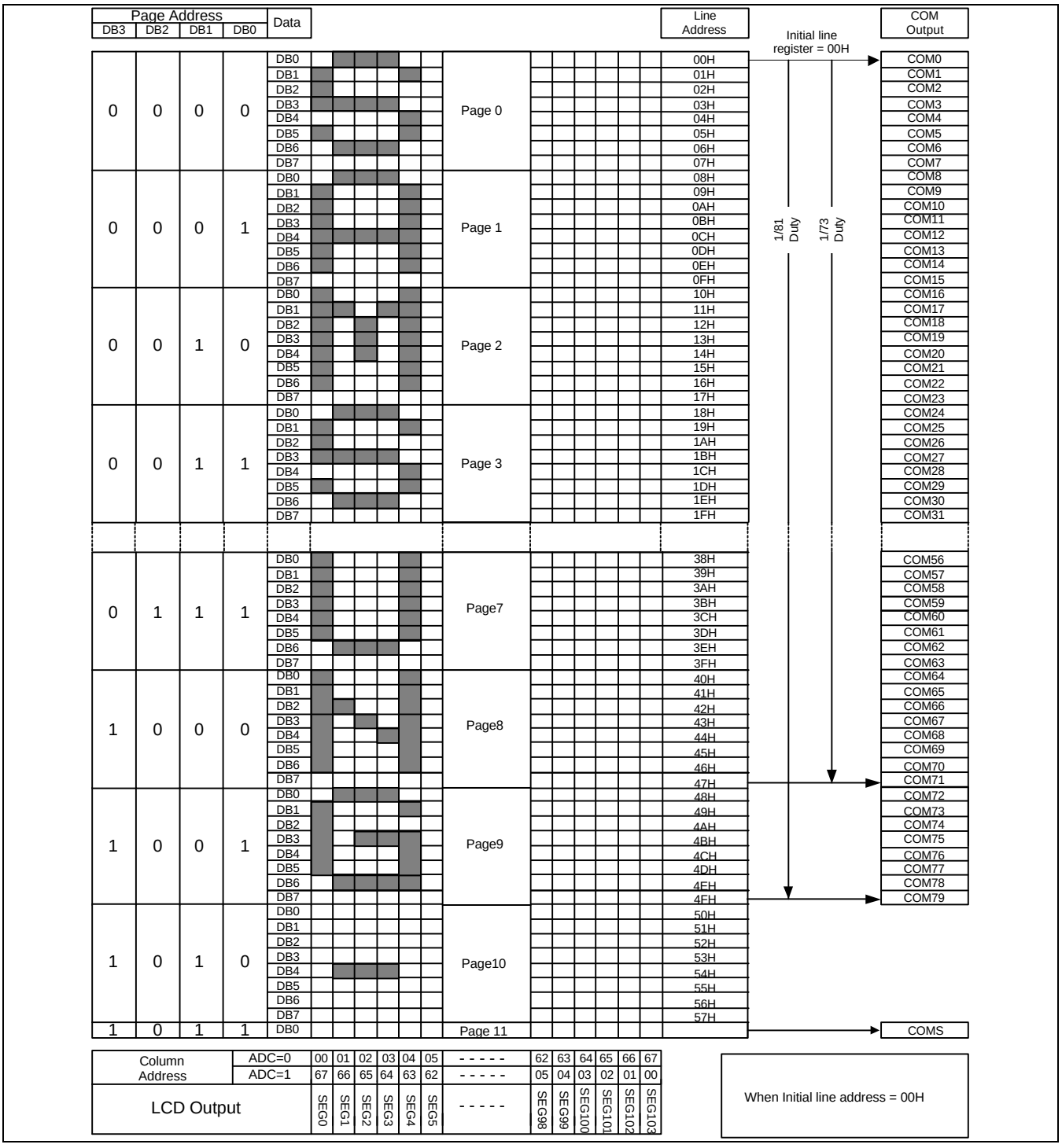

Figure 8. Display Data RAM Map (Initial Line Address = 00H)

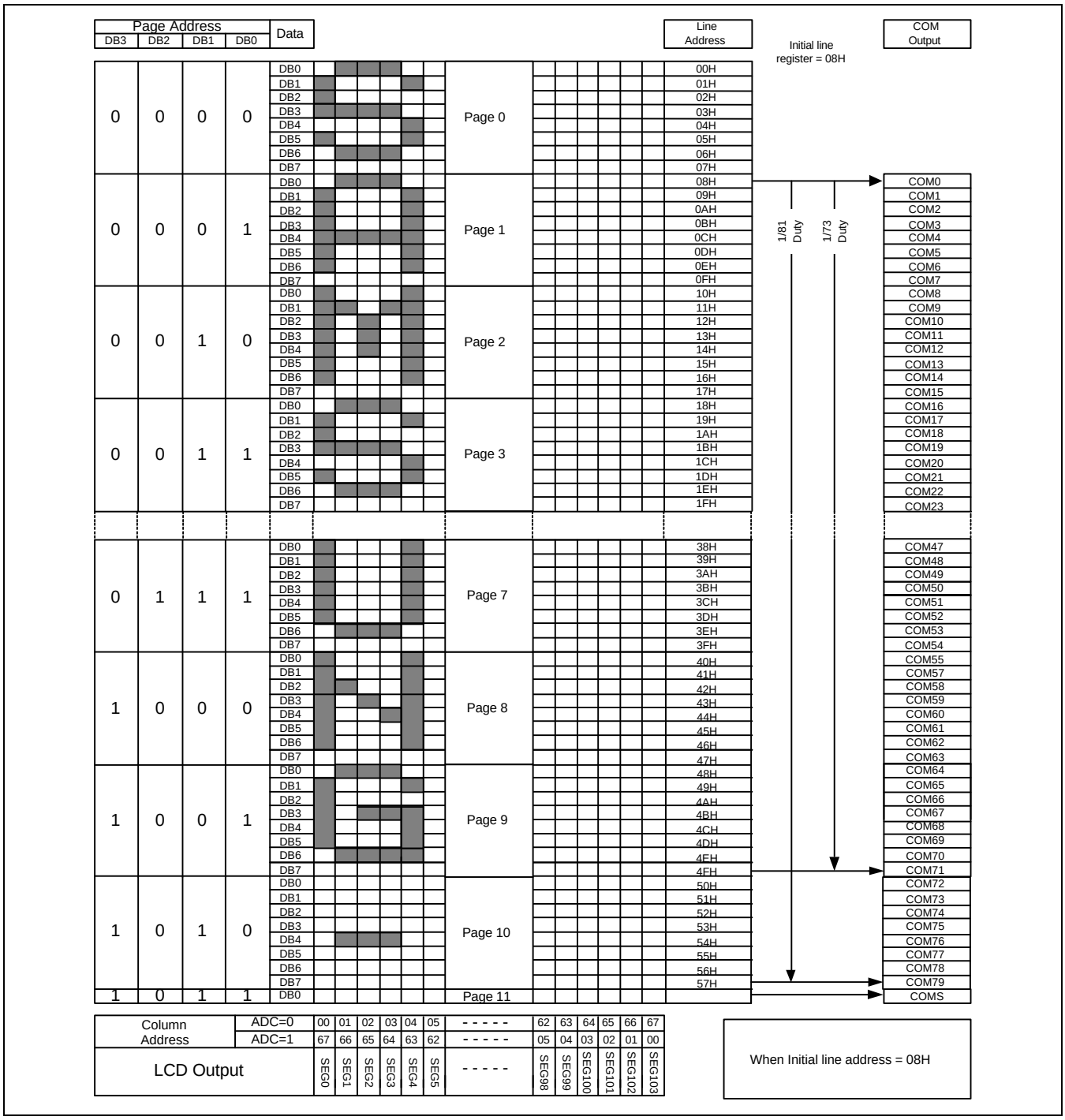

Figure 9. Display Data RAM Map (Initial Line Address = 08H)

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip Oscillator and its frequency is nearly independent of V_{DD}. This Oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the display data latch circuit latches the 104-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in figure 10.

In a multiple chip configuration, the slave chip requires the CL, M and SYNC signals from the master. Table 11 shows the CL, SYNC, and M status.

Table 11. Master and Slave Timing Signal Status

Operation mode	Oscillator	CL	SYNC	M
Master	ON (internal clock used)	Output	Output	Output
Slave	OFF (external clock used)	Input	Input	Input

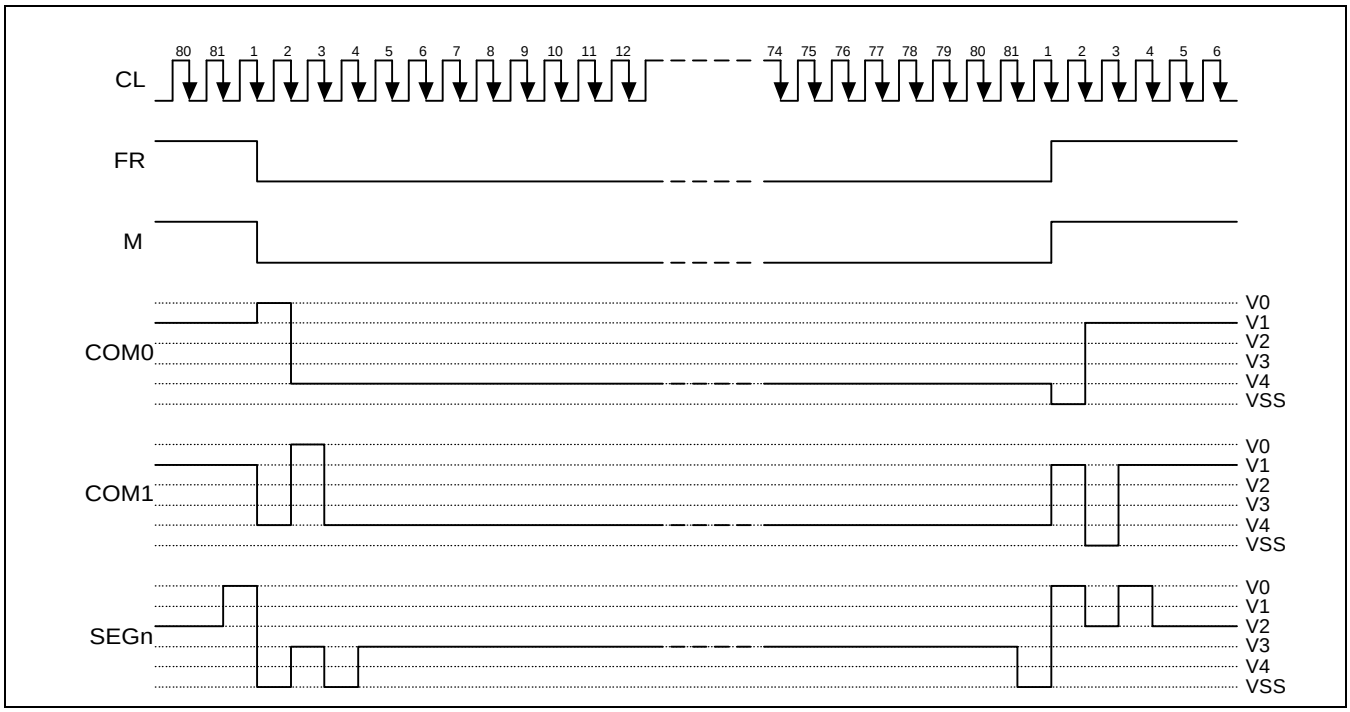

Figure 10. 2-frame AC Driving Waveform (Duty Ratio = 1/81)

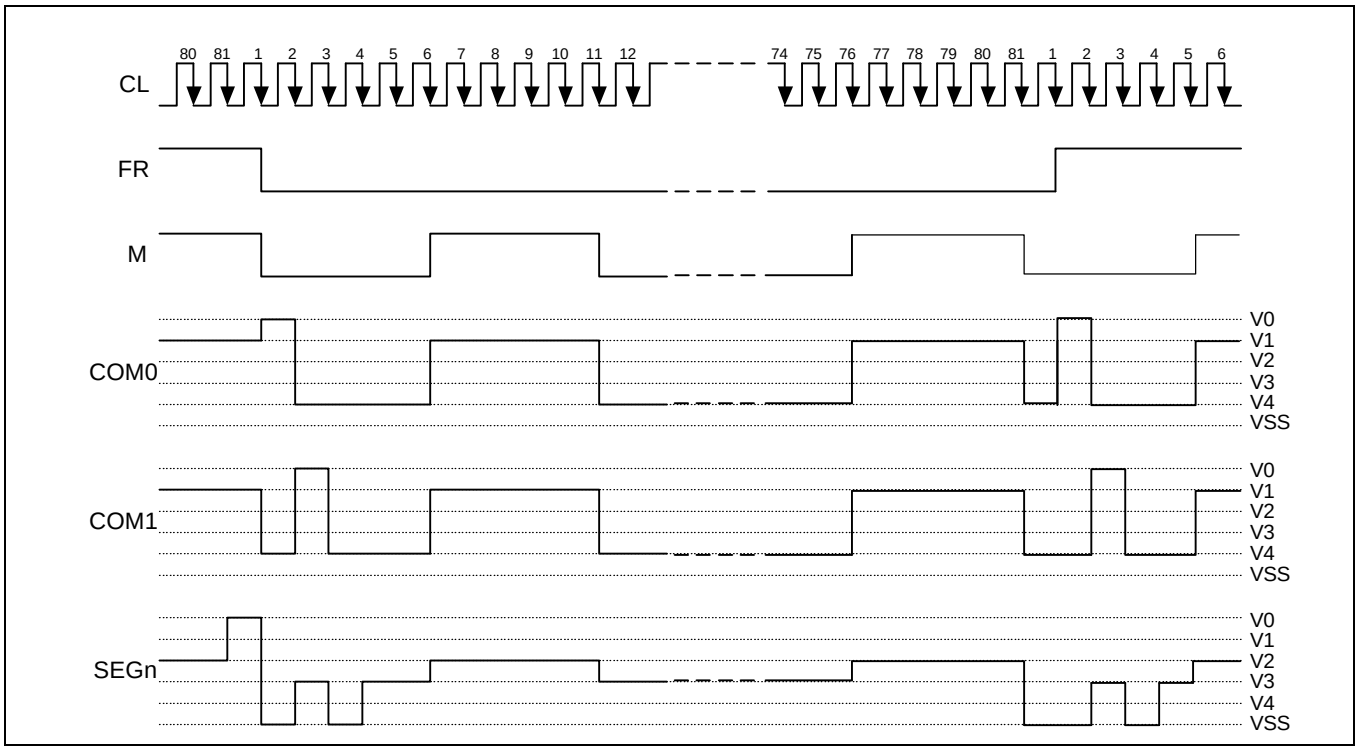

Figure 11. N-line Inversion Driving Waveform (N = 5, Duty Ratio = 1/81)

LCD DRIVER CIRCUIT

81-channel common driver and 104-channel segment driver configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.

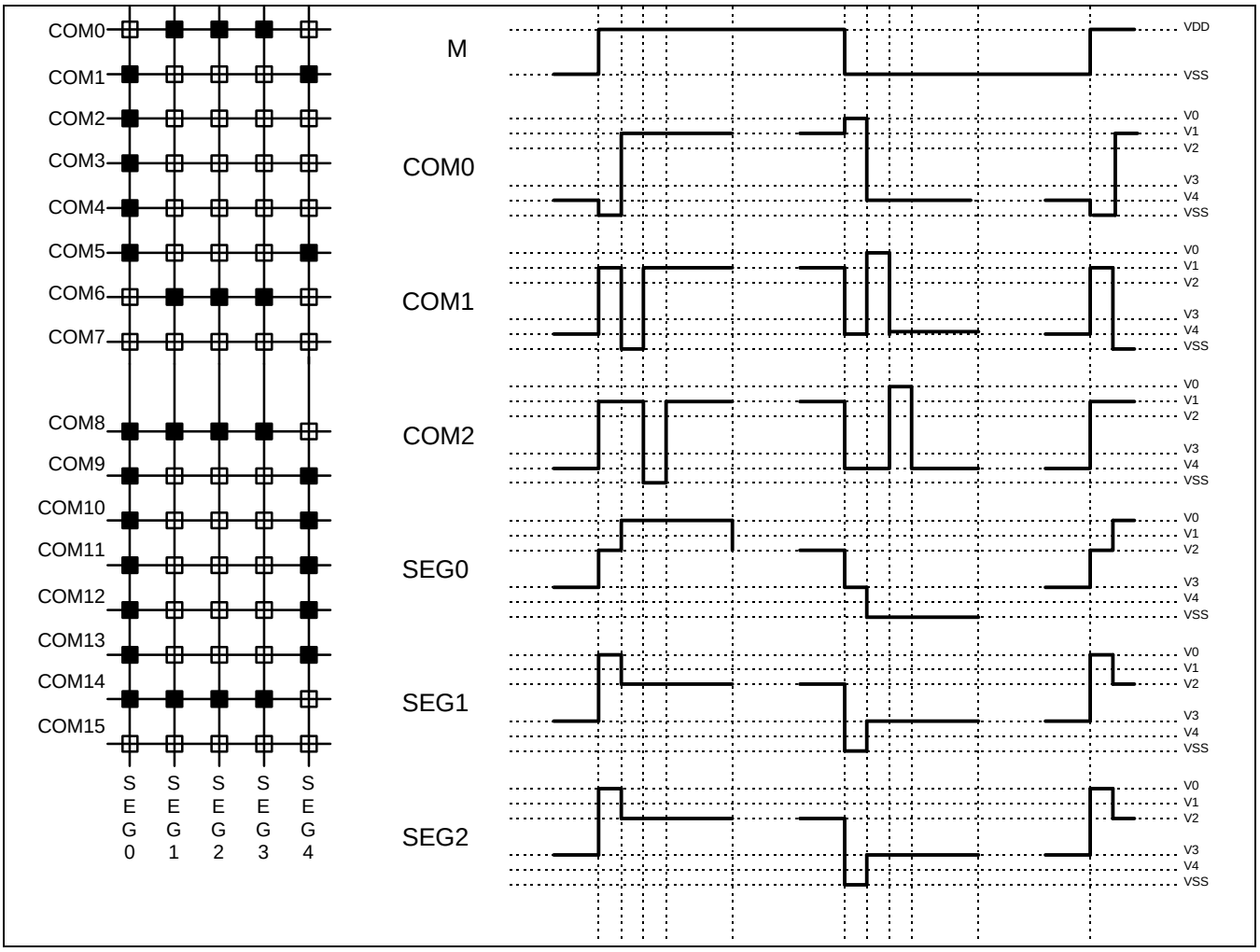

Figure 12. Segment and Common Timing

Partial Display on LCD

The KS0718 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

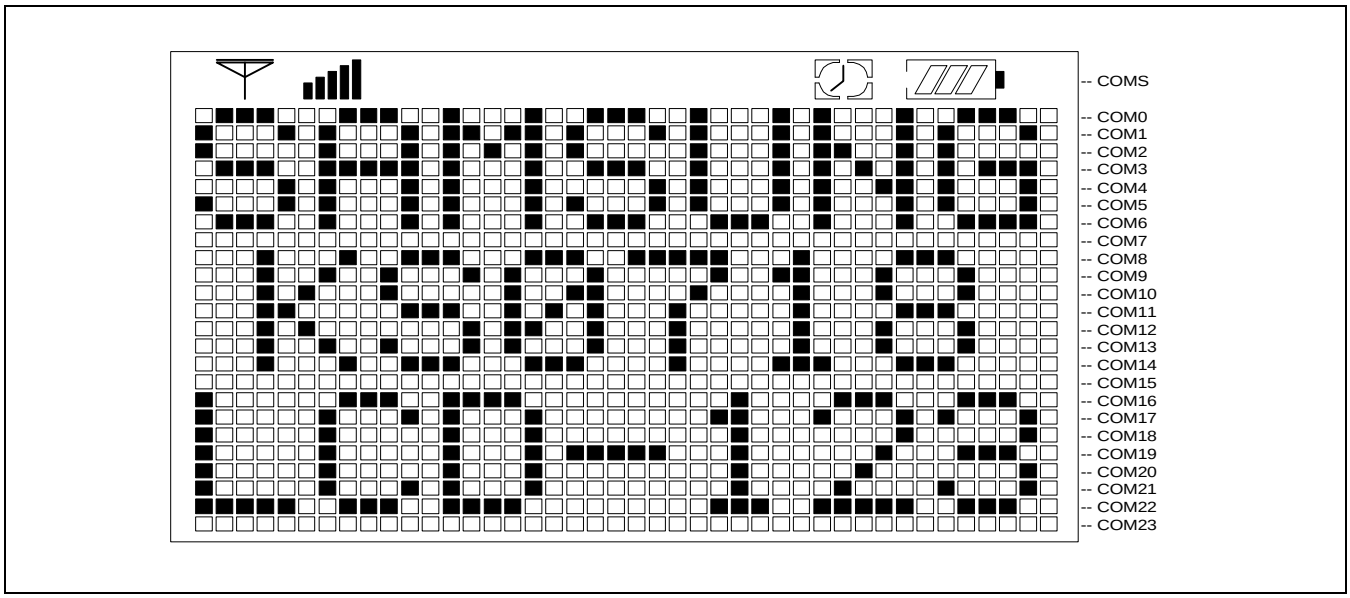

Figure 13. Reference Example for Partial Display (Display Duty = 25)

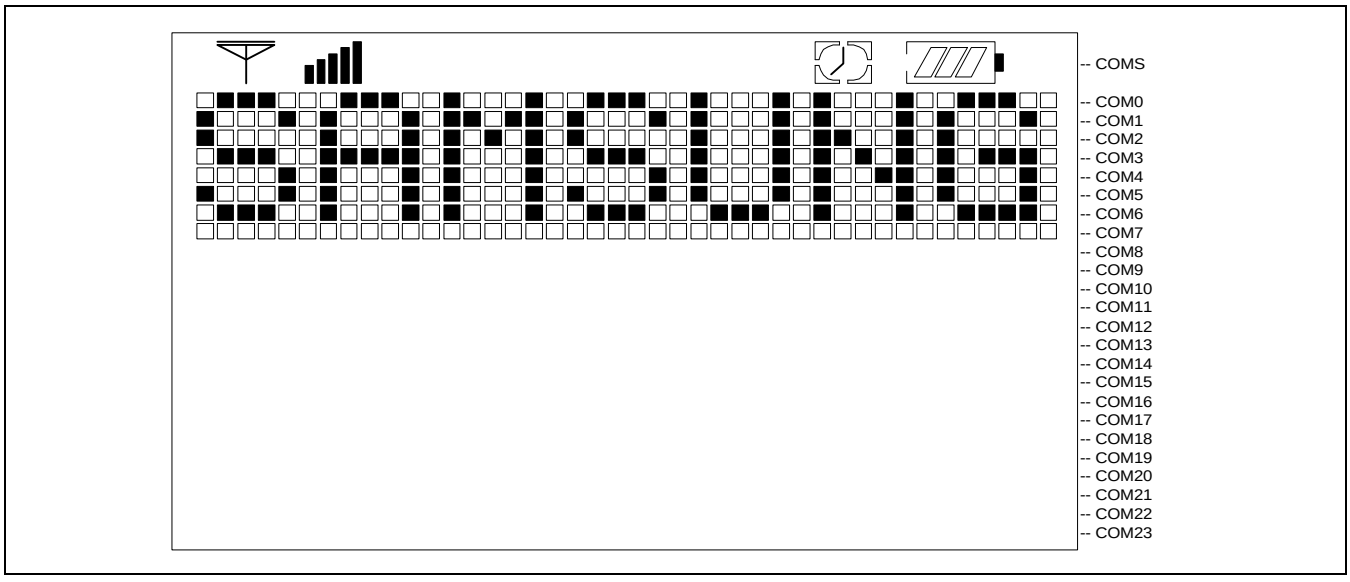

Figure 14. Partial Display (Partial Display Duty = 9, Initial COM0 = 0)

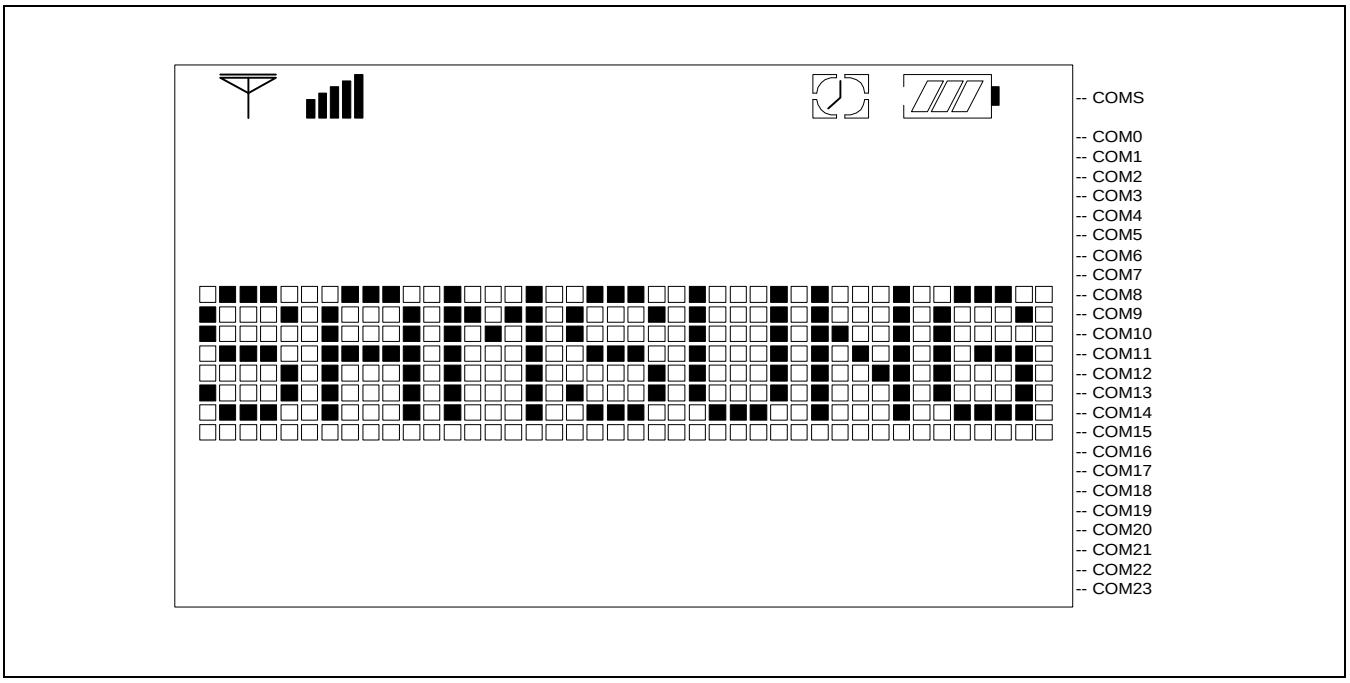

Figure 15. Moving Display (Partial Display Duty = 9, Initial COM0 = 8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 12 shows the referenced combinations in using Power Supply circuits.

Table 12. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	External input	Open	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by “Set DC-DC Step-up” instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 ㎌]

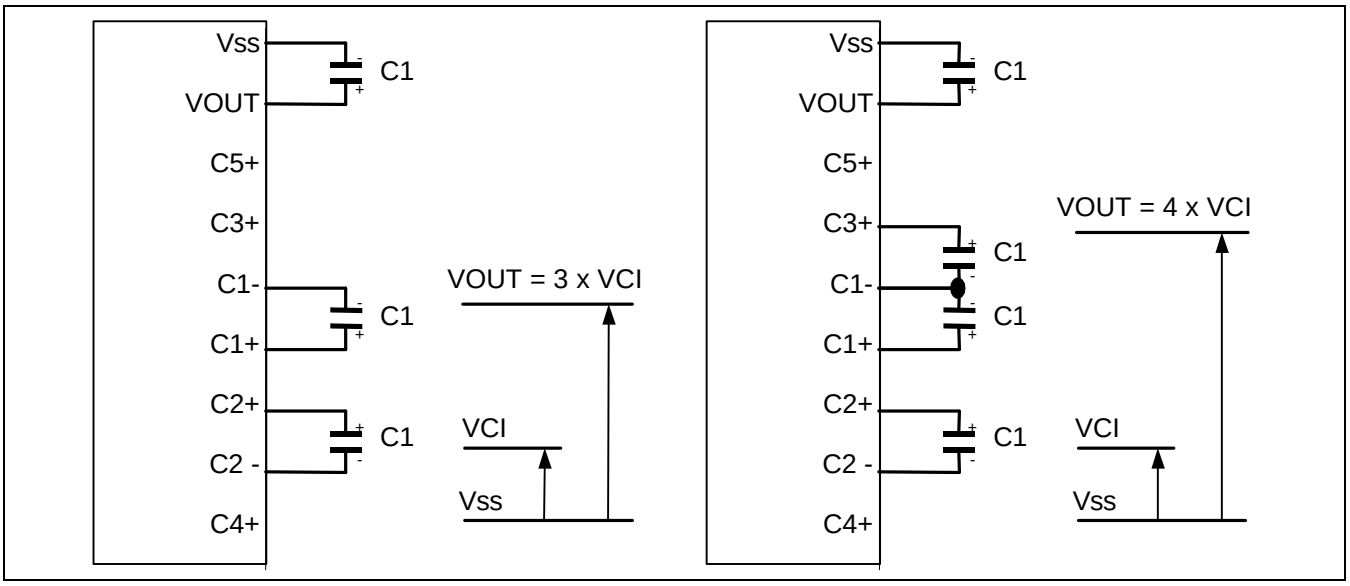

Figure 16. Three Times Boosting Circuit

Figure 17. Four Times Boosting Circuit

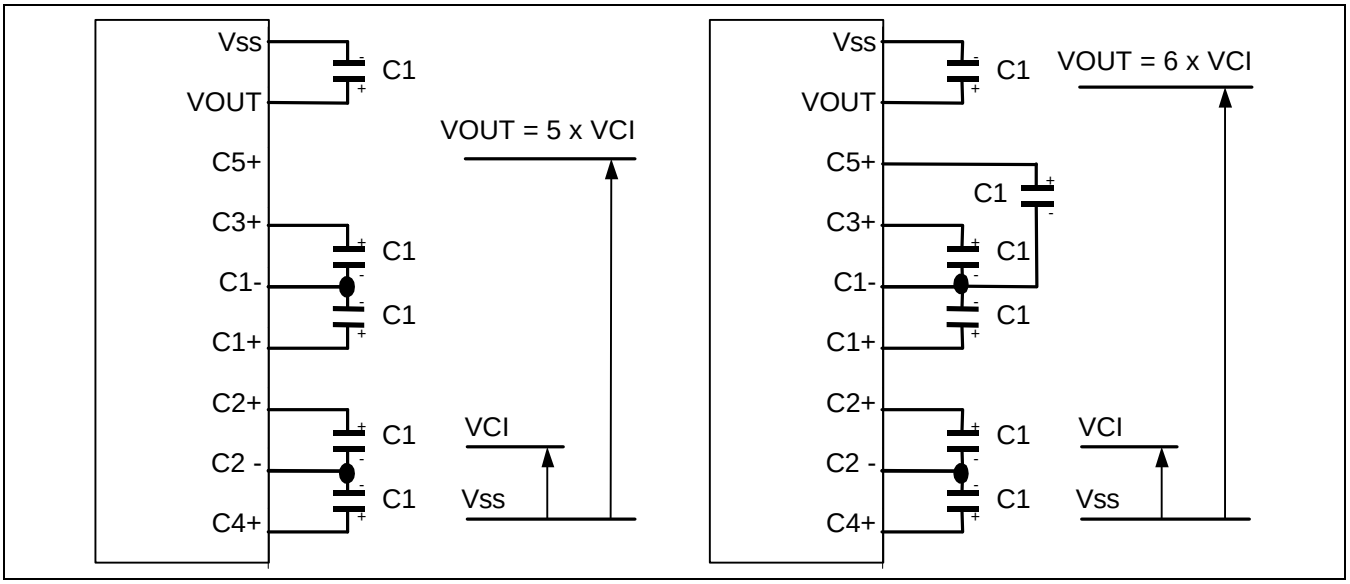

Figure 18. Five Times Boosting Circuit

Figure 19. Six Times Boosting Circuit

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 20, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta= 25°C is shown in Table 13.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{200}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 13. . V_{REF} Voltage at Ta = 25°C

REF	Temp. coefficient	V_{REF} [V]
1	-0.05% / °C	2.0
0	External input	VEXT

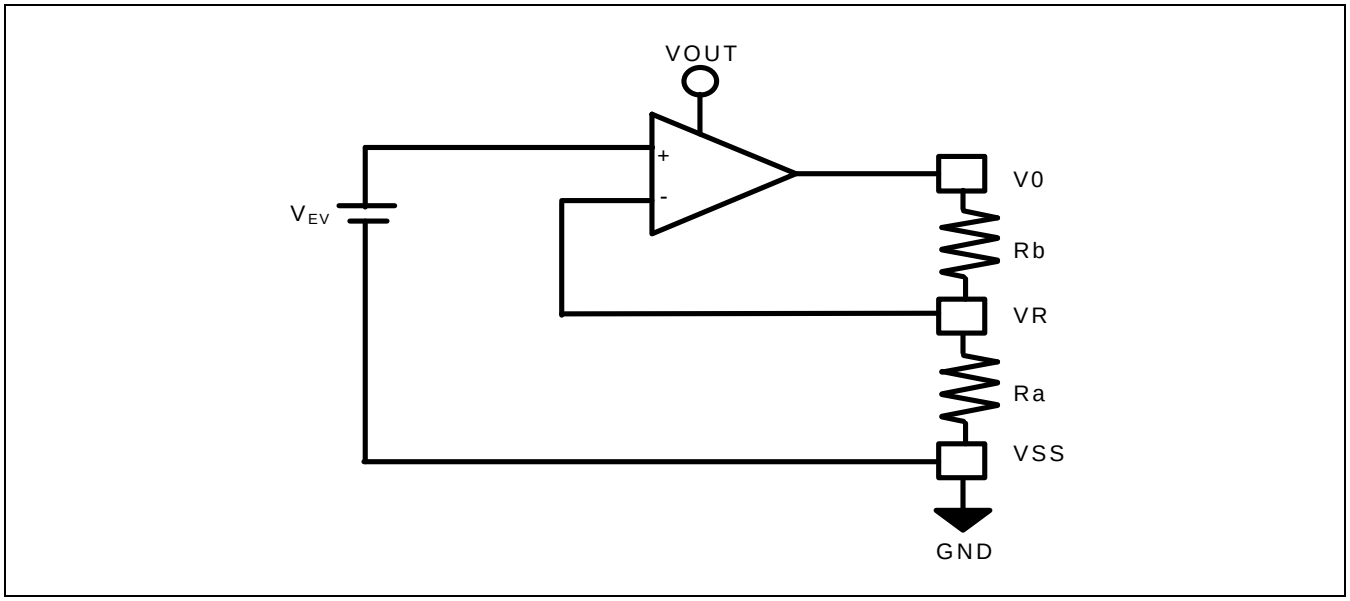

Figure 20. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is **"**H**"**, resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 14. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.6	3.4	4.2	5.0	5.8	6.6	7.4	8.3

Figure 21 Shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

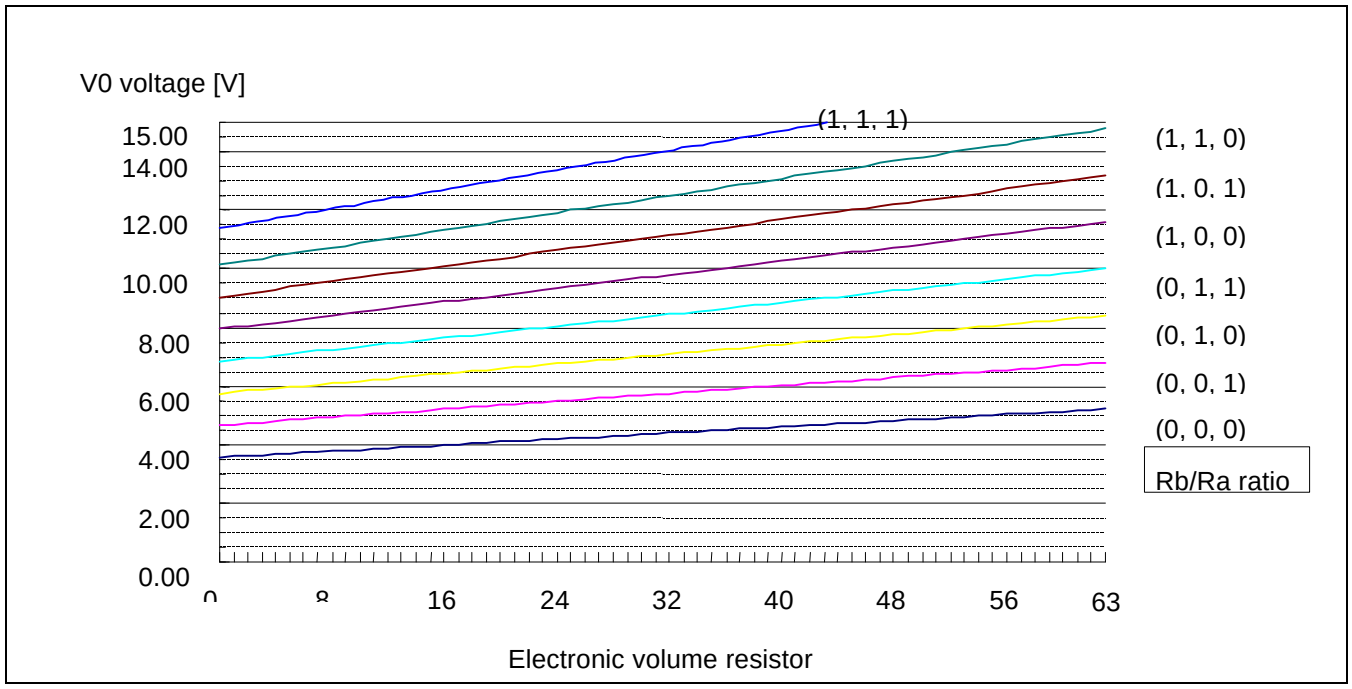

Figure 21. Electronic Volume Level (Temp. Coefficient = -0.05% / °C)

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is **"L"**, it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 1

$$V_{EV} = \left(1 - \frac{(63 - 32)}{200}\right) \times 2.0 = 1.69 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [uA]} \quad \text{------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5

Ra = 1.69 [MΩ]

Rb = 8.31 [MΩ]

Table 15 Shows the Range of V0 depending on the above Requirements.

Table 15. The Range of V0

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.10	.....	10.00	.....	11.83

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 16 shows the relationship between V1 to V4 level and each duty ratio.

Table 16

LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-1)/N x V0	2/N x V0	1/N x V0	N = 4 to 11

REFERECE CIRCUIT EXAMPLES

[C1 = 1.0 to 4.7 [µF], C2 = 0.1 to 0.47 [µF]]

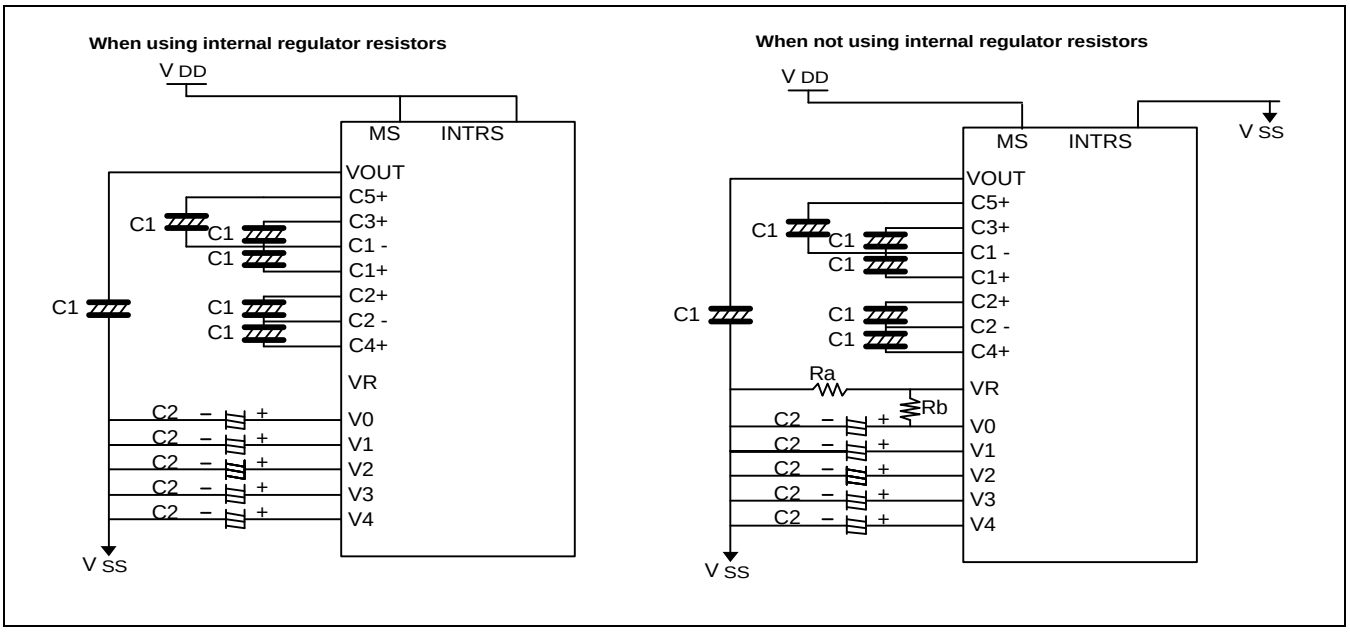

Figure 22. When Using all LCD Power Circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

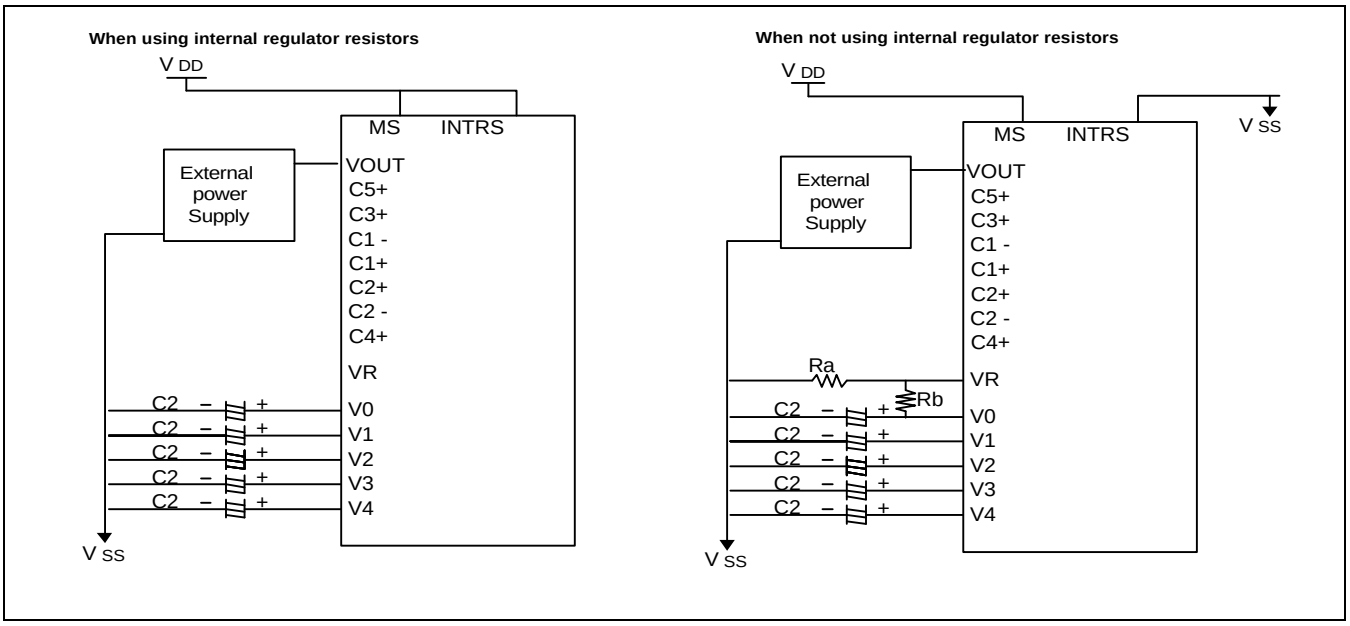

Figure 23. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

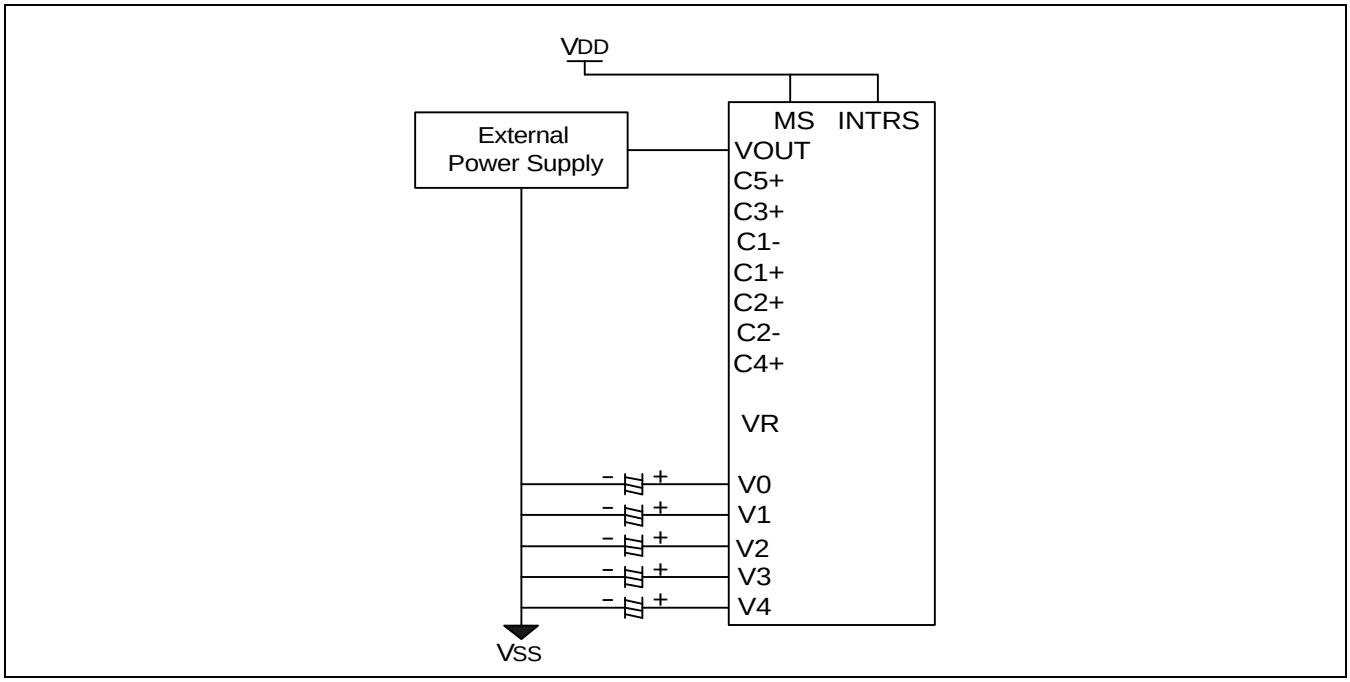

Figure 24. When Using only Voltage Follower Circuit (V/C: OFF, V/R: OFF, V/F: ON)

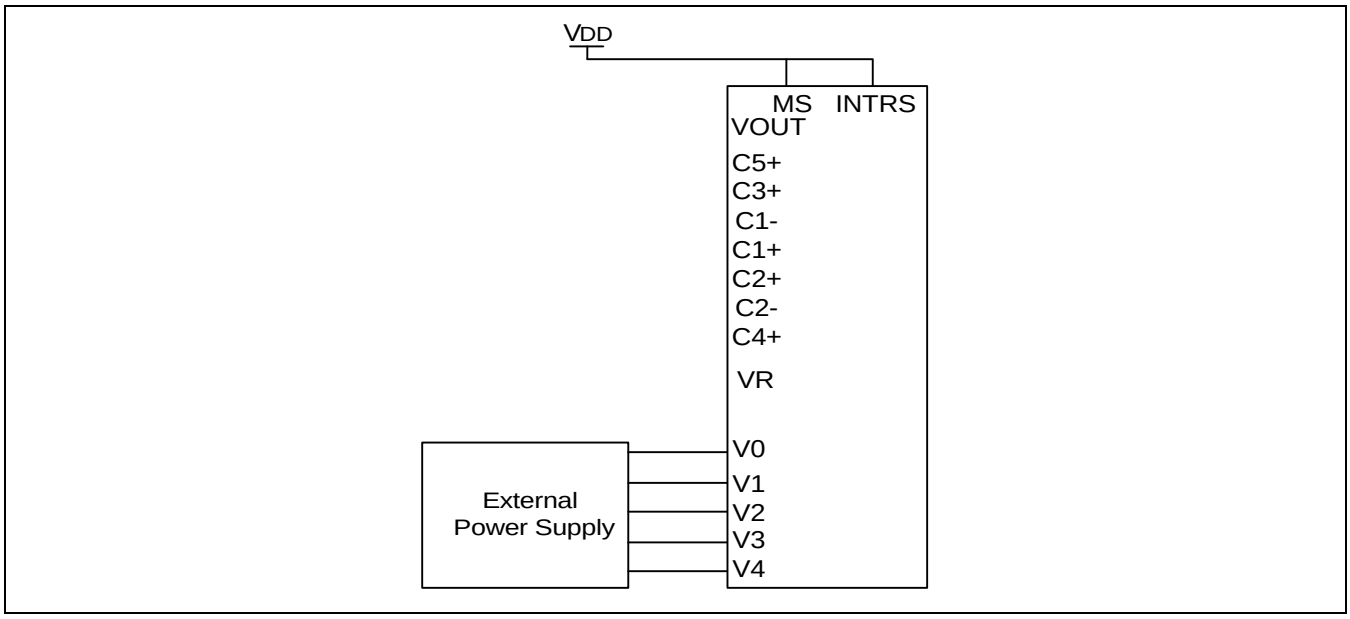

Figure 25. When Not Using all LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to **"L"** or Reset instruction can initialize internal function.
When RESETB becomes **"L"**, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display duty ratio: 1/81
Reverse display ON / OFF: OFF (normal)
n-line inversion register: 0 (disable)
Entire display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC step up: 3 times converter circuit = (0, 0)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register: (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
LCD bias ratio: 1/10
SHL select: OFF (normal)
ADC select: OFF (normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Oscillator status: OFF
Power save mode: release

When RESET instruction is issued, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Other instruction registers : Not changed

While RESETB is **"L"** or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes **"L"**, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 17. Instruction Table

×: Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON	RES	0	0	0	0	Read the internal status
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	0	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Display ON / OFF	0	0	1	0	1	0	1	1	1	D	D = 0: display OFF D = 1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	×	×	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	×	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	2-byte instruction to set partial display duty ratio
	0	0	×	D6	D5	D4	D3	D2	D1	D0	
Set n-line inversion	0	0	0	1	0	0	1	1	×	×	2-byte instruction to set n-line inversion register
	0	0	×	×	×	N4	N3	N2	N 1	N0	
Release n-line inversion	0	0	1	1	1	0	0	1	0	0	Release n-line inversion mode
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	REV = 0: normal display REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	EON = 0: normal display EON = 1: entire display ON

Table 17. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the electronic volume register
	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM bi-directional selection SHL = 0: normal direction SHL = 1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC = 0: normal direction ADC = 1: reverse direction
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	2-byte instruction to specify the static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	
Oscillator ON start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P = 0: standby mode P = 1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
NOP	0	0	1	1	1	0	0	0	1	1	***No operation***
Test instruction	0	0	1	1	1	1	×	×	×	×	***Don't use this instruction.***

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is incremented by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is incremented by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

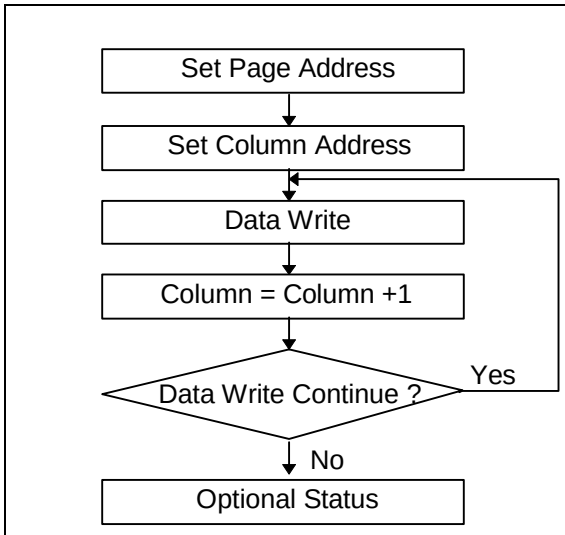

Figure 26. Sequence for Writing Display Data

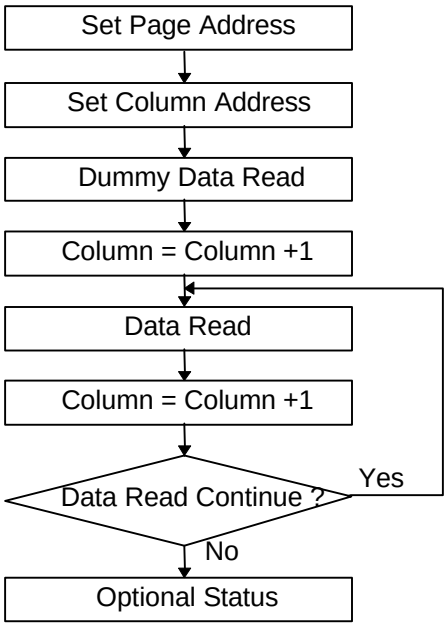

Figure 27. Sequence for Reading Display Data

Read Status

Indicates the internal status of the KS0718

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON	RES	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG103 → SEG0), 1: normal direction (SEG0 → SEG103)
ON	Indicates display ON / OFF status. 0: display ON, 1: display OFF
RES	Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset.

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Selected page	Description
0	0	0	0	0	Accessible pages for displaying dot-matrix display data
0	0	0	1	1	
0	0	1	0	2	
:	:	:	:	:	
1	0	0	1	9	
1	0	1	0	10	
1	0	1	1	11	Accessible page for displaying icons
1	1	0	0	12	Not accessible page. Do not use these pages.
1	1	0	1	13	
1	1	1	0	14	
1	1	1	1	15	

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the column address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically incremented.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y6	Y5	Y4	Y3	Y2	Y1	Y0	Selected column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	1	0	0	1	0	1	101
1	1	0	0	1	1	0	102
1	1	0	0	1	1	1	103
1	1	0	1	0	0	0	Not accessible column Do not use these columns.
:	:	:	:	:	:	:	
:	:	:	:	:	:	:	
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the Write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

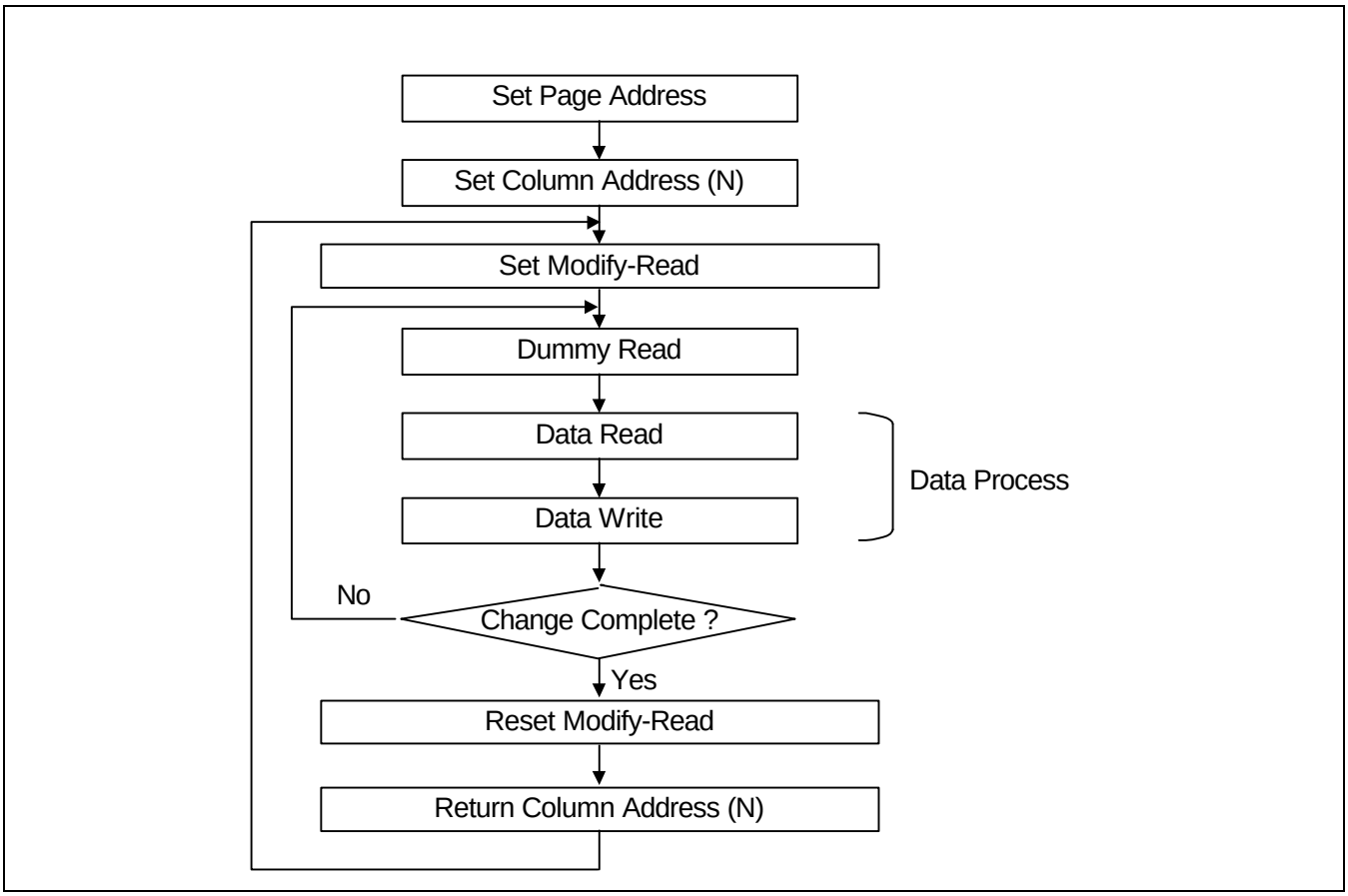

Figure 28. Sequence for Cursor Display

Display ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	D

D = 1: display ON
D = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top row (COM0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Selected line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	0	1	0	1	1	0	86
1	0	1	0	1	1	1	87
1	0	1	1	0	0	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

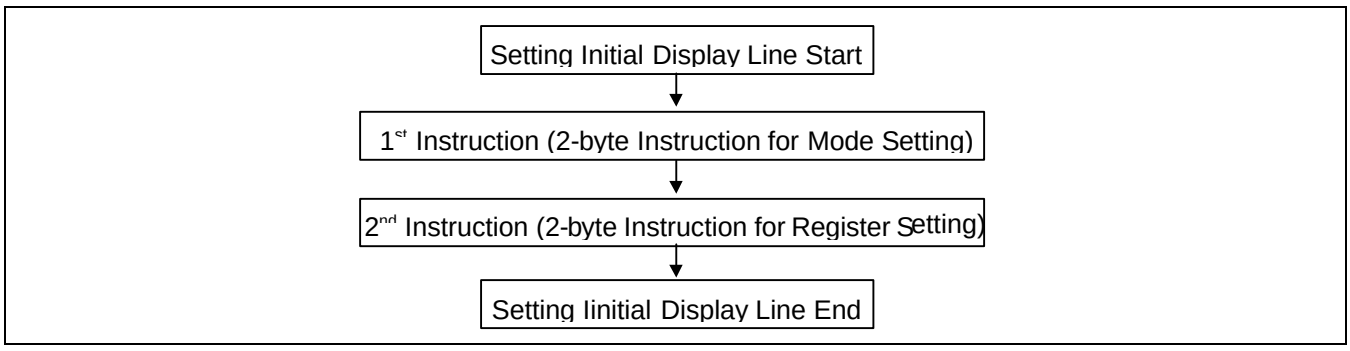

Figure 29. The Sequence for Setting the Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	0	0	1	1	0	0	COM76
1	0	0	1	1	0	1	COM77
1	0	0	1	1	1	0	COM78
1	0	0	1	1	1	1	COM79
1	0	1	0	0	0	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

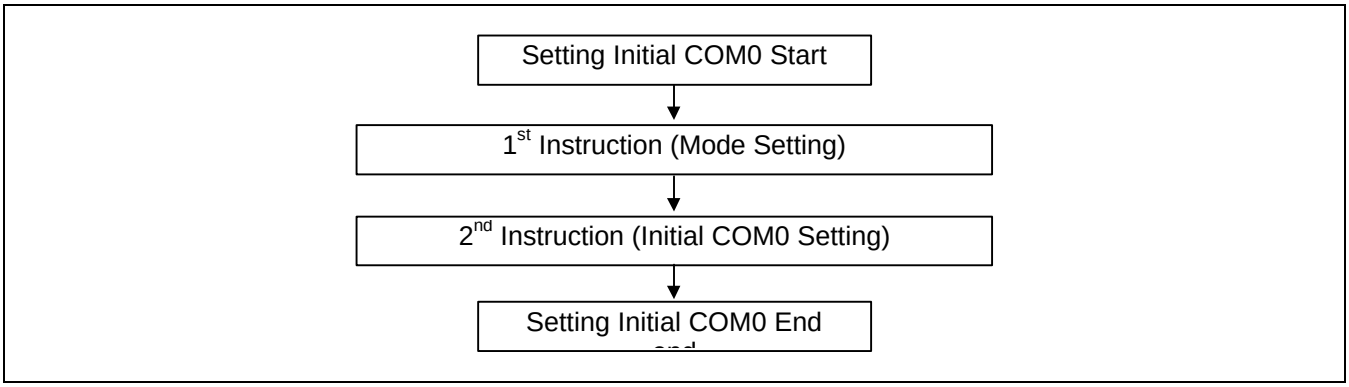

Figure 30. Sequence for Setting the Initial COM0

Set Partial Display Duty Ratio

Sets the duty ratio within range of 9 to 81 to realize partial display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	D6	D5	D4	D3	D2	D1	D0

D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio
0	0	0	0	0	0	0	No operation
:	:	:	:	:	:	:	
0	0	0	1	0	0	0	
0	0	0	1	0	0	1	1/9
0	0	0	1	0	1	0	1/10
0	0	0	1	0	1	1	1/11
0	0	0	1	1	0	0	1/12
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1/78
1	0	0	1	1	1	1	1/79
1	0	1	0	0	0	0	1/80
1	0	1	0	0	0	1	1/81
1	0	1	0	0	1	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

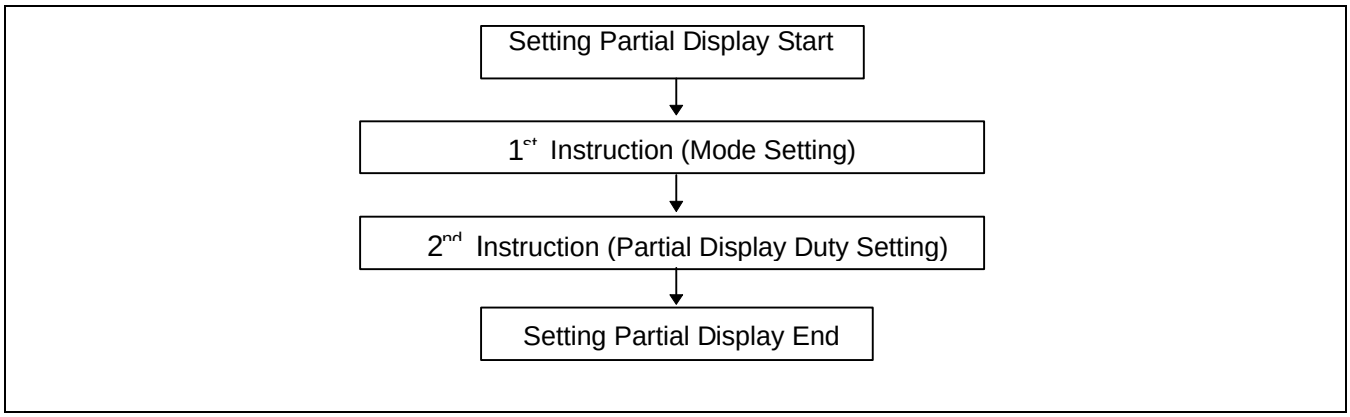

Figure 31. Sequence for Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

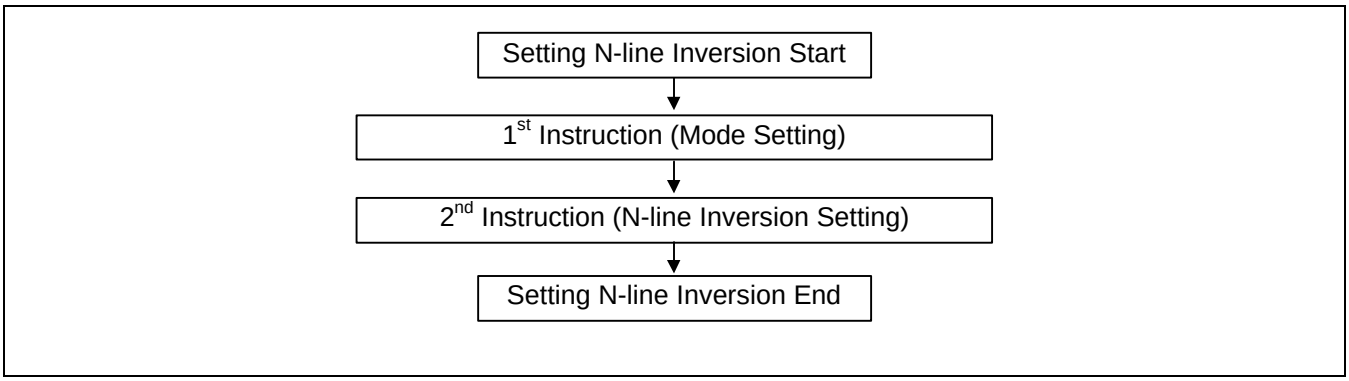

Figure 32. Sequence for Setting Partial Display

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (entire)	LCD pixel is illuminated	LCD pixel is illuminated

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Select DC-DC Step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb / Ra] ratio
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

Set Electronic Volume Register

Consists of 2-byte instruction
The 1st instruction sets electronic volume mode, the 2nd one updates the contents of electronic volume register. After second instruction, electronic volume mode is released.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

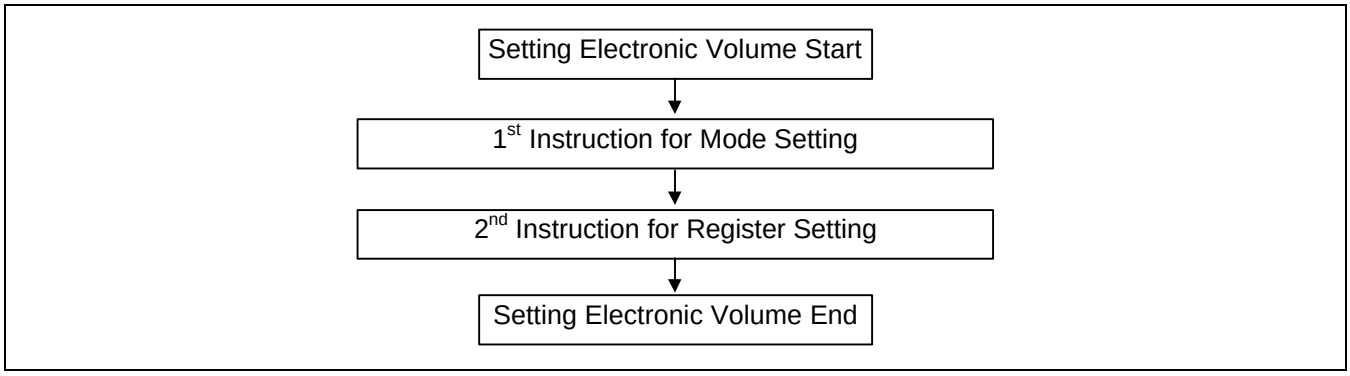

Figure 33. Sequence for Setting the Electronic Volume

Select LCD Bias

Selects LCD Bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	Selected LCD bias
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	0	1/10
1	1	1	1/11

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

SHL = 0: normal direction (COM0 → COM79)
SHL = 1: reverse direction (COM79 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG103)
ADC = 1: reverse direction (SEG103 → SEG0)

Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator mode) enables the second byte instruction (set Static Indicator register) to be valid. The first byte sets the Static Indicator ON / OFF. When it is on, the second byte updates the contents of Static Indicator register without issuing any other instruction and this Static Indicator state is released after setting the data of indicator register.

The 1st Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The 2nd Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 0.5 second blinking)
1	0	ON (about 1 second blinking)
1	1	ON (always ON)

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Power Save

The KS0718 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: standby mode
P = 1: sleep mode

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

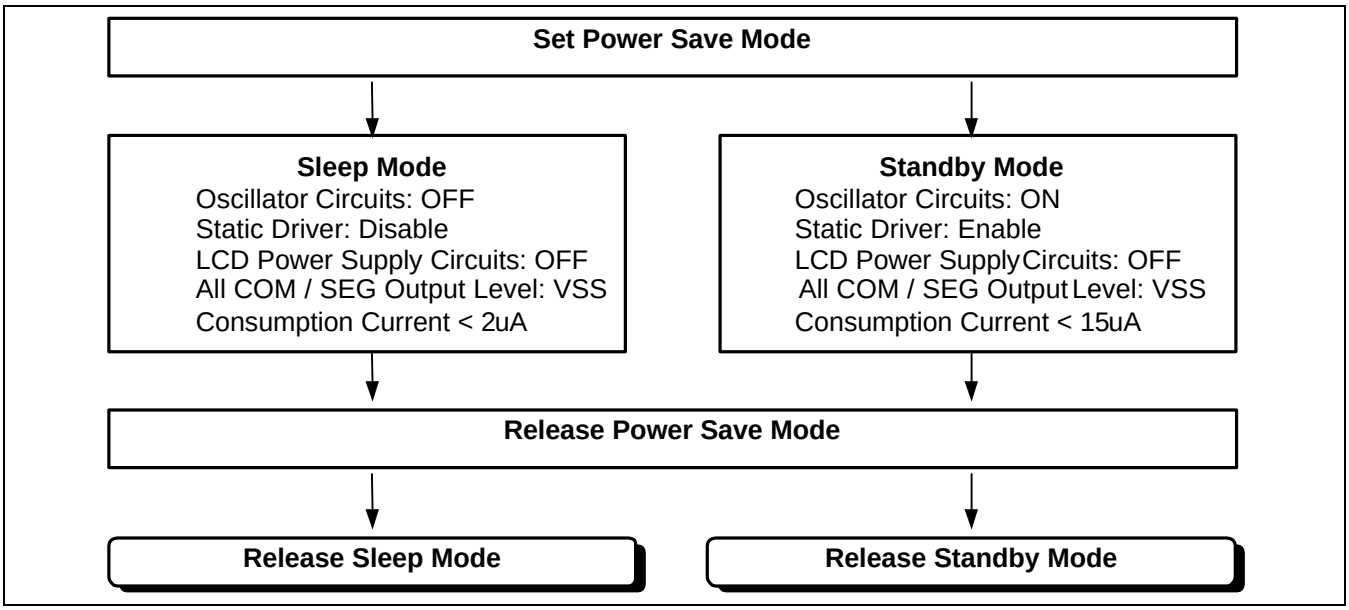

Figure 34. Power Save Routine

NOP

Non Operation Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

Referential Instruction Setup Flow: Initializing with the Built-in Power Supply Circuits

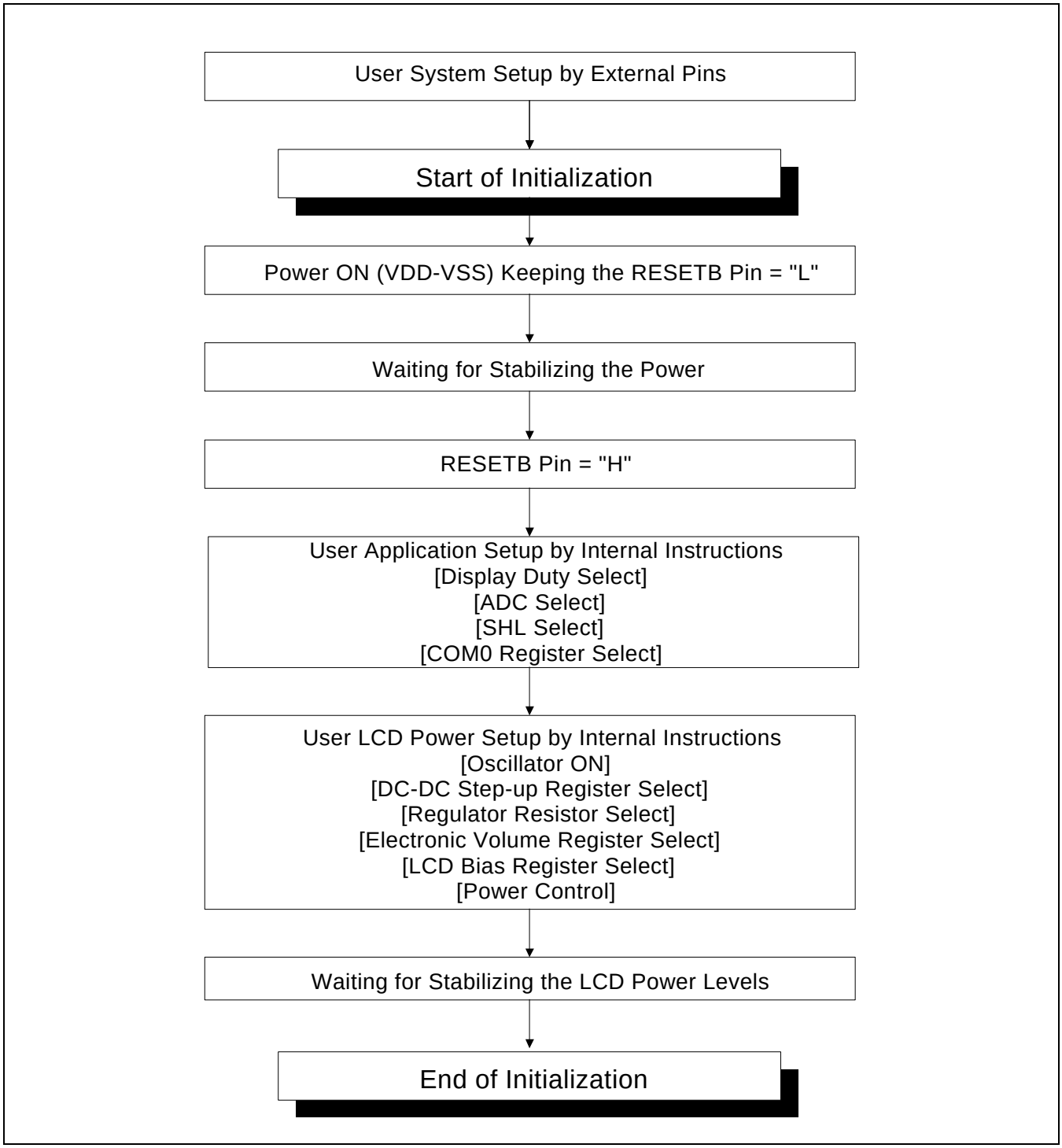

Figure 35. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the Built-in Power Supply Circuits

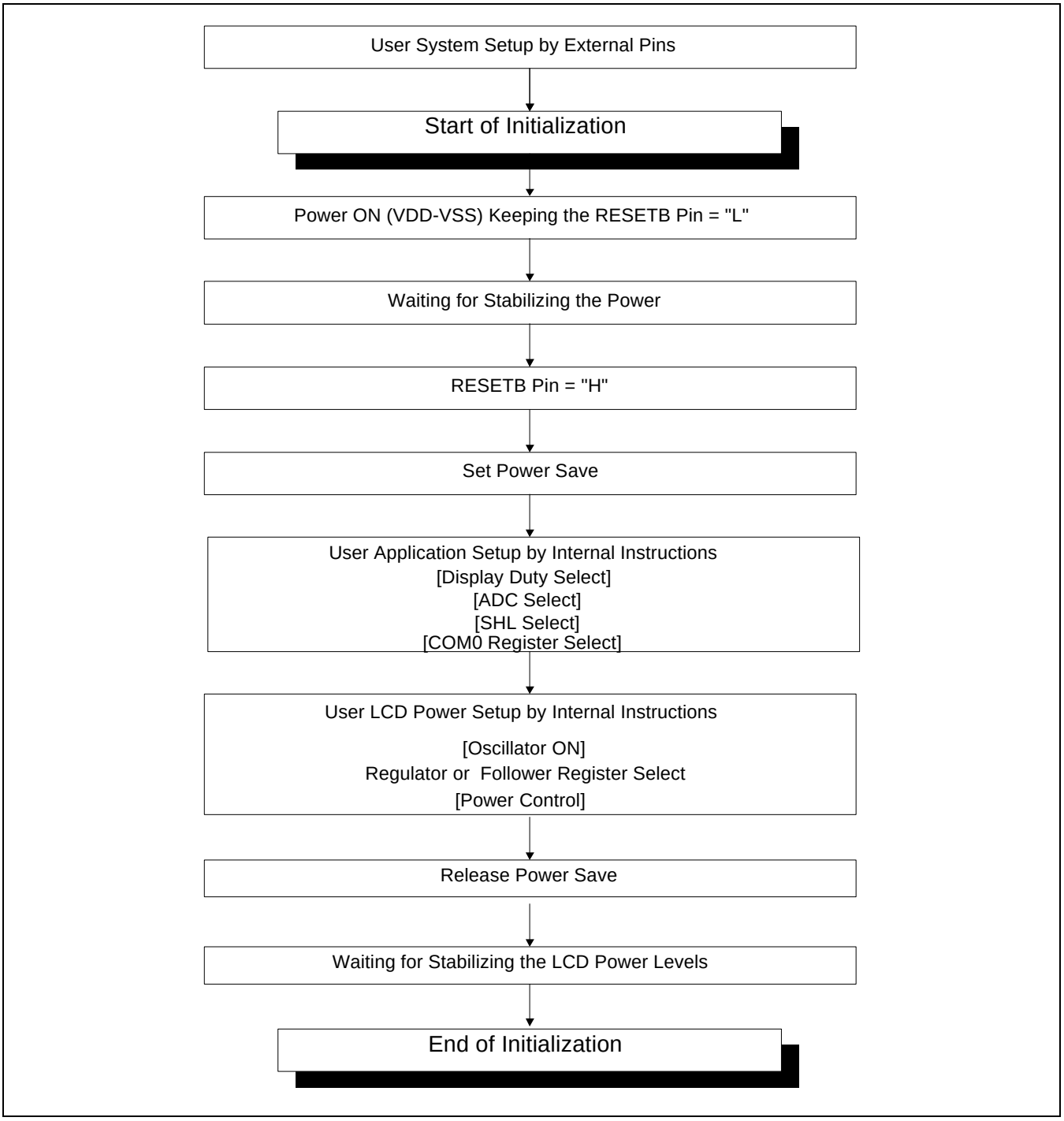

Figure 36. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

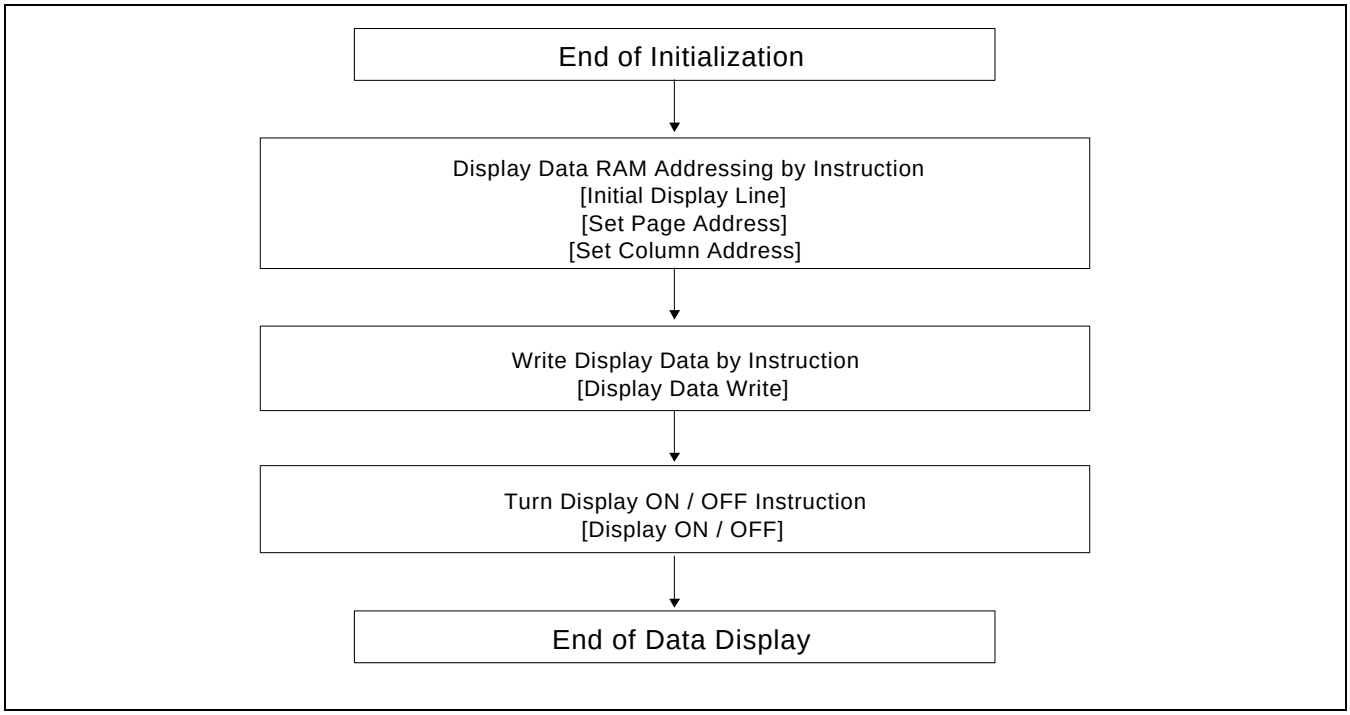

Figure 37. Data Displaying

Referential Instruction Setup Flow: Power OFF

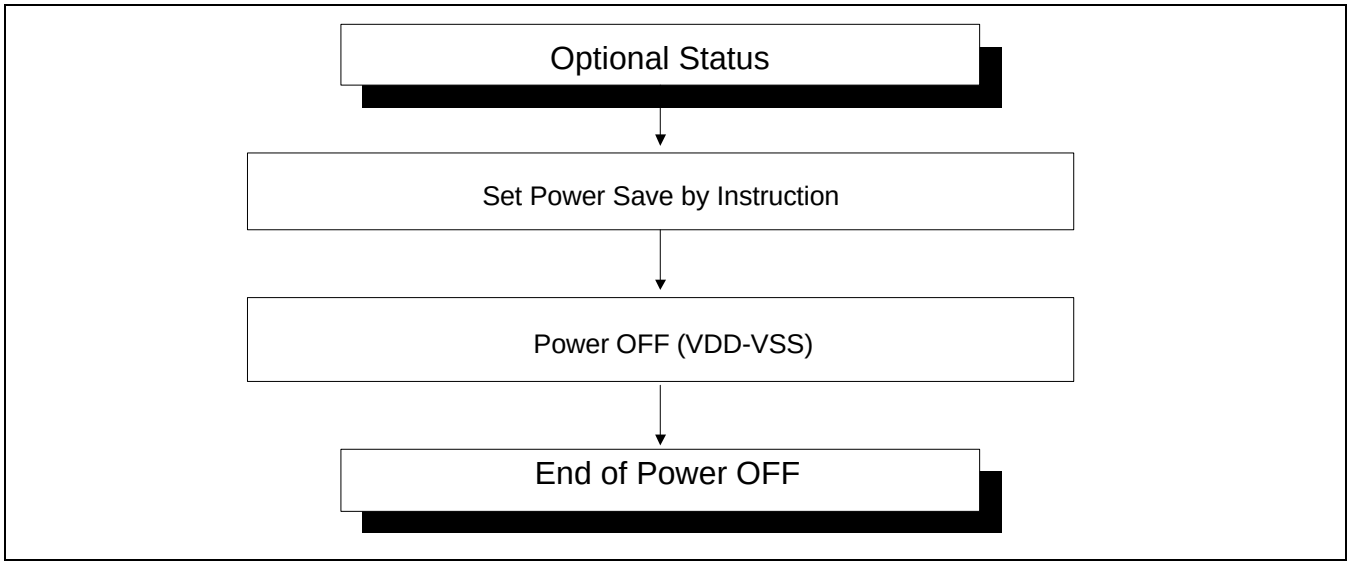

Figure 38. Power OFF

Referential Instruction Setup Flow: Partial Duty Changing

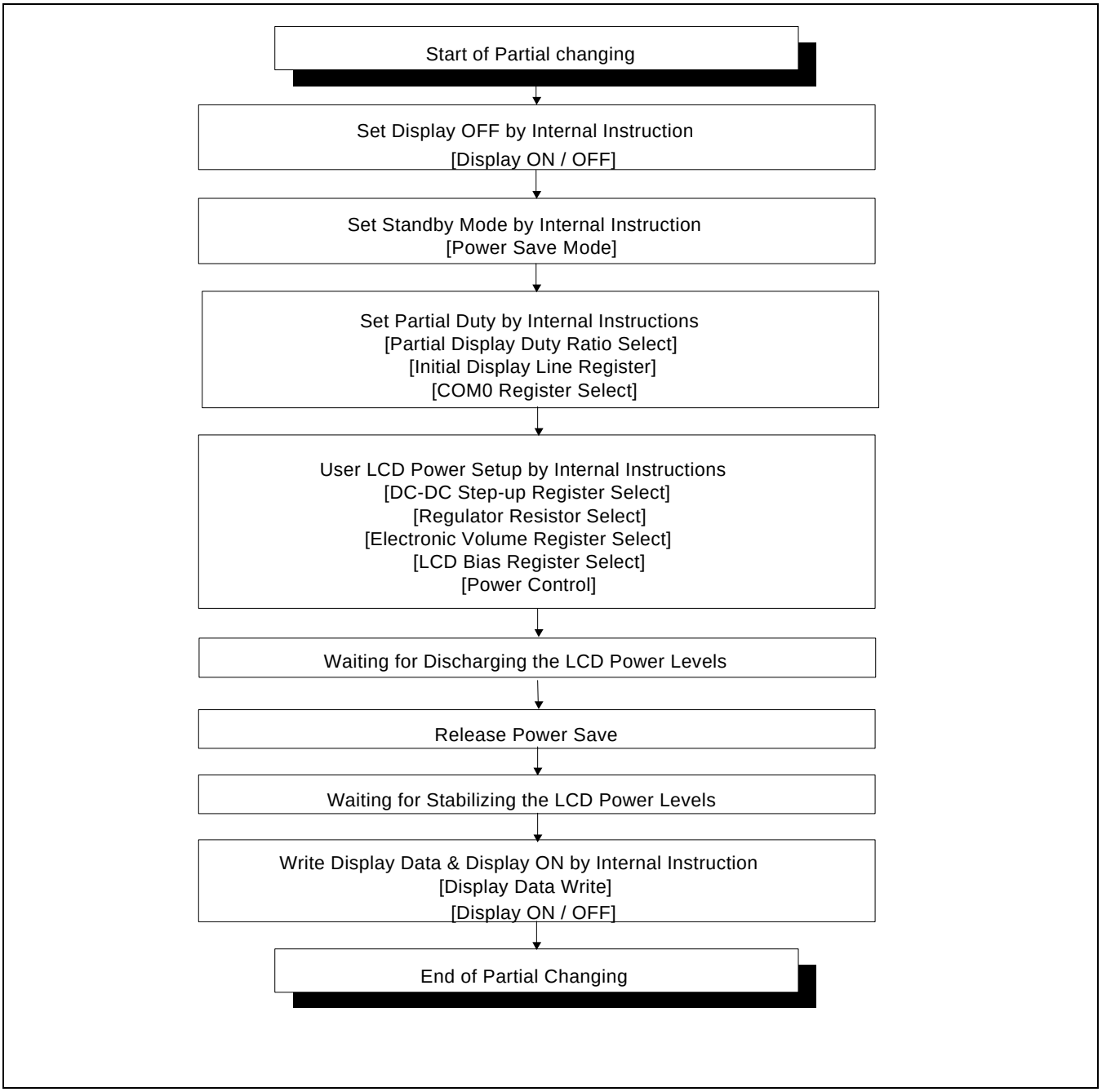

Figure 39. Partial Duty Changing

NOTE:1. Partial COM0 register setting for COM H/W half: [80 – (user duty)] / 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 18. Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 ~ + 7.0	V
	V_0, V_{OUT}	+ 0.3 ~ + 17.0	V
	V_1, V_2, V_3, V_4	+ 0.3 ~ V_0	V
External reference voltage	V_{EXT}	+0.3 ~ V_{DD}	
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STR}	- 55 ~ + 125	°C

NOTES:

1. VDD, V0, VOUT, V1 to V4, VEXT and VCI are based on VSS = 0V.
2. Voltage VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 19. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4~5.5V, Ta=-40~85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		2.4	-	5.5	V	VDD *1
Operating voltage (2)		V_0		4.0	-	15.0	V	V0, *2
Input voltage	High	V_{IH}		$0.8V_{DD}$	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	$0.2V_{DD}$		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	$0.8V_{DD}$	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	$0.2V_{DD}$		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*3
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*5
LCD driver ON resistance		R_{ON}	Ta = 25°C, V_0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *6
Frame frequency		f_{FR}	Ta = 25°C	70	85	100	Hz	FR *7

Table 20. DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Voltage converter circuit output voltage	V_{OUT}	×3 / ×4 / ×5 / ×6 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator circuit operating voltage	V_{OUT}		6.0	-	15.0	V	VOUT
Voltage follower circuit operating voltage	V_0		4.0	-	15.0	V	V0 *8
Reference voltage	V_{REF}	Ta = 25°C	1.94	2.00	2.06	V	*9

Dynamic Current Consumption (1) when An External Power Supply is used.

Table 21. Dynamic Current 1 (External Power)

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V0-Vss = 12.0V, duty = 1/81 (Display Off)	-	-	10	µA	*10
		V0-Vss = 12.0V, duty = 1/81 (Display On , Checker Pattern)	-	-	15	µA	*10

Dynamic Current Consumption (2) when The Internal Power Supply is ON

Table 22. . Dynamic Current 2 (Internal Power)

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V0 - Vss = 12.0V, x5 boosting, duty = 1/81, normal mode (Display Off)	-	-	150	µA	*10
		V0 - Vss = 12.0V, x5 boosting, duty = 1/81, normal mode (Display On , Checker Pattern)	-	-	300	µA	*10

Current Consumption during Power Save Mode

Table 23. Power Save Mode Current

(V_{DD} = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	During sleep	-	-	2	µA	*10
Standby mode current	I_{DDS2}	During standby	-	-	15	µA	*10

Table 24. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	f_{osc}
1/N	On-chip oscillator circuit is used	$f_{FR} \times N$	$f_{FR} \times 4 \times N$

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 9 to 81)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, REF, CL, M and SYNC.
*4. DB0 to DB7, FR, FRS, SYNC, M and CL.
*5. Applies when the DB0 to DB7, SYNC, M, and CL pins are in high impedance.
*6. Resistance value when -0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
*7. See Table 24 for the relationship between oscillation frequency and frame frequency.
*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors(Rb and Ra) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MP)

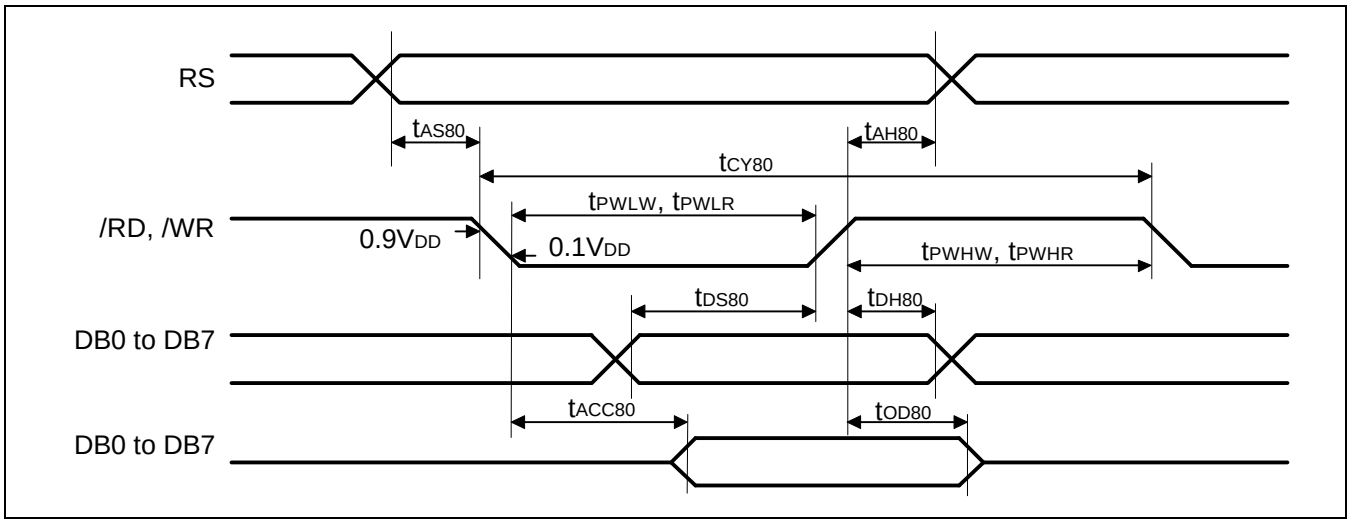

Figure 40. Read / Write Characteristics (8080-series MPU)

Table 25

(V_{DD} = 2.4 ~ 4.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System cycle time		t_{CY80}		400	-	ns
Pulse width low for write Pulse width high for write	RW_WR (/WR)	t_{PWLW} t_{PWHW}		60 60	- -	ns
Pulse width low for read Pulse width high for read	E_RD (/RD)	t_{PWLR} t_{PWHR}		120 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}		40 15	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	- 10	140 100	ns

Table 26

(V_{DD} = 4.5 ~ 5.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System cycle time		t_{CY80}		166	-	ns
Pulse width low for write Pulse width high for write	RW_WR (/WR)	t_{PWLW} t_{PWHW}		30 70	- -	ns
Pulse width low for read Pulse width high for read	E_RD (/RD)	t_{PWLR} t_{PWHR}		30 30	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{ACC80} t_{OD80}		30 10	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	C_L = 100 pF	- 5	70 50	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (t_{CY80} - t_{PWLW} - t_{PWHW}) for write, (tr + tf) < (t_{CY80} - t_{PWLR} - t_{PWHR}) for read

Read / Write Characteristics (6800-series Microprocessor)

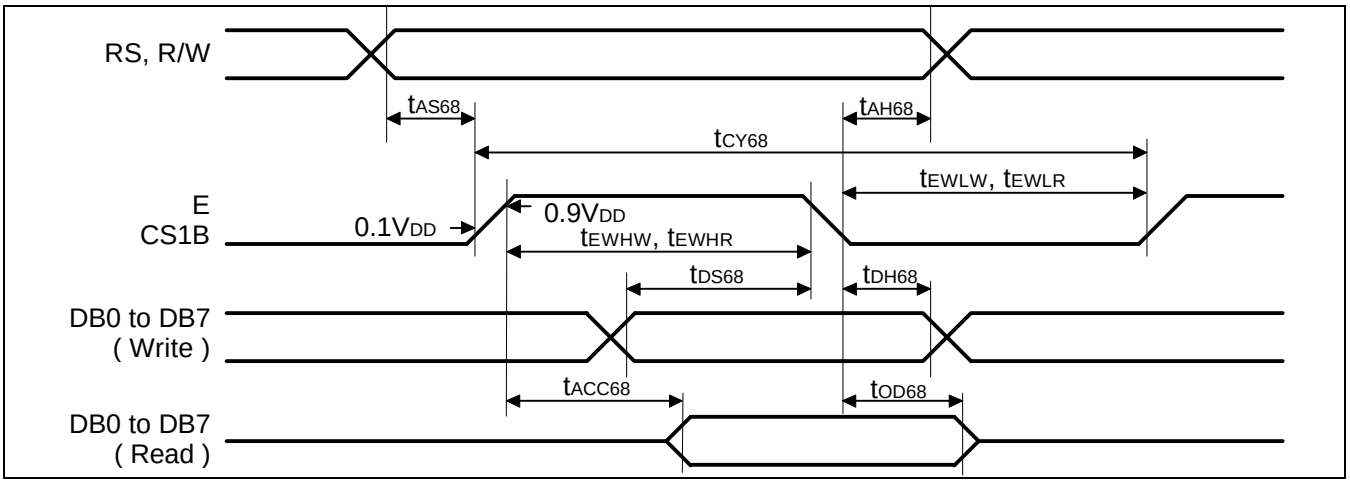

Figure 41. Read / Write Characteristics (6800-series Microprocessor)

Table 27

(V_{DD} = 2.4 ~ 4.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		0 0	- -	ns
System cycle time		t_{CY68}		400	-	ns
Enable width high for write Enable width low for write	E_RD (E)	t_{EWHW} t_{EWLW}		60 60	- -	ns
Enable width high for read Enable width low for read	E_RD (E)	t_{EWHR} t_{EWLR}		120 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		40 15	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	- 10	140 100	ns

Table 28

(V_{DD} = 4.5 ~ 5.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		0 0	- -	ns
System cycle time		t_{CY68}		166	-	ns
Enable width high for write Enable width low for write	E_RD (E)	t_{EWHW} t_{EWLW}		30 30	- -	ns
Enable width high for read Enable width low for read	E_RD (E)	t_{EWHR} t_{EWLR}		70 30	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		30 10	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	- 5	70 50	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY68 - tEWHW - tEWLW) for write, (tr + tf) < (tCY68 - tEWHR - tEWLR) for read

Serial Interface Characteristics

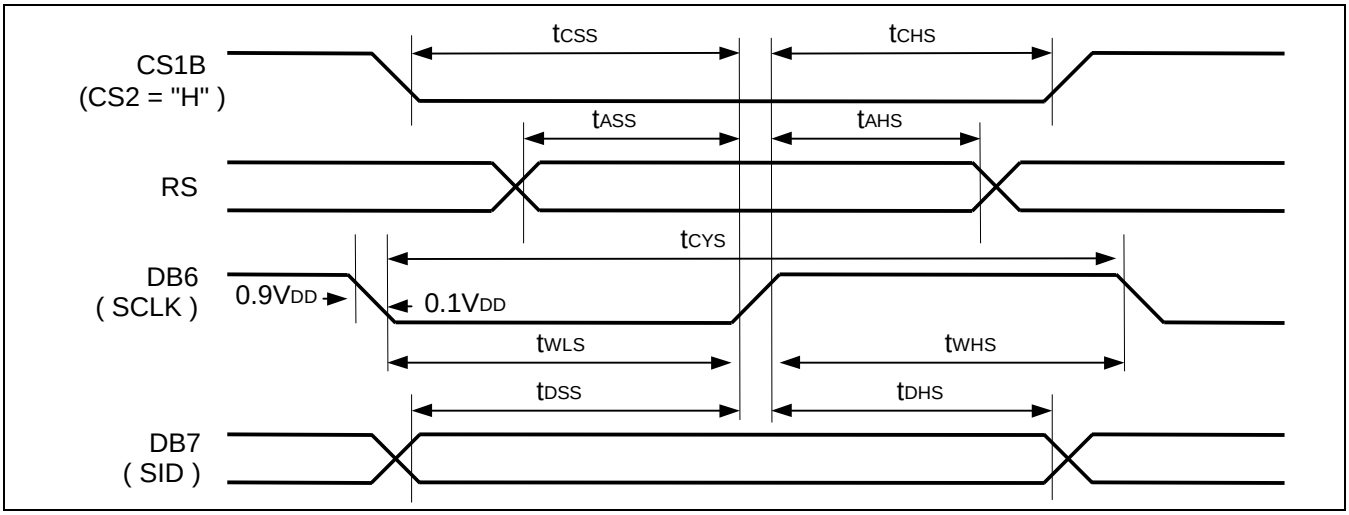

Figure 42

Table 29

(V_{DD} = 2.4 ~ 4.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{SCY} t_{SHW} t_{SLW}		250 100 100	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		150 150	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		100 100	- -	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}		150 150	- -	ns

Table 30

(V_{DD} = 4.5 ~ 5.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{SCY} t_{SHW} t_{SLW}		200 75 75	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		50 100	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		50 50	- -	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}		100 100	- -	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

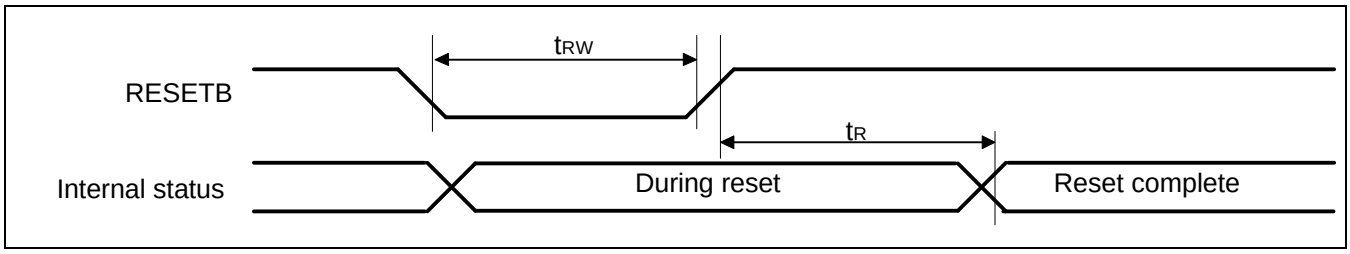

Figure 43

Table 31

(V_{DD} = 2.4 ~ 4.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

Table 32

(V_{DD} = 4.5 ~ 5.5V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}		500	-	ns
Reset time	-	t_R		-	500	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

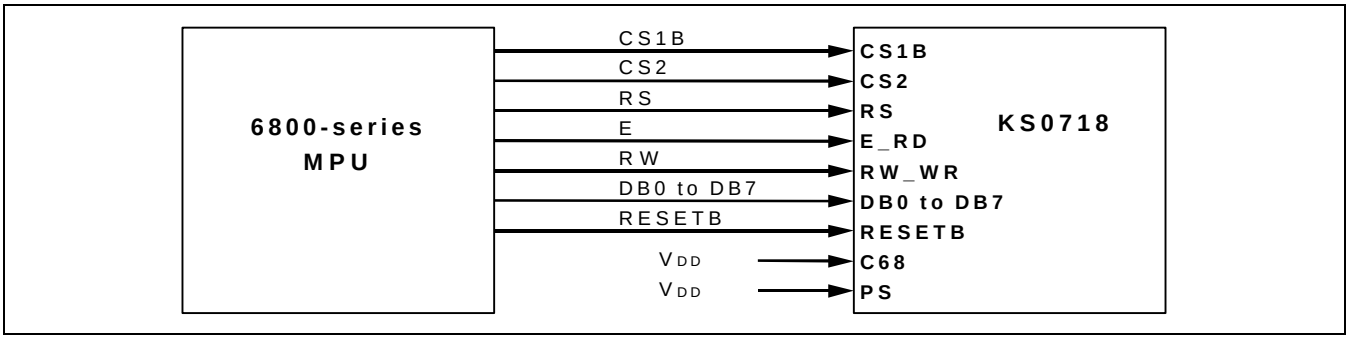

Figure 44. In Case of Interfacing with 6800-series (PS = "H", C68 = "H")

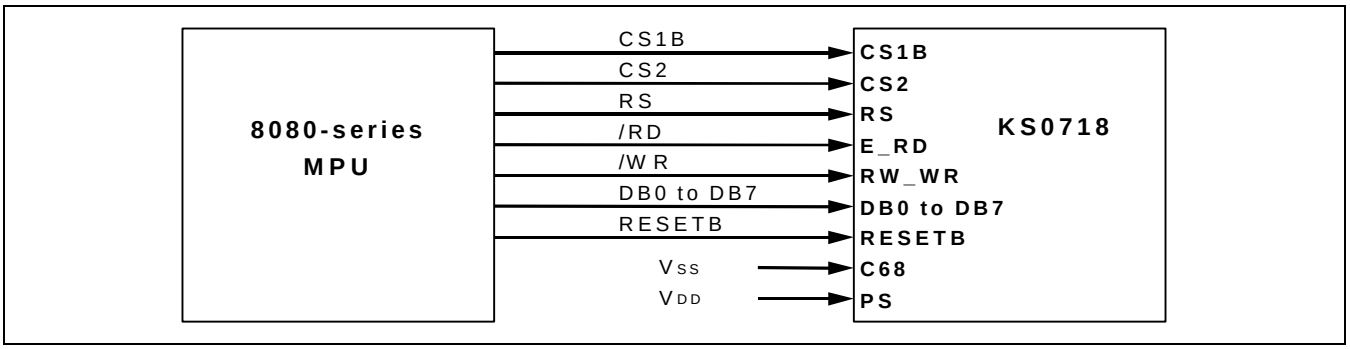

Figure 45. In Case of Interfacing with 8080-series (PS = "H", C68 = "L")

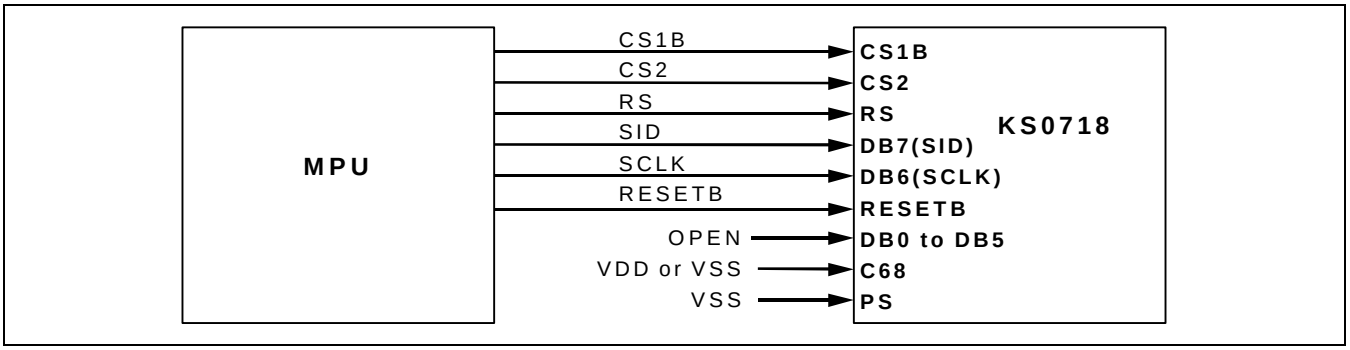

Figure 46. In Case of Serial Interface (PS = "L", C68 = "H/L")

CONNECTIONS BETWEEN KS0718 AND LCD PANEL

Single Chip Configurations (1/81 Duty)

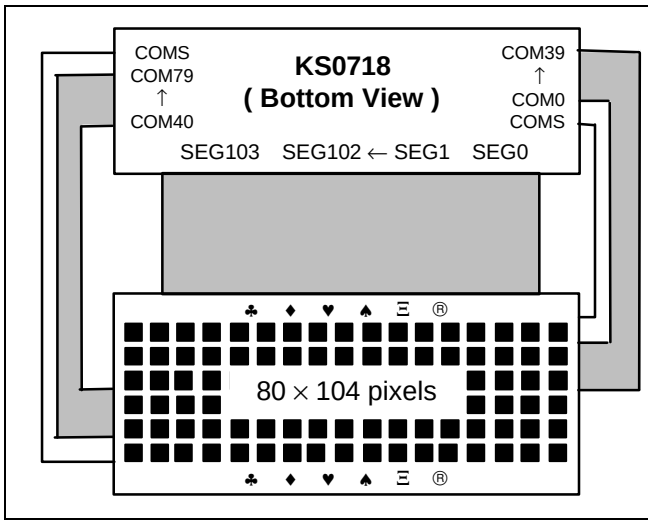

Figure 47. SHL = 0, ADC = 1

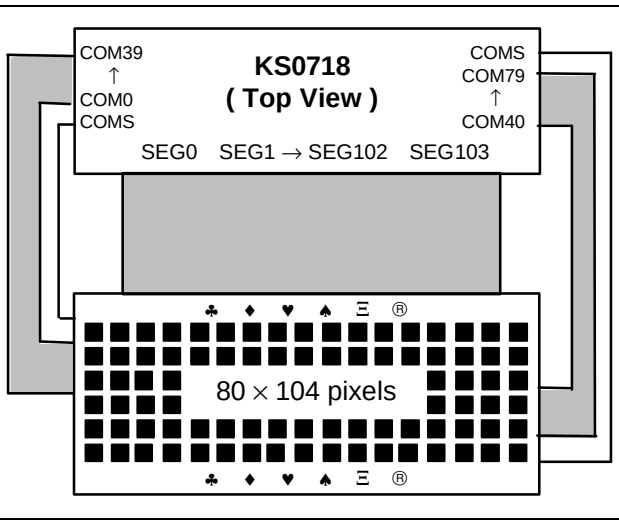

Figure 48. SHL = 0, ADC = 0

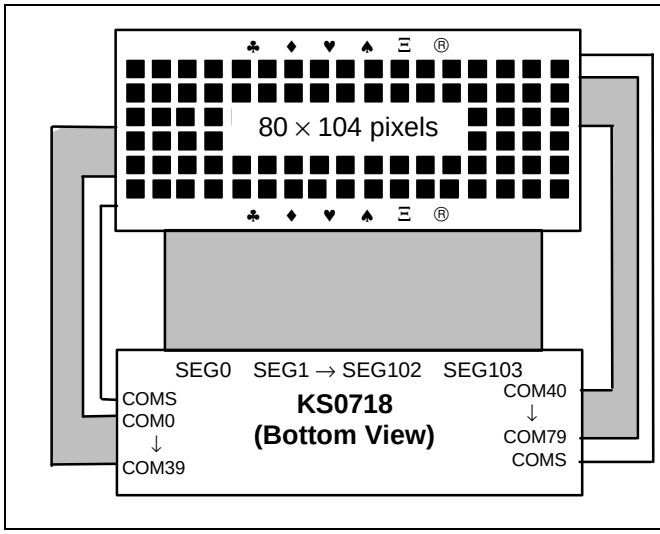

Figure 49. SHL = 1, ADC = 0

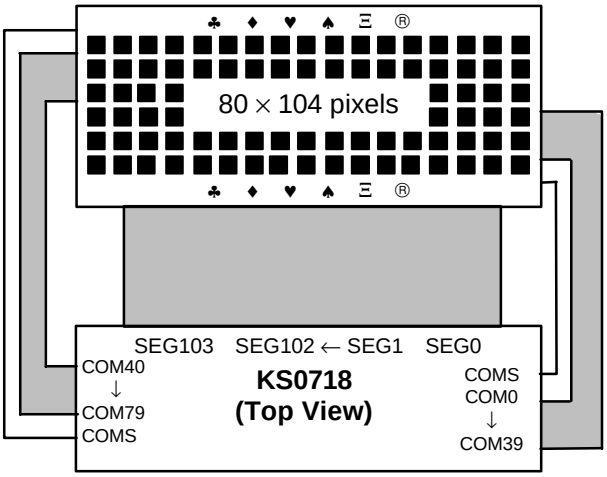

Figure 50. SHL = 1, ADC = 1

Multiple Chip Configurations (1/81 Duty)

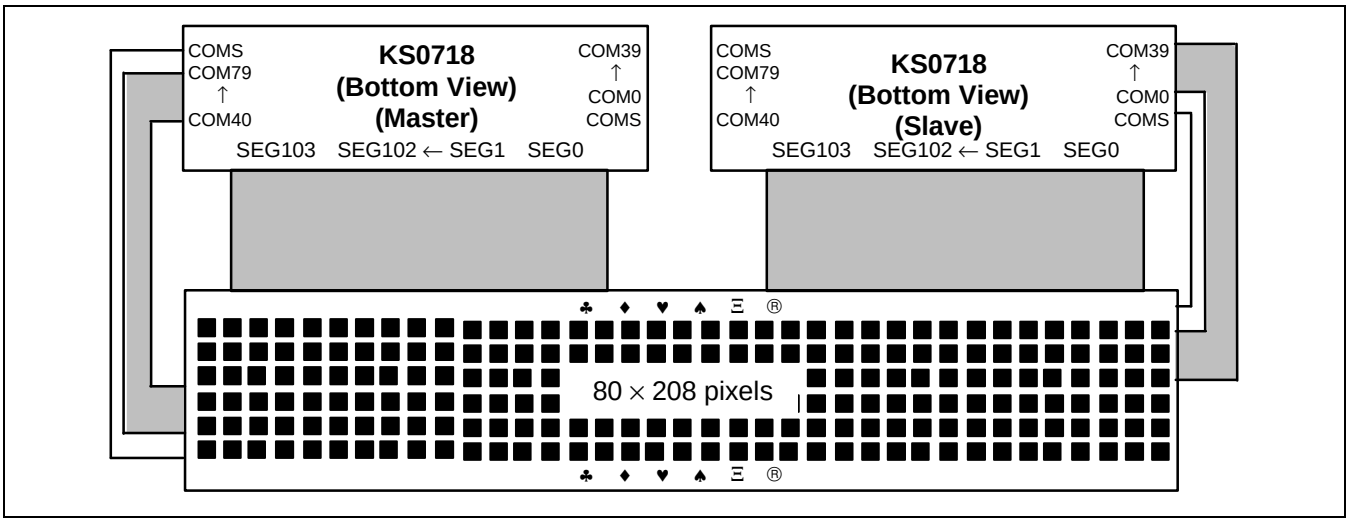

Figure 51. SHL = 0, ADC = 1

- Connect the following pins of two chips each other:
  - Display clock pins: CL, M, SYNC
  - LCD power pins: V0, V1, V2, V3, V4

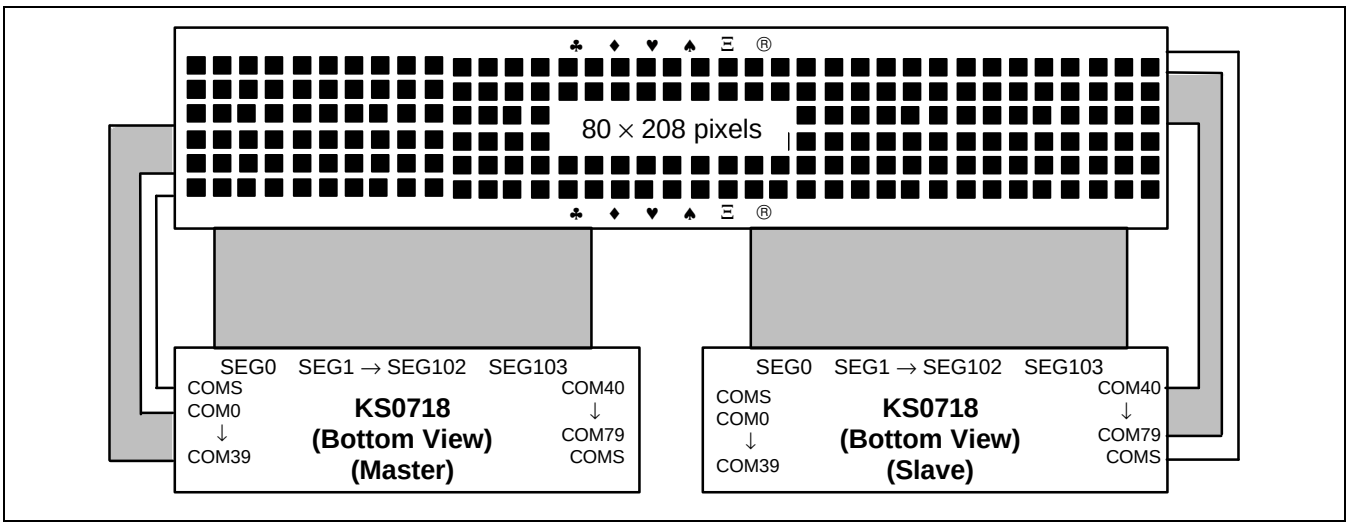

Figure 52. SHL = 1, ADC = 0

- Connect the following pins of two chips each other:
  - Display clock pins: CL, M, SYNC
  - LCD power pins: V0, V1, V2, V3, V4