MDmesh™ PERFORMANCE EVALUATION IN A CONTINUOUS MODE PFC BOOST CONVERTER

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1. ABSTRACT

A new high voltage MOSFET structure is presented which results in static as well as dynamic performances far ahead conventional Power MOSFET devices. The impact of the particular features of the device is analyzed and quantified in a case study regarding a DC-DC boost converter, which is used in a power factor corrector (PFC) converter. Results obtained from the analysis of the electrical and thermal behavior of the component in the specific are discussed.

2. INTRODUCTION.

Standard technology for high voltage suited Power MOSFETs has been dramatically improved, thus the physical limit in terms of reduction of the device's on-state resistance is going to be reached. In fact, such a device parameter is strongly affected by the drain resistivity value, which is designed according to the requirements of the high voltage blocking capability. Recently, an innovative concept of Power MOSFET design has been proposed that is able to enhance the device's performance [1, 2]. In these new devices the charge balance makes the electric field constant over the whole drain volume in spite of the low resistivity in this conducting region. In breakdown conditions the electric field has a value almost equal to the critical one for silicon.

In this paper the main issues of process technology are shortly recalled and discussed. The static and dynamic characteristics are shown aiming to evaluate the advantages of the new device in comparison to standard Power MOSFETs having both the same rated voltage and current carrying capability. Finally, the evaluation of the performance is focused on in a specific application, in particular in a boost-based power factor corrector (PFC) converter.

3. TRENDS ON POWER MOSFET (MDmesh™) DEVICE TECHNOLOGY.

A revolutionary three-dimensional design of the drain device volume is at the basis of the MDmesh™ MOSFET device. The extension of the top strip layout to the whole drain volume, by p-doped column insertion under device stripes, allows a strong resistivity reduction of the conduction n-doped layer and an impressive decrease of the device's on-state resistance when compared to a conventional MOSFET [1]. The cross section of an MDmesh™ device is depicted in figure 1, where both the strip layout and the column insertion under the device stripes are shown. As a consequence of this approach, the known theoretical limit of performance for vertical Power MOSFET devices decreases. In fact, the MDmesh™ MOSFET overcomes this limit allowing a mass production of devices with improved performance and reduced area. For example, a 500V MDmesh™ MOSFET is almost three times smaller than a conventional MOSFET having the same blocking voltage.

Figure 1: Three-Dimensional Cross Section Of MDmesh™ Device
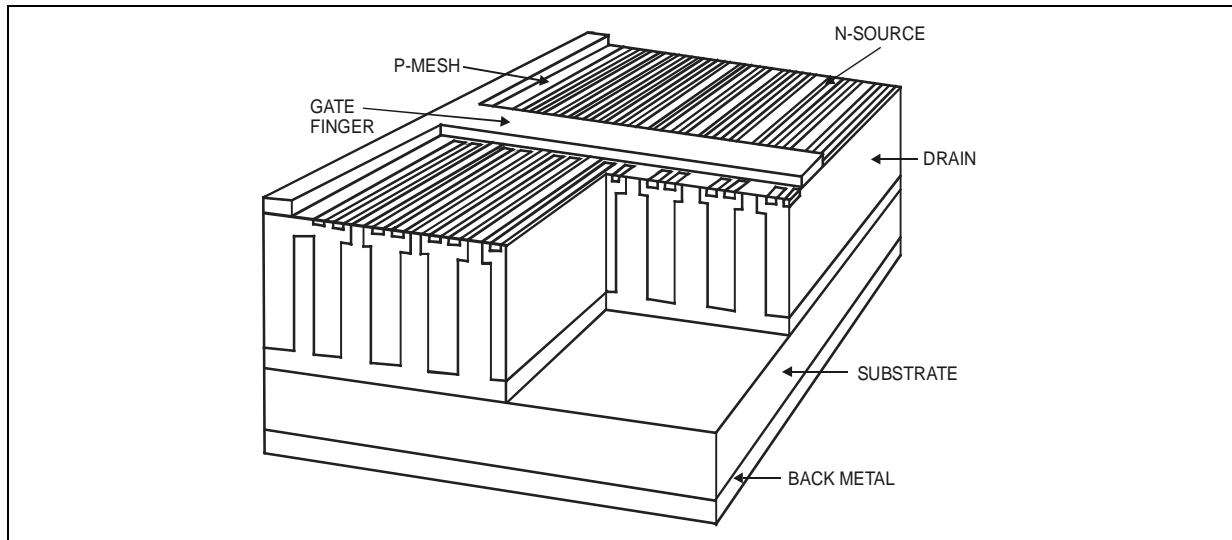
The static output characteristics of an MDmesh™ MOSFET in comparison to a standard device with the same silicon area are reported in figure 2. Moreover, simulation analysis and theoretical considerations show that in MDmesh™ technology the device's on-state resistance increases linearly as function of the breakdown voltage, according to the traces shown in figure 3. The direct consequence of this result is that the extension of the MDmesh™ MOSFETs towards higher blocking voltage values will continually increase the advantages of this technology. The fabrication of a 1000V MDmesh™ MOSFET will require, as expected from the design, a silicon area seven (7) times smaller than a conventional MOSFET with the same on-state resistance and blocking voltage capability. This will cause a package reduction and a major improvement in any application based on these devices, as consequence of the strong reduction obtained on volume and weight of the board. The extension to very high blocking voltage of MDmesh™ MOSFETs will represent a real revolution in high voltage converter applications.

Figure 2: Static Output Characteristics (I/V Curves) Of An MDmesh™ (STP12NM50) And A Standard MOSFET Having Equal Silicon Area
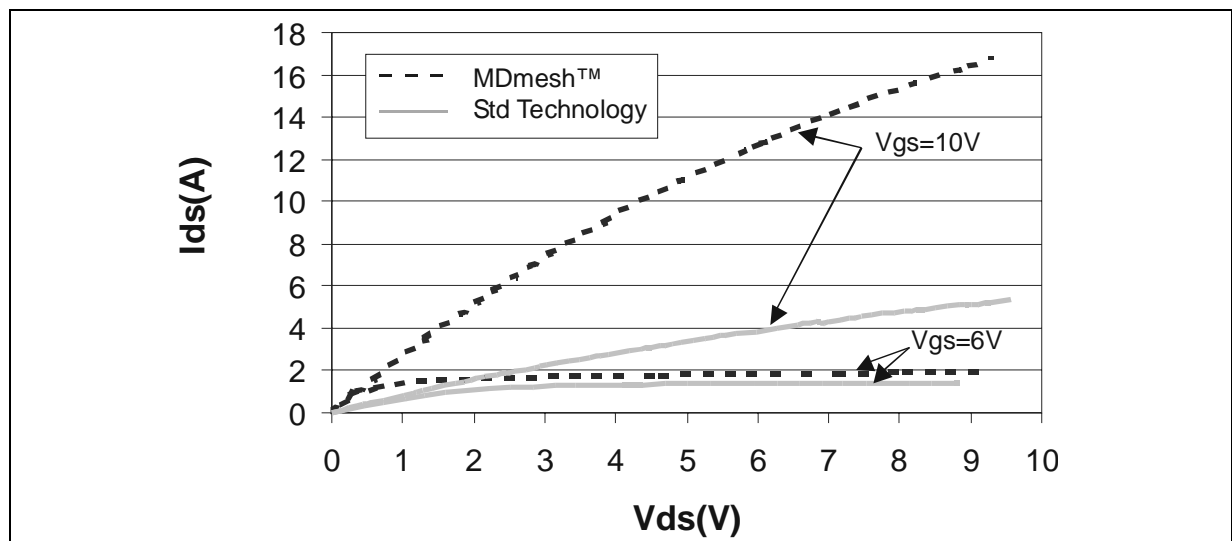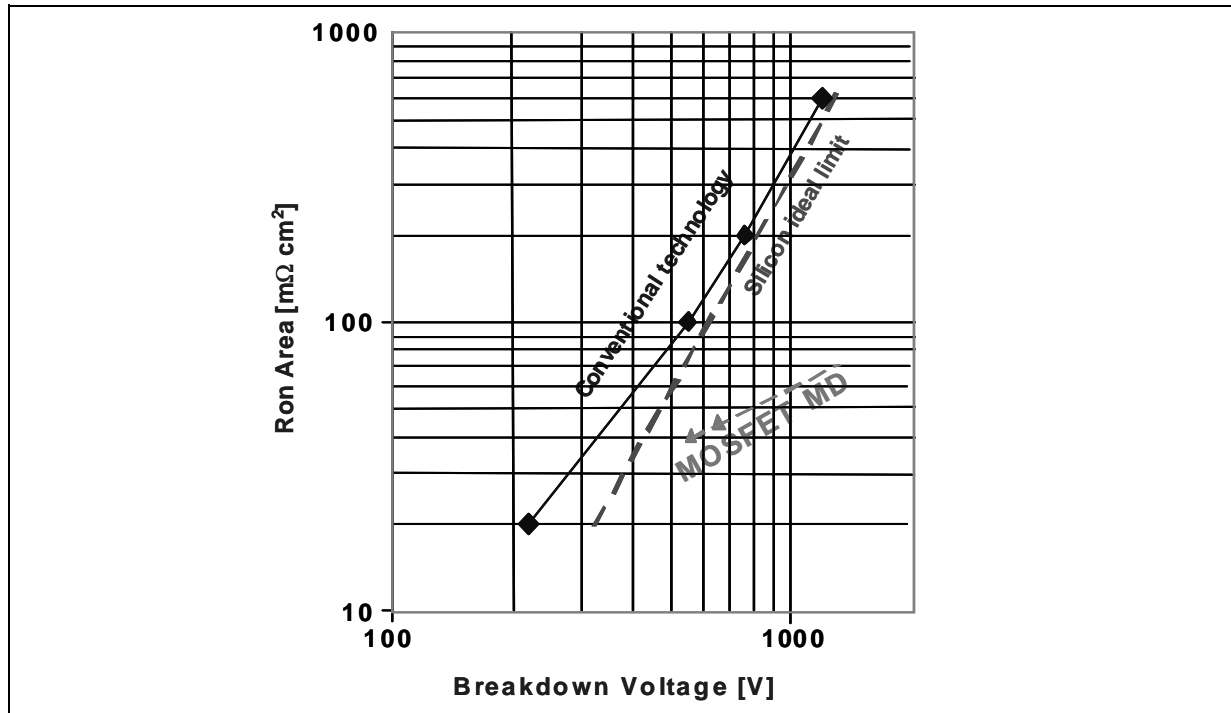
Figure 3: Standard MOSFET and MDmesh™ Dependence Of On-State Resistance As A Function Of The Breakdown Voltage

Another important feature obtained by the proposed approach reduction of the intrinsic capacitances [3], in comparison to the one of a more traditional device, as seen in table 1. In switch mode power supply (SMPS) and PFC applications the reduction of the intrinsic parasitic capacitance allows a commutation time decrease, thus enabling the increase of the switching frequency. As known, this will result in important reduction of both volume and cost of the reactive components used to filter the output and/or electrical quantities.

Table 1. Main Characteristics Comparison

	Part Number	BV_{DSS} [V]	$R_{DS(on)}$ @ 25°C [Ohm]	Ciss [pF]	Coss [pF]	Crss [pF]	Package
Standard	STW15NB50	>500	0.36	2600	330	40	TO-247
MDmesh™	STP12NM50	>500	0.38	1000	160	25	TO-220

4. SWITCHING CHARACTERISTICS.

A characterization of the new device has been carried out in order to give evidence to the good switching performance of the new device. The silicon area shrinking allowed by the MDmesh™ technology adds a further benefit to the device's gate charge due to the parasitic capacitance reduction. The gate charge comparison of figure 4 refers to two devices with equal rated electrical characteristics. At the driving voltage of 10V the MDmesh™ requires a gate charge reduced by a factor of 3.5 in respect to the traditional counterpart, at a drain current of 12A and a drain-source voltage of 200V. The charge stored in the input capacitance is reduced from 50nC (STW15NB50) to 25nC (STP12NM50). This immediately suggests to the end-user an effective driving loss reduction. Moreover, as a consequence, this feature allows an improvement of the performance during the switching transients in comparison with conventional devices [4].

The switching transient evaluation has been performed at room temperature on inductive load at several gate-driving conditions. The main quantities of a typical commutation, in hard switching conditions on inductive load, are reported in table 2, while in figure 5 the traces of an experimental turn-off switching transients are shown.

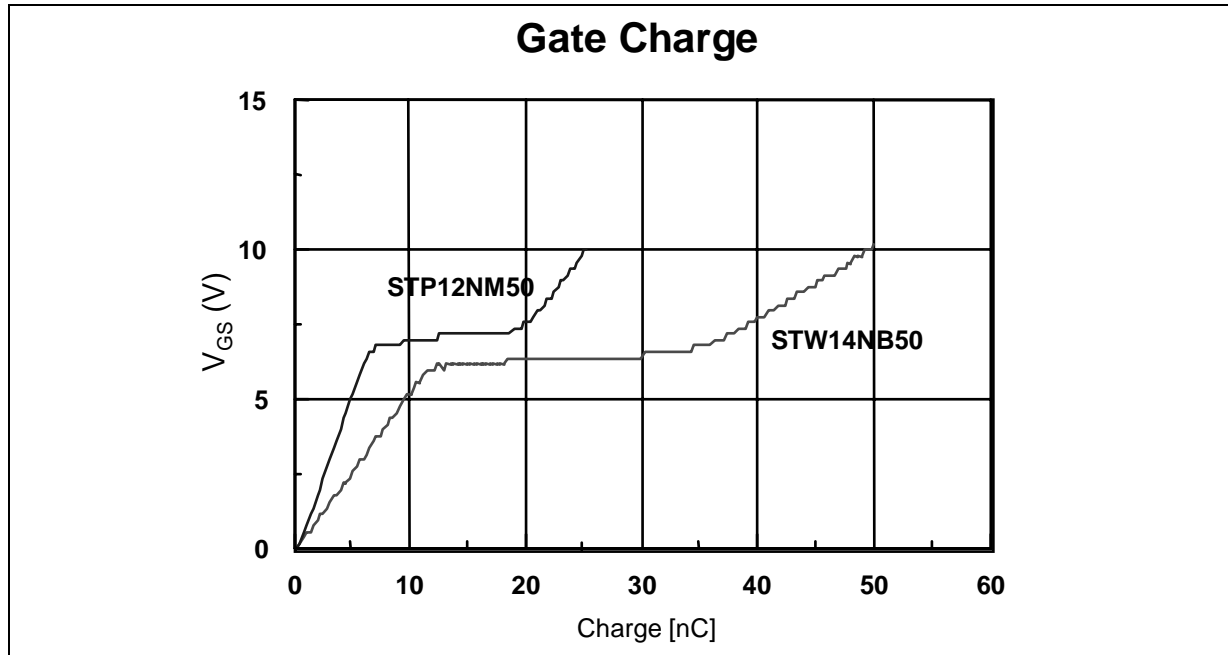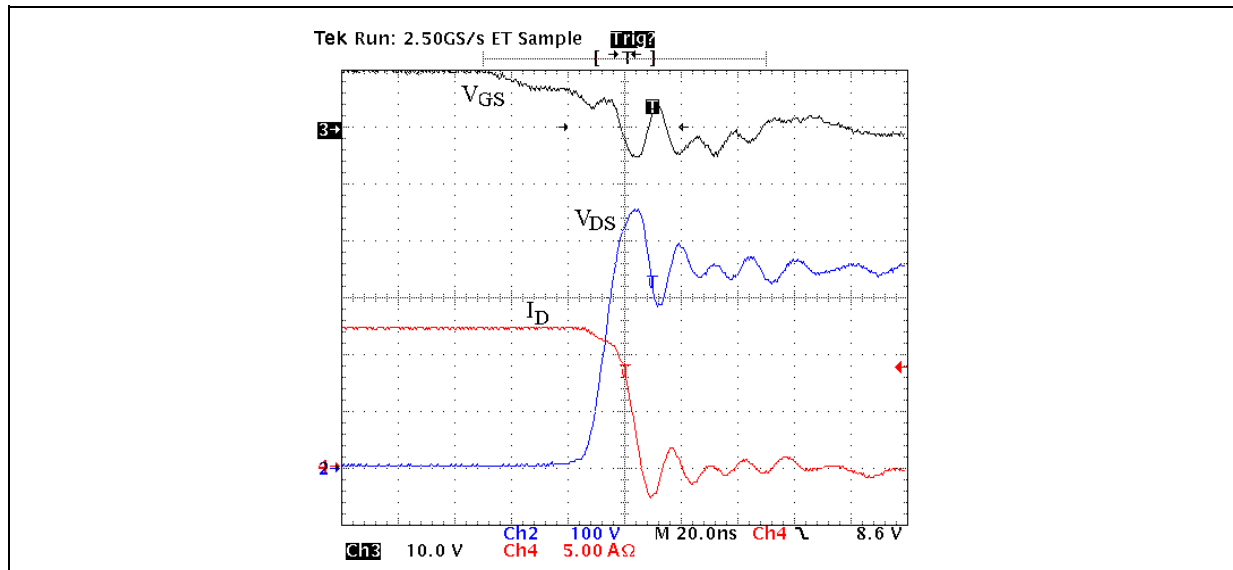**Figure 4: Gate Charge Behavior Of Two Different Power MOSFET Devices**

Table 2. MDmesh™ Typical Switching Quantities (RG=4.7Ohm)

| E_{off} [μJ]	t_{fall} [ns]	t_{rise} [ns]	di/dt [A/ns]	dv/dt [V/ns]	t_{delay} [ns]
28.6	10.8	7.6	888.9	36.84	33.6

Figure 5: Current And Voltage Traces During A Typical Turn-Off Transient Of An MDmesh™ (V_{DS}=100V/div, V_{GS}=10V/div, I_D=5A/div, t=20ns/div)

5. INTRINSIC BODY-DRAIN DIODE.

In some industrial equipment, which requires a converter configuration with bi-directional switches, the intrinsic diode of the MOSFET device may be used as antiparallel diode if its own characteristics are adequate. In order to optimize the design, the performance of the body-drain diode of the new device has been investigated. In particular, the switching behavior of the body-drain diode has been widely tested. The well-established technique of Platinum implanting has been performed in order to reduce the reverse recovery time (t_{rr}) of the body-drain diode by reducing the carrier lifetime. Platinum implanting acts as a lifetime killer by introducing a mid gap center in the silicon. By increasing the Platinum dose (Φ) a t_{rr} reduction is observed. The obtained experimental waveforms during a reverse recovery transient for three devices with different Platinum doses are reported in figure 6 that is related to a current slope di/dt equal to 100A/ms.

Figure 6: Reverse Recovery Of The Body-Drain Diode In Case Of Different Platinum Doses (ID=5A/div, t=100ns/div)
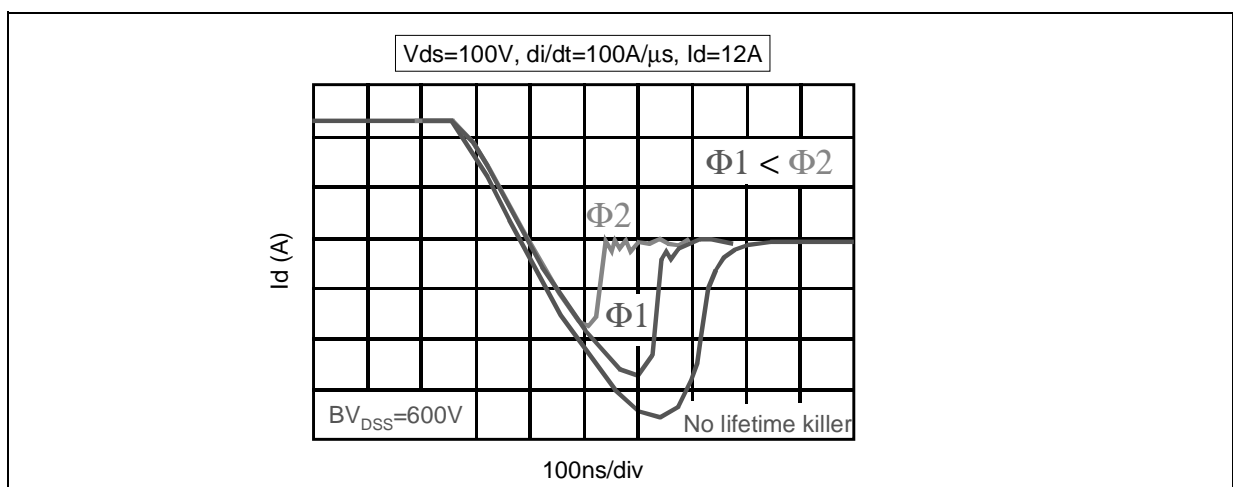
6. MDmesh DEVICE IN A PFC CONVERTER APPLICATION.

Power MOSFET devices are very suitable for many power converter applications, operating at high frequency, which have been proposed aiming to develop SMPS with high power factor value. In these applications the devices experience high voltage, low current and high frequency. In particular, a PFC circuit has been considered, which is based on a boost converter topology in order to obtain high power factor. The control of the converter is performed by an L4981A integrated circuit that behaves as a continuous mode PFC controller and uses the technique of the average current control [5]. A prototype of the converter has been prepared and its simplified schematic is shown in figure 7.

Figure 7: A Simplified Block Schematic Of The Control Stage And Power Stage Of The PFC Application
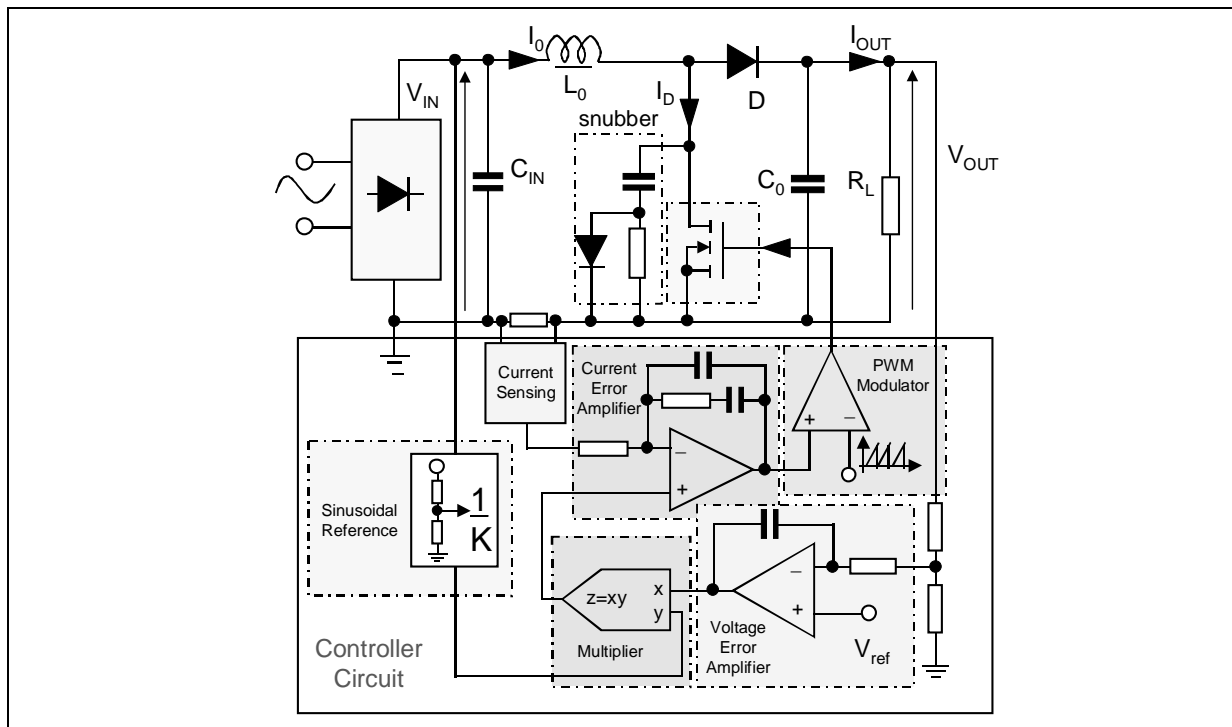
The constraints adopted to design the PFC converter are the following:
• Input AC voltage from universal mains VIN=88V up to 264V, frequency 50/60Hz;
• DC regulated output voltage VOUT=400V;
• Full load output ripple voltage DVr<16V;
• Rated output power POUT=200W;
• Maximum output voltage VO(max)=450V;
• Switching frequency in the range of 100-200kHz;
• Maximum inductor current ripple DIL=35%;
• Input power factor PF>0.99;
• Total harmonic distortion of the line current < 5%.

The values of some passive components of the converter circuit are reported in table 3 in the case of two different switching frequencies, namely 100kHz and 200kHz. In the structure of the PFC converter a

snubber circuit has been used for the switching device in order to reduce its power losses and to maintain a low value of the dv/dt looking for the EMI requirements. According to the design criteria of the RCD snubber, and by imposing for the drain voltage to have a rise time t_r=40ns, the capacitor value has been fixed at C=350pF (630V) while the resistance value depends on the working frequency.

The value is R=1.8kOhm at 100kHz, and 680Ohm at 200kHz. The efficiency of the power converter is mainly dependant on the power losses of both the switching device and the snubber circuit.

Table 3. Passive Component Values Selected For Two Switching Frequencies

Switching Frequency [kHz]	L_0 [mH]	C_{IN} [nF]	C_0 [µF]
100	0.9	220	100
200	0.45	114	100

7. THERMAL BEHAVIOR OF THE POWER SWITCH.

The total power losses P_t of a switching device can be split into the following components: the commutation power losses (turn-on and turn-off) and the on-state power losses:

$$P_t = P_{ON} + P_{OFF} + P_{con} \qquad (1)$$

The turn-on losses, which depend on both the diode choice and the dv/dt imposed by the $R_{G(on)}$, can be designed as a trade off between the power losses and the EMI requirements. The snubber circuit reduces the turn-off switching power losses, which, in turn, cannot be included. The main contribute to the device power losses is given by the conduction component that depends on the $R_{DS(on)}$ of the device. With reference to the symbol used in figure 7, the rms current on the inductor is given by:

$$I_0 = \frac{P_{OUT}}{\eta V_{IN}} \qquad (2)$$

where η is the converter efficiency. The current reaches a maximum value at the minimum value of the main voltage $V_{IN,MIN}$. From relation (2) and by considering that the duty cycle of the switch is modulated at twice the frequency of the main line, the *rms* current in the MOSFET can be calculated by (as given in [6]):

$$I_D = \frac{P_{OUT}}{\eta V_{IN}} k\left(\frac{V_{IN}}{V_{OUT}} L, f_s, R_0\right) \qquad (3)$$

where the function *k* operates as a reduction factor. Finally the on-state power losses P_{con} can be evaluated by:

$$P_{con} = R_{DS(on)} I_D^2 \qquad (4)$$

At constant output power this value changes according to the variation of the main voltage. The maximum value of this rms current occurs in the case of the lowest value of the main voltage $V_{IN,MIN}$ (88V). In the case study a typical figure for the efficiency η is in the range 0.88-0.90. The maximum peak value of the device current is given by:

$$I_{D,max} = I_{0,max} + \frac{\Delta I_0}{2} \qquad (5)$$

where ΔI_0 is the current ripple on the inductor.

Calculating from (5) for the $I_{D,max}$ gives a current of 4A in the case of 200W output of the converter. Moreover, accounting for the peak of the current due to the reverse recovery of the diode, and by adding a suitable safe margin, a switching device with a rated current carrying capability of 8A has been selected. The breakdown voltage of the device is determined according to the following relation:

$$BV_{DSS} \geq V_{OUT} + \Delta V_r + V_m \qquad (6)$$

where the voltage V_m is a suitable value ranging between 10% and 15% of the maximum output voltage. With the above constraints, we need a device having at least BV_{DSS}=500V.

Finally, the freewheeling diode has been specified as a 6A, 600V fast diode, with a reverse recovery time t_{rr}=25ns.

8. JUNCTION TEMPERATURE CALCULATION.

A dynamic characterization of the Power MOSFET has been carried out. The device is very fast and has a good switching performance. The current and voltage waveforms of the device during a typical turn-off transient are reported in figure 8. We can observe that the rise time of the drain voltage in the case shown is coherent with the design constraints on the voltage slope.

Figure 8: Turn-Off Switching Transient In The PFC Converter At A Main Voltage Of 88V (V_{DS}=100V/ div, I_D=2A/div, E=1kVA/div, t=50ns/div)
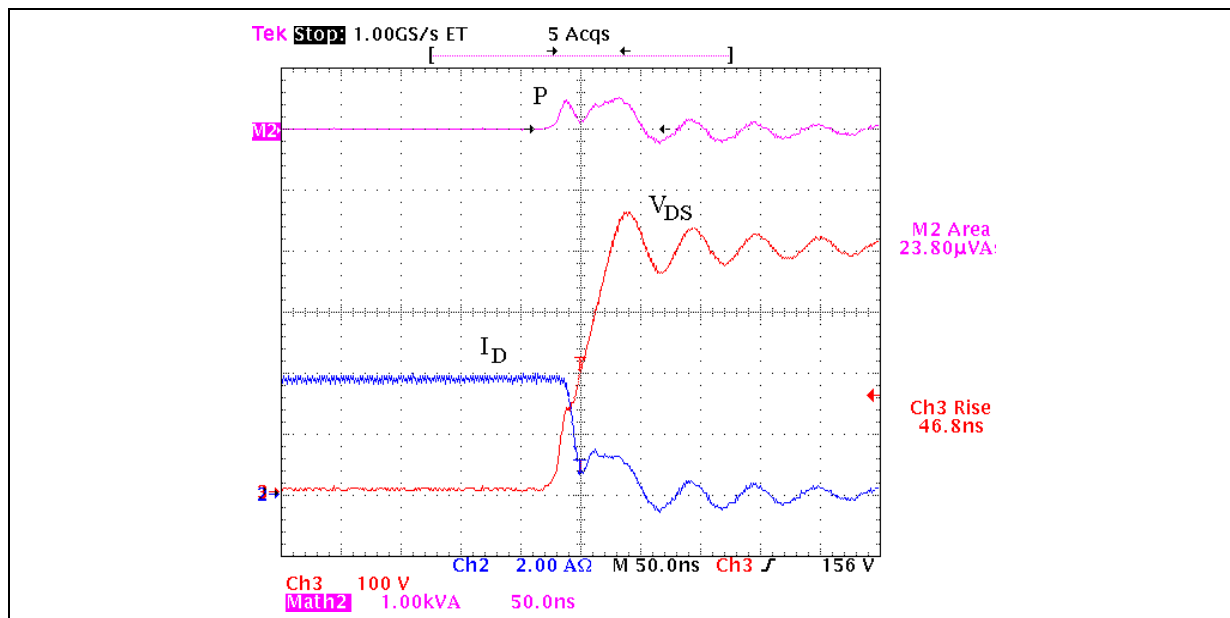
The thermal behavior has been performed by a set-up measurement shown in figure 9, where the thermal model of the device is also indicated. In steady state condition we measured the heatsink temperature at a different value of the input voltage, and namely at 88V, 110V and 220V. The junction temperature is higher than the heatsink temperature and can be estimated by the following procedure.

Figure 9: Block Schematic Of The Measurement System To Determine The Heatsink Temperature, As Well As The Steady State Thermal Model Of The Device
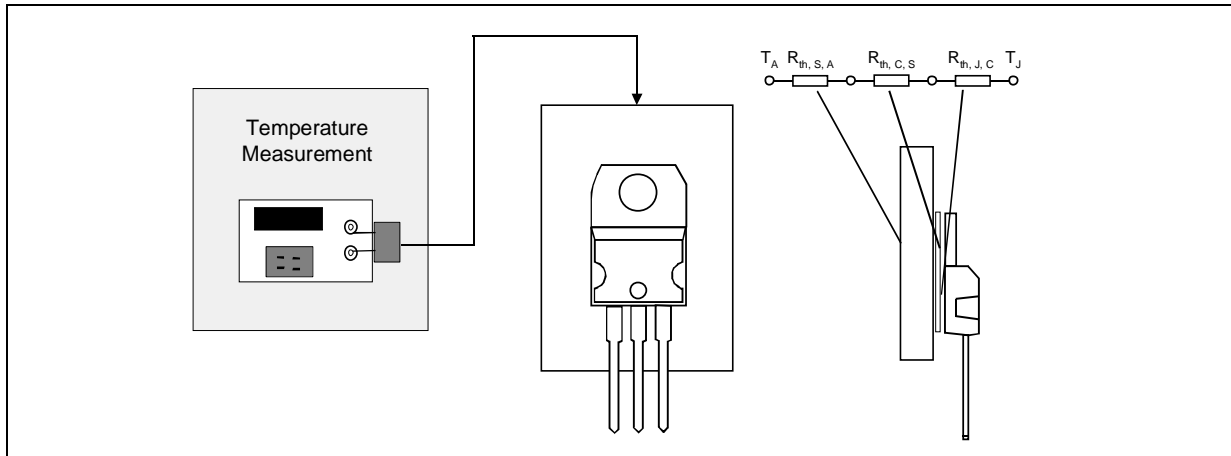
Firstly, the power loss is calculated:

$$P_D = \frac{T_H - T_A}{R_{th(H,A)}} \qquad (7)$$

where T_H is the measured heatsink temperature, T_A is the ambient temperature fixed at 27°C, and $R_{th,H,A}$ is the thermal resistance of the heatsink established at 7°C/W. Then the junction temperature is calculated by:

$$T_j = T_H + P_D(R_{th(J,C)} + R_{th(C,H)}) \qquad (8)$$

where T_J is the junction temperature, $R_{th(J,C)}$ is the thermal resistance between the junction and the case and $R_{th(C,H)}$ is the thermal resistance between the case and the heatsink. The results for the two switching frequencies considered are reported in table 4. Other results obtained for the same output power and the results of the experimental tests done at different voltages and frequencies are reported in table 5. The tests have been carried out at the beginning of the experiments (room temperature, T=27°C) and in steady state conditions.

Table 4. Heatsink And Junction Temperatures For Different Voltage And Frequency Values

V_{IN} [V]	T_H [°C]	P_D [W]	T_J [°C]
100kHz			
88	92	9.28	107
110	70	6.14	80
220	46	2.71	50
220kHz			
88	98	10.14	114.5
110	75	6.86	86.2
220	49	3.14	54.1

Table 5. Results Of The Experimental Tests At Different Voltages And Frequencies

T_H [°C]	V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	$\eta\%$
100kHz							
27	88	2.4	211	393.7	0.485	191	90.5
92		2.472	217	395.8	0.488	193.1	89
27	110	1.88	206.6	394.6	0.484	190.9	92.4
70		1.931	212.3	397.1	0.49	194.6	91.8
27	220	0.934	204.5	396.8	0.49	194.4	95.1
46		0.948	206.3	397	0.489	194.1	94.7
200kHz							
27	88	2.487	217.8	395	0.482	190.4	87.4
98		2.577	226.7	395	0.483	190.8	84.2
27	110	1.957	211.9	398	0.489	195	92
75		2.016	220.7	398	0.499	198.6	90
27	220	0.959	211	398.5	0.49	195.3	93
49		0.968	213	398	0.49	195	91.6

9. HARMONIC DISTORTION.

The main results for the converter from the stand point of the harmonic content are reported in table 6, where the term A-THD% stands for the total-harmonic-distortion (in percentage) of the main current, and PF is the power factor. The test-rig used to obtain the data given in table 6 is depicted in figure 10. The better performance of the PFC is at a main voltage of 110V and 60Hz. In figure 11 we can see the near zero-value of the phase shift between the input waveforms of the voltage and current. The PF measured in such a case is 0.999, as reported in table 6. Finally, the voltage and current traces in a whole switching cycle of the MDmesh™ device are reported in figure 12a, 12c. The test conditions are switching frequency 200kHz and main voltage $V_{IN, MIN}$=88V.

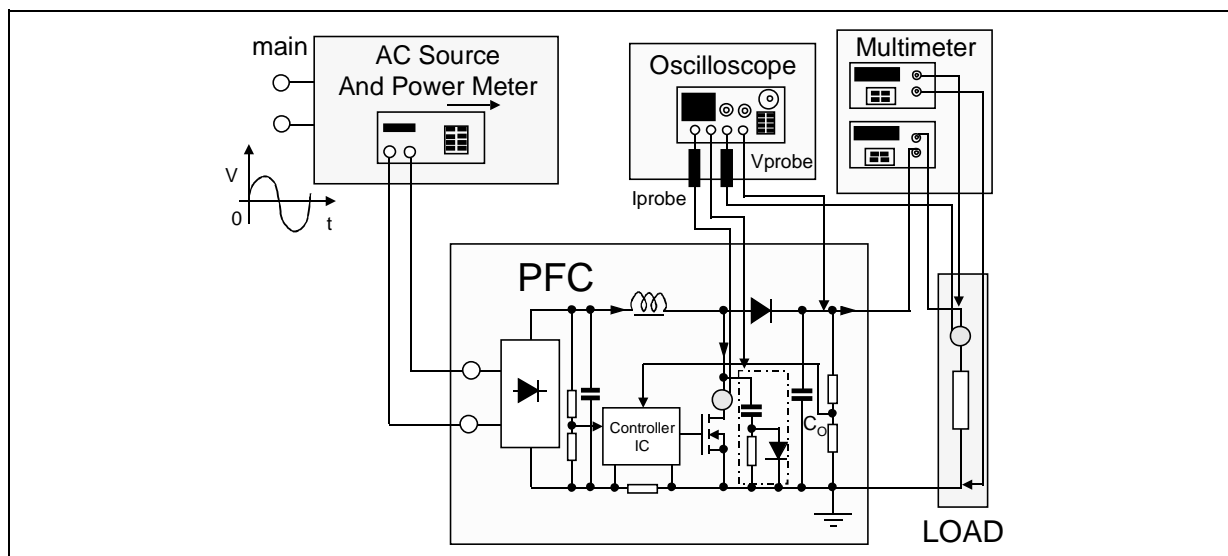**Figure 10: Experimental Set-Up To Measure The Harmonic Distortion And The Power Factor**

Figure 11: Experimental Traces Of The Input And Output Waveforms (V$_{IN}$=110V, f=60Hz, f$_s$=200kHz, V$_{IN}$=100V/div, V$_{OUT}$=100V/div, I$_{OUT}$=500mA, I$_{IN}$=1A/div, t=2ms/div)
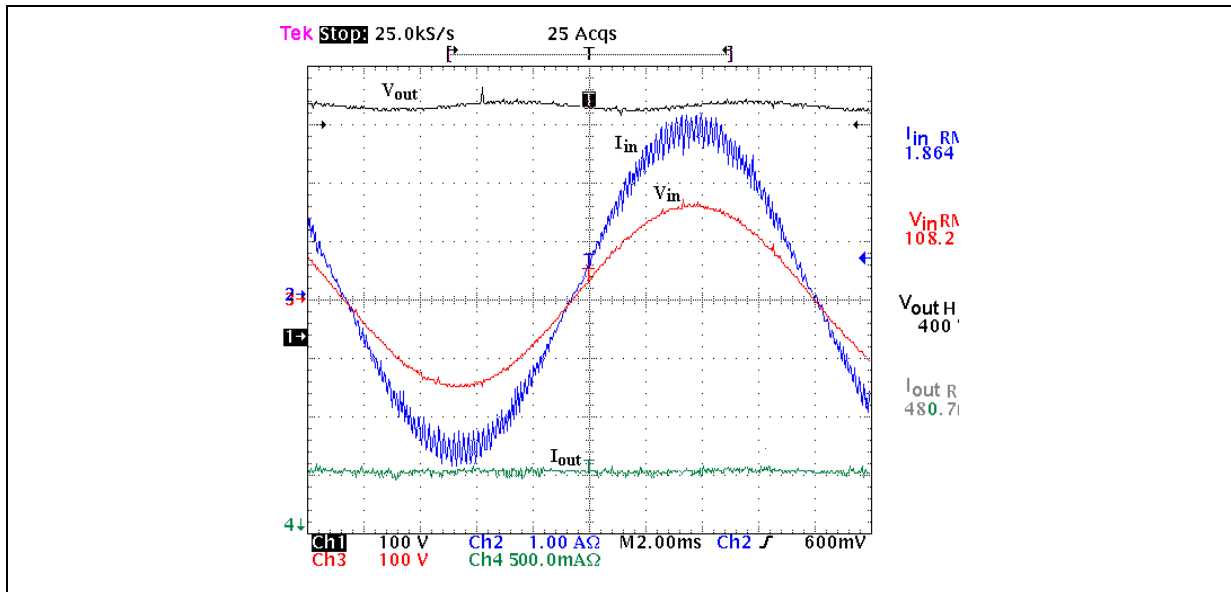

Figure 12a: Working Cycles Of The Power MOSFET Device In Loaded Conditions @ 200kHz (V$_{DS}$=100V/div, I$_D$=2A/div, t=1µs/div)
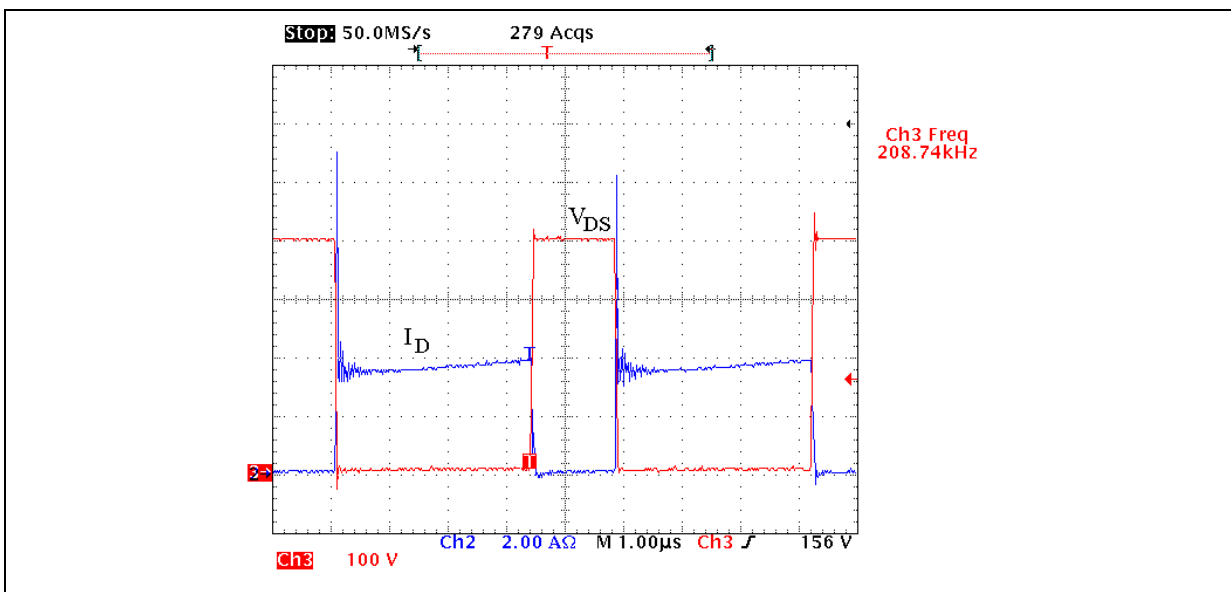
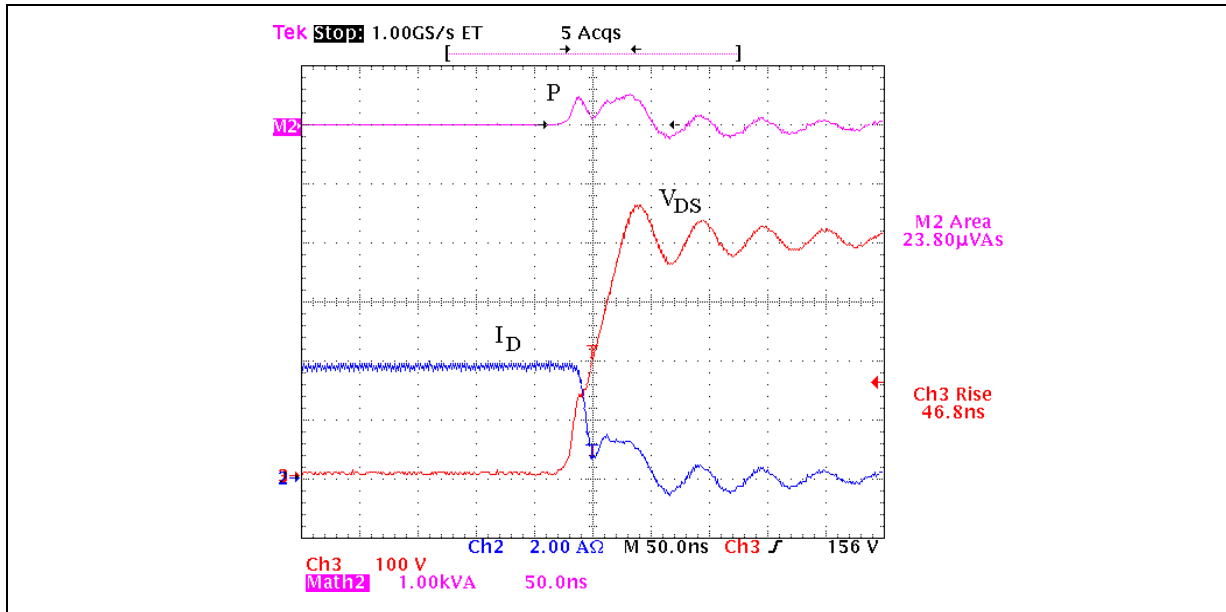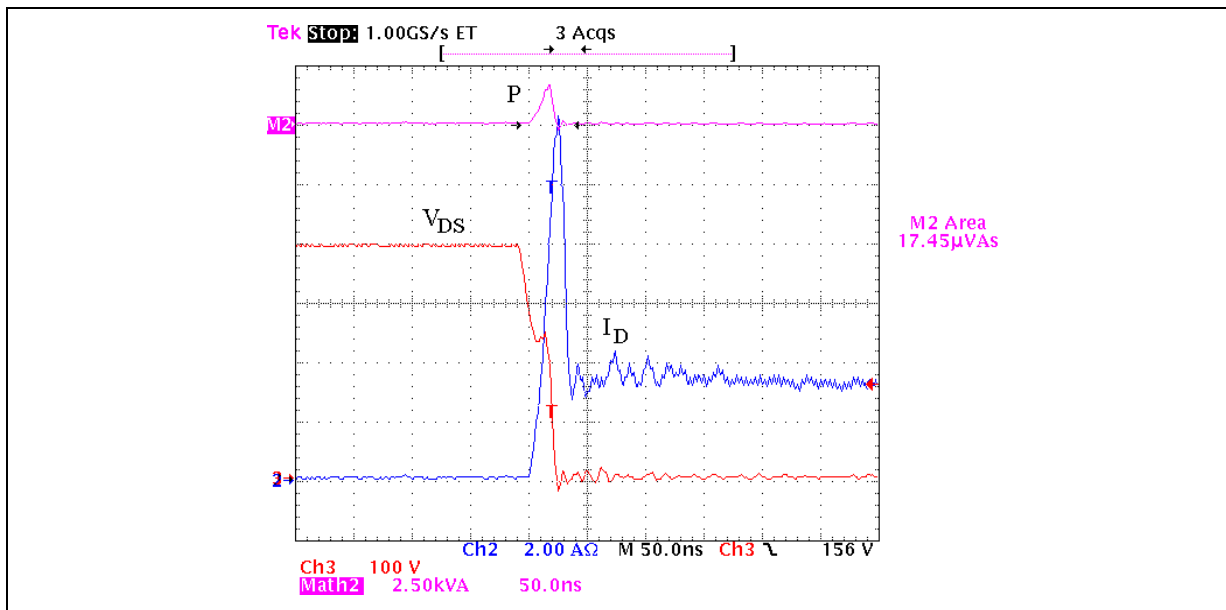**Figure 12b: The MDmesh™ Turn-off In Loaded Conditions (V$_{DS}$=100V/div, I$_D$=2A/div, E=1kVA/div, t=50ns/div)**

Figure 12c: The MDmesh™ Turn-on In Loaded Conditions (V$_{DS}$=100V/div, I$_D$=2A/div, E=1kVA/div, t=50ns/div)

Table 6. Performance Of The PFC As A Non-linear Switching Load

V_IN [V]	f_s [Hz]	I_IN [A]	PF	A - THD%	V_OUT [V]	ΔV_OUT [V]
f = 100kHz						
88	60	2.472	0.9984	4	393.7	13
110	60	1.931	0.994	2.4	394.6	13
220	50	0.948	0.9976	4.9	396.8	14
f = 200kHz						
88	60	2.577	0.9986	3.7	393	15
110	60	2.016	0.997	1.7	394.6	14
220	50	0.968	0.9981	4.4	397	15

10. DISCUSSION OF THE RESULTS.

The new device features good performance in the experimental tests. In particular, the device works very well in terms of efficiency and harmonic distortion in a typical power conversion application, like the PFC. However, it is worth it to note that equivalent results may be obtained by traditional Power MOSFETs having a larger silicon area. In fact, an equivalent standard device should have two times the area of the device presented here. The consequence is a smaller package for the MDmesh™ device than a standard MOSFET, and a lower cost. However, in such a case at equal power losses the smaller device will assume a greater junction temperature. Obviously we are presuming different total thermal resistance, which is the case. On the other hand, the new equivalent device has a high current density, good switching performance and on-state losses comparable to standard MOSFETs.

11. CONCLUSION.

In this paper an extended characterization of a new class of Power MOSFETs has been performed. The advantages and drawbacks relative to the new device has been highlighted. An important improvement in comparison with equivalent conventional devices consists in the area reduction of the silicon. As a consequence the current density of the proposed device is higher than the current density of a standard one. The switching performance is improved due to the lower parasitic capacitance and the low on-state resistance adds major advantages in terms of forward voltage drop.

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