Preliminary Information

AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Revision Guide

Publication # **25912**	Revision: **3.00**
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Revision History

Date	Revision	Description
June 2003	3.00	Initial public release.

AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Revision Guide

The purpose of the *AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Revision Guide* is to communicate updated product information on the AMD-8151™ HyperTransport™ AGP3.0 graphics tunnel to designers of computer systems and software developers. This guide consists of three major sections:

- **Revision Determination:** This section, which starts on page 6, describes the mechanism by which the current revision of the part is identified.
- **Product Errata:** This section, which starts on page 7, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from product specifications, and as such may cause the behavior of the AMD-8151 HyperTransport AGP3.0 graphics tunnel to deviate from the published specifications.
- **Documentation Support:** This section, which starts on page 13, provides a listing of available technical support resources.

Revision Guide Policy

Occasionally, AMD identifies product errata that cause the AMD-8151 HyperTransport AGP3.0 graphics tunnel to deviate from published specifications. Descriptions of identified product errata are designed to assist system and software designers in using the AMD-8151 HyperTransport AGP3.0 graphics tunnel. Furthermore, this revision guide may be updated periodically.

Revision Determination

The BIOS checks the PCI revision ID register at DevA:0x08 to determine the version of silicon as shown in Table 1.

Table 1. AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Revision IDs

Sequence	Revision	DevA:0x08 DevB:0x08
5	B2	13h

Product Errata

This section documents AMD-8151™ HyperTransport™ AGP3.0 graphics tunnel product errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the part to each erratum. An "X" indicates that the erratum applies to the revision. The absence of an "X" indicates that the erratum does not apply to the revision.

Note: *There may be missing errata numbers. Errata that have been resolved from early revisions of the device have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 2. Cross-Reference of Product Revision to Errata

Errata Numbers and Description	Revision Number
	B2
22 Incorrect Value For DevA:0xA4[Host translation#]	X
23 Link Electrical Issue When Operating At 800 MHz	X
24 Deadlock Scenario With Peer-To-Peer Traffic	X
25 Input Leakage Parameter Out Of Spec	X
26 DevB:0x00[DevID] Is Read Only	X

22 Incorrect Value For DevA:0xA4[Host translation#]

Description

DevA:0xA4[Host translation#] is a read-only bit, fixed in the high state in the graphics tunnel. Per the AGP specification, this indicates that core logic does not translate host transactions addressed to the Graphics Aperature through the GART. However, on AMD platforms that use the graphics tunnel, such host transactions can be translated through the GART.

Potential Effect on System

None.

Suggested Workaround

Software should presume that this bit is low for the graphics tunnel.

Fix Planned

No

23 Link Electrical Issue When Operating At 800 MHz

Description

The graphics tunnel A-side link may not operate properly at 800 MHz.

Potential Effect on System

Transfer of erroneous data and system deadlocks are possible.

Suggested Workaround

The A-side link should be configured to operate at 600 MHz instead of 800 MHz.

Alternatively, more restrictive system board layout rules for the A-side link may be employed. See the *AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Motherboard Design Guide,* order# 25617 for details.

Fix Planned

No

24 Deadlock Scenario With Peer-To-Peer Traffic

Description

Some PCI cards generate peer-to-peer posted-write traffic targeting the AGP bridge (from the PCI bus, through the graphics tunnel, to the host, back to the graphics tunnel to the AGP bus). The combination of such cards and some AGP cards can generate traffic patterns that result in a system deadlock.

Potential Effect on System

The system deadlocks.

Suggested Workaround

Do not support PCI cards that generate peer-to-peer traffic to the AGP bridge.

Fix Planned

No

25 Input Leakage Parameter Out Of Spec

Description

When operating with AGP2.0 signaling, the input leakage current (I_{LI}) is specified to be limited to less than ±10 μA. However, input leakage current may be as much as ±20 μA in some graphics tunnel parts.

Potential Effect on System

None.

Suggested Workaround

None required.

Fix Planned

No

26 DevB:0x00[DevID] Is Read Only

Description

The four LSBs of DevB:0x00[DevID] should be "write once". However, they are "read only" instead.

Potential Effect on System

A generic graphics driver may be loaded even if the platform does not support the generic driver.

Suggested Workaround

None required.

Fix Planned

No

Documentation Support

The following documents provide additional information regarding the operation of the AMD-8151™ HyperTransport™ AGP3.0 graphics tunnel:

- *AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Data Sheet*, order# 24888
- *HyperTransport™ I/O Link Specification* (www.hypertransport.org)

See the AMD Web site at *www.amd.com* for the latest updates to documents. For documents subject to a non-disclosure agreement, please contact your local sales representative.