



TABLE 1. PIN DESCRIPTION

| PIN | SYMBOL              | DESCRIPTION  |
|-----|---------------------|--|
| 1   | $V_{IN}$            | Analog Input Range: $V_{REF(-)}$ to $V_{REF(+)}$ .   |
| 2   | DB0                 | Data Output. Three State Output, bit 0 (LSB)   |
| 3   | DB1                 | Data Output. Three State Output, bit 1   |
| 4   | DB2                 | Data Output. Three State Output, bit 2   |
| 5   | DB3                 | Data Output. Three State Output, bit 3   |
| 6   | $\overline{WR/RDY}$ | WRITE control input/READY status output.   |
| 7   | Mode                | Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. It is internally tied to GND through a 50 $\mu$ A current source.   |
| 8   | $\overline{RD}$     | READ Input. $\overline{RD}$ must be low to access data from the part.  |
| 9   | $\overline{INT}$    | INTERUPT Output. $\overline{INT}$ going low indicates that the conversion is complete $\overline{INT}$ returns high on rising the edge of $\overline{RD}$ or $\overline{CS}$ .   |
| 10  | GND                 | Ground   |
| 11  | $V_{REF-}$          | Lower limit of reference span. Range: $GND \leq V_{REF(-)} \leq V_{REF(+)}$  |
| 12  | $V_{REF+}$          | Upper limit of reference span. Range: $GND \leq V_{REF(-)} \leq V_{REF(+)} \leq V_{DD}$  |
| 13  | $\overline{CS}$     | Chip Select Input. $\overline{CS}$ , the decoded device address, must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.   |
| 14  | DB4                 | Data Output. Three State Output, bit 4   |
| 15  | DB5                 | Data Output. Three State Output, bit 5   |
| 16  | DB6                 | Data Output. Three State Output, bit 6   |
| 17  | DB7                 | Data Output. Three State Output, bit 7 (MSB)   |
| 18  | $\overline{OFL}$    | Overflow Output. If the analog input is higher than $(V_{REF(+)} - 1/2LSB)$ , $\overline{OFL}$ will be low at the end of conversion. It is a non three state output which can be used to cascade 2 or more devices to increase resolution. |
| 19  | NC                  | No Connection.   |
| 20  | $V_{DD}$            | Power supply voltage, +5V  |

TABLE 2. 7820 ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| PARAMETER  | MIN            | MAX            | UNIT |
|--|----------------|----------------|------|
| $V_{DD}$ to GND                                    | -0             | 7.0            | V    |
| Digital Input Voltage to GND (Pins 6-80, 13)       | -0.3           | $V_{DD} + 0.3$ | V    |
| Digital Output Voltage to GND (Pins 2-5, 9, 14-18) | 0.3            | $V_{DD} + 0.3$ | V    |
| $V_{REF (+)}$ to GND                               | 0              | $V_{DD} + 0.3$ | V    |
| $V_{REF (-)}$ to GND                               | $V_{SS} - 0.3$ | $V_{REF (+)}$  | V    |

TABLE 2. 7820 ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| PARAMETER                 | MIN  | MAX                  | UNIT  |
|---------------------------|------|----------------------|-------|
| V <sub>IN</sub> to GND    | -0.3 | V <sub>DD</sub> +0.3 | V     |
| Operating Temperature     | -55  | 125                  | °C    |
| Storage Temperature Range | -65  | 150                  | °C    |
| Power Dissipation to 75°C | --   | 450                  | mW    |
| Derates above +75°C       | --   | 6                    | mW/°C |

1. **CAUTION:** ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

TABLE 3. 7820 DC ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +5V; V<sub>REF(+)</sub> = +5V; V<sub>REF(-)</sub> = GND = 0V, UNLESS OTHERWISE SPECIFIED) (RD MODE (PIN 7 = 0V))  
(T<sub>A</sub> = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER  | TEST CONDITIONS | SUBGROUPS | MIN                 | TYP | MAX                 | UNIT |
|--|-----------------|-----------|---------------------|-----|---------------------|------|
| <b>Accuracy</b>  |                 |           |                     |     |                     |      |
| Resolution   | --              |           | 8                   | --  | --                  | Bits |
| Total Unadjusted Error <sup>1</sup>                          | --              |           | --                  | --  | ±1.0                | LSB  |
| Minimum Resolution for which No Missing Codes are Guaranteed | --              |           | --                  | --  | 8                   | Bits |
| <b>Reference Input</b>                                       |                 |           |                     |     |                     |      |
| Input Resitance  | --              | 1, 2, 3   | 1.0                 | --  | 4.0                 | kΩ   |
| V <sub>REF (+)</sub> Input Voltage Range                     | --              | 1, 2, 3   | V <sub>REF(-)</sub> | --  | V <sub>DD</sub>     | V    |
| V <sub>REF (-)</sub> Input Voltage Range                     | --              | 1, 2, 3   | GND                 | --  | V <sub>REF(+)</sub> | V    |
| <b>Analog Input</b>  |                 |           |                     |     |                     |      |
| Input Voltage Range  | --              | 1, 2, 3   | V <sub>REF(-)</sub> | --  | V <sub>REF(+)</sub> | V    |
| Input Leakage Current  | --              | 1, 2, 3   | --                  | --  | ±3                  | μA   |
| Input Capacitance <sup>2</sup>                               | --              | 1, 2, 3   | --                  | 45  | --                  | pF   |
| <b>Logic Inputs</b>  |                 |           |                     |     |                     |      |
| CS, WR, RD   |                 |           |                     |     |                     |      |
| V <sub>INH</sub>   | --              | 1, 2, 3   | 2.4                 | --  | --                  | V    |
| V <sub>INH</sub>   | --              | 1, 2, 3   | --                  | --  | 0.8                 | V    |
| I <sub>INH</sub> (CS, RD)                                    | --              | 1, 2, 3   | --                  | --  | 1                   | μA   |
| I <sub>INH</sub> (WR)  | --              | 1, 2, 3   | --                  | --  | 3                   | μA   |
| I <sub>INL</sub> (WR)  | --              | 1, 2, 3   | --                  | --  | -1                  | μA   |
| Input Capacitance <sup>2</sup>                               | --              | 1, 2, 3   | --                  | 5   | 8                   | pF   |

TABLE 3. 7820 DC ELECTRICAL CHARACTERISTICS  
 ( $V_{DD} = +5V$ ;  $V_{REF(+)} = +5V$ ;  $V_{REF(-)} = GND = 0V$ , UNLESS OTHERWISE SPECIFIED) (RD MODE (PIN 7 = 0V))  
 ( $T_A = -55$  TO  $125$  °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER  | TEST CONDITIONS                                 | SUBGROUPS | MIN | TYP        | MAX       | UNIT       |
|--|---|-----------|-----|------------|-----------|------------|
| <b>Mode</b>  |   |           |     |            |           |            |
| $V_{INH}$  | --  | 1, 2, 3   | 3.5 | --         | --        | V          |
| $I_{INH}$  | --  | 1, 2, 3   | --  | --         | 200       | $\mu A$    |
| $I_{INL}$  | --  | 1, 2, 3   | --  | --         | -1        | $\mu A$    |
| Input Capacitance <sup>2</sup>                         | --  | 1, 2, 3   | --  | 5          | 8         | pF         |
| <b>Logic Outputs</b><br>DB0-DB7, OFL, $\overline{INT}$ |   |           |     |            |           |            |
| $V_{OH}$   | ISOURCE =<br>360 $\mu A$                        | 1, 2, 3   | 4   | --         | --        | V          |
| $V_{OL}$   | ISINK = 1.6 mA                                  | 1, 2, 3   | --  | --         | 0.4       | V          |
| $I_{OUT}$ (DB0-DB7)                                    | Floating State<br>Leakage                       | 1, 2, 3   | --  | --         | $\pm 3$   | $\mu A$    |
| Output Capacitance <sup>2</sup>                        | --  | 1, 2, 3   | --  | 5          | 8         | pF         |
| <b>RDY</b>   |   |           |     |            |           |            |
| $V_{OL}$   | ISINK = 2.6mA                                   | 1, 2, 3   | --  | --         | 0.4       | V          |
| $I_{OUT}$  | Floating State<br>Leakage                       | 1, 2, 3   | --  | --         | $\pm 3$   | V          |
| Output Capacitance <sup>2</sup>                        | --  | 4, 5, 6   | --  | 5          | 8         | pF         |
| Slew Rate, Tracking <sup>2</sup>                       | --  | 1, 2, 3   | --  | 0.2        | 0.1       | V/ $\mu s$ |
| <b>Power Supply</b>                                    |   |           |     |            |           |            |
| $V_{DD}$   | $\pm 5\%$ for speci-<br>fied perfor-<br>mance   | 1, 2, 3   | --  | --         | 5         | V          |
| $I_{DD}$   | $\overline{CS} = \overline{RD} = \overline{OV}$ | 1, 2, 3   | --  | --         | 20        | mA         |
| Power Dissipation                                      | --  | 1, 2, 3   | --  | 40         | --        | mW         |
| Power Supply Sensitivity                               | $V_{DD} = 5V \pm 5\%$                           | 1, 2, 3   | --  | $\pm 1/16$ | $\pm 1/4$ | LSB        |
|  |   |           |     |            |           |            |

1. Total unadjusted error includes offset, full scale and linearity error.
2. Guaranteed by design.

TABLE 4. 7820 AC ELECTRICAL CHARACTERISTICS<sup>1</sup> $(V_{DD} = +5V; V_{REF(+)} = +5V; V_{REF(-)} = GND = 0V, \text{ UNLESS OTHERWISE SPECIFIED})$  (RD MODE (PIN 7 = 0V)) $(T_A = -55 \text{ TO } 125 \text{ }^\circ\text{C UNLESS OTHERWISE SPECIFIED})$ 

| PARAMETER  | SUBGROUPS | SYMBOL     | MIN | MAX            | UNIT          |
|--|-----------|------------|-----|----------------|---------------|
| CS to RD/WR Setup Time                             | 9, 10, 11 | $t_{CSS}$  | 0   | --             | ns            |
| CS to RD/WR Hold Time                              | 9, 10, 11 | $t_{CSH}$  | 0   | --             | ns            |
| CS to Delay Time (Pull-up Resistor = 5k $\Omega$ ) | 9, 10, 11 | $t_{RDY}$  | --  | 100            | ns            |
| Conversion Time (RD Mode)                          | 9, 10, 11 | $t_{CRD}$  | --  | 2.5            | $\mu\text{s}$ |
| Data Access Time (RD Mode)                         | 9, 10, 11 | $t_{ACCD}$ | --  | $t_{CRD} + 50$ | ns            |
| RD to INT Delay (RD Mode)                          | 9, 10, 11 | $t_{INTH}$ | --  | 225            | ns            |
| Data Hold Time                                     | 9, 10, 11 | $t_{DH}$   | --  | 100            | ns            |
| Delay Time Between Conversions                     | 9, 10, 11 | $t_p$      | 600 | --             | ns            |
| Write Pulse Width                                  | 9, 10, 11 | $t_{WR}$   | 600 | --             | ns            |
|  |           |            | --  | 50             | $\mu\text{s}$ |
| Delay Time Between WR and RD Pulses                | 9, 10, 11 | $t_{RD}$   | 700 | --             | ns            |
| Data Access Time (WR-RD Mode)                      | 9, 10, 11 | $t_{ACC1}$ | --  | 250            | ns            |
| RD to INT Delay                                    | 9, 10, 11 | $t_{R1}$   | --  | 225            | ns            |
| WR to INT Delay                                    | 9, 10, 11 | $t_{INTL}$ | --  | 1700           | ns            |
| Data Access Time (WR-RD Mode)                      | 9, 10, 11 | $t_{ACC2}$ | --  | 110            | ns            |
| WR to INT Delay (Stand-Alone Operation)            | 9, 10, 11 | $t_{HWR}$  | --  | 150            | ns            |
| Data Access Time After INT (Stand-Alone Operation) | 9, 10, 11 | $t_{ID}$   | --  | 75             | ns            |

1. Sample tested at 25°C to ensure compliance. Only on process design change.

FIGURE 1. LOAD CIRCUITS FOR DATA ACCESS TIME TEST

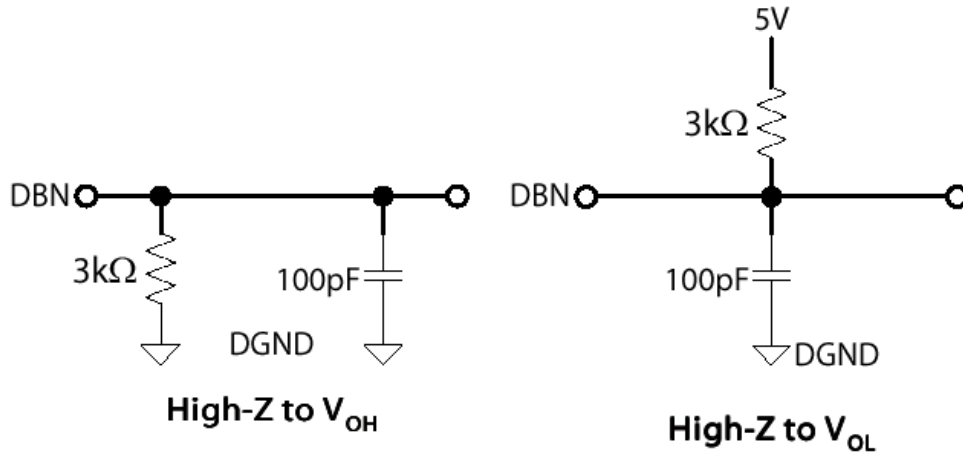


FIGURE 2. LOAD CIRCUITS FOR DATA HOLD TIME RESET

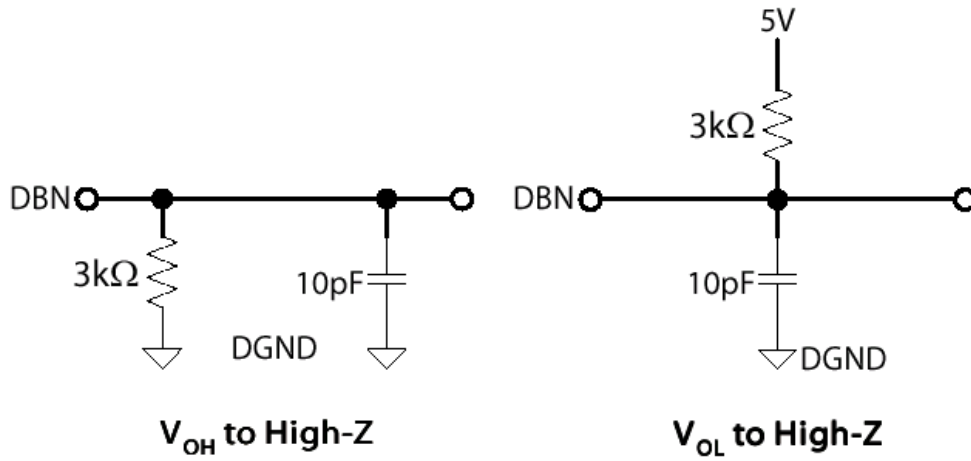


FIGURE 3. LOAD CIRCUIT FOR ACCESS TIME

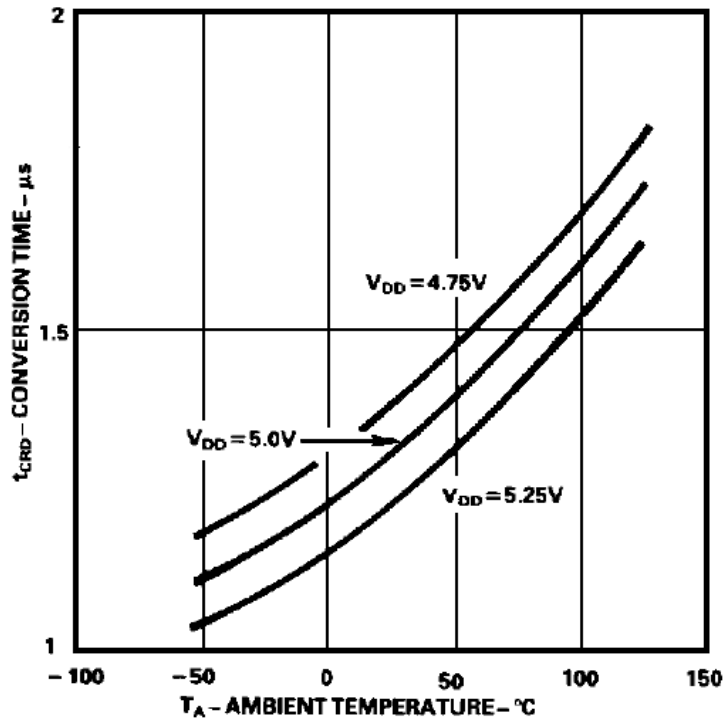


FIGURE 4. LOAD CIRCUIT FOR OUTPUT FLOAT DELAY

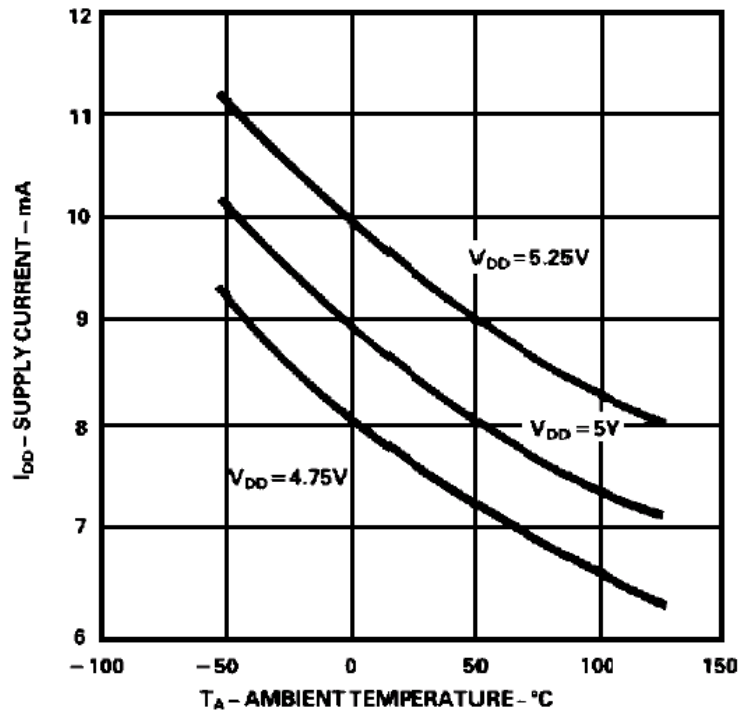


FIGURE 5. ACCURACY VS.  $T_{WR}$

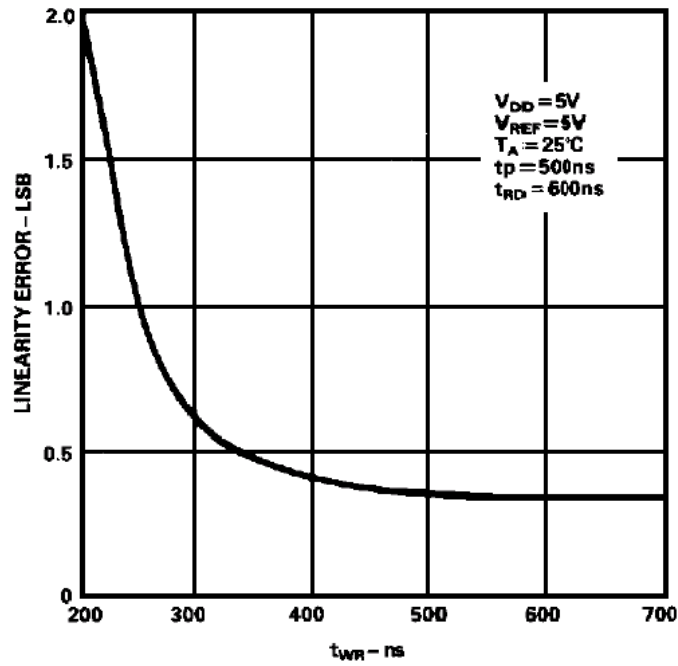


FIGURE 6. ACCURACY VS.  $T_{RD}$

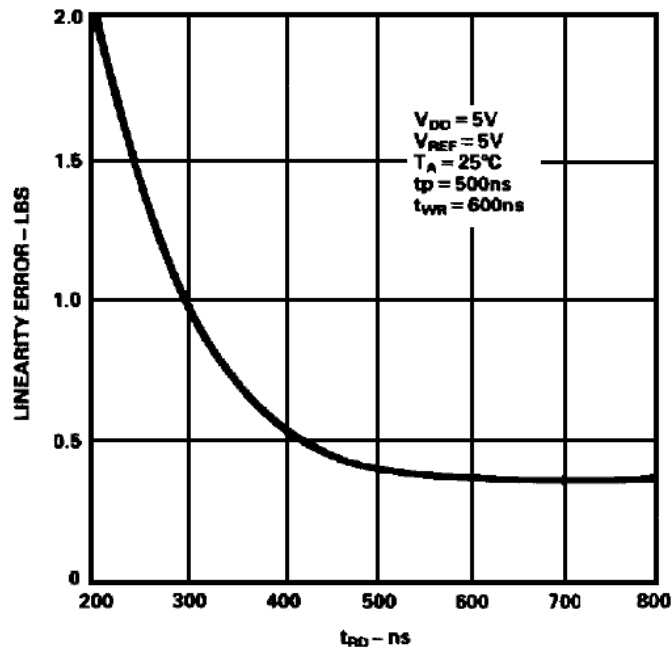




FIGURE 7. ACCURACY VS.  $T_{SP}$

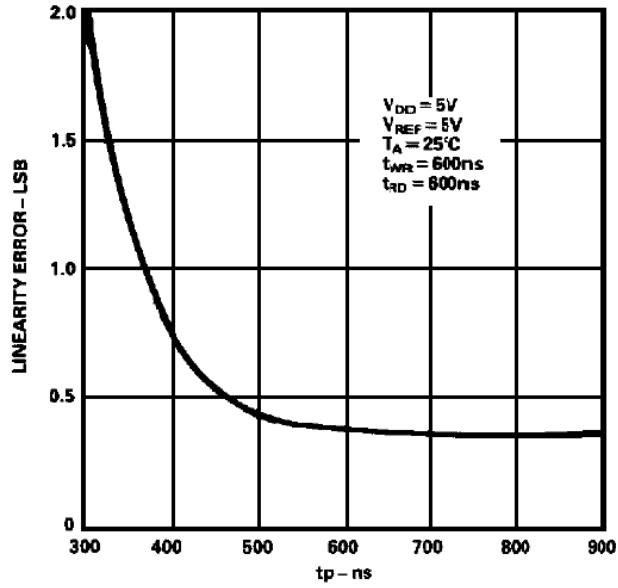


FIGURE 8. ACCURACY VS.  $T_{REF}$  [ $V_{REF} = V_{REF}(+) - V_{REF}(-)$ ]

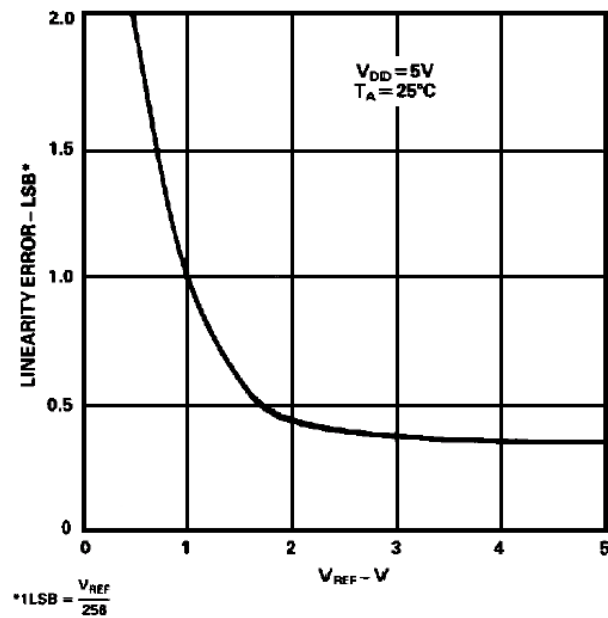


FIGURE 9. SIGNAL-NOISE RATIO VS. INPUT FREQUENCY

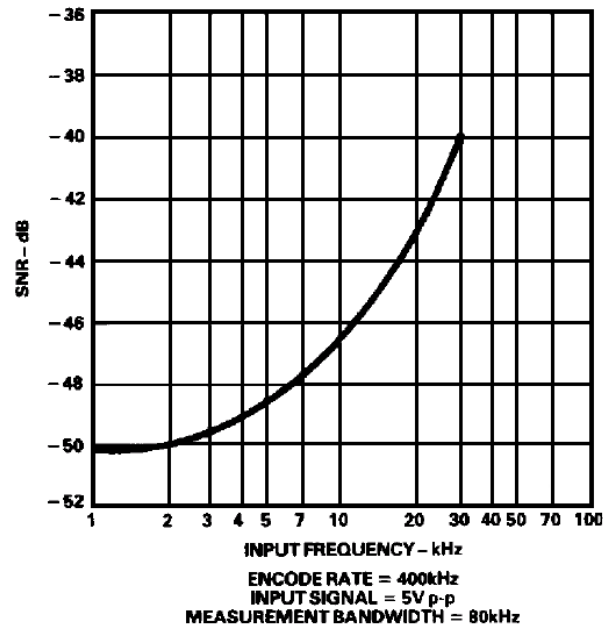


FIGURE 10.  $T_{INTL}$  INTERNAL TIME DELAY VS. TEMPERATURE

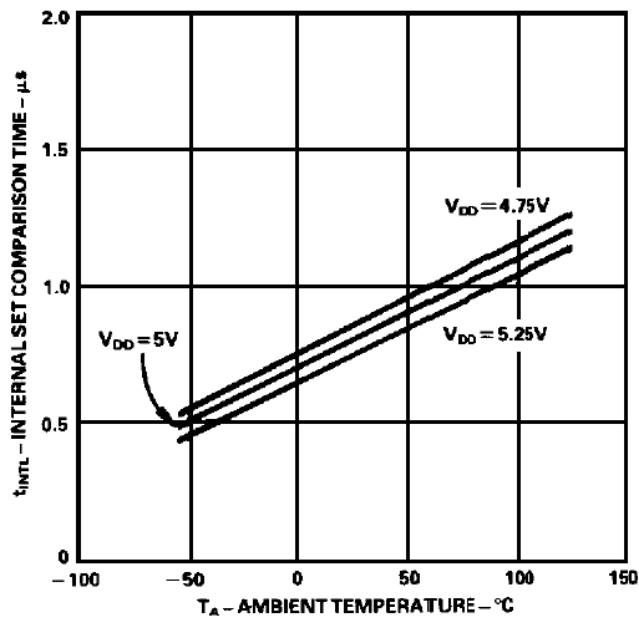


FIGURE 11. OUTPUT CURRENT VS. TEMPERATURE

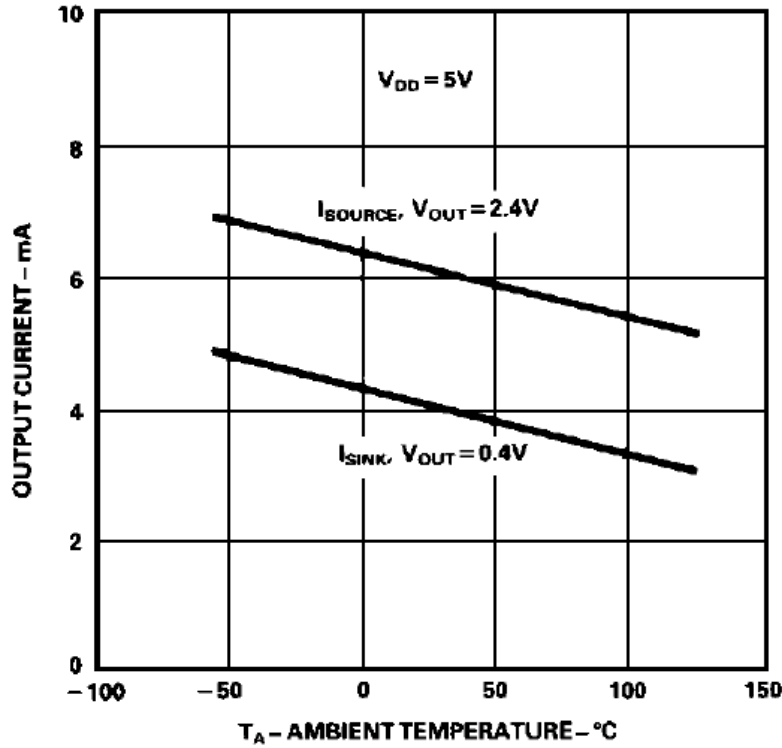


FIGURE 12. OPERATING SEQUENCE (WR-RD MODE)

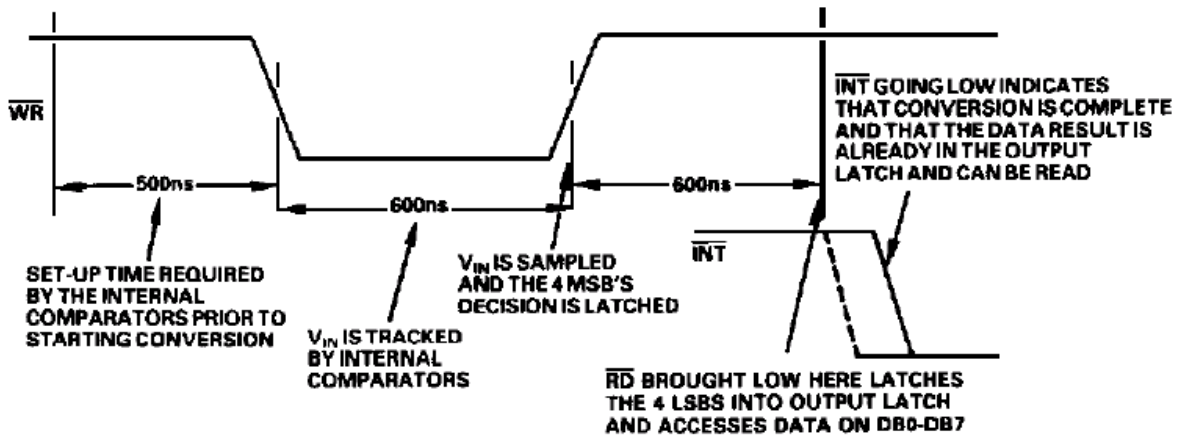


FIGURE 13. RD MODE

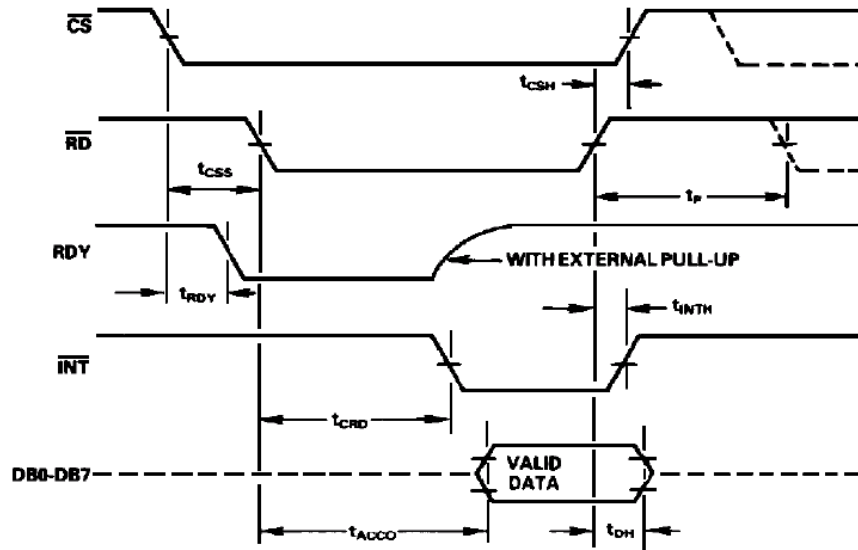


FIGURE 14. WR-RD MODE ( $TRD > TINTL$ )

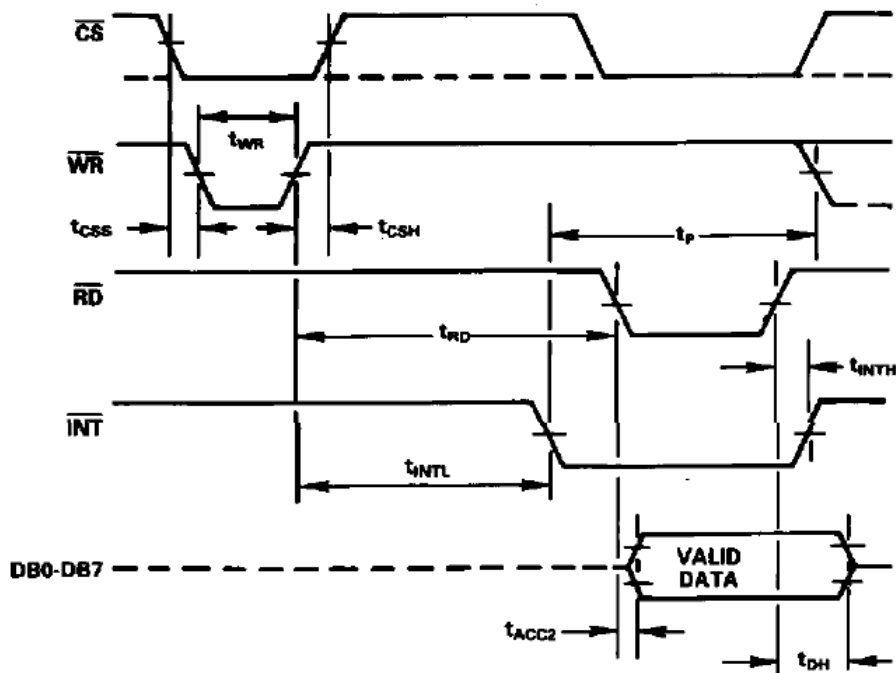


FIGURE 15. WR-RD MODE ( $T_{RD} < T_{INTL}$ )

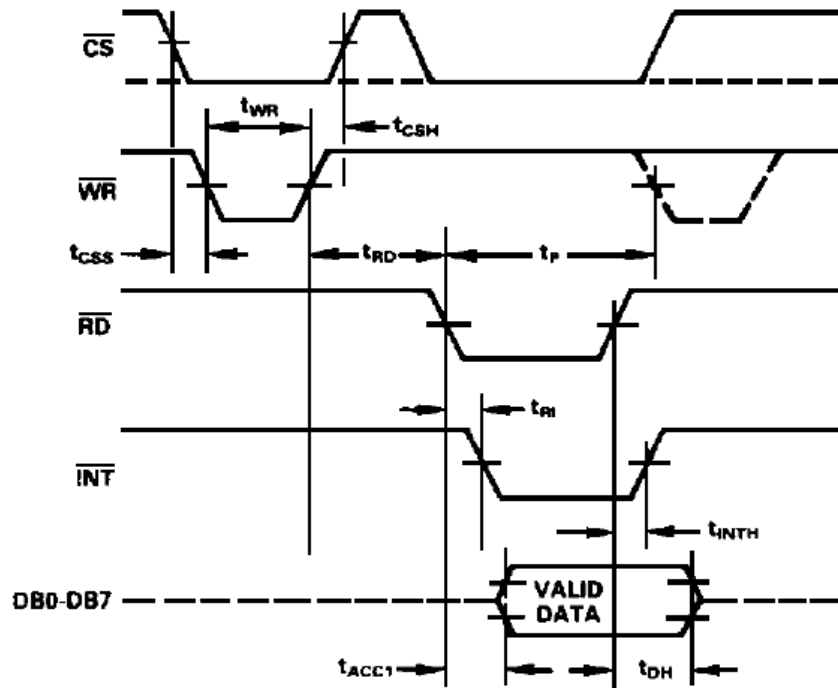


FIGURE 16. WR-RD MODE STAND-ALONE OPERATION ( $\overline{CS} = \overline{RD} = 0$ )

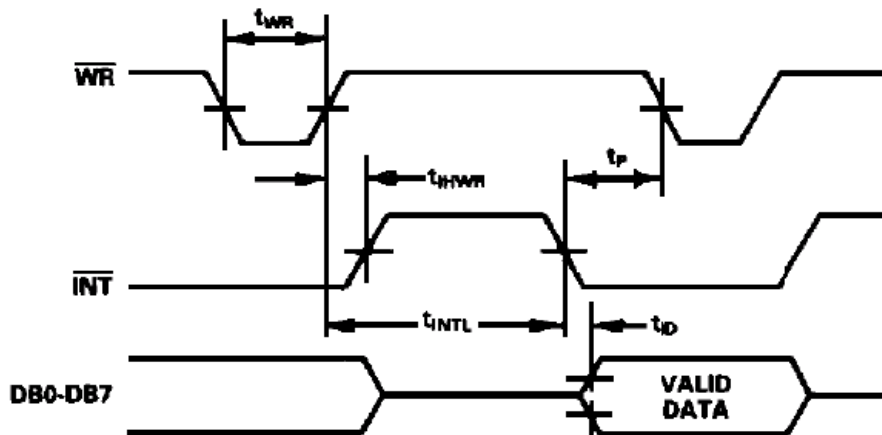


FIGURE 17. POWER SUPPLY AS REFERENCE

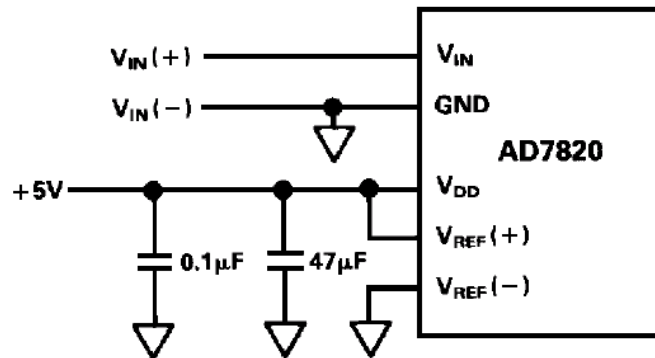


FIGURE 18. INPUT NOT REFERENCED TO GND

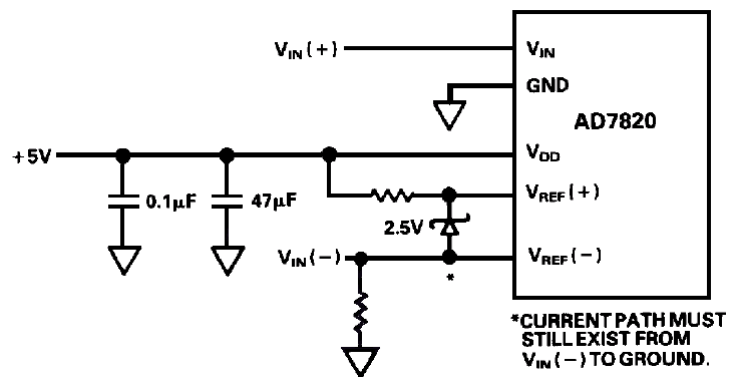


FIGURE 19. EQUIVALENT INPUT CIRCUIT

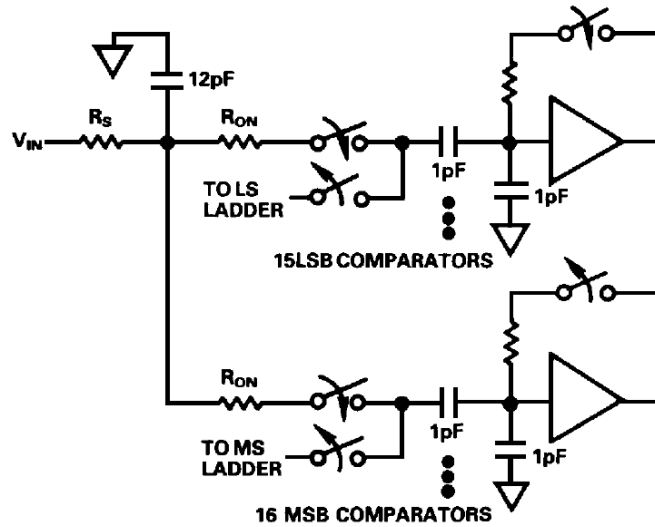
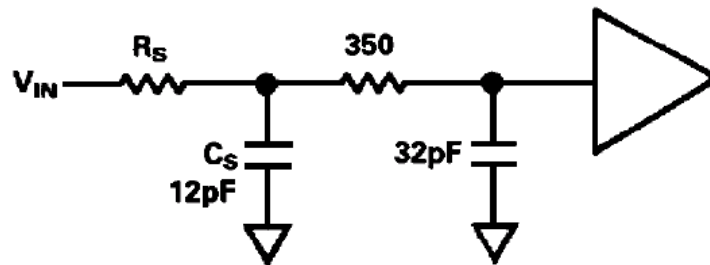
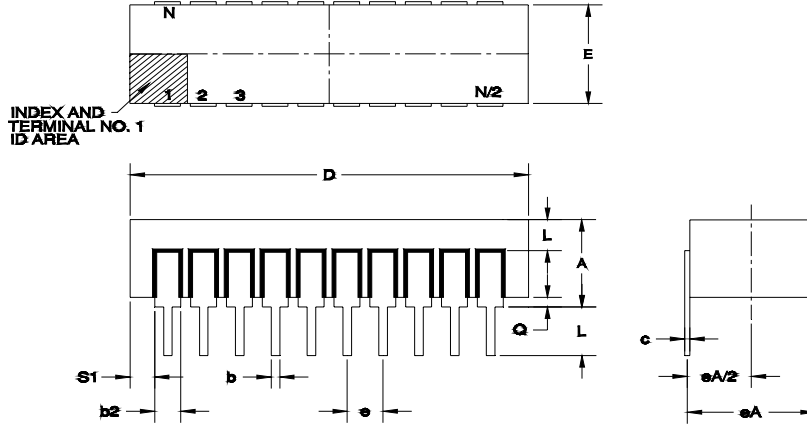


FIGURE 20. RC NETWORK MODEL





20 PIN RAD-PAK® DUAL IN LINE PACKAGE

| SYMBOL | DIMENSION |       |       |
|--------|-----------|-------|-------|
|        | MIN       | NOM   | MAX   |
| A      | --        | 0.202 | 0.230 |
| b      | 0.014     | 0.018 | 0.026 |
| b2     | 0.045     | 0.050 | 0.065 |
| c      | 0.008     | 0.010 | 0.018 |
| D      | --        | 1.000 | 1.060 |
| E      | 0.220     | 0.295 | 0.310 |
| eA     | 0.300 BSC |       |       |
| eA/2   | 0.150 BSC |       |       |
| e      | 0.100 BSC |       |       |
| L      | 0.135     | 0.145 | 0.155 |
| Q      | 0.015     | 0.045 | 0.070 |
| S1     | 0.005     | 0.025 | --    |
| S2     | 0.005     | --    | --    |
| N      | 20        |       |       |

Note: All dimensions in inches



## Important Notice:

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