SIEMENS

ICs for Communications

ISDN Echocancellation Circuit for NT and Terminal Applications
IEC-Q NTE

PSB 21910 Version 5.1

Delta Sheet 01.97

T2191-0V51-L1-7600

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Previous Version: none		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

Edition 01.97

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1 Overview

The PSB 21910 IEC-Q NTE Version 5.1 is a specific version of the PEB 2091 IEC-Q for terminal and PBX applications. It features all necessary functions required for NTs and terminal applications like PC add-on cards and terminal adapters. This Delta Sheet refers to the IEC-Q V 4.3 User's Manual 2.95, IEC-Q V4.4 and V5.1 Delta Sheet and IEC-Q V5.1 Errata Sheet.

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ISDN Echocancellation Circuit for NT and Terminal Applications
IEC-Q NTE

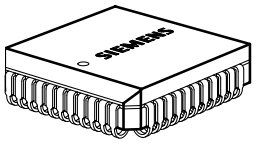
PSB 21910

Delta Sheet for the Version 5.1

CMOS

2 Features

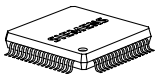
- Compatible to PEB 2091 IEC-Q V5.1 in NT modes and TE mode
- IOM-2 interface in NT mode compatible to PEB 2081 (SBCX)
- IOM-2 interface in TE mode compatible to PSB2186 and PSB 7110 for D-channel access



P-LCC-44

The IEC-Q NTE V 5.1 comes in a PLCC-44 package or a T-QFP 64 package.

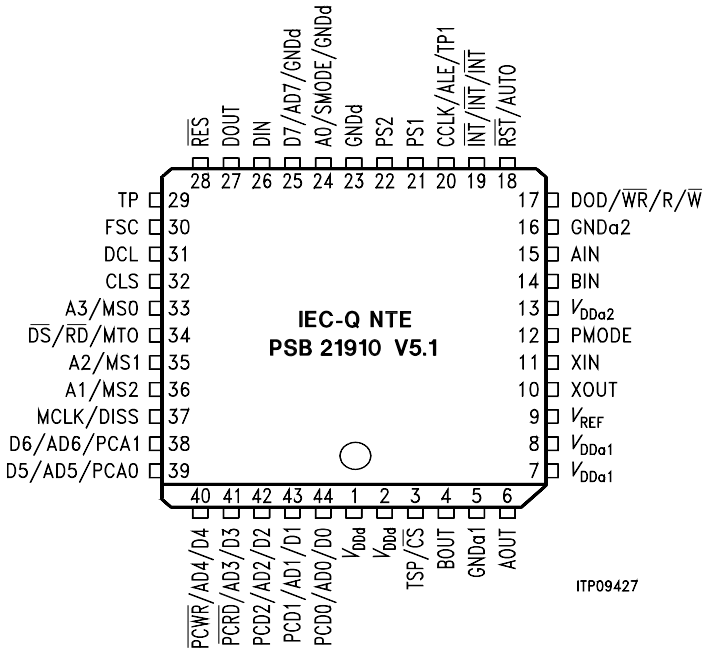
PSF version with extended temperature range (-40 ... +85 C) available on request.



T-QFP 64

Type	Ordering Code	Package
PSB 21910F V5.1	Q 67101-H6886	T-QFP 64
PSB 21910N V5.1	Q 67107-H6873	P-LCC-44

2.1 Pin Configuration



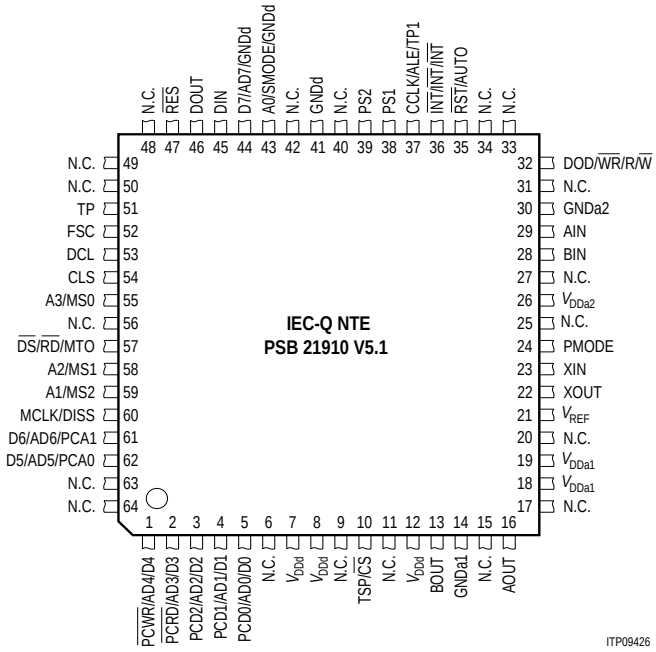


Figure 1
Pin Configuration P-LCC-44 and T-QFP 64 Package (top view)

2.2 Pin Definitions and Functions

Pin names and pin numbers of the P-LCC 44 package in stand alone mode are as in former versions of the IEC-Q.

Pin No. P-LCC-44	Pin No. T-QFP64	Symbol	Input (I) Output (O)	Function
Power Supply Pins				
1, 2	7, 8, 12	V_{DDD}	I	5 V ± 5 % digital supply voltage
5	14	GNDA1	I	0 V analog
7, 8	18, 19	V_{DDA1}	I	5 V ± 5 % analog supply voltage
9	21	V_{REF}	O	V_{REF} pin to buffer internally generated voltage with capacitor 100 nF vs GND
13	26	V_{DDA2}	I	5 V ± 5 % analog supply voltage
16	30	GNDA2	I	0 V analog
23	41	GNDD	I	0 V digital
Mode Selection Pins				
3	10	TSP	I	**Single pulse test mode (Stand alone mode):** For activation refer to table 2 on page 48 in the IEC-Q V 4.3 user´s manual. When active, alternating 2.5 V pulses are issued in 1.5 ms intervals. Tie to GND if not used.
3	10	$\overline{CS}$	I	**Chip select (Multiplexed, demultiplexed and serial modes):** Low active.
18	35	AUTO	I	**Auto (Stand alone mode):** Selection between auto- and transparent mode for EOC channel processing. (Automode = (1))
18	35	$\overline{RST}$	O	**Reset output (Multiplexed, demultiplexed and serial modes):** Low active.

Pin No. P-LCC-44	Pin No. T-QFP64	Symbol	Input (I) Output (O)	Function
24	43	GNDd	I	**GNDd (Stand alone mode):** Must be connected to GNDd in stand alone mode.
24	43	SMODE	I	**Serial mode pin:** SMODE = 1 selects serial mode, SMODE = 0 enables the multiplexed mode.
24	43	A0	I	**Address bus pin (Demultiplexed mode)**
25	44	GNDd	I	**GNDd (Stand alone mode):** Must be connected to GNDd in stand alone mode.
25	44	D7	I/O	**Data bus pin (Multiplexed, demultiplexed modes)**
25	44	not used	I	**(Serial mode)** tie to GND.
33	55	MS0	I	**Mode Selection 0 (Stand alone mode)**
33	55	not used	I	**(Multiplexed mode)** tie to GND.
33	55	A3	I	**Address bus pin (Demultiplexed mode)**.
33	55	not used	I	**(Serial mode)** tie to GND.
35	58	MS1	I	**Mode Selection 1 (Stand alone mode)**
35	58	not used	I/O	**(Multiplexed mode)** tie to GND.
35	58	A2	I/O	**Address bus pin (Demultiplexed mode)**.
35	58	CDOUT	O	**Controller Data Out (Serial mode):** CCLK determines the data rate. CDOUT is "high Z" if no data is transmitted.
36	59	MS2	I	**Mode Selection 2 (Stand alone mode)**
36	59	not used	I	**(Multiplexed mode)** tie to GND.
36	59	A1	I	**Address bus pin (Demultiplexed mode)**.

Pin No. P-LCC-44	Pin No. T-QFP64	Symbol	Input (I) Output (O)	Function
36	59	CDIN	I	**Controller Data In (Serial mode):** CCLK determines the data rate.
28	47	$\overline{\text{RES}}$	I	**Reset:** Low active , must be (0) at least for 10 ns.

Power Controller Interface Pins

44	5	PCD0	I/O	**Data Bus of power controller interface 0 (Stand alone mode):** internal pull-up.
44	5	AD0	I/O	**Address/Data bus pin (Multiplexed mode)**
44	5	D0	I/O	**Data bus pin (Demultiplexed mode)**
44	5	not used	I	**(Serial mode)** tie to GND.
43	4	PCD1	I/O	**Data Bus of power controller interface 1 (Stand alone mode):** Internal pull-up.
43	4	AD1	I/O	**Address/Data bus pin (Multiplexed mode)**
43	4	D1	I/O	**Data bus pin (Demultiplexed mode)**
43	4	not used	I	**(Serial mode)** tie to GND.
42	3	PCD2	I/O	**Data Bus of power controller interface 2 (Stand alone mode):** Internal pull-up.
42	3	AD2	I/O	**Address/Data bus pin (Multiplexed mode)**
42	3	D2	I/O	**Data bus pin (Demultiplexed mode)**
42	3	not used	I	**(Serial mode)** tie to GND.
39	62	PCA0	O	**Address bus of power controller interface (Stand alone mode)**.
39	62	D5	I/O	**Data bus pin (Multiplexed, demultiplexed modes)**
39	62	not used	I	**(Serial mode)** tie to GND.
38	61	PCA1	O	**Address bus of power controller interface (Stand alone mode)**.

Pin No. P-LCC-44	Pin No. T-QFP64	Symbol	Input (I) Output (O)	Function
38	61	D6	I/O	**Data bus pin (Multiplexed, demultiplexed modes)**
38	61	not used	I	**(Serial mode)** tie to GND.
41	2	$\overline{\text{PCRD}}$	O	**Power controller bus read request (Stand alone mode):** Low active.
41	2	AD3	I/O	**Address/Data bus pin (Multiplexed mode)**
41	2	D3	I/O	**Data bus pin (Demultiplexed mode)**
41	2	not used	I	**(Serial mode)** tie to GND.
40	1	$\overline{\text{PCWR}}$	O	**Power controller bus write request (Stand alone mode):** Low active.
40	1	D4	I/O	**Data bus pin (Multiplexed and demultiplexed modes)**
40	1	not used	I	**(Serial mode)** tie to GND.
19	36	INT	I	**Interrupt (Stand alone mode):** Change-sensitive. After a change of level has been detected the C/I code “INT” will be issued on IOM. Tie to GND during operation.
19	36	$\overline{\text{INT}}$	O	**Interrupt line (Multiplexed, demultiplexed and serial modes):** Low active**.**
37	60	DISS	O	**Disable power supply (Stand alone mode):** This pin is set to ’1’ after receipt of MON-0 LBBD in auto-mode.
37	60	MCLK	O	**Microprocessor clock output (Multiplexed, demultiplexed and serial modes):** provided with four programmable clock rates: 7.68 MHz, 3.84 MHz, 1.92 MHz and 0.96 MHz.
21	38	PS1	I	**Power status 1 (primary)**. ’1’ indicates primary power supply ok. The pin value is identical to the overhead bit ’PS1’ value.

Pin No. P-LCC-44	Pin No. T-QFP64	Symbol	Input (I) Output (O)	Function
22	39	PS2	I	**Power status 2 (secondary)**. '1' indicates secondary power supply ok. The pin value is identical to the overhead bit 'PS2' value.

Miscellaneous Function Pins

10	22	XOUT	O	**Crystal OUT:** 15.36-MHz crystal is connected with 30 pF in parallel. Leave open if not used.
11	23	XIN	I	**Crystal IN:** External 15.36-MHz clock signal or 15.36-MHz crystal with 30 pF in parallel is connected.
17	32	DOD	I	**DOUT open drain (Stand alone mode):** Select open drain with DOD = (1) (external pull-up resistor required) and tristate with DOD = (0) .
17	32	$\overline{WR}$	I	**Write (Siemens/Intel multiplexed and demultiplexed modes):** indicates a write operation, active low.
17	32	R/$\overline{W}$	I	**Read/Write (Motorola demultiplexed mode):** indicates a read (high) or write (low) operation.
17	32	not used	I	**(Serial mode)** tie to GND.
29	51	TP	I	**Test pin:** Not available to user. Do not connect. Internal pull-down resistor.
20	37	TP1	I	**Test pin (Stand alone mode):** Not available to user. Do not connect. Internal pull-down resistor .
20	37	ALE	I	**Address Latch Enable (Multiplexed mode):** In the Siemens/Intel µP interface modes a high indicates an address on the AD0..3 pins which is latched with the falling edge of ALE.

Pin No. P-LCC-44	Pin No. T-QFP64	Symbol	Input (I) Output (O)	Function
20	37	ALE	I	**Address Latch Enable (Demultiplexed mode):** ALE tied to GND selects the Siemens/Intel type. ALE tied to VDD selects the Motorola type.
20	37	CCLK	I	**Controller data clock (Serial mode):** Shifts data from or to the device.
32	54	CLS	O	**Clock Signal:** A 7.68MHz clock, synchronous to the U-interface, is provided on this pin.
12	24	PMODE	I	**Processor Interface Enable:** Setting PMODE to "1" enables the Processor Interface **(Multiplexed, demulti-plexed and serial modes).** Tie to GND or do not connect to select stand alone mode. Internal pull down.
34	57	MTO	I	**Monitor procedure timeout (Stand alone mode):** Disables the internal 6 ms monitor timeout when set to (1). Internal pull-down resistor.
34	57	$\overline{RD}$	I	**Read (Siemens/Intel multiplexed and demultiplexed modes):** indicates a read operation, active low.
34	57	$\overline{DS}$		**Data Strobe (Motorola demultiplexed mode):** indicates a data transfer, active low.
34	57	not used	I	**(Serial mode)** tie to GND.

IOM®-Pins

31	53	DCL	I/O	**Data clock:** Clock output 512 or 1536 kHz. Remains input in processor mode until programming of STCR register.

Pin No. P-LCC-44	Pin No. T-QFP64	Symbol	Input (I) Output (O)	Function
30	52	FSC	I/O	**Frame synchronization clock:** The start of the B1-channel in time-slot 0 is marked. FSC = (1) for one DCL-period indicates a superframe marker. FSC = (1) for at least two DCL-periods marks a standard frame. Remains input in processor mode until programming of STCR register.
26	45	DU	I	**Data Upstream:** Input of IOM-data synchronous to DCL-clock.
27	46	DD	O	**Data Downstream:** Output of IOM-data synchronous to DCL-clock.

U-Interface Pins

15	29	AIN	I	**Differential U-Interface input:** Connect to hybrid.
14	28	BIN	I	**Differential U-Interface input:** Connect to hybrid.
6	16	AOUT	O	**Differential U-Interface output:** Connect to hybrid.
4	13	BOUT	O	**Differential U-Interface output:** Connect to hybrid.

2.3 Operation Modes

	Input Pins			Output Pins U Synchronized		
Mode	**MS2**	**MS1**	**MS0**	**DCL OUT**	**CLS OUT**	**Super-frame-marker**
NT	0	0	0	512	7680	no
NT	1	0	0	512	7680	yes
NT-Auto	0	0	1	512	7680	no
TE	0	1	0	1536	7680	no
TE	1	1	0	1536	7680	yes
NT-RP	1	0	1	512	7680	yes

Table 1 Modes of Operation

The IEC-Q NTE supports the operating modes NT, NT-Auto, TE and NT-Repeater. The selection is done via the MS2-0 inputs in stand alone mode and via the register bits MS2-0 in the STCR register in processor mode.

2.4 STCR Register

Default: $C4_H$

Name:	7	6	5	4	3	2	1	0	Default
STCR	TEST1	TEST2	MS2	MS1	MS0	TM1	TM2	AUTO	$C4_H$

The Status Control Register (STCR) selects the operating modes of the IEC-Q NTE V 5.1 as given in the section 2.2 on page 47 of the IEC-Q V 4.3 user´s manual.

TEST1: Test Bit 1

Must be written to ’0’ together with mode setting of MS2-0 after reset.

TEST2: Test Bit 2

Must be written to ’0’ together with mode setting of MS2-0 after reset.

MS2: Mode Selection 2

Selects operation mode according to table above.

MS1: Mode selection 1

Selects operation mode according to table above.

MS0: Mode Selection 0

Selects operation mode according to table above.

TM1: Test-Mode-Bit 1

This bit determines, in combination with STCR:TM2, the operation modes. See table below.

TM2: Test-Mode-Bit 2

This bit determines, in combination with STCR:TM1, the operation modes. See table below.

Test-Mode	TM1	TM2
Normal Mode	1	0
Send Single-Pulses	1	1
Data-Through	0	1

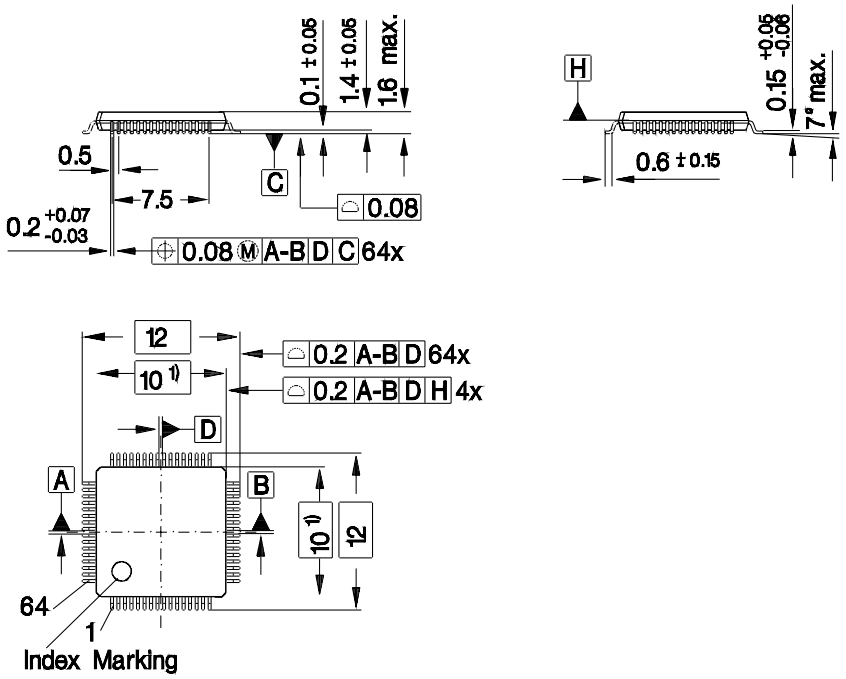
AUTO: Selection between auto- and transparent mode

AUTO = 1 sets the automode for EOC channel processing.

AUTO = 0 sets the transparent mode for EOC channel processing.

3 Package Outlines

T-QFP 64
(Thin Quad Flat Package)



For package outlines of the P-LCC 44 package please refer to the PEB 2091 V4.3 User's Manual 2.95, page 217.

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm