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Status	Product Specification
FAST Products	

FEATURES for 74F711A/711-1

- Consists of five 2-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- Output inverting/non-inverting option
- 30 ohm termination impedance on each output-'F711-1
- Outputs sink 64mA ('F711A only)

FEATURES for 74F712A/712-1

- Consists of five 3-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- 30 ohm termination impedance on each output-'F712-1
- Outputs sink 64mA ('F712A only)

DESCRIPTION

The 74F711A/711-1 consist of five 2-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 'F711A has a common select (S) input, an Output Enable (OE) input and an Output Inverting (INV) input to control the 3-state outputs. The outputs source 15mA and sink 64mA. The 'F711-1 is the same as the 'F711A except that it has a 30 ohm termination impedance on each output to reduce line noise and the 3-state outputs sink 5mA.

When the inverting input (INV) is Low, the input data path is inverted.

FAST 74F711A/711-1, 74F712A/712-1 Multiplexers

74F711A Quint 2-to-1 Data Selector Multiplexer (3-State)

74F711-1 Quint 2-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance (3-State)

74F712A Quint 3-to-1 Data Selector Multiplexer

74F712-1 Quint 3-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711A	6.0ns	30mA
74F711-1	6.5ns	29mA
74F712A	5.5ns	25mA
74F712-1	6.5ns	25mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
20-Pin Plastic DIP	N74F711AN, N74F711-1N
24-Pin Plastic Slim DIP (300 mil)	N74F712AN, N74F712-1N
20-Pin Plastic SOL	N74F711AD, N74F711-1D
24-Pin Plastic SOL	N74F712AD, N74F712-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F711A/ 'F711-1	D_{na}, D_{nb}	Data inputs	1.0/0.066	20µA/40µA
	S	Select input	1.0/0.033	20µA/20µA
	<u>OE</u>	Output Enable input (active Low)	1.0/0.033	20µA/20µA
	<u>INV</u>	Output Inverting input (active Low)	1.0/0.033	20µA/20µA
	$Q_0 - Q_4$	Data outputs for 'F711A	750/106.7	15mA/64mA
	$Q_0 - Q_4$	Data outputs for 'F711-1	750/8.33	15mA/5mA
'F712A/ 'F712-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.066	20µA/40µA
	S_0, S_1	Select inputs	1.0/0.033	20µA/20µA
	$Q_0 - Q_4$	Data outputs for 'F712A	750/106.7	15mA/64mA
	$Q_0 - Q_4$	Data outputs for 'F712-1	750/8.33	15mA/5mA

NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

To improve speed and noise immunity, V_{CC} and GND side pins are used.

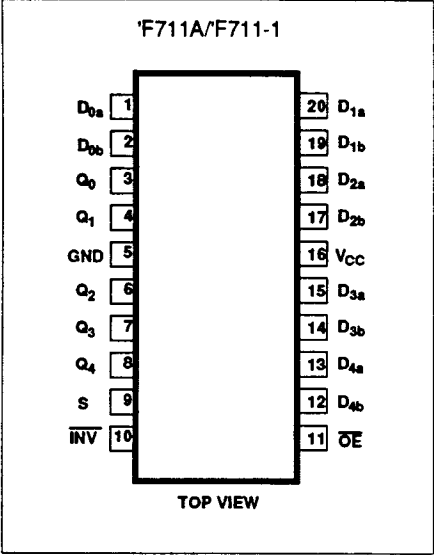
The 74F712A/712-1 consist of five 3-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 'F712A has two select (S_0, S_1) inputs to determine which

set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 'F712-1 is the same as the 'F712A except that it has a 30 ohm termination impedance on each output to reduce line noise and the outputs sink 5mA.

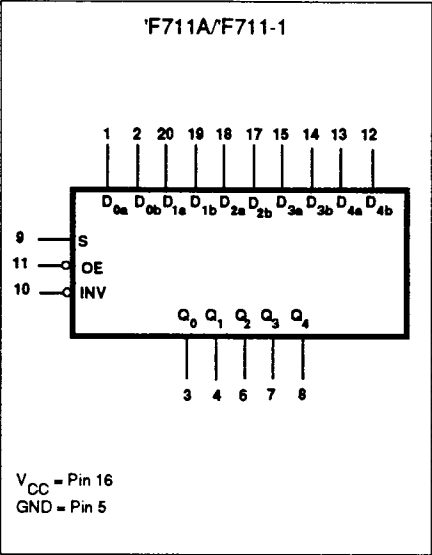
Multiplexers

FAST 74F711A/711-1, 74F712A/712-1

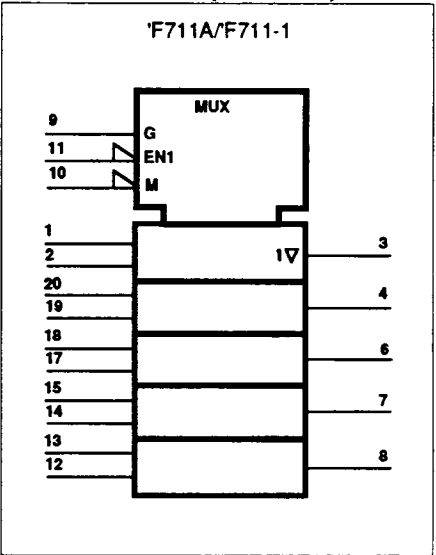
PIN CONFIGURATION



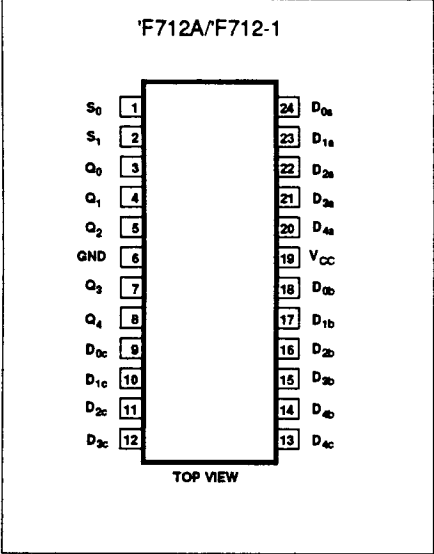
LOGIC SYMBOL



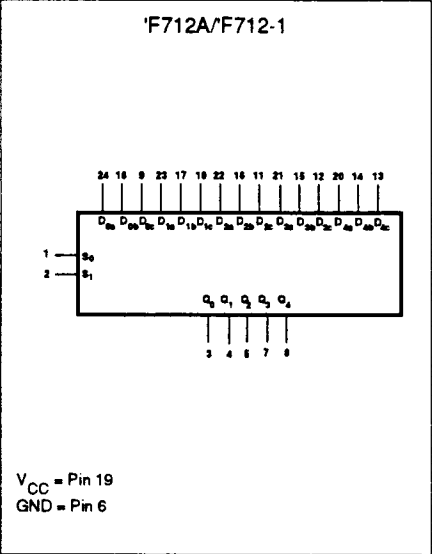
LOGIC SYMBOL(IEEE/IEC)



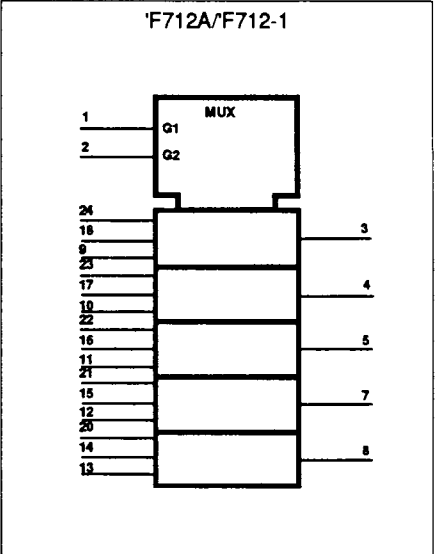
PIN CONFIGURATION



LOGIC SYMBOL



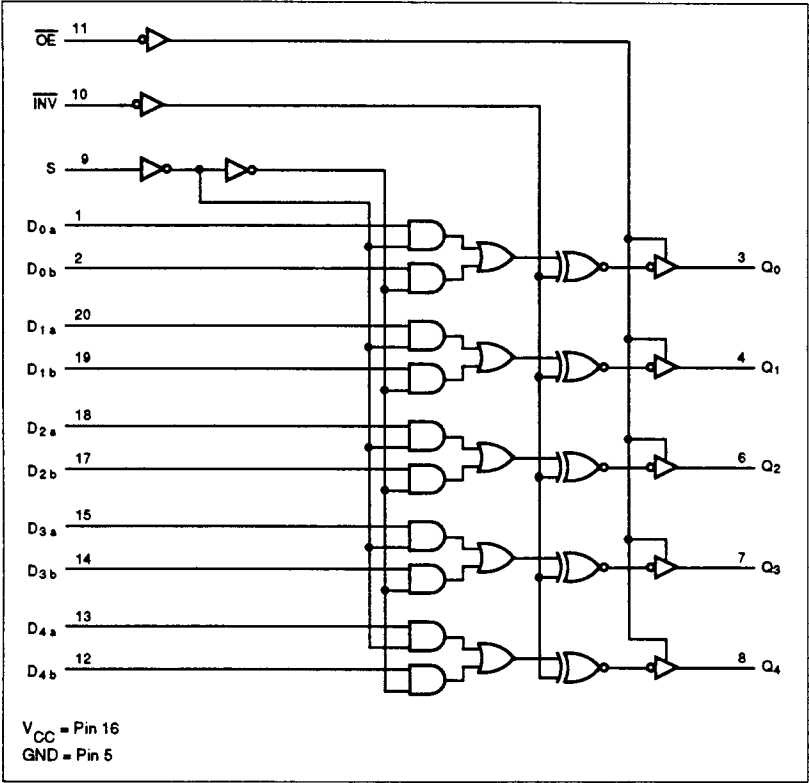
LOGIC SYMBOL(IEEE/IEC)



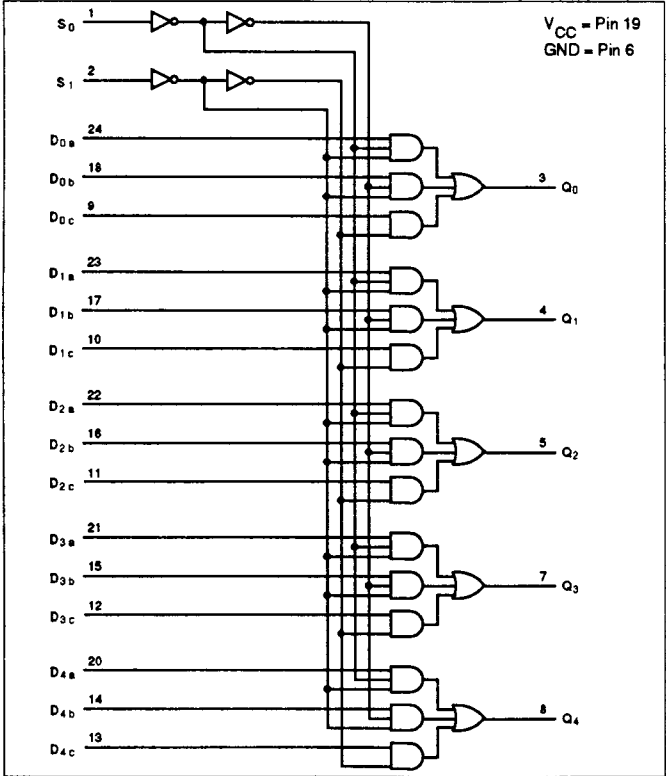
Multiplexers

FAST 74F711A/711-1, 74F712A/712-1

LOGIC DIAGRAM for 'F711A/F711-1



LOGIC DIAGRAM, 'F712A/F712-1



Multiplexers

FAST 74F711A/711-1, 74F712A/712-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _{IN}	Input voltage		-0.5 to +7.0	V
I _{IN}	Input current		-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state		-0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	'F711A, 'F712A	96	mA
		'F711-1, 'F712-1	10	mA
T _A	Operating free-air temperature range		0 to +70	°C
T _{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V _{CC}	Supply voltage		4.5	5.0	5.5	V
V _{IH}	High-level input voltage		2.0			V
V _{IL}	Low-level input voltage				0.8	V
I _{IK}	Input clamp current				-18	mA
I _{OL}	High-level output current				-15	mA
I _{OL}	Low-level output current	'F711A, 'F712A			64	mA
		'F711-1, 'F712-1			5	mA
T _A	Operating free-air temperature		0		70	°C

Multiplexers

FAST 74F711A/711-1, 74F712A/712-1

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						Min	Typ ²	Max	
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -3mA	±10%V _{CC}	2.4			V
					±5%V _{CC}	2.7	3.4		V
				I _{OH} = -15mA	±10%V _{CC}	2.0			V
					±5%V _{CC}	2.0			V
V _{OL}	Low-level output voltage	'F711A/ 'F712A only	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	±10%V _{CC}		0.38	0.55	V
				I _{OL} = 5mA	±5%V _{CC}		0.42	0.55	V
					±10%V _{CC}		0.38	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				-0.73	-1.2	V
I _I	Input current at maximun input voltage		V _{CC} = MAX, V _I = 7.0V					100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current	Others	V _{CC} = MAX, V _I = 0.5V					-20	μA
		D _n only						-40	μA
I _{OZH}	Off-state output current High-level voltage applied	'F711A/ 'F711-1 only	V _{CC} = MAX, V _O = 2.7V					50	μA
I _{OZL}	Off-state output current Low-level voltage applied		V _{CC} = MAX, V _O = 0.5V					-50	μA
I _{OS}	Short circuit output current ³	'F711-1/ 'F712-1	V _{CC} = MAX			-60		-150	mA
I _O	Output current ⁴	'F711A/ 'F712A	V _{CC} = MAX, V _O = 2.25V			-60		-150	mA
I _{CC}	Supply current (total)	'F711A	I _{CC} H	V _{CC} = MAX			25	35	mA
			I _{CC} L				33	46	mA
			I _{CC} Z				27	40	mA
		'F711-1	I _{CC} H	V _{CC} = MAX			26	40	mA
			I _{CC} L				33	45	mA
			I _{CC} Z				28	45	mA
		'F712A	I _{CC} H	V _{CC} = MAX			20	27	mA
			I _{CC} L				30	40	mA
		'F712-1	I _{CC} H	V _{CC} = MAX			20	30	mA
			I _{CC} L				29	40	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

Multiplexers

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AC ELECTRICAL CHARACTERISTICS for 74F711A/74F711-1

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω		
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} to Q _n	74F711A	Waveform 1, 2	2.5 2.5	5.0 4.0	7.5 7.0	2.0 2.0	8.0 7.5	ns
t _{PLH} t _{PHL}	Propagation delay S to Q _n		Waveform 1,3	7.0 5.0	9.0 8.0	12.0 11.0	5.5 4.5	13.5 12.0	ns
t _{PLH} t _{PHL}	Propagation delay <u>INV</u> to Q _n		Waveform 1,3	6.0 4.0	9.0 8.0	12.5 11.0	5.0 3.5	14.0 11.5	ns
t _{PZH} t _{PZL}	Output Enable time <u>OE</u> to Q _n		Waveform 4 Waveform 5	2.5 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
t _{PHZ} t _{PLZ}	Output Disable time <u>OE</u> to Q _n		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 8.0	2.0 2.5	8.0 8.5	ns
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} to Q _n	74F711-1	Waveform 1, 2	3.0 2.0	4.5 4.5	7.5 7.5	2.0 2.5	9.0 8.0	ns
t _{PLH} t _{PHL}	Propagation delay S, <u>INV</u> to Q _n		Waveform 1,3	6.5 4.5	10.0 8.5	13.5 11.5	5.5 4.0	14.5 12.5	ns
t _{PZH} t _{PZL}	Output Enable time <u>OE</u> to Q _n		Waveform 4 Waveform 5	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	9.0 8.0	ns
t _{PHZ} t _{PLZ}	Output Disable time <u>OE</u> to Q _n		Waveform 4 Waveform 5	2.0 3.5	4.5 5.5	7.0 8.5	2.0 3.0	8.0 9.5	ns

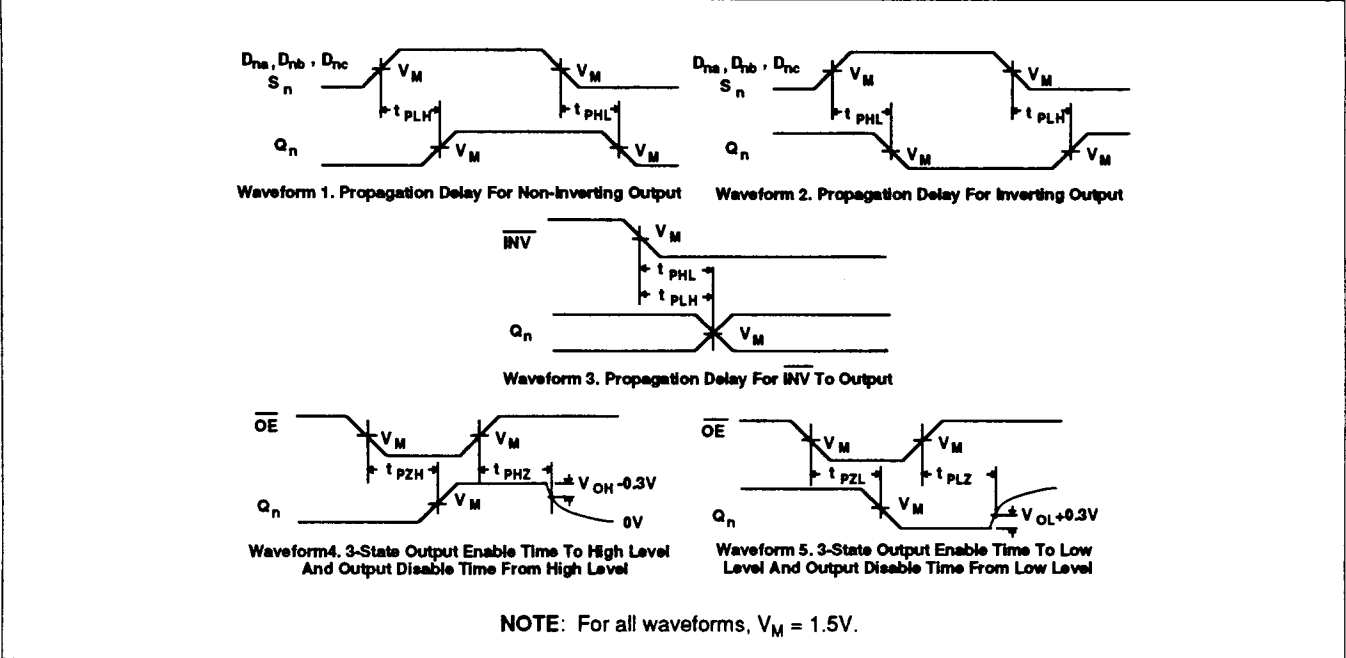
AC ELECTRICAL CHARACTERISTICS for 74F712A/74F712-1

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω		
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} , D _{nc} to Q _n	74F712A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 7.0	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ to Q _n		Waveform 1	6.5 5.0	8.0 7.5	11.5 10.0	5.5 4.5	13.5 11.0	ns
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} , D _{nc} to Q _n	74F712-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ to Q _n		Waveform 1	7.0 5.5	9.0 7.5	12.0 10.5	6.0 5.5	13.5 11.0	ns

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

