

# 4-Mbit (256 K × 18) Flow through Sync SRAM

## Features

- 256 K × 18 common I/O
- 3.3 V core power supply (V<sub>DD</sub>)
- 2.5 V or 3.3 V I/O power supply (V<sub>DDQ</sub>)
- Fast clock-to-output times
- 6.5 ns (133 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed write
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package, Pb-free and non Pb-free 119-ball BGA Package
- “ZZ” sleep mode option

## Functional Description

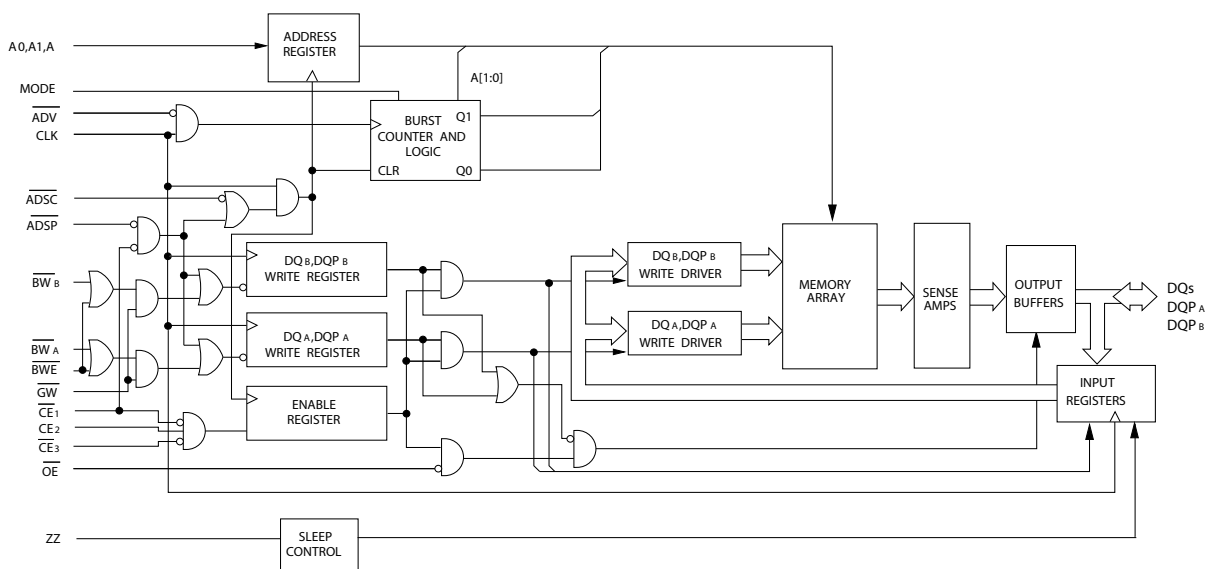
The CY7C1325G<sup>[1]</sup> is a 256 K × 18 synchronous cache RAM designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2 bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ( $\overline{CE}_1$ ), depth-expansion chip enables ( $\overline{CE}_2$  and  $\overline{CE}_3$ ), burst control inputs (ADSC, ADSP, and ADV), write enables ( $BW_{[A:B]}$ , and BWE), and global write (GW). Asynchronous inputs include the output enable ( $\overline{OE}$ ) and the ZZ pin.

The CY7C1325G allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

The CY7C1325G operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

## Logic Block Diagram



**Note**

1. For best practice recommendations, refer to the Cypress application note “System Design Guidelines” on [www.cypress.com](http://www.cypress.com).

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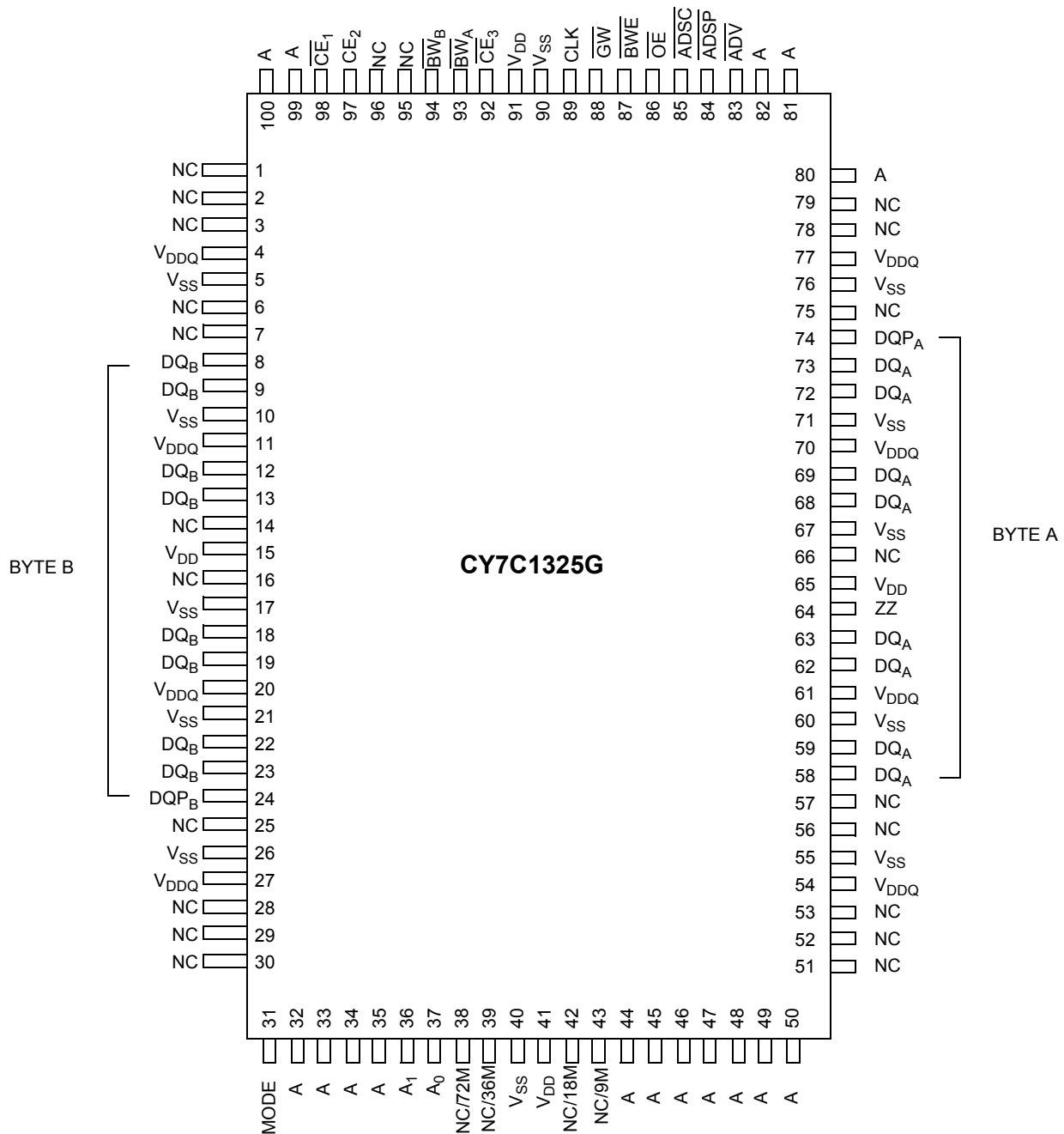
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**Selection Guide**

Description	133 MHz	100 MHz	Unit
Maximum access time	6.5	8.0	ns
Maximum operating current	225	205	mA
Maximum standby current	40	40	mA

**Pin Configurations**

**Figure 1. 100-pin TQFP Pinout**



**Pin Configurations** (continued)

**Figure 2. 119-ball BGA Pinout**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC/288M	CE <sub>2</sub>	A	$\overline{\text{ADSC}}$	A	$\overline{\text{CE}}_3$	NC/576M
<b>C</b>	NC/144M	A	A	V <sub>DD</sub>	A	A	NC/1G
<b>D</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>A</sub>	NC
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{CE}}_1$	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	$\overline{\text{OE}}$	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>G</b>	NC	DQ <sub>B</sub>	$\overline{\text{BW}}_B$	$\overline{\text{ADV}}$	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>H</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	$\overline{\text{BW}}_A$	DQ <sub>A</sub>	NC
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>B</sub>	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>P</b>	NC	DQP <sub>B</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	NC	A	NC
<b>T</b>	NC/72M	A	A	NC/36M	A	A	ZZ
<b>U</b>	V <sub>DDQ</sub>	NC	NC	NC	NC	NC	V <sub>DDQ</sub>

**Pin Definitions**

Name	I/O	Description
A0, A1, A	Input-synchronous	<b>Address inputs used to select one of the 256 K address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> are sampled active. A <sub>[1:0]</sub> feed the 2 bit counter.
$\overline{\text{BW}}_A, \overline{\text{BW}}_B$	Input-synchronous	<b>Byte write select inputs, active LOW.</b> Qualified with $\overline{\text{BWE}}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{\text{GW}}$	Input-synchronous	<b>Global write enable input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{\text{BW}}_{[A:B]}$ and $\overline{\text{BWE}}$ ).
$\overline{\text{BWE}}$	Input-synchronous	<b>Byte write enable input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-clock	<b>Clock input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{\text{CE}}_1$	Input-synchronous	<b>Chip enable 1 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and $\overline{\text{CE}}_3$ to select/deselect the device. ADSP is ignored if $\overline{\text{CE}}_1$ is HIGH. $\overline{\text{CE}}_1$ is sampled only when a new external address is loaded.
CE <sub>2</sub>	Input-synchronous	<b>Chip enable 2 input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>3</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded.
$\overline{\text{CE}}_3$	Input-synchronous	<b>Chip enable 3 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>2</sub> to select/deselect the device. CE <sub>3</sub> is sampled only when a new external address is loaded.
$\overline{\text{OE}}$	Input-asynchronous	<b>Output enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{\text{OE}}$ is masked during the first clock of a read cycle when emerging from a deselected state.

**Pin Definitions** (continued)

Name	I/O	Description
ADV	Input-synchronous	<b>Advance input signal, sampled on the rising edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-synchronous	<b>Address strobe from processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when $\overline{CE}_1$ is deasserted HIGH.
ADSC	Input-synchronous	<b>Address strobe from controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	Input-asynchronous	<b>ZZ “sleep” input, active HIGH.</b> When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. During normal operation, this pin has to be low or left floating. ZZ pin has an internal pull-down.
DQs DQP <sub>A</sub> , DQP <sub>B</sub>	I/O-synchronous	<b>Bidirectional data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP <sub>[A:B]</sub> are placed in a tristate condition.
V <sub>DD</sub>	Power supply	<b>Power supply inputs to the core of the device.</b>
V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b>
V <sub>DDQ</sub>	I/O power supply	<b>Power supply for the I/O circuitry.</b>
MODE	Input-static	<b>Selects burst order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
NC		<b>No connects.</b> Not Internally connected to the die.
NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	<b>No connects.</b> Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins that are not internally connected to the die.

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CDV}$ ) is 6.5 ns (133 MHz device).

The CY7C1325G supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select ( $BW_{[A:B]}$ ) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip selects ( $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$ ) and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output tristate control. ADSP is ignored if  $CE_1$  is HIGH.

### Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$  are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the  $\overline{OE}$  input is asserted LOW, the requested data is available at the data outputs, a maximum to  $t_{CDV}$  after clock rise. ADSP is ignored if  $CE_1$  is HIGH.

### Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$  are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and  $BW_{[A:B]}$ ) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the

appropriate data is latched and written into the device. Byte writes are allowed. During byte writes,  $BW_A$  controls  $DQ_A$  and  $BW_B$  controls  $DQ_B$ . All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous  $\overline{OE}$  input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to  $DQ_S$ . As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$  are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted HIGH, and (4) the write input signals (GW, BWE, and  $BW_{[A:B]}$ ) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to  $DQ_{[A:D]}$  is written into the specified address location. Byte writes are allowed. During byte writes,  $BW_A$  controls  $DQ_A$ ,  $BW_B$  controls  $DQ_B$ . All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous  $\overline{OE}$  input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to  $DQ_S$ . As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Burst Sequences

The CY7C1325G provides an on-chip two bit wraparound burst counter inside the SRAM. The burst counter is fed by  $A_{[1:0]}$ , and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode.  $\overline{CE}$ s, ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

**Interleaved Burst Address Table  
(MODE = Floating or V<sub>DD</sub>)**

First Address A <sub>1</sub> , A <sub>0</sub>	Second Address A <sub>1</sub> , A <sub>0</sub>	Third Address A <sub>1</sub> , A <sub>0</sub>	Fourth Address A <sub>1</sub> , A <sub>0</sub>
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**Linear Burst Address Table (MODE = GND)**

First Address A <sub>1</sub> , A <sub>0</sub>	Second Address A <sub>1</sub> , A <sub>0</sub>	Third Address A <sub>1</sub> , A <sub>0</sub>	Fourth Address A <sub>1</sub> , A <sub>0</sub>
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>DDZZ</sub>	Sleep mode standby current	ZZ ≥ V <sub>DD</sub> - 0.2 V	-	40	mA
t <sub>ZZS</sub>	Device operation to ZZ	ZZ ≥ V <sub>DD</sub> - 0.2 V	-	2t <sub>CYC</sub>	ns
t <sub>ZZREC</sub>	ZZ recovery time	ZZ ≤ 0.2 V	2t <sub>CYC</sub>	-	ns
t <sub>ZZI</sub>	ZZ active to sleep current	This parameter is sampled	-	2t <sub>CYC</sub>	ns
t <sub>RZZI</sub>	ZZ inactive to exit sleep current	This parameter is sampled	0	-	ns

## Truth Table

The Truth Table for part CY7C1325G is as follows. [2, 3, 4, 5, 6]

Cycle Description	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	X	X	X	L	H	L	X	X	X	L-H	Tri-state
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-state
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-state
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-state
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-state
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-state
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-state
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

### Notes

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = L$  when any one or more Byte Write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ) and  $\overline{BWE} = L$  or  $\overline{GW} = L$ .  $\overline{WRITE} = H$  when all Byte write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ),  $\overline{BWE}$ ,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_{[A:B]}$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate.  $\overline{OE}$  is a don't care for the remainder of the write cycle.
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).



**Truth Table for Read/Write**

The Truth Table for Read/Write for part CY7C1325G is as follows. [7]

Function	GW	BWE	BW <sub>B</sub>	BW <sub>A</sub>
Read	H	H	X	X
Read	H	L	H	H
Write byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	H	L	H	L
Write byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

**Note**

7. X = "Don't Care." H = Logic HIGH, L = Logic LOW.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power applied .....	-55 °C to +125 °C
Supply voltage on V <sub>DD</sub> relative to GND .....	-0.5 V to +4.6 V
Supply voltage on V <sub>DDQ</sub> relative to GND .....	-0.5 V to +V <sub>DD</sub>
DC voltage applied to outputs in tristate .....	-0.5 V to V <sub>DDQ</sub> + 0.5 V
DC input voltage .....	-0.5 V to V <sub>DD</sub> + 0.5 V
Current into outputs (LOW) .....	20 mA
Static discharge voltage .....	> 2001 V (per MIL-STD-883, method 3015)
Latch-up current .....	> 200 mA

## Operating Range

Range	Ambient Temperature <sup>1</sup>	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V <sub>DD</sub>
Industrial	-40 °C to +85 °C		

## Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical single bit upsets	25 °C	361	394	FIT/Mb
LMBU	Logical multi bit upsets	25 °C	0	0.01	FIT/Mb
SEL	Single event latch up	85 °C	0	0.1	FIT/Dev

\* No LMBU or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

## Electrical Characteristics

Over the Operating Range <sup>[8, 9]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit	
V <sub>DD</sub>	Power supply voltage		3.135	3.6	V	
V <sub>DDQ</sub>	I/O supply voltage		2.375	V <sub>DD</sub>	V	
V <sub>OH</sub>	Output HIGH voltage	for 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4	–	V	
		for 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0	–	V	
V <sub>OL</sub>	Output LOW voltage	for 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	–	0.4	V	
		for 2.5 V I/O, I <sub>OL</sub> = 1.0 mA	–	0.4	V	
V <sub>IH</sub>	Input HIGH voltage	for 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V	
		for 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V	
V <sub>IL</sub>	Input LOW voltage <sup>[8]</sup>	for 3.3 V I/O	-0.3	0.8	V	
		for 2.5 V I/O	-0.3	0.7	V	
I <sub>X</sub>	Input leakage current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA	
	Input current of MODE	Input = V <sub>SS</sub>	-30	–	μA	
		Input = V <sub>DD</sub>	–	5	μA	
	Input current of ZZ	Input = V <sub>SS</sub>	-5	–	μA	
Input = V <sub>DD</sub>		–	30	μA		
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> ; output disabled	-5	5	μA	
I <sub>DD</sub>	V <sub>DD</sub> operating supply current	V <sub>DD</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5 ns cycle, 133 MHz	–	225	mA
		10 ns cycle, 100 MHz	–	205	mA	

### Notes

- Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5 V (Pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL</sub>(AC) > -2 V (Pulse width less than t<sub>CYC</sub>/2).
- T<sub>power up</sub>: Assumes a linear ramp from 0 V to V<sub>DD</sub>(min) within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

**Electrical Characteristics** (continued)

Over the Operating Range [8, 9]

Parameter	Description	Test Conditions	Min	Max	Unit	
I <sub>SB1</sub>	Automatic CE power-down current—TTL inputs	Max V <sub>DD</sub> , device deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> , inputs switching	7.5 ns cycle, 133 MHz	–	90	mA
			10 ns cycle, 100 MHz	–	80	mA
I <sub>SB2</sub>	Automatic CE power-down current—CMOS inputs	Max V <sub>DD</sub> , device deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0, inputs static	All speeds	–	40	mA
I <sub>SB3</sub>	Automatic CE power-down current—CMOS inputs	Max V <sub>DD</sub> , device deselected, V <sub>IN</sub> ≥ V <sub>DDQ</sub> – 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = f <sub>MAX</sub> , inputs switching	7.5 ns cycle, 133 MHz	–	75	mA
			10 ns cycle, 100 MHz	–	65	mA
I <sub>SB4</sub>	Automatic CE power-down current—TTL inputs	Max V <sub>DD</sub> , device deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> – 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0, inputs static	All speeds	–	45	mA

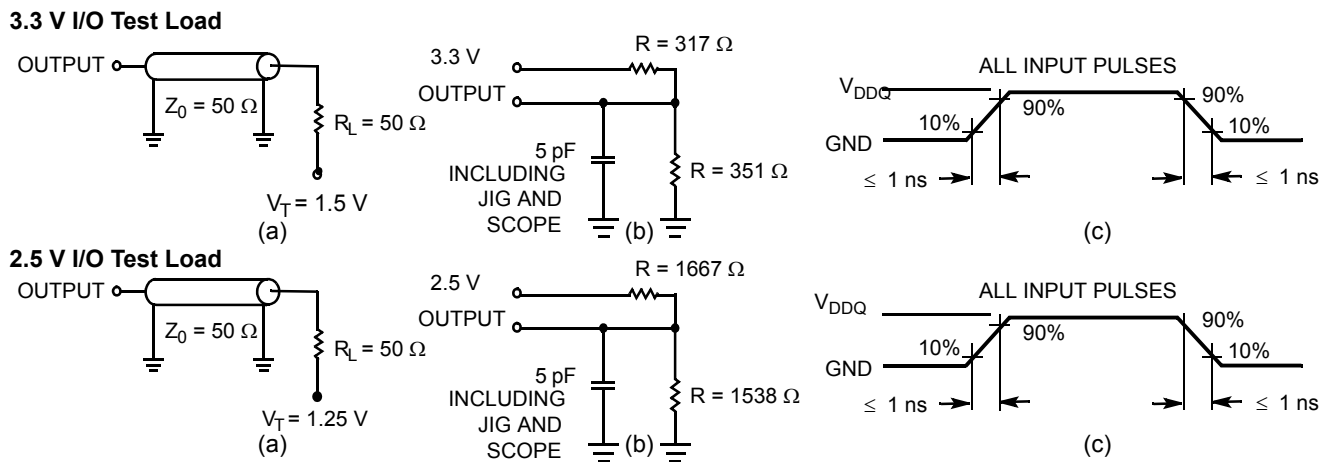
**Capacitance**[10]

Parameter	Description	Test Conditions	100-pin TQFP Max	119-ball BGA Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>DD</sub> = 3.3 V, V <sub>DDQ</sub> = 3.3 V	5	5	pF
C <sub>CLK</sub>	Clock input capacitance		5	5	pF
C <sub>I/O</sub>	Input/output capacitance		5	7	pF

**Thermal Resistance**[10]

Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	34.1	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		6.85	14.0	°C/W

**Figure 3. AC Test Loads and Waveforms**



**Note**  
10. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range<sup>[11, 12]</sup>

Parameter	Description	-133		-100		Unit
		Min	Max	Min	Max	
t <sub>POWER</sub>	V <sub>DD</sub> (Typical) to the first access <sup>[13]</sup>	1	–	1	–	ms
<b>Clock</b>						
t <sub>CYC</sub>	Clock cycle time	7.5	–	10	–	ns
t <sub>CH</sub>	Clock HIGH	2.5	–	4.0	–	ns
t <sub>CL</sub>	Clock LOW	2.5	–	4.0	–	ns
<b>Output Times</b>						
t <sub>CDV</sub>	Data output valid after CLK rise	–	6.5	–	8.0	ns
t <sub>DOH</sub>	Data output hold after CLK rise	2.0	–	2.0	–	ns
t <sub>CLZ</sub>	Clock to low Z <sup>[14, 15, 16]</sup>	0	–	0	–	ns
t <sub>CHZ</sub>	Clock to high Z <sup>[14, 15, 16]</sup>	–	3.5	–	3.5	ns
t <sub>OEV</sub>	OE LOW to output valid	–	3.5	–	3.5	ns
t <sub>OELZ</sub>	OE LOW to output low Z <sup>[14, 15, 16]</sup>	0	–	0	–	ns
t <sub>OEHZ</sub>	OE HIGH to output high Z <sup>[14, 15, 16]</sup>	–	3.5	–	3.5	ns
<b>Setup Times</b>						
t <sub>AS</sub>	Address setup before CLK rise	1.5	–	2.0	–	ns
t <sub>ADS</sub>	ADSP, ADSC setup before CLK rise	1.5	–	2.0	–	ns
t <sub>ADVS</sub>	ADV setup before CLK rise	1.5	–	2.0	–	ns
t <sub>WES</sub>	GW, BWE, BW <sub>X</sub> setup before CLK rise	1.5	–	2.0	–	ns
t <sub>DS</sub>	Data input setup before CLK rise	1.5	–	2.0	–	ns
t <sub>CES</sub>	Chip enable setup	1.5	–	2.0	–	ns
<b>Hold Times</b>						
t <sub>AH</sub>	Address hold after CLK rise	0.5	–	0.5	–	ns
t <sub>ADH</sub>	ADSP, ADSC hold after CLK rise	0.5	–	0.5	–	ns
t <sub>WEH</sub>	GW, BWE, BW <sub>X</sub> hold after CLK rise	0.5	–	0.5	–	ns
t <sub>ADVH</sub>	ADV hold after CLK rise	0.5	–	0.5	–	ns
t <sub>DH</sub>	Data input hold after CLK rise	0.5	–	0.5	–	ns
t <sub>CEH</sub>	Chip enable hold after CLK rise	0.5	–	0.5	–	ns

### Notes

11. Timing reference level is 1.5 V when V<sub>DDQ</sub> = 3.3 V and is 1.25 V when V<sub>DDQ</sub> = 2.5 V.

12. Test conditions shown in (a) of Figure 3 on page 11 unless otherwise noted.

13. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD</sub>(minimum) initially before a read or write operation can be initiated.

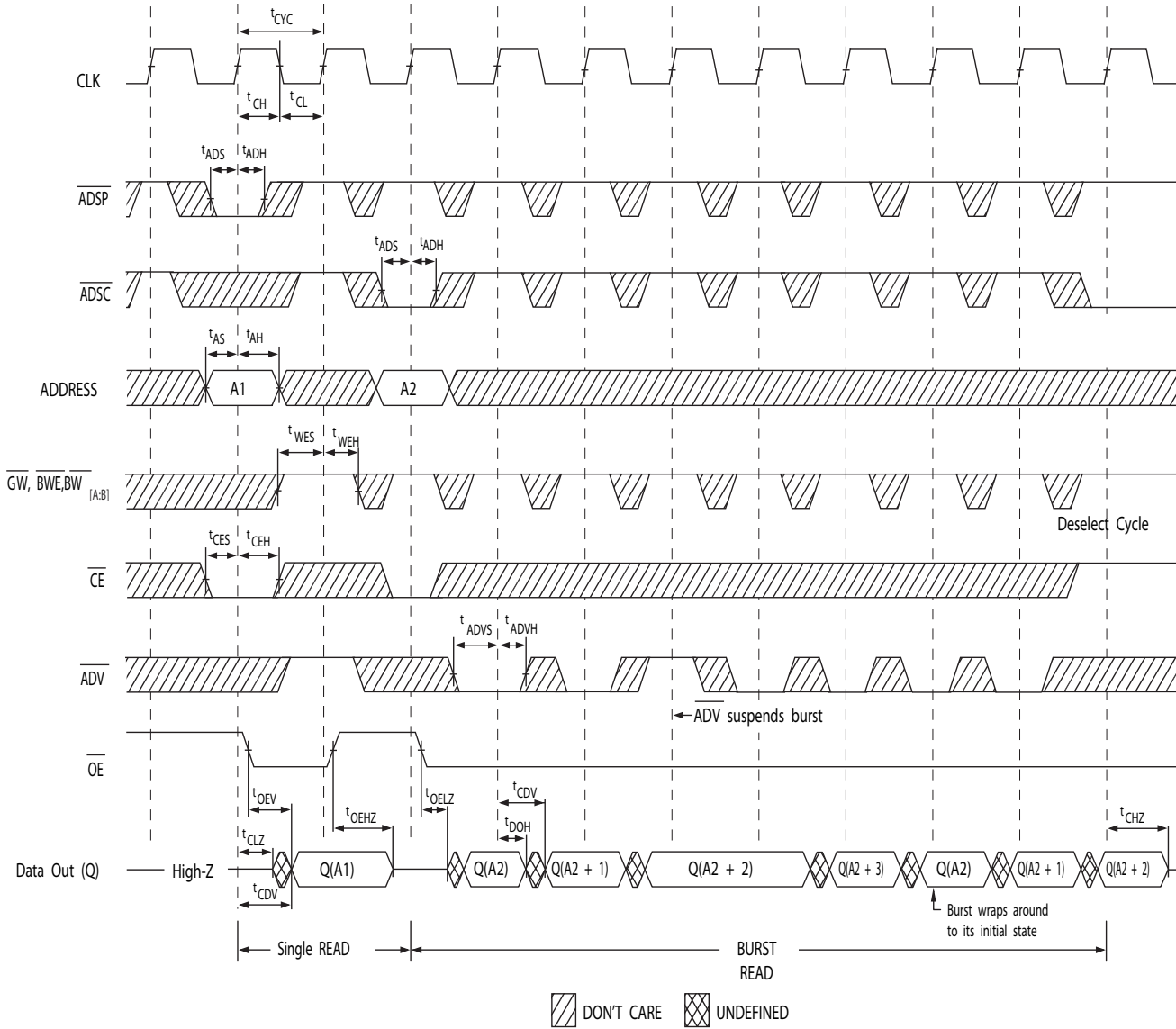
14. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OELZ</sub>, and t<sub>OEHZ</sub> are specified with AC test conditions shown in part (b) of Figure 3 on page 11. Transition is measured ± 200 mV from steady-state voltage.

15. At any voltage and temperature, t<sub>OEHZ</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

16. This parameter is sampled and not 100% tested.

Timing Diagrams

Figure 4. Read Cycle Timing<sup>[17]</sup>

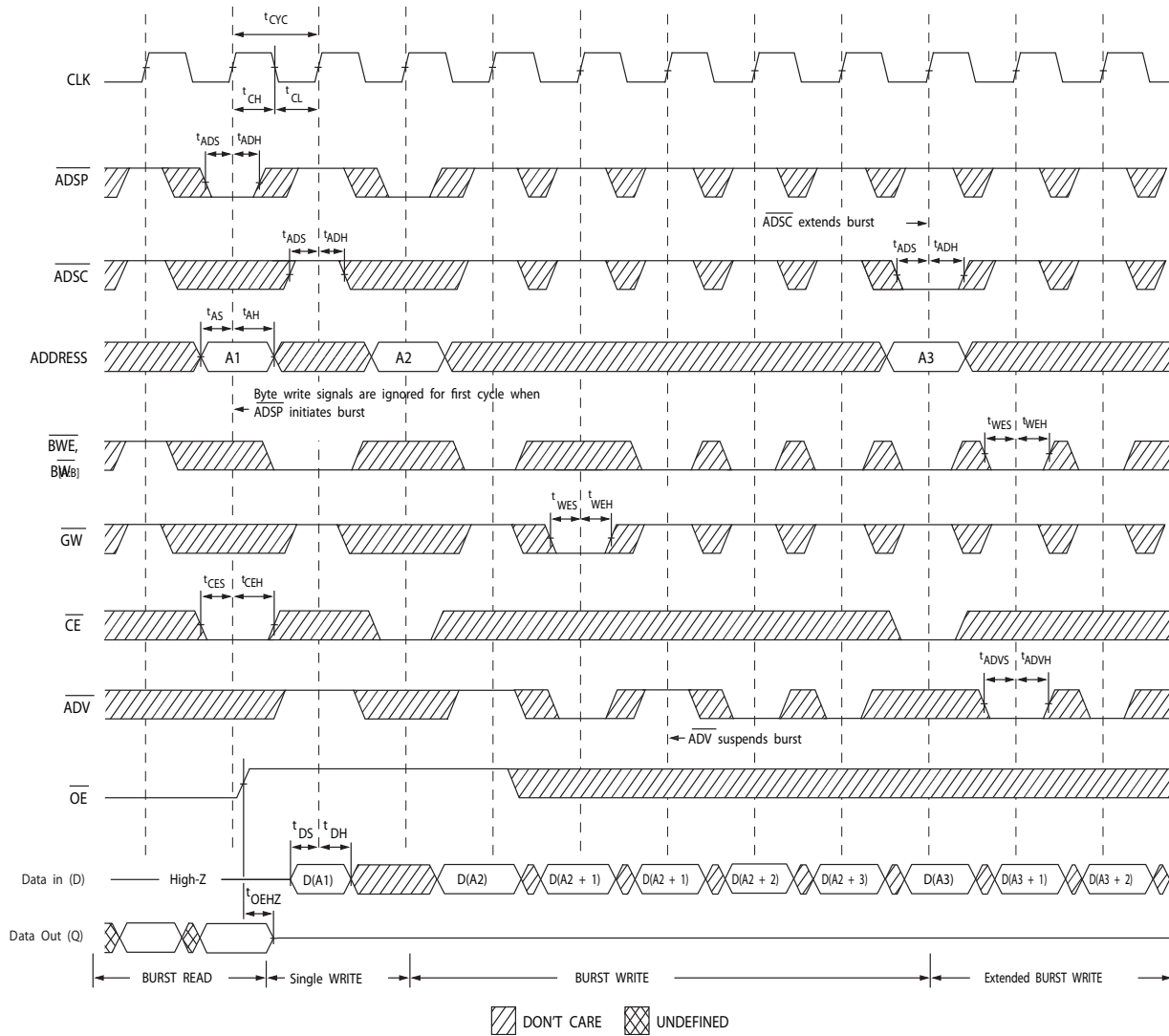


Note

17. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

Timing Diagrams (continued)

Figure 5. Write Cycle Timing [18, 19]



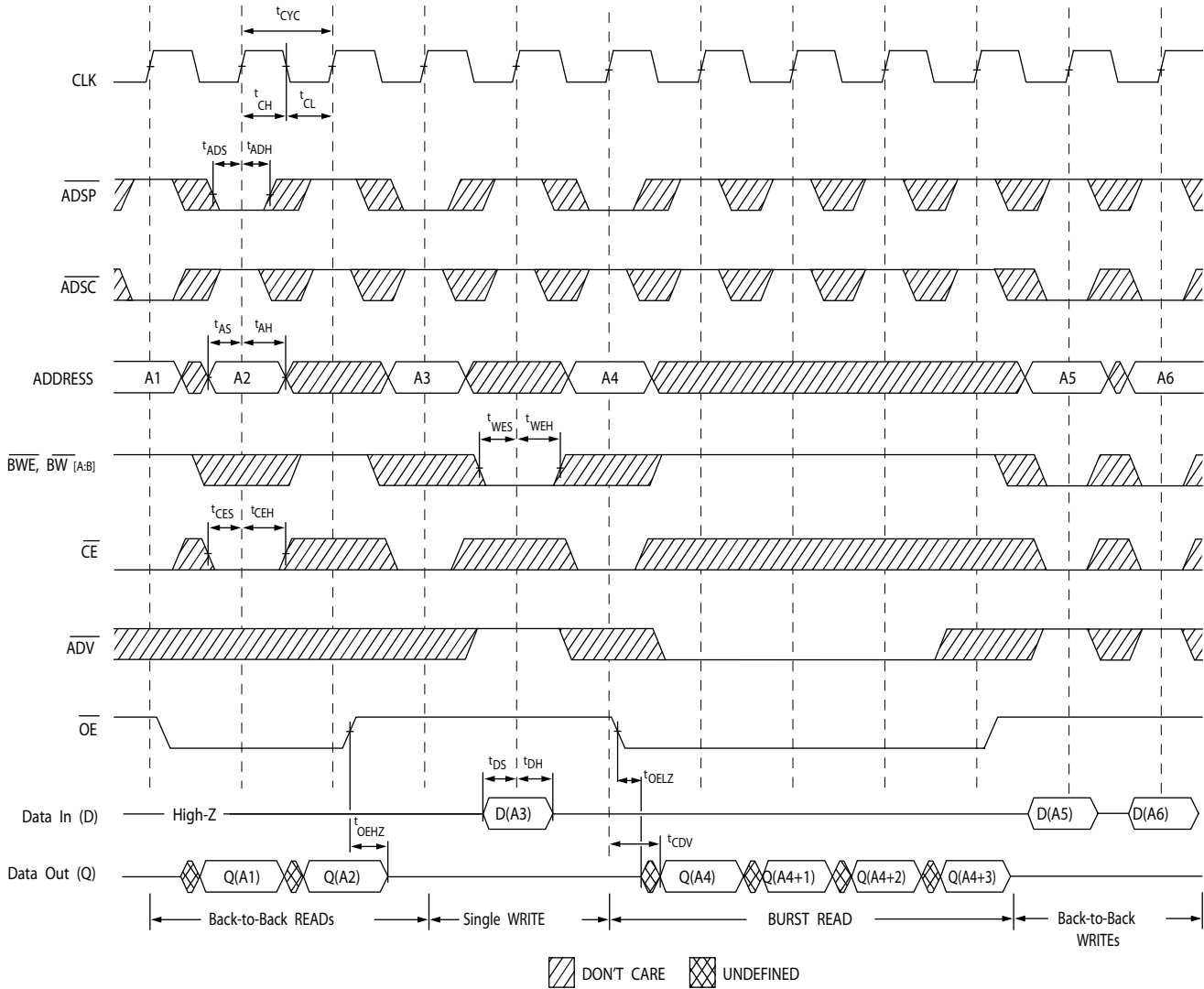
Notes

18. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.

19. Full width write can be initiated by either  $\overline{GW}$  LOW; or by  $\overline{GW}$  HIGH,  $\overline{BWE}$  LOW and  $\overline{BW}_{[A:B]}$  LOW.

Timing Diagrams (continued)

Figure 6. Read/Write Timing<sup>[20, 21, 22]</sup>

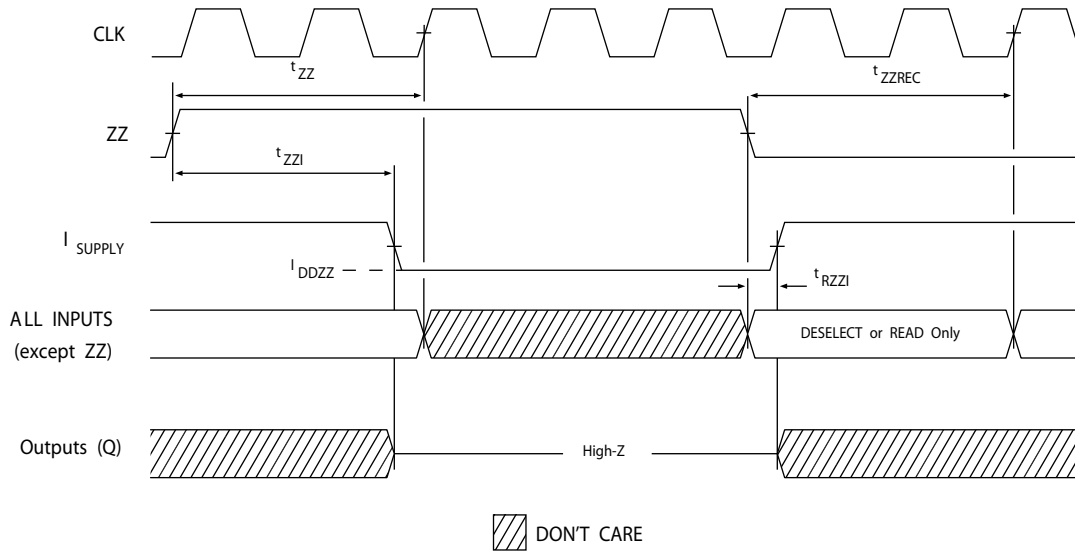


Notes

- 20. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.
- 21. The data bus (Q) remains in High Z following a WRITE cycle, unless a new read access is initiated by  $\overline{ADSP}$  or  $\overline{ADSC}$ .
- 22. GW is HIGH.

Timing Diagrams (continued)

Figure 7. ZZ Mode Timing<sup>[23, 24]</sup>



Notes

- 23. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
- 24. DQs are in High Z when exiting ZZ sleep mode.



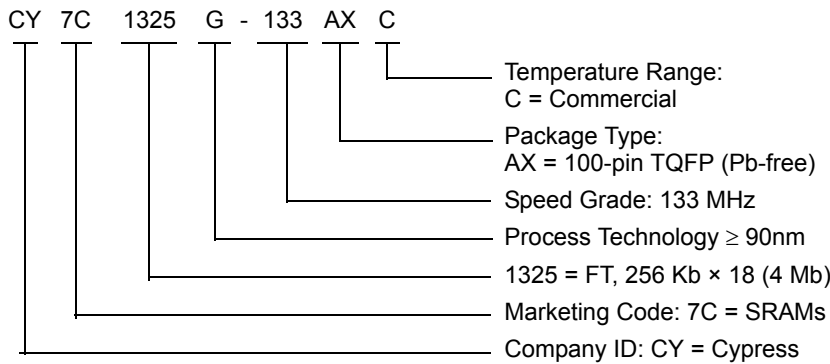
### Ordering Information

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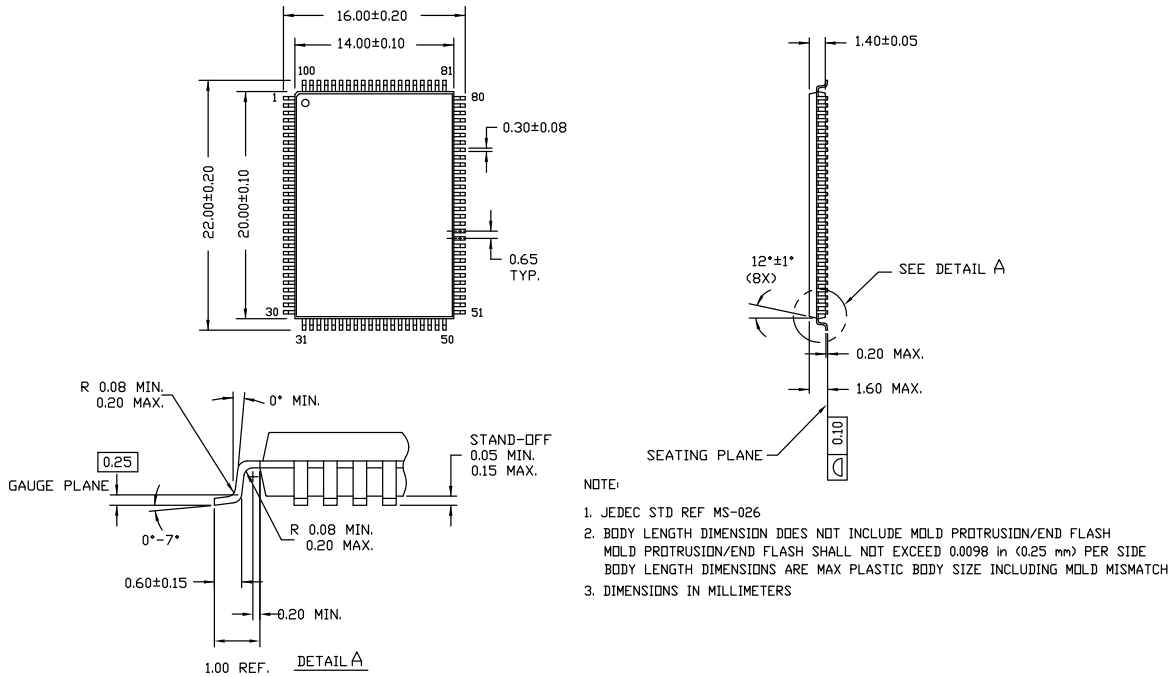
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1325G-133AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial

### Ordering Code Definitions



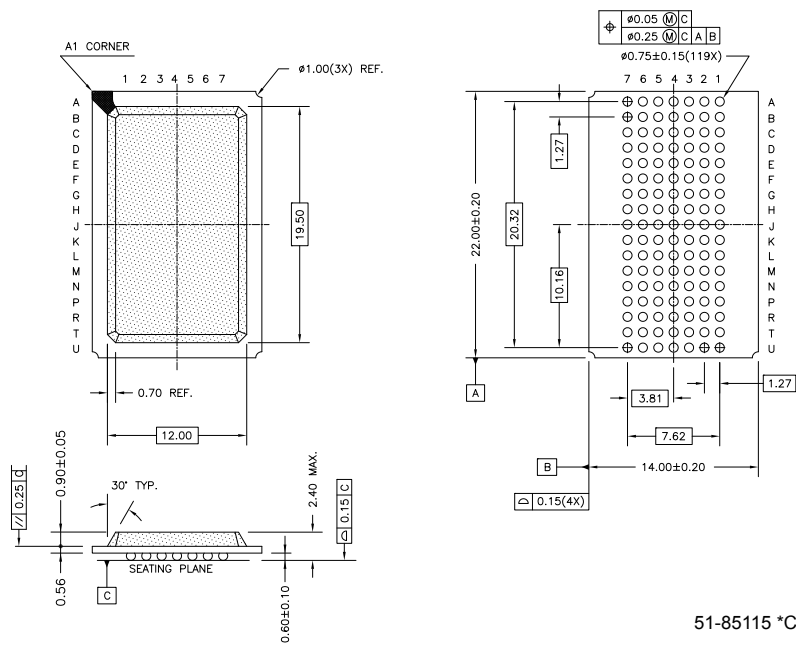
Package Diagrams

Figure 8. 100-pin TQFP (14 × 20 × 1.4 mm), 51-85050



51-85050 \*D

Figure 9. 119-ball BGA (14 × 22 × 2.4 mm), 51-85115



51-85115 \*C

## Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
CE	chip enable
CEN	clock enable
I/O	input/output
OE	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

**Document History Page**

Document Title: CY7C1325G, 4-Mbit (256 K × 18) Flow through Sync SRAM				
Document Number: 38-05518				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	224366	RKF	See ECN	New datasheet
*A	283775	VBL	See ECN	Deleted 66 MHz Changed TQFP package to Pb-Free TQFP in Ordering Information section Added BG Pb-Free package
*B	333626	SYT	See ECN	Removed 117 MHz speed bin Modified Address Expansion balls in the pinouts for 100 TQFP and 119 BGA Packages as per JEDEC standards and updated the Pin Definitions accordingly Modified $V_{OL}$ , $V_{OH}$ test conditions Replaced 'Snooze' with 'Sleep' Replaced TBD's for $\theta_{JA}$ and $\theta_{JC}$ to their respective values on the Thermal Resistance table Changed the package name for 100 TQFP from A100RA to A101 Removed comment on the availability of BG Pb-Free package Updated the Ordering Information by shading and unshading MPNs as per availability
*C	418633	R XU	See ECN	Converted From Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Modified test condition in Footnote from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$ Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table. Replaced Package Name column with Package Diagram in the Ordering Information table Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information
*D	480124	VKN	See ECN	Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND. Updated the Ordering Information table.
*E	2756998	VKN	08/28/09	Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information.
*F	3036073	NJY	09/22/2010	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Minor edits and updated in new template.
*G	3052903	NJY	10/08/10	Removed the following pruned part from the ordering information table. CY7C1325G-100AXI
*H	3208774	NJY	03/29/2011	Updated <a href="#">Ordering Information</a> . Updated <a href="#">Package Diagrams</a> .

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