# AN1228
# APPLICATION NOTE

# RELATE LDMOS DEVICE PARAMETERS TO RF PERFORMANCE

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## 1. ABSTRACT

This second installment of a two-part paper series on LDMOS technology (see *Understanding LDMOS Device Fundamentals*, AN1226) will explain LDMOS circuit-level performance through MOS intrinsic device characteristics. Understanding current laterally diffused Metal-Oxide-Semiconductor (LDMOS) technology is necessary to optimally use these devices in high-power RF circuitry. RF circuit designers must come to an understanding of the relationship between circuit performance and device characteristics beyond first-order approximations. These higher-order device relationships can offer insight into many common device parameters and their interdependencies and, more important, enable the design engineer to monitor the semiconductor manufacture process more effectively.

In general, for LDMOS devices and MOS field-effect transistors (MOSFETs) the channel is of primary importance. The channel is the inversion layer created within the body of the device that electrically connects the source and drain, as described in the first part of this series. The channel dimensions and its doping determine the forward transconductance ($g_{fs}$) and contribute to the body-related capacitances that ultimately influence RF power gain and frequency response. The body-doping profile is critical for device ruggedness and reliability. Since the introduction of LDMOS devices for high-voltage commercial RF applications device dimensions have evolved from supermicron to submicron in only a few short years. This progress is indicative of future LDMOS generations and it should be noted that the reduction in device size below one micron has not necessarily followed traditional scaling laws.

Specification sheets for RF MOSFETs include many parameters that will be explained in the context of circuit design and performance criteria. The order in which these device parameters are presented here is not indicative of relative importance.

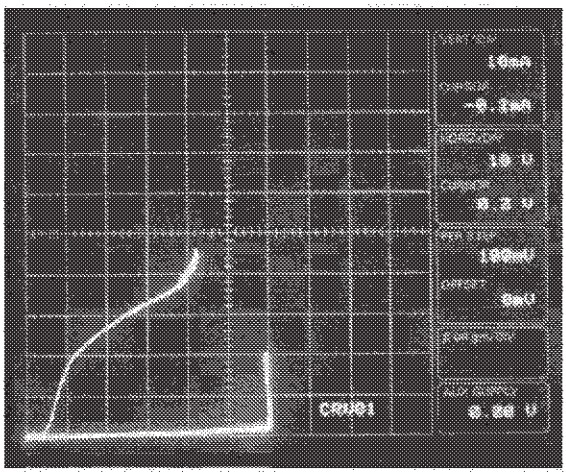
## 2. BREAKDOWN VOLTAGE.

The saturated-drain-source breakdown voltage ($BV_{DSS}$) of a MOSFET device is specified at a particular value of current with the drain biased and the gate, as well as the source, shorted. BVDSS can take many forms as represented in Fig. 1 which shows the curve tracer displays for LDMOS breakdown. A $BV_{DSS}$ curve can have a soft breakdown with multiple breaks in the curve which is indicative of non-uniformities in the stress within the inter-digitated cell structure.

Figure 1 shows a $BV_{DSS}$ curve with characteristics that are typical of a device exhibiting punch-through due to an improper body-doping profile. There are four significant areas on this curve - the low, mid, high and breakdown drain-voltage regions which reflect leakage, punch-through, space-charge-limited current and avalanche current respectively. Figure 1 also shows a curve with a very sharp break where the current suddenly increases. There are two significant regions on this curve - pre-breakdown and post-breakdown. Prior to breakdown, leakage current exists that could be from many sources, such as the normal p-type, n-type (pn) junction leakage due to recombination and generation of carriers in the

quasi-neutral region of the junction. The breakdown-voltage regime is the avalanching of carriers due to the electric field being greater than the critical electric field (approximately $1x10^5$ V/cm). Under these conditions an electron can be accelerated by the electric field. Due to elastic and inelastic scattering this electron acceleration can generate more than one carrier and thus a multiplication scheme transpires.

**Figure 1: Typical Breakdown Curves of a LDMOS Transistor**



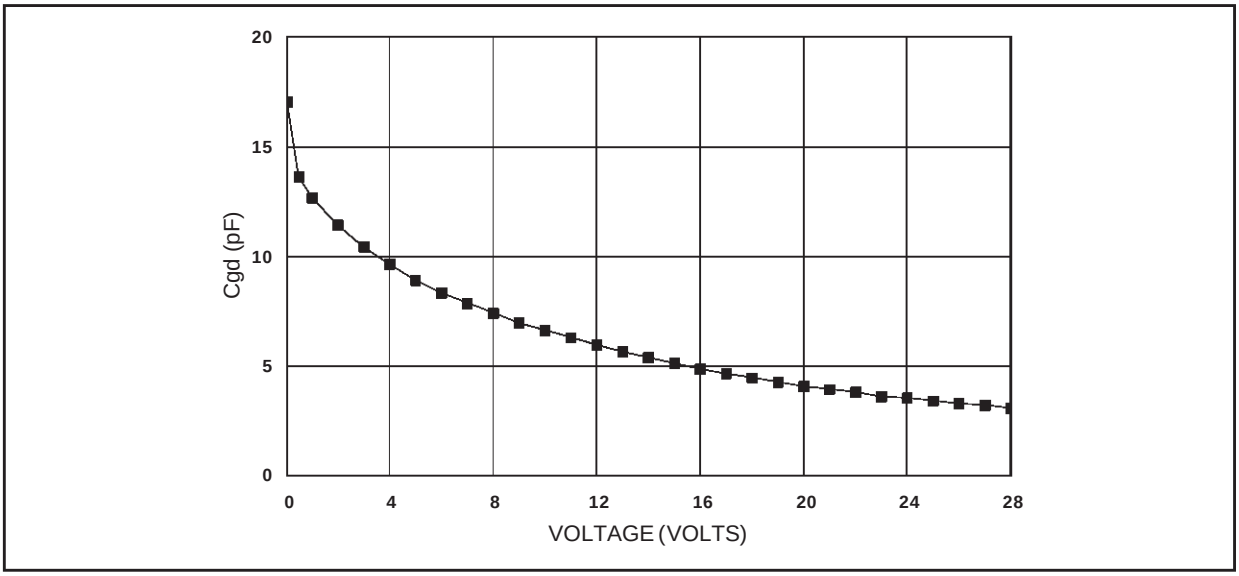
Operating near $BV_{DSS}$ is a reliability risk since the device sustains high-stress conditions. Under these conditions the high-energy carriers can alter the device characteristics by creating, filling and emptying interface traps. For an LDMOS device, if this avalanche condition exists under or near the gate, the hot carriers can penetrate the gate oxide as well as alter the on- and off-state characteristics. Typical problems due to this avalanching include threshold-voltage drift and increased gate leakage. While evaluating devices for this parameter large variations are indicative of inconsistencies in device fabrication. For RF circuit design a general rule of thumb states that the $BV_{DSS}$ should be 2 to 2.5 times the operating voltage in order to support variations in RF voltage.

The saturated gate-source current ($I_{GSS}$) is the leakage current generated when the gate is biased at a specified voltage while maintaining all other terminals at ground. $I_{GSS}$ due to many factors that are related to the integrity of gate oxide and surrounding regions. Ideally this value would be zero for voltage levels that are less than the voltage required to reach the dielectric strength of the gate oxide. However, in practice this condition is not achieved due to the omnipresence of impurities that exist in all wafer fabs and the vagaries of the oxide growth with the temperature profiles used. $I_{GSS}$ can be used to evaluate reliability of this integral component of the MOSFET. Increase of this parameter with a particular device stress can be used to extrapolate the mean time failure (MTTF) of the gate oxide. Overstressing the gate either periodically with RF or statically with DC can also cause an increase in this parameter and thus degrades device performance with respect to RF power gain. Other considerations for the gate oxide include careful electrostatic-discharge (ESD) precautions since the gate oxide is easily damaged.

$I_{DSS}$ is the current produced when the drain is biased at a specific voltage while maintaining source and gate contacts at ground. $I_{DSS}$ has many component contributions. Normal pn junction leakage is not a reliability problem as long as it is maintained at a specified value and does not continue to increase indefinitely. Other sources of $I_{DSS}$ include minority carrier injection from the source due to carriers overcoming the energy barrier resulting from surface band bending and also from subcritical avalanching caused by high electric fields due to a non-ideal body as well as the Laterally-Diffused-Drain (LDD) doping profile.

The reverse transfer capacitance $C_{gd}$ is the feedback capacitance from the device drain to the gate that limits MOS device high-frequency gain. This capacitance is a function of many factors including the gate area, the gate-drain metallurgical over-lap as well as the dynamics of the drain-source depletion spread as a function of drain bias. The three regions of the capacitance-voltage (CV) characteristics in figure 2 are indicative of device formation.

**Figure 2: Reverse Transfer Capacitance vs. Supply Voltage**




For LDMOS devices the zero-volt capacitance is mainly due to the gate-oxide capacitance ($C_{ox}$). The initial decrease in $C_{gd}$ as bias is applied due to the formation of a depletion capacitance, dictated by the doping profile that is in series with $C_{ox}$. It is important that the slope of this initial decrease is large and approaches its final value at some voltage near the saturated drain-source voltage ($V_{DS(sat)}$) due to linearity considerations. The gate-source capacitance ($C_{gs}$) is the capacitance formed between the gate and the ground plane. The LDMOS source, body, epitaxial layer and substrate form the referenced ground plane. The charge formed by application of a voltage to the gate is dependent on the area of the gate, the doping of the body and the metallurgical gate-source overlap. This capacitance is critical since it is the largest component of the input capacitance and constrains device switching speed which is comparable to limiting the maximum frequency of operation. $C_{ds}$ is the capacitance formed between the drain and ground plane where the referenced ground plane is formed by the LDMOS source, body, epitaxial layer and substrate. The charge formed by application of a voltage to the drain is dependent on the area of the LDD and the heavily doped drain, the concentration of the epitaxial layer and, to a lesser extent, the body doping. This capacitance is critical since it is the largest component of the output capacitance and influences device efficiency.

Device data sheets identify these primary capacitances in the form of $C_{rss}$, $C_{iss}$, and $C_{oss}$. Capacitance $C_{rss}$ is simply the gate-drain capacitance, $C_{gd}$, whereas $C_{iss}$ is the parallel combination of $C_{gs}$ and $C_{gd}$. Capacitance $C_{oss}$ is the parallel combination of $C_{ds}$ and $C_{gd}$.

The forward transconductance ($g_{fs}$) identifies the differential drain current for a differential gate voltage. There are three major regions of the function $G_{fs}$ versus $V_{gs}$. As $V_{gs}$ increases from low to mid-range values $G_{fs}$ expands until a linear $G_{fs}$ region is reached. Beyond this region, as high $V_{gs}$ voltages are applied, $G_{fs}$ compresses. For Class AB operation the peak device current should remain below the $G_{fs}$

compression region for maximum linearity. The $G_{fs}$ specification is usually measured in the $G_{fs}$ linear region as shown on device data sheets.

### 3. DEFINING RUGGEDNESS.

The ruggedness or the load-mismatch tolerance of LDMOS technology can be defined in two ways. The first is that after being subjected to extreme load conditions there shall not be any degradation in device performance or output power. A more-stringent criterion would be that there would not be any degradation in the device parameters such as a shift in threshold voltage, an increase in leakage current or a subtle increase in $R_{ds(on)}$. Changes in these parameters can be an indication of long-term reliability problems. The overall ruggedness of a device when tested in extreme load conditions is related to the amount of localized thermal stress, the ability to sustain high levels of drain-source current in $BV_{dss}$ maxi-mum current capability and the intensity of avalanching occurring under or near the gate structure.

### 4. CONCLUSION

The sagacious engineer will take heed of the previously defined parameters and their relationship to circuit performance and reliability. These parameters can be very helpful when identifying problems early in the design stage. Other parameters, such as substrate current, may be even more sensitive but are not always accessible to the design engineer. The implications of the instability of these parameters are manifold and can ultimately be expressed from the sub-atomic device physics regime to the circuit performance. This paper has focused on aspects that the design engineer would consider tractable. By better understanding the relationship of these basic MOSFET parameters to circuit performance, designers can more accurately create effective amplifiers and other active circuits.