Implementing a Common Layout for AMD MirrorBit™ and Intel StrataFlash™ Memory Devices

Application Note

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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Implementing a Common Layout for AMD MirrorBit™ and Intel StrataFlash™ Memory Devices

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Overview

This document describes the benefits of designing with AMD MirrorBit™ Flash memory and the ease with which system designers can layout a board to accommodate high-density flash devices from both AMD and Intel. The layouts shown accept AMD's single-bit per cell LV family, AMD's new two-bit per cell MirrorBit family, and Intel StrataFlash™ 32Mb-128Mb flash memory devices.

What are AMD MirrorBit Devices

AMD's patented MirrorBit technology is a breakthrough flash architecture solution that enables AMD Flash memory devices to hold twice as much data per transistor cell as a standard flash product. What's revolutionary about this accomplishment is that for the first time, this enhanced density is being delivered without sacrificing device performance, endurance, and reliability. AMD provides this technology in devices starting at 32Mb density. These products are pinout and functionally compatible with previous single-bit per cell LV family devices and provide an easy migration path from lower density 2 Megabit to 64Megabit LV devices up to 1 Gigabit MirrorBit devices. For more information on the specifics of MirrorBit architecture visit the AMD web site for a comprehensive white paper and online reference material.

Advantages of Designing with AMD MirrorBit

AMD's new MirrorBit technology provides a low-cost, more reliable alternative to Multi-Level Cell (MLC) solutions. MLC products such as Intel's StrataFlash suffer from performance and reliability concerns inherent when detecting between multiple charge levels in a single Flash cell. The following Table 1 provides a comparison between AMD's MirrorBit and Intel's StrataFlash device features.

Table 1. AMD and Intel 64 Mb Flash Memory Comparison

Specification	AMD LV	AMD MirrorBit	Intel StrataFlash	Notes
Bus Width	x8 only, x8/x16, and x16 only	x8 only, x8/x16, and x16 only	x8/x16	Both selectable via BYTE# pin
Core Supply Voltage	2.7–3.6 V or 3.0–3.6 V	2.7–3.6 V or 3.0–3.6 V	2.7 V–3.6 V	Same core voltage range
I/O Voltage Range	2.7–3.6 V or 3.0–3.6 V	1.65 V–3.6 V	2.7 V–3.6 V	AMD features Enhanced $V_{I/O}$ range 1.65V - 3.6V
Sector Size	64Kbyte	64Kbyte	128Kbyte	64KB is AMD standard sector size
Random Access Time	90 ns	90 ns	120 ns	Access times unchanged on MirrorBit technology
Page Access Time	N/A	25 ns	25 ns	
Page Length	N/A	4 word	4 word	
Word Programming	11us	15 us	13.625 us	MirrorBit and StrataFlash calculated using write buffer (See Note)
Sector Erase Time (typ)	1600ms	400 ms	1000 ms	MirrorBit technology improves erase times for AMD devices
Operating Temp. Range	–40°C to 85°C	–40°C to 85°C	–40°C to 85°C	

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Table 1. AMD and Intel 64 Mb Flash Memory Comparison (Continued)

Specification	AMD LV	AMD MirrorBit	Intel StrataFlash	Notes
Data Retention	20 years @ 125°C	20 years @125°C	Not guaranteed	Intel does not specify a data retention guarantee
Write/Erase Cycles (Endurance)	1 Million	100K	100K	AMD's target for MirrorBit is 1 million cycles
Security Region (OTP Sector)	256Bytes	256Bytes	128 bit	
Current Consumption				
Read Current	9 mA	30 mA	40 mA	Typical values using byte read at 200ns intervals with CMOS inputs.
Erase/Program Current	26 mA	50 mA	35 mA	
Standby Mode Current	0.20 µA	1 µA	50 µA	

Note: *For information on increasing the speed of programming operations using the write buffer functionality, refer to publication number 25539, MirrorBit Flash Memory Write Buffer Programming and Page Buffer Read.*

AMD provides customers with a superior memory solution at each associated density, and pinout compatible migration from lower densities. Density upgrade paths are available in industry-standard TSOP and FBGA packaging. Figure 1 illustrates AMD's migration path in TSOP packages. The added 56-pin TSOP package used for high-density devices (64 Mb and above) will include the same internal footprint as the legacy 48-pin TSOP package. For a detailed view of TSOP and BGA migration paths available for MirrorBit devices, refer to publication number 25694, "MirrorBit Packages."

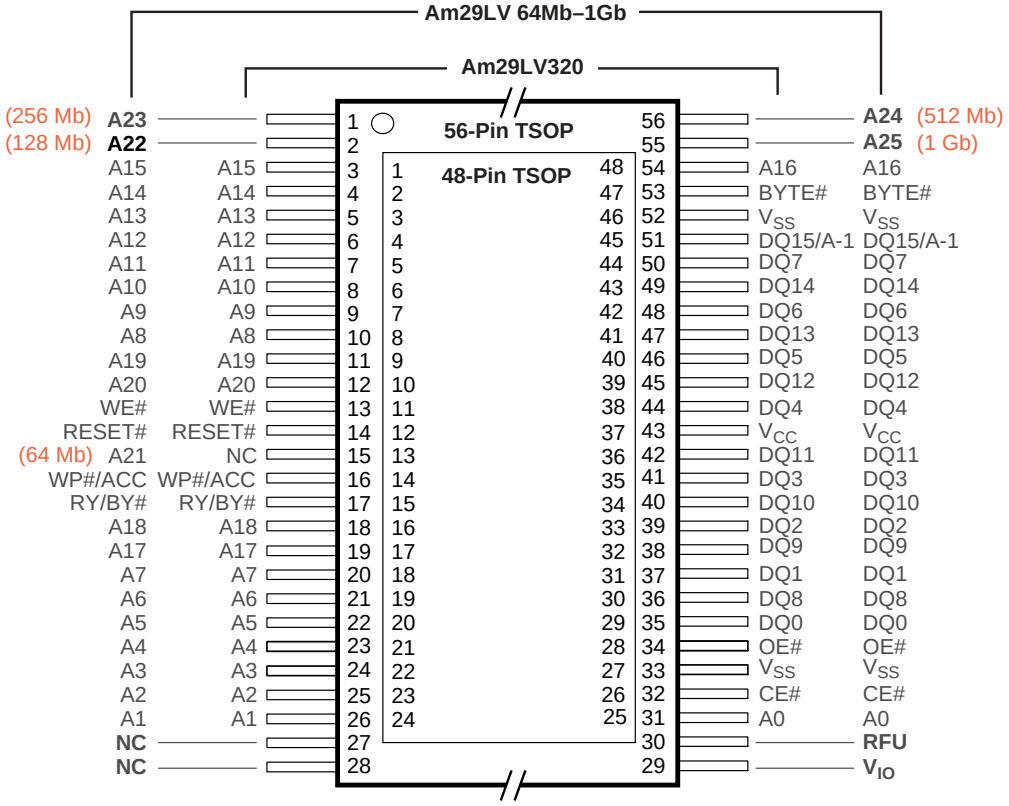


Figure 1. AMD TSOP Pinout Migration for 3V LV Family

Implementing a Multi-Sourced Layout

Customers wanting to take advantage of the benefits and savings associated with AMD's Mirror-Bit technology as well as the security of a second source supplier can implement a multi-sourced board layout. This section describes the changes that may be required to enable an AMD LV, AMD MirrorBit and Intel StrataFlash dual-source layout for 32Mb, 64Mb, and 128Mb designs.

Pinout Differences

The AMD LV-Mirror-Bit family and Intel StrataFlash devices are not pin-compatible or drop-in replacements, however the differences are documented below and in most cases, they can be worked around. In those cases where an easy work-around is not possible, this section helps a design engineer choose a minimal feature-set common to both product families.

Table 2. AMD and Intel Pinout Compatibility

Feature	AMD Pin(s)	Intel Compatible Pin(s)	Design Notes
Chip Enable	CE#	CE0, CE1, CE2	Intel's 3 chip enable pins could potentially replace chip select logic for cascaded memory arrays for up to eight devices. Most designers place such chip select logic in a PLD/ASIC already on board. Connect AMD's CE pin to Intel's CE0 pin and tie CE1 and CE2 to GND.
Status Pin	RY/BY#	STS	In default mode the STS functions like RY/BY. Both are open-drain outputs and should be tied to V_{CC} with a pull-up resistor.
Hardware Write Protection	WP#	V_{PEN}	WP# can be pulled Low to protect first or last two (boot) sectors of memory. StrataFlash does not have WP# functionality but does use V_{PEN} to protect the entire device from alteration.
Program Accelerate Pin	ACC	N/A	Intel chose to remove this functionality on its 3V Strata. AMD uses the WP#/ACC pin as a dual function pin.
Chip Reset	RESET#	RP#	Both pins reset the device and are active low.
I/O Buffer Power	V_{IO}	V_{CCQ}	A separate pin for the I/O buffer voltage supply allowing the device to interface with lower voltage range bus signals. Available on selected AMD memories.
Address Pins	DQ15/A-1, A0-A23, A24-A25	A0, A1-A24	In Byte mode the AMD DQ15/A-1 pin functions as the byte selector where Intel uses A0. Remaining pins are connected in sequence AMD A0-A23 to Intel A1-A24. AMD supports A24-A25 for densities up to 1Gbit
Data Pins	DQ0–DQ15	DQ0–DQ15	Connect data pins together.
Byte Enable	BYTE#	Byte#	BYTE# selects between Byte Mode (x8) and Word mode (X16)

Dual Footprint Layouts

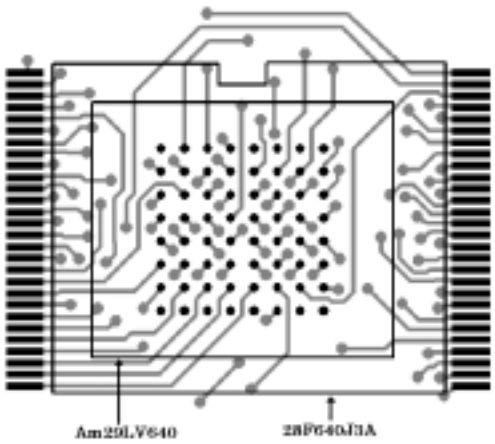
Designing a dual footprint layout is relatively easy with routing software. As an example, three dual footprint designs are included. The layouts show that standard design rules are sufficient: 6/7 mil track and spacing, 10 mil vias (20 mil pad size/10 mil drill size), and 45° routing. The designs are all done with only two routing layers and separate Power and Ground planes. Although these layouts can be used as shown, it is highly recommended that system designers develop their own layouts to optimize routing characteristics for their boards.

These layouts were generated using Innoveta's (PADS) PowerPCB™ design studio. Sample PowerPCB files, Gerber schematics, and bit-map images can be obtained from AMD's website or by contacting your local AMD sales representative.

Layout I

For designs where board space comes at a significant premium, one solution is to place the footprint of an AMD Am29LVxxx Fortified BGA inside the footprint of a 56-pin TSOP StrataFlash. The dual footprint effectively occupies the same space as a 56-pin TSOP footprint. The appropriate pads from each footprint are then connected together to allow either device to be placed on the board.

Top
Routing Layer



Bottom
Routing Layer

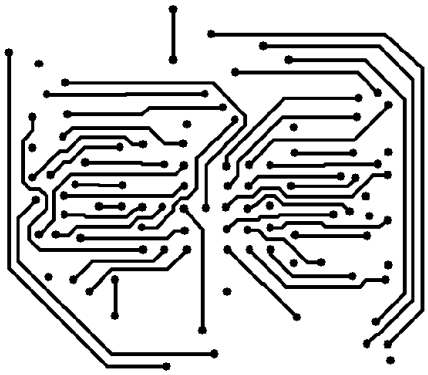


Figure 2. Multi-Sourced Layout for 64-Ball FBGA AMD Am29LV640 and 56TSOP Intel 28F640J3A (Layout I)

Layout II

A much simpler dual footprint can be achieved using two TSOP packages and offsetting the pads for each package. The degree of offset is dependent on the design rules and will define the total amount of board space required for this solution. In this example dual footprint effectively covers 1.5X the same space as a 56-pin TSOP footprint. The tighter the design rules the closer the two devices can be placed together.

Top
Routing Layer

Bottom
Routing Layer

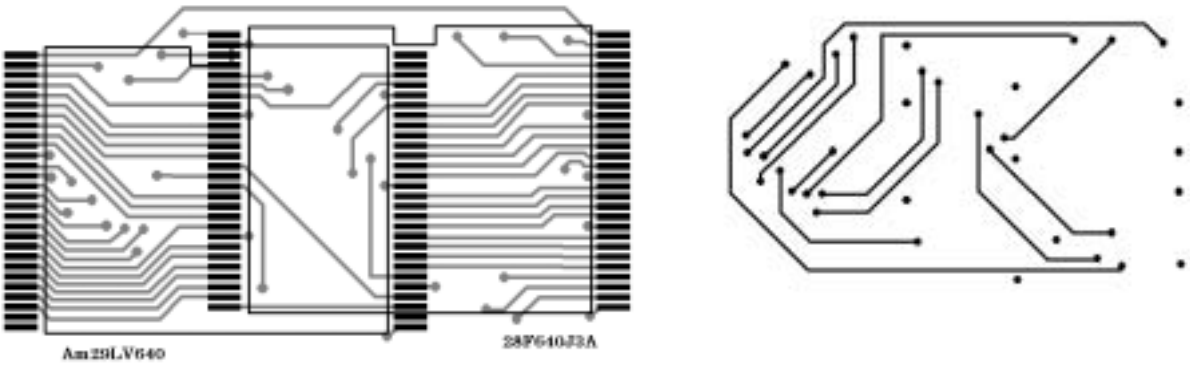


Figure 3. Multi-Sourced Layout for AMD 56-Pin TSOP Am29LV640M and 56-Pin TSOP Intel 28F640J3A (Layout II)

Layout III

For designs where components can be placed on opposite sides of the PCB board, AMD's Reverse TSOP packaging option on some devices allows for an easy dual footprint. In this example the LV640M 56-pin Reverse TSOP is placed on one side of the board and Intel 56TSOP on the other. Because of the incompatible pinouts between the two devices, the devices cannot be placed directly over each other unless the number of routing layers is increased beyond 2 layers.

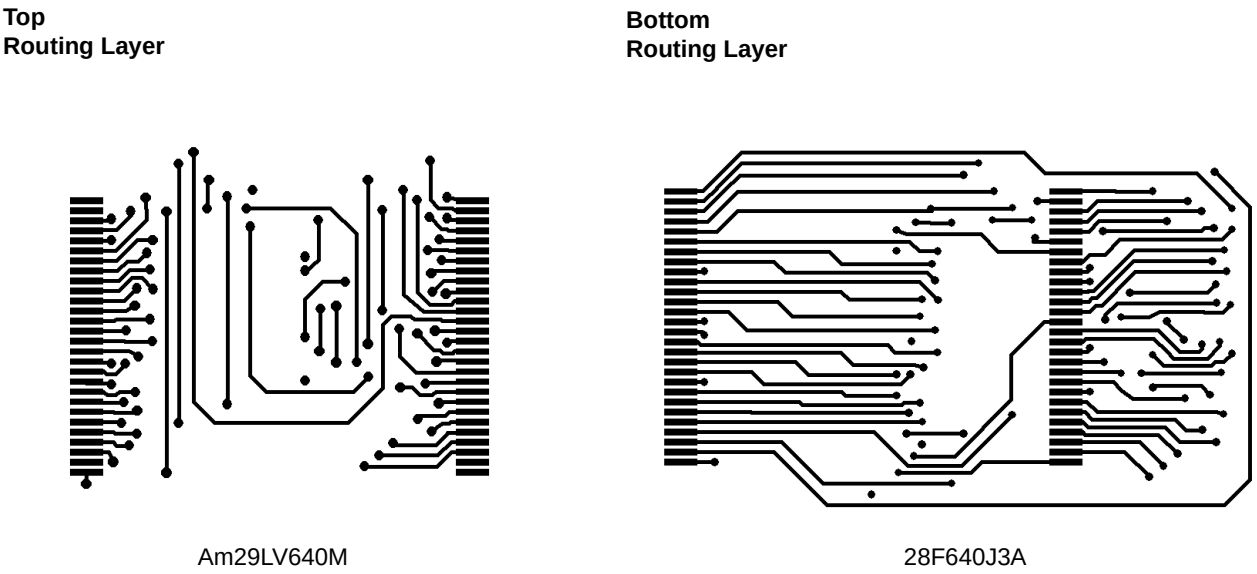


Figure 4. Multi-Sourced Layout for AMD 56-Pin Reverse TSOP Am29LV640M and 56-Pin TSOP Intel 28F640J3A (Layout III)

Command Sets and Software Compatibility

Designing dual footprints to insure hardware compatibility is just one step of implementing a multi-sourced layout. Just as much emphasis needs to be placed on software adaptability. AMD and Intel each use different command sets. AMD uses two to six bus cycle commands to better prevent unintended commands from being executed due to system noise or errant code execution. This method provides an additional level of software write protection. Most Intel commands require only two bus write cycles. Figure 3 lists AMD and Intel's equivalent commands for their "Standard Command Set" in the Address/Data format.

Table 3. AMD and Intel Pinout Compatibility

Command	AMD (Addr/Data)	Intel (Addr/Data)
Read Device ID	5555h/AAh, 2AAAH/55h 5555h/90h	XXXXh/90h
Read (Reset) Mode	XXXXh/F0h	XXXXh/FFh
Sector (Blk) Erase	5555h/AAh, 2AAAh/55h, 5555h/80h, 5555h/AAh, 2AAAh/55h, Blk Addr/30h	Blk Addr/20h, Blk Addr/D0h
Program (Write)	5555h/AAh, 2AAAh/55h, 5555h/A0h, Addr/Data	Addr/40h, Addr/Data
Erase Suspend	XXXXh/B0h	XXXXh/B0h
Erase Resume	XXXXh/30h	XXXXh/D0h

For applications that require only minimal Flash operations such as reading and programming a device and do not require a highly optimized driver, designers can choose to implement a flash driver that queries the flash device identification (ID) and branches to that vendor's associated instruction set. In this case a manufacturer ID can be read from internal registers within the flash device to determine which instruction set to use. A sample algorithm has been included that enables a flash driver to distinguish between AMD and Intel devices and branches to the appropriate algorithms.

Device ID Changes on AMD MirrorBit Devices

AMD's new generation of LV family devices using the breakthrough MirrorBit technology are designed to function as drop-in replacements to the traditional LV devices. The only modification a design engineer must take into account is the new 3-byte Device IDs AMD will implement in this and future generations of flash devices. The 3-byte Device IDs are a change from the traditional single byte IDs used in the past and will require the software to use three read-cycles to gather all the information instead of one (see Figure 5). For a complete up-to-date description of changes to device code structure, refer to publication number 25538: Migrating from Single-byte to Three-byte Device IDs Application Note, and datasheets posted on www.amd.com.

Write Buffer and Page Read Buffer Options

A Write Buffer is implemented in MirrorBit flash memory devices to speed programming operations. The write buffer is a set of registers that can be used to hold several words that are to be programmed as a group. Overall write performance is increased because the overhead operations required to program each byte or word are only performed once for the entire group of words. Similarly, a Page Read Buffer in MirrorBit devices can be used to increase read performance. For more details on using the Write of Read Buffers, refer to publication number 25539: MirrorBit Flash Memory Write Buffer Programming and Page Buffer Read Application Note.

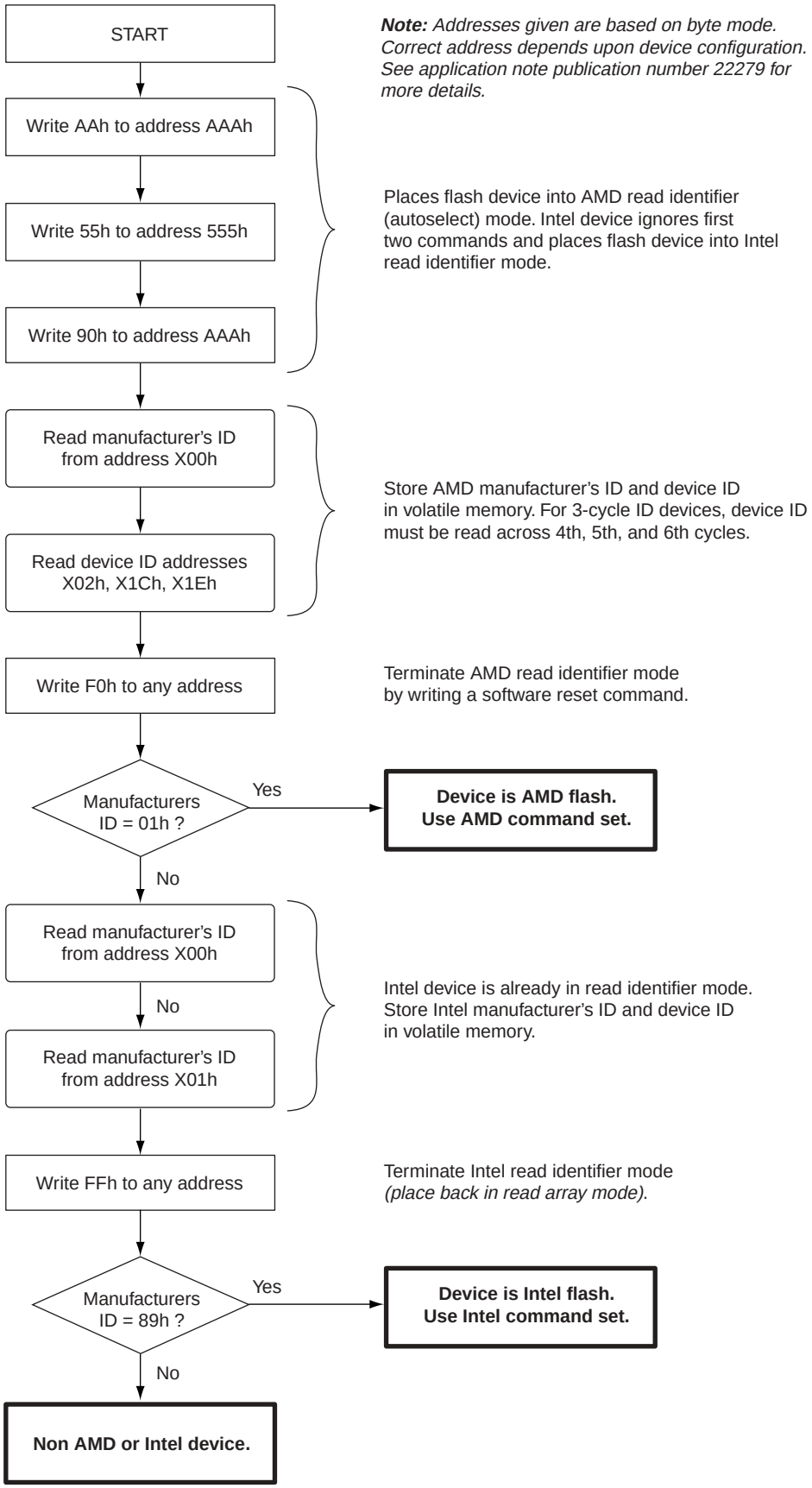


Figure 5. Selecting between AMD and Intel Command Sets

Implementing Flexible Device Drivers with CFI

For applications requiring a more optimized driver that will take advantage of device specific functions such as different sector sizes, sector protection, write buffers, or precise timing characteristics system designers can take advantage of a table that stores this data within each flash device. Command Flash Interface (CFI) is a standardized data structure and command set that was specifically created to allow system designers to query the installed flash device to determine its command sets and configuration data. Flexible drivers can then be written to take advantage of manufacturer-specific command sets or device-specific features.

To use CFI the software must know where to locate vendor-specific information, in what format the data appears, and which parameters are of interest. Figure 6 shows an example of a CFI query algorithm that can be used to gather the required information from both AMD and Intel CFI compliant devices. This algorithm assumes you have used an algorithm similar to Figure 5 to determine the proper Device ID and Manufacturer ID.

The first step is to enter CFI mode by sending command 98h to address 55h. The device must be in read array mode to accept this command. A list of address locations can then be read in any order to access any required information in the CFI Table. The entire table is structured in two main sections. The first holds standard device identifiers and command sets common to all flash devices such as voltage ranges, timing parameters and device geometry. The second section contains vendor-specific commands such as page mode, sector protection schemes, and top/bottom boot flags. For more detailed information on CFI table structure refer to CFI publication 100 found at www.amd.com/ http://www.amd.com/products/nvd/overview/cfi.html.

The algorithm below focuses on the first half of the CFI table by detecting device size, erase sector architecture, and device timeouts. It can easily be extended to query vendor-specific information.

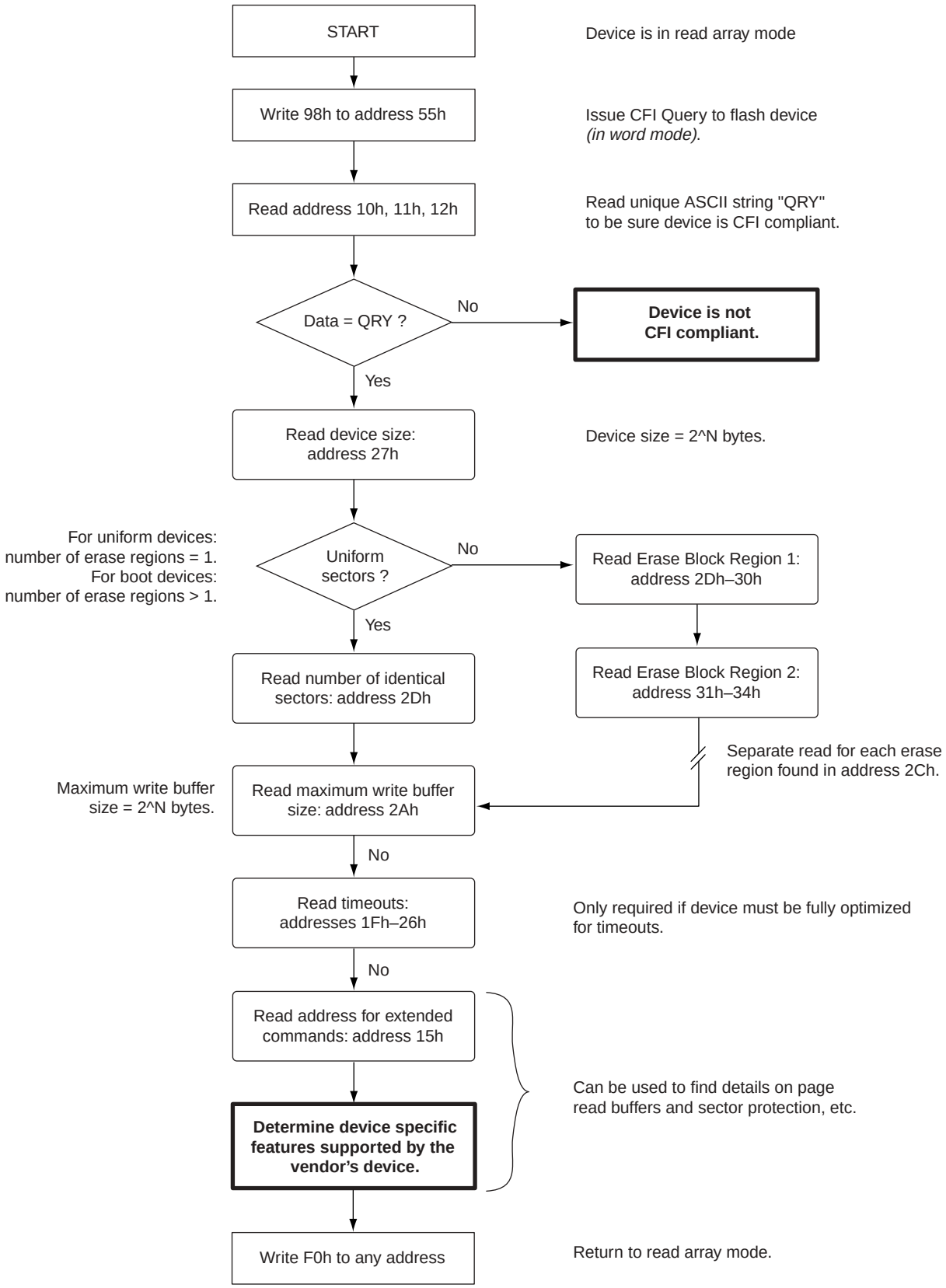


Figure 6. Using CFI to Implement Flexible Drivers

Uniform vs. Boot Sectors

Boot sector devices differ from uniform sector devices because they contain a group of smaller sectors either at the top (top boot device) or bottom (bottom boot device) of the memory map. These smaller sectors are usually used to store boot code or parametric data that can be protected or updated separate from the remaining sectors. The CFI algorithm in Figure 6 can be used to detect whether a device has uniform or boot sectors. AMD's current LV320 is only offered with boot sectors while Intel's StrataFlash devices are only offered with uniform sectors. Additional software would be required to support both architectures in a dual layout.

Software for use with boot sector devices must be able to handle these different sector sizes. Systems that are read-only or use chip-erase to erase the entire device need not worry about sector architecture. For more details on the differences between uniform or boot sectors and the software requirements that need to be considered, refer to AMD application note 22374 (Migrating Between Boot and Uniform Sectored Flash Device).

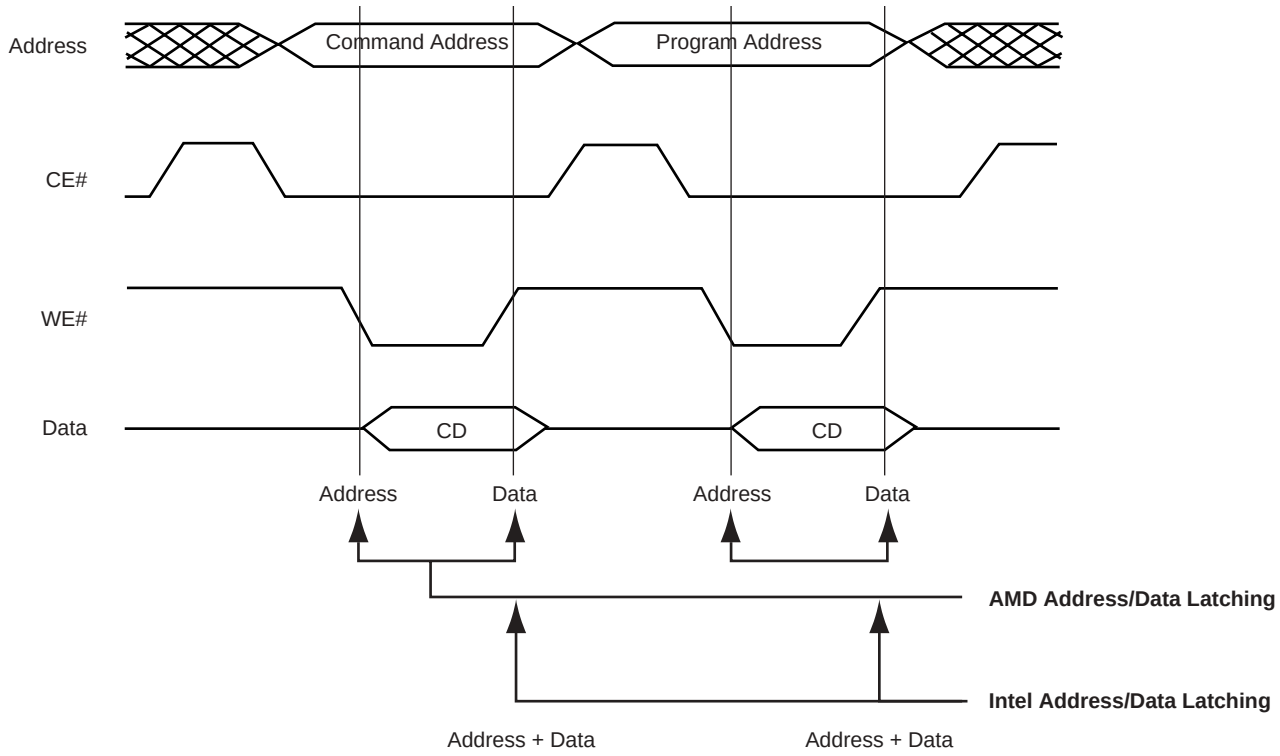
Design Considerations for AC Timing Specs

Systems designers must account for differences in AC Timing specifications for both read and write operations. One way to implement flexibility in the design is to design the software to account for the worst-case scenario using max timings of the slowest device, in which case the tables below provide a clear comparison between vendors. Read timings as shown in Table 5, are much faster for AMD devices. If a designer wants to take full advantage of faster access times for AMD devices, the software driver can be written to fully optimize timing characteristics by using CFI to query device timings to provide data for the appropriate timing variables.

Table 4. AC Characteristics for Read Operations

JEDEC Spec	Description	AMD (ns)		Intel (ns)		
		32Mb, 64Mb	128Mb, 256Mb	32Mb	64Mb	128Mb
T_{AVAV}	Read Cycle Time (min)	90	100	110	120	150
T_{AVQV}	Address to Output Delay	90	100	110	120	150
T_{ELQV}	CE# to Output Delay	90	100	110	120	150
T_{GLQV}	OE# to Output Delay	30		50		
T_{EHQZ}	CE# to Output High Z	16		55		
T_{GHQZ}	OE# to Output High Z	16		15		

For write operations, the AC timings between AMD and Intel devices differ far more because the two companies take a different approach to address and data latching. AMD devices latch the address and data on opposite ends of the write enable pulse (WE#). Intel latches both address and data on the rising edge of the write pulse. This results in some timing specifications being defined differently between the two companies. As a result, it is difficult to simply write a driver that queries CFI and sets the appropriate variables to optimize for program timings. For write operations, the design should allow adequate time for the address and data to be set up and latched on both the rising and falling edges of the write enable pulse (see Figure 7).



Note: *Address must be on the bus long enough to be latched at both ends of WE#.*

Figure 7. AMD and Intel Address/Data Latching Techniques

Table 5. AC Characteristics for Write Operations

AC Write Spec	AMD (ns) 32Mb-128Mb			Intel (ns) 32Mb–128Mb		Notes
Total Write Cycle	T_{WC}	90 (32, 64Mb)	100 (128, 256Mb)	T_{WP} + T_{WPH}	100	Minimum time between WP# assertions
Address Setup	T_{AVWL}	0		T_{AVWH}	55	Setup and hold times differ because of different techniques used by AMD and Intel to latch address data
Address Hold	T_{WLAX}	45		T_{WHAX}	0	
Data Setup	T_{DVWH}	45		T_{DVWH}	50	Data must be setup earlier to accommodate for Intel's longer setup times
Data Hold	T_{WHDX}	0		T_{WHDX}	0	
Write Pulse Width	T_{WLWH}	35		T_{WPH}	70	Write pulse width is directly related to data setup time

Status Notification Schemes

Both AMD and Intel have simplified the work required to design in flash by embedding the algorithms for many common functions of the flash device. This allows the device to act both as a memory device and a peripheral unit to the CPU. As with any peripheral unit, AMD and Intel flash devices also provide a method of monitoring the status of these embedded operations. The actual implementation however, does differ between the two manufacturers.

AMD provides a status register called the Operation Status Bits that are multiplexed with the Data pins after a Program or Erase operation begins. This register can then be accessed by data polling the device using a simple Read cycle. The host system is then free to perform other task and can poll the device periodically to get latest status of the device.

Intel uses a similar status register, however the CPU must issue a separate software command to poll the register and a second command to clear the register.

This method creates added overhead on the host system and renders the device inactive until the Clear Status Register command is given.

AMD and Intel both offer a second method for checking the status of the flash device, by using the Ready/Busy (RY/BY# for AMD devices, STS# for Intel devices) pin. This pin can then be tied directly to an interrupt input of the microprocessor. This way the host system is not required to actively poll the flash device for status information freeing it to perform other tasks. In default mode Intel's STS# functions just like AMD's RY/BY#. Both are open-drain outputs and should be tied to V_{CC} with a pull-up resistor.

Summary

The design techniques described in this application note allows designers to take advantage of AMD's superior LV family and MirrorBit family Flash memory devices while having the security of a second source supplier. Most MirrorBit memories are footprint compatible to AMD's single-bit per cell LV family of flash devices. This allows one memory layout to support superior and cost-competitive Flash solutions for designers requiring densities from 2Megabit to 1Gigabit.

REVISION SUMMARY

Revision A (January 2, 2002)

Initial release.

Revision A+1 (April 12, 2002)

Corrected illustrations in figure 3.

Revision A+2 (October 21, 2002)

Corrected pinout in figure 1.

Revision A + 3 (March 5, 2003)

Updated Table 1.

Updated Figure 1.

Updated Table 4.

Updated Table 5.