Tel: 886-2-66296288
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Low Power High Sensitivity 315/434 MHz OOK/ASK Superheterodyne Receiver **Preliminary** **PT4301**

DESCRIPTION

The PT4301 is a very low power consumption and high sensitivity single chip OOK/ASK superheterodyne receiver for the 315MHz and 434MHz frequency bands which offers a high level of integration and requires only a few external components. The PT4301 consists of a low-noise amplifier (LNA), an image-rejection mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) and loop filter, a 10.7MHz intermediate frequency (IF) limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data recovery circuitry (data filter, peak detector, and data slicer). The PT4301 also implements a discrete one-step automatic gain control (AGC) that reduces the LNA gain by 20dB when the RF input signal is greater than -60dBm. The PT4301 is available in 24-pin SSOP package and is specified over the extended temperature range (-40 to +85^{o}C).

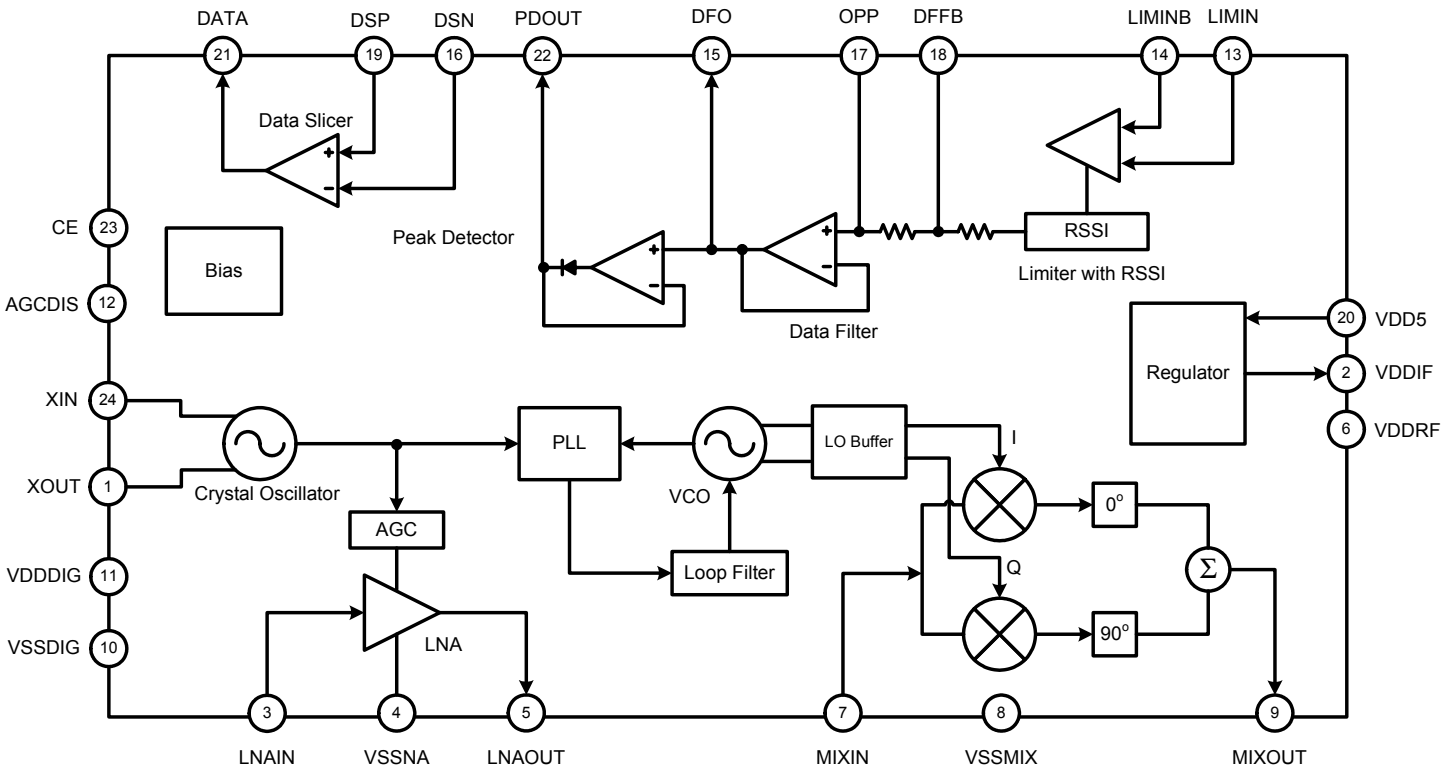
FEATURES

- Low current consumption (5mA fully active mode at 315MHz)
- 2.4 to 5.5V supply voltage operation range
- Optimized for 315 or 434MHz ISM Band
- On-chip image-rejection function
- High dynamic range with on-chip AGC
- Power down mode with very low supply current (<1μA)
- High sensitivity of -114dBm (2Kb/s AM 99% square-wave modulation, 315MHz)
- Low external parts count
- 24-pin SSOP package

APPLICATIONS

- Remote keyless entry (RKE) systems
- Remote control systems including garage door and gate openers
- Alarm and security systems
- Wireless sensors

BLOCK DIAGRAM



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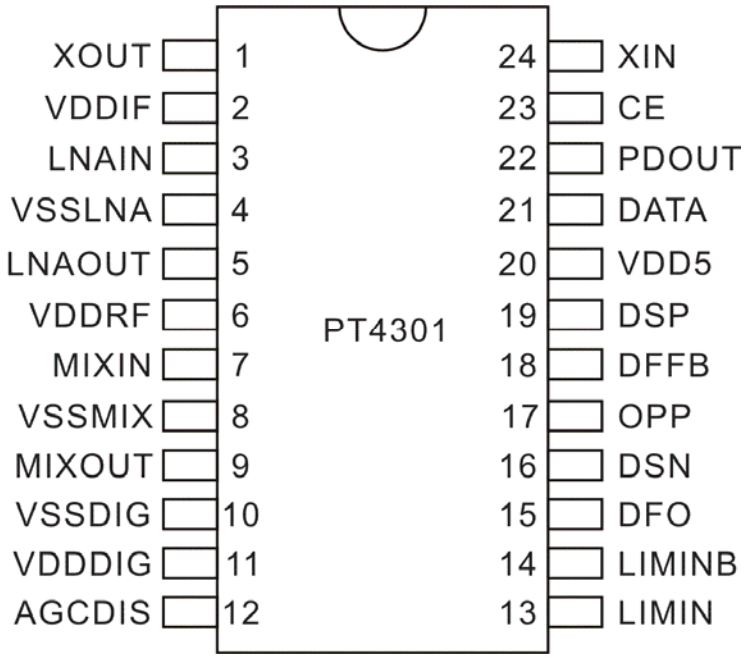
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
XOUT	O	Crystal oscillator output	1
VDDIF	P	Power supply for IF portion	2
LNAIN	I	LNA input	3
VSSLNA	G	Ground for LNA	4
LNAOUT	O	LNA output	5
VDDRF	P	Power supply for RF portion	6
MIXIN	I	Mixer input	7
VSSMIX	G	Ground for image-rejection mixer	8
MIXOUT	O	Mixer output	9
VSSDIG	G	Ground for LO and digital portions	10
VDDDIG	P	Power supply for LO and digital portions	11
AGCDIS	I	AGC control pin Pull high (connect to VDD5) to disable AGC	12
LIMIN	I	Limiting amplifier input	13
LIMINB	I	Limiter amplifier de-coupling input	14
DFO	O	Data filter output	15
DSN	I	Negative data slicer input	16
OPP	I	Non-inverting op-amp input for Sallen-Key data filter	17
DFFB	I/O	Data filter feedback node	18
DSP	I	Positive data slicer input	19
VDD5	P	5V supply voltage	20
DATA	O	Data output	21
PDOUT	O	Peak detector output	22
CE	I	Chip enable pin Pull high (connect to VDD5) to power on the chip	23
XIN	I	Crystal oscillator input	24

ABSOLUTE MAXIMUM RATINGS

V_{SS}=0V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	V_{SS} - 0.3 to V_{SS} + 6.0	V
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STG}	-55 to 125	°C
Soldering temperature	T_{SLD}	225	°C
Soldering time	t_{STG}	10	s

RECOMMENDED OPERATING CONDITIONS

V_{SS}=0V

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage range	V_{DD5}	2.4	5.0	5.5	V
Operating temperature	T_A	-40	27	+85	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, VDD = 5.0V, VSS= 0V, CE = HIGH, Temp = 27°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
General Characteristics						
Frequency range	f_{RF}		250	-	500	MHz
Maximum receiver input level	$P_{RF, MAX}$		-25	-20	-	dBm
Sensitivity[a]	S_{IN}	ASK[b], peak power level@315MHz	-	-114	-112	dBm
		OOK, peak power level@315MHz	-	-108	-106	dBm
		ASK, peak power level@434MHz	-	-112	-110	dBm
		OOK, peak power level@434MHz	-	-106	-104	dBm
Data rate[c]			-	2	50	Kb/s
Image rejection ratio	IMR		25	35	-	dB
LO leakage	L_{LO}	Measured at RF input	-	-	-80	dBm
System start-up time	$T_{start-up}$	RF input power=-60dBm	-	-	10	mS
Power Supply						
Supply voltage	V_{DD}	Connect the supply voltage to VDD5 pin only	2.4	5.0	5.5	V
Consumption DC current	I_{DD}	CE=HIGH @315MHz	-	5.0	5.5	mA
		CE=HIGH @434MHz	-	5.3	5.9	mA
Standby DC current	$I_{stand-by}$	CE=LOW	-	-	1.0	μA
LNA						
Power gain	G_{LNA}	Matched to 50Ω@315MHz	13	16	20	dB
		Matched to 50Ω@434MHz	12	15	18	dB
Noise figure	NF_{LNA}	Matched to 50Ω		3	3.6	dB
Input third-order intermodulation intercept point	$IIP3_{LNA}$	Matched to 50Ω	-20		-	dBm
Auto Gain Control (AGC)[d]						
AGC hysteresis	H_{AGC}		-	6	-	dB
LNA voltage gain reduction	G_{Red}		-	20	30	dB
AGC delay time	DY_{AGC}	$T_{REF}=1/f_{REF}$	-	$2^{20}xT_{REF}$	-	s
Down-conversion Mixer						
Conversion voltage gain	G_{MIX}	@315MHz	15	18	22	dB
		@434MHz	12	15	18	dB
Input third-order intermodulation intercept point	$IIP3_{MIX}$		-18	-	-	dBm
Output impedance	$Z_{OUT,MIX}$		-	330	-	Ω

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
PLL						
Reference frequency	f_{REF}		6	-	16	MHz
VCO frequency range	f_{VCO}		220	-	550	MHz
Limiter Amplifier and RSSI						
IF frequency	f_{IF}		-	10.7	-	MHz
Input impedance	$Z_{IN,LIM}$		-	330	-	Ω
RSSI dynamic range	DR_{RSSI}		-	80	-	dB
RSSI gain	SL_{RSSI}		-	13	-	mV/dB

Notes:
a. BER=1e-3, data rate=2Kb/s
b. AM 99% square-wave modulation
c. The selection of data rate depends upon the component values use for the data filter, peak detector, and slicer.
d. AGC hysteresis and LNA gain reduction depend upon the gain setting and matching circuits of the LNA. The AGC delay time depends upon the PLL reference frequency.
e. The bandwidth of the data filter is determined by the external components.

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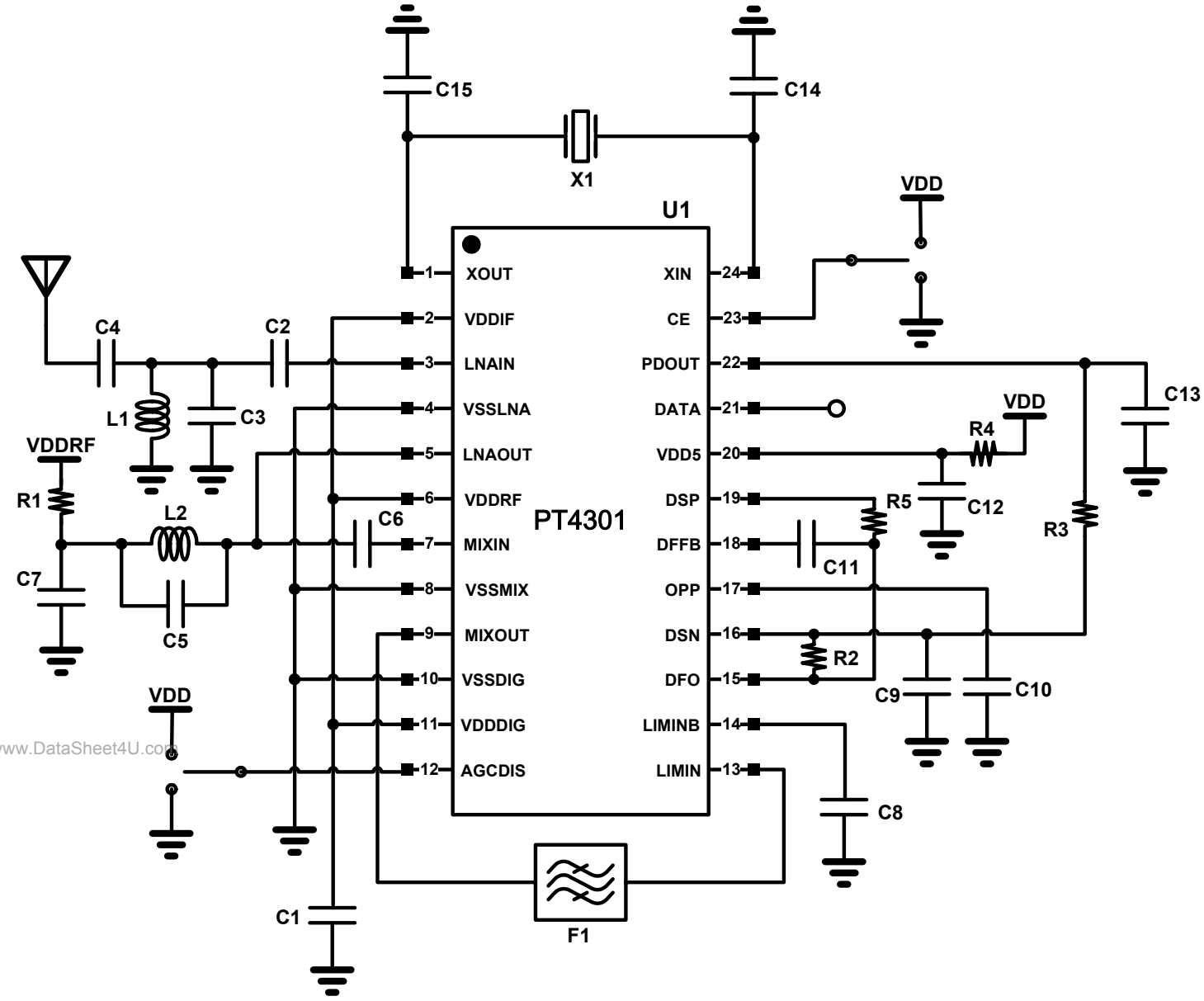
APPLICATION CIRCUIT



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BILL OF MATERIALS

Component	Value		Unit
	315MHz	433.92MHz	
R1, R4	10	10	Ω
R2	5.6K	5.6K	Ω
R3	15K	15K	Ω
R5	220K	220K	Ω
L1	68n	39n	H
L2	47n	22n	H
C1[a]	100n	100n	F
C2	10p	10p	F
C3	-	-	F
C4	1.5p	1.2p	F
C5	-	-	F
C6	100p	100p	F
C7, C12	100n	100n	F
C8	1.5n	1.5n	F
C9	1μ	1 μ	F
C10	220p	220p	F
C11	1.2n	1.2n	F
C13	1μ	1μ	F
C14, C15	39p	39p	F
F1[b]	10.7M	10.7M	Hz
X1	9.509M	13.226M	Hz
U1	PT4301 IC		-

Notes:
a. C1 could be separated into three de-coupling capacitors and connect them against the three VDD pins as close as possible.
b. F1 is the 10.7MHz ceramic filter. The recommended part number is Murata SFELA10M7HA00-B0.

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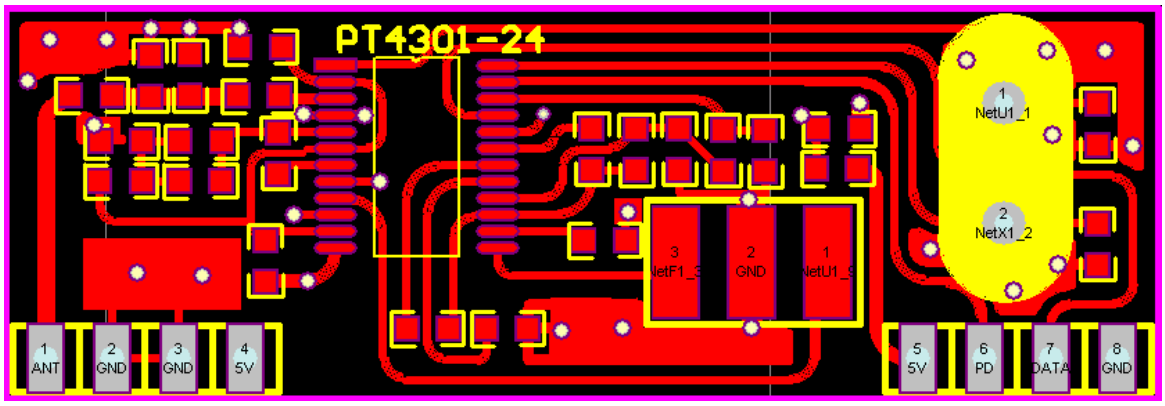
TEST BOARD LAYOUT



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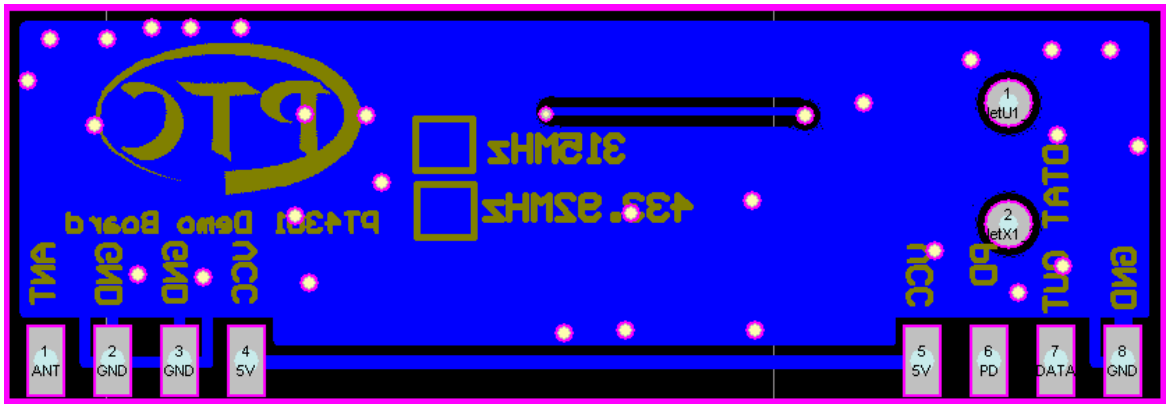

<Bottom Side>

Example of test board layout

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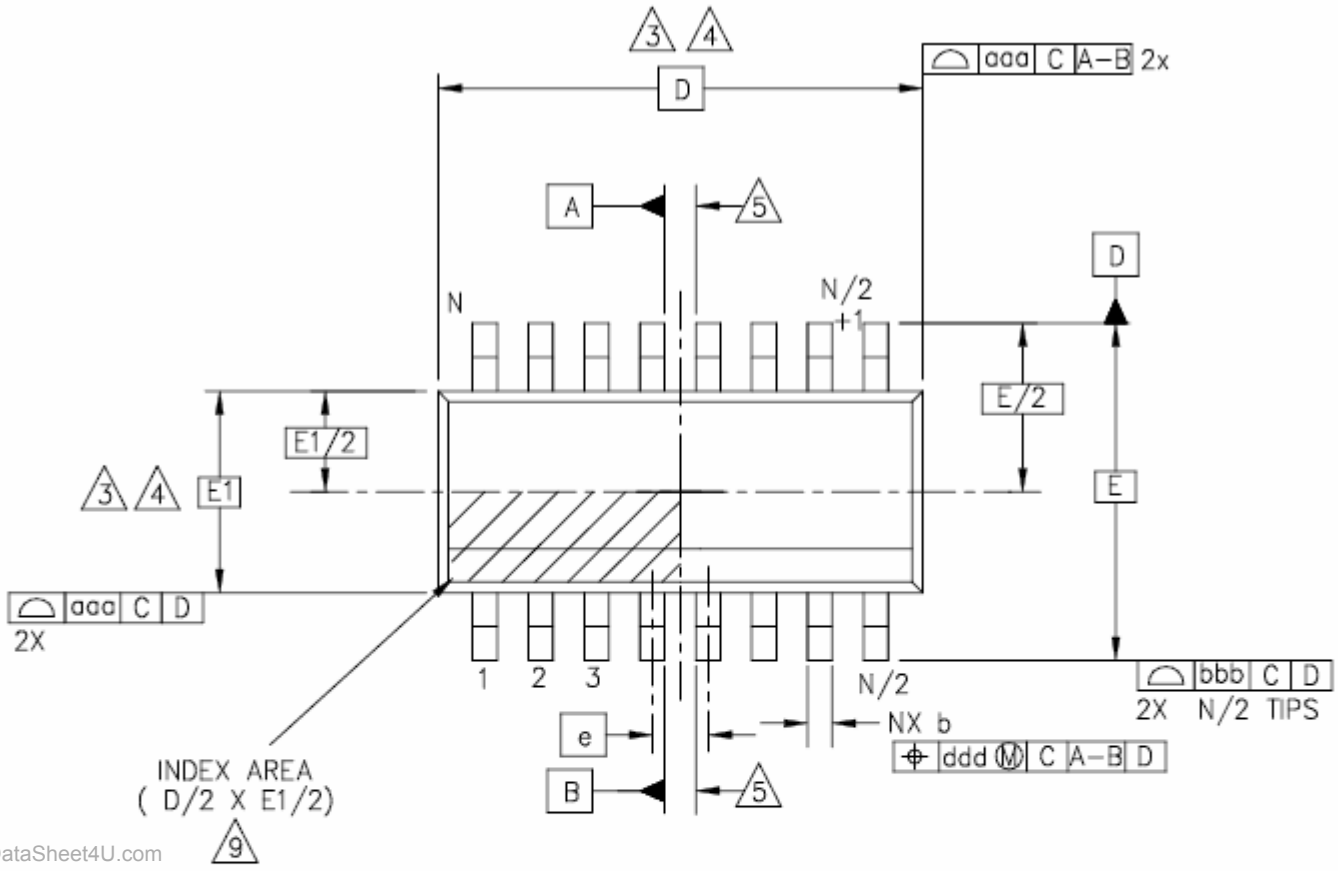
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4301-X (L)	24 Pins, SSOP, 150 mil	PT4301-X

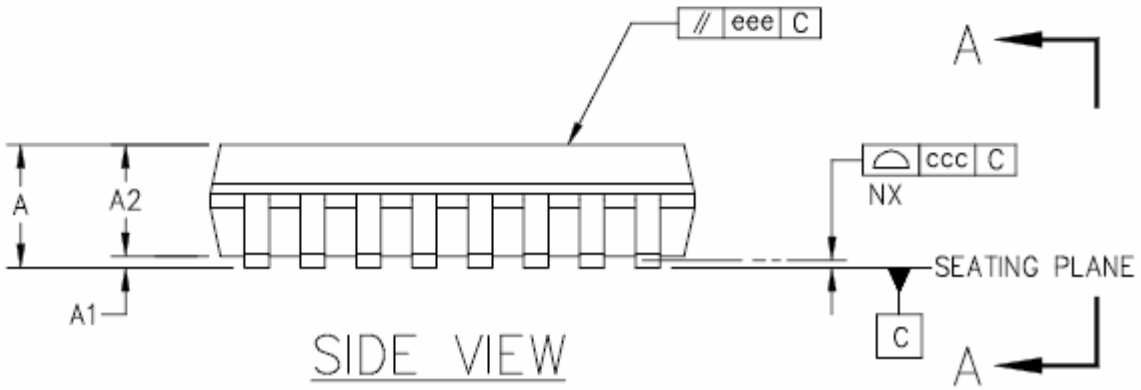
Notes:
1. (L) means Lead Free.
2. The Lead Free mark is placed in-front of the date code.

PACKAGE INFORMATION

24 PINS, SSOP, 150MIL



TOP VIEW



SIDE VIEW

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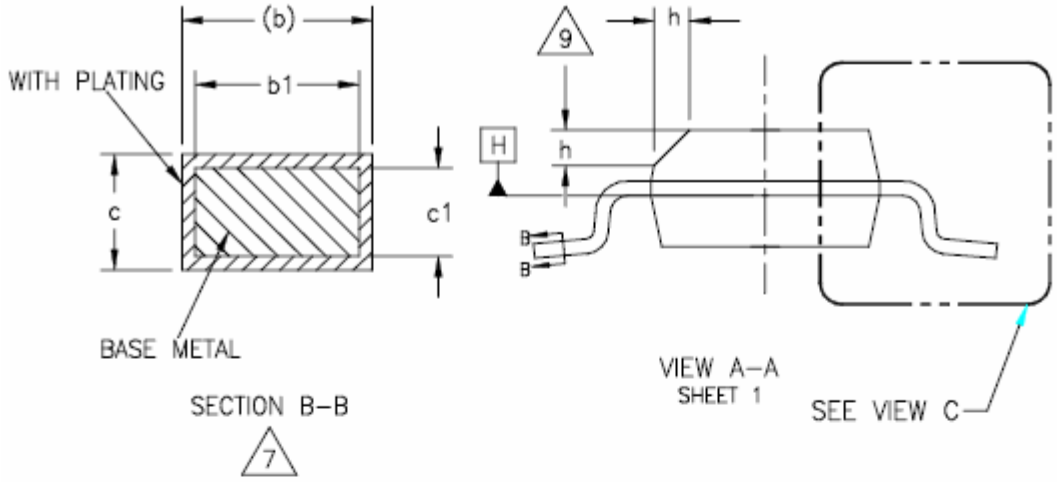
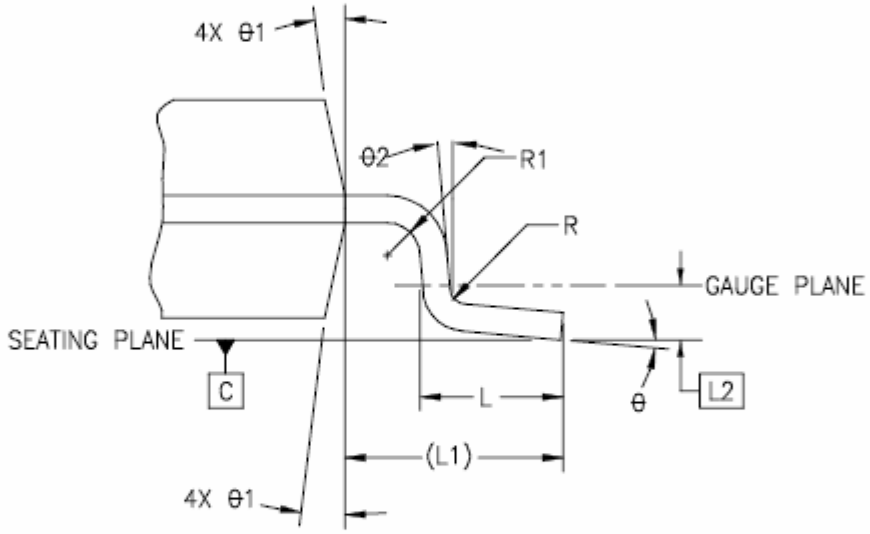
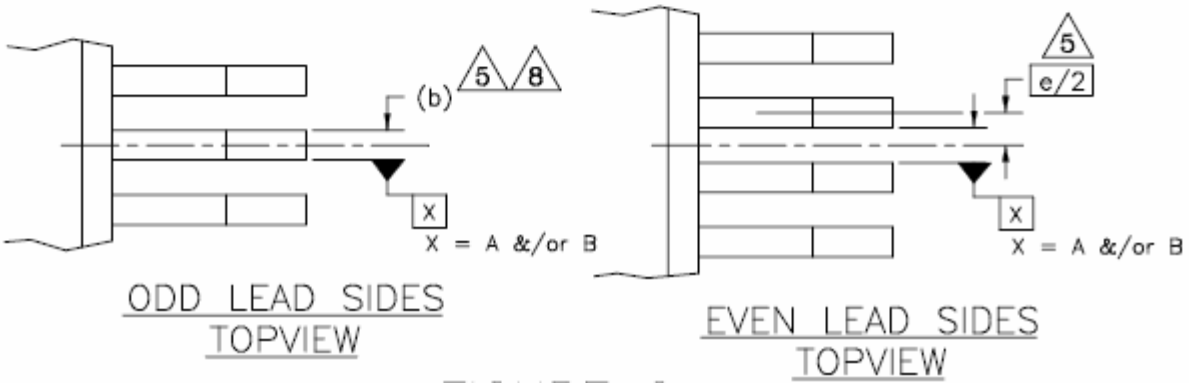




VIEW C



Symbol	Min.	Nom.	Max.
A	0.053	-	0.069
A1	0.004	-	0.010
A2	0.049	-	0.065
b	0.008	-	0.012
b1	0.008	0.010	0.011
c	0.006	-	0.010
c1	0.006	0.008	0.009
D	0.341 BSC		
E	0.236 BSC		
E1	0.154 BSC		
e	0.025 BSC		
L	0.016	-	0.050
L1	0.041 REF		
L2	0.010 BSC		
R	0.003	-	-
R1	0.003	-	-
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-
aaa	0.004		
bbb	0.008		
ccc	0.004		
ddd	0.007		
eee	0.004		

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimensions in inches (angles in degrees)
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006” per end. Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed “0.006” per side. D1 and E1 dimensions are determined at dutum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic.
5. Datums A and B to be determined at datum H.
6. N is the maximum number of terminal position. (N=24)
7. The dimensions apply to the flat section of the lead between 0.004 to 0.010 inches from the lead tip.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.004” total in excess of b dimension at maximum material condition. The dambar can not be located on the lower radius of the foot.
9. Refer to JEDEC MO-137 Variation BC.
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