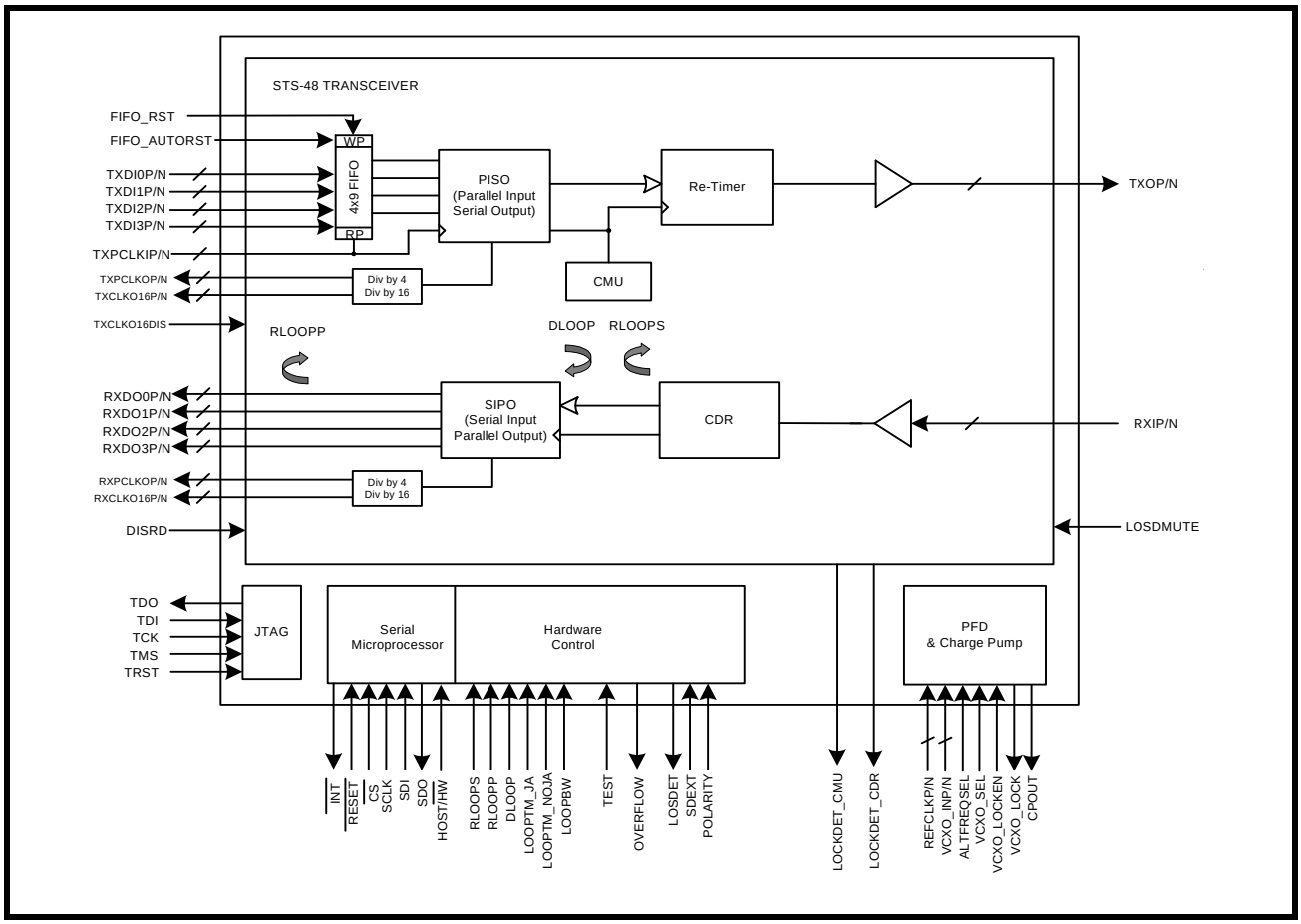
GENERAL DESCRIPTION

The XRT91L80 is a fully integrated SONET/SDH transceiver for SONET OC-48/STM-16 applications supporting the use of Forward Error Correction (FEC) capability. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from a slower external clock reference. It also provides Clock and Data Recovery (CDR) functions by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The chip provides serial-to-parallel and parallel-to-serial converters and 4-bit LVDS system interfaces in both receive and transmit directions. The transmit section includes a 4x9 Elastic Buffer (FIFO) to absorb any phase differences between the transmitter clock input and the internally generated transmitter reference clock. In the event of an overflow, an internal FIFO control circuit outputs an OVERFLOW indication. The FIFO under the control of the FIFO_AUTORST pin can automatically recover from an overflow condition. The operation of the device can be monitored by checking the status of the LOCKDET_CMU, LOCKDET_CDR, and LOSDET output signals. An on-chip phase/frequency detector and charge-pump offers the ability to form a de-jittering PLL with an external VCXO that can be used in loop timing mode to clean up the recovered clock in the receive section.

APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches and Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

FIGURE 1. BLOCK DIAGRAM OF XRT91L80



FEATURES

- 2.488 / 2.666 Gbps Transceiver
- Targeted for SONET OC-48/SDH STM-16 Applications
- Selectable full duplex operation between standard rate of 2.488 Gbps or Forward Error Correction rate of 2.666 Gbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, and clock data recovery (CDR) functions
- 4-bit LVDS signaling data paths running at 622.08/666.51 Mbps compliant with OIF SFI-4 Implimentation Agreement
- Non-FEC and FEC rate REFCLKP/N single reference input port
- Supports 77.76/83.31 MHz or 155.52/166.63 MHz transmit and receive external reference input port
- Optional VCXO input port support multiple de-jittering modes
- On-chip phase detector and charge pump for external VCXO based de-jittering PLL
- Internal FIFO decouples transmit parallel clock input and transmit parallel clock output
- Provides Local, Remote Serial, Remote Parallel and Split Loopback modes as well as Loop Timing mode
- Diagnostics features include various lock detect functions and transmit CMU and receive CDR Lock Detect
- Host mode serial microprocessor interface simplifies monitor and control
- Meets Telcordia, ANSI and ITU-T jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, GR-253 CORE, GR-253 ILR SONET Jitter specifications.
- Operates at 1.8V CMOS and CML with 3.3V I/O
- 490mW Typical Power Dissipation
- Package: 12 x 12 mm 196-pin STBGA
- IEEE 1149.1 Compatable JTAG port

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT91L80IB	196 STBGA	-40℃ to +85℃

FIGURE 2. 196 BGA PINOUT OF THE XRT91L80 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AGND_RX	TRST	LOSDMUTE	NC	DGND	RXCLKO16P	RXCLKO16N	VDD3.3	SDI	$\overline{CS}$	RLOOPP	DGND	VDD1.8	RXDO3P
B	AGND_RX	AGND_RX	DGND	NC	SDEXT	DLOOP	VDD1.8	DGND	SCLK	RESET	TDO	DGND	VDD1.8	RXDO3N
C	RXIP	AGND_RX	AGND_RX	POLARITY	LOSDET	LOOPTM_JA	LOCKDET_CDR	SDO	HOST/$\overline{HW}$	RLOOPS	$\overline{INT}$	DISRD	RXDO2P	RXDO1P
D	RXIN	AGND_RX	AVDD3.3_RX	AVDD1.8_RX	AVDD1.8_RX	AVDD1.8_RX	AGND_RX	AVDD1.8_RX	VDD3.3	VDD3.3	VDD3.3	VDD1.8	RXDO2N	RXDO1N
E	AGND_RX	AGND_RX	AVDD3.3_RX	AGND_RX	TGND	TGND	TGND	TGND	TGND	TGND	VDD3.3	VDD1.8	RXDO0P	RXPCLKOP
F	XRES1N	AGND_RX	AVDD1.8_RX	AGND_RX	TGND	TGND	TGND	TGND	TGND	TGND	DGND	DGND	RXDO0N	RXPCLKON
G	XRES1P	AGND_RX	AVDD1.8_RX	AGND_RX	TGND	TGND	TGND	TGND	TGND	TGND	DGND	DGND	DGND	DGND
H	AGND_RX	AGND_RX	AGND_RX	AGND_RX	TGND	TGND	TGND	TGND	TGND	TGND	DGND	DGND	TXDI0P	TXPCLKIP
J	AVDD1.8_TX	AGND_TX	AGND_TX	AVDD1.8_TX	TGND	TGND	TGND	TGND	TGND	TGND	DGND	DGND	TXDI0N	TXPCLKIN
K	TXOP	AGND_TX	AGND_TX	AGND_TX	TGND	TGND	TGND	TGND	TGND	TGND	VDD1.8	DGND	TXDI2P	TXDI1P
L	TXON	AGND_TX	DGND	AGND_TX	AGND_TX	AVDD1.8_TX	AVDD1.8_TX	AVDD1.8_TX	VDD1.8	VDD1.8	DGND	DGND	TXDI2N	TXDI1N
M	AGND_TX	AVDD1.8_TX	AVDD1.8_TX	AGND_TX	AGND_TX	VCXO_SEL	LOOPBW	TDI	VDD1.8	VDD1.8	VDD1.8	TXCLKO16DIS	OVERFLOW	TXDI3P
N	TMS	LOCKDET_CMU	TCK	VCXO_INN	AGND_TX	REFCLKN	AGND_TX	VCXO_LOCK	AVDD1.8_TX	TXCLKO16P	TXCLKO16N	FIFO_AUTORST	FIFO_RST	TXDI3N
P	ALTFREQSEL	LOOPTM_NOJA	VCXO_LOCKEN	VCXO_INP	AVDD3.3_TX	REFCLKP	AGND_TX	CPOUT	AVDD3.3_TX	TXPCLKOP	TXPCLKON	DGND	VDD3.3	VDD3.3

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PIN DESCRIPTIONS

SERIAL MICROPROCESSOR INTERFACE

NAME	LEVEL	TYPE	PIN	DESCRIPTION
HOST/$\overline{HW}$	LVTTL, LVCMOS	I	C9	**Host or Hardware Mode Select Input** The XRT91L80 offers two modes of operation for interfacing to the device. The Host mode uses a serial microprocessor interface for programming individual registers. The Hardware mode is controlled by the state of the hardware pins set by the user. When left unconnected, by default, the device is configured in the Hardware mode. "Low" = Hardware Mode "High" = Host Mode This pin is provided with an internal pull-down.
$\overline{CS}$	LVTTL, LVCMOS	I	A10	**Chip Select Input (Host Mode Only)** Active "Low" signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial microprocessor is disabled when the chip select signal returns "High". ***NOTE:*** *The serial microprocessor interface does **not** support burst mode. Chip Select must be de-asserted after each operation cycle.* This pin is provided with an internal pull-up.
SCLK	LVTTL, LVCMOS	I	B9	**Serial Clock Input (Host Mode Only)** Once $\overline{CS}$ is pulled "Low", the serial microprocessor interface requires 16 clock cycles for a complete Read or Write operation. This pin is provided with an internal pull-down.
SDI	LVTTL, LVCMOS	I	A9	**Serial Data Input (Host Mode Only)** When $\overline{CS}$ is pulled "Low", the serial data input is sampled on the rising edge of SCLK. This pin is provided with an internal pull-down.
SDO	LVCMOS	O	C8	**Serial Data Output (Host Mode Only)** If a Read function is initiated, the serial data output is updated on the falling edge of SCLK8 through SCLK15, with the LSB (D0) updated first. This enables the data to be sampled on the rising edge of SCLK9 through SCLK16.
$\overline{INT}$	LVCMOS	O	C11	**Interrupt Output (Host Mode Only)** Active "Low" signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". ***NOTE:*** *This pin requires an external pull-up resistor.*
$\overline{RESET}$	LVTTL, LVCMOS	I	B10	**Master Reset Input** Active "Low" signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. This pin is provided with an internal pull-up.

HARDWARE COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RLOOPS	LVTTL, LVCMOS	I	C10	**Serial Remote Loopback** The serial remote loopback mode interconnects the receive serial data input to the transmit serial data output. If serial remote loopback is enabled, the 4-bit parallel transmit data input is ignored while the 4-bit parallel receive data output is maintained. "Low" = Disabled "High" = Serial Remote Loopback Mode Enabled ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.* This pin is provided with an internal pull-down.
RLOOPP	LVTTL, LVCMOS	I	A11	**Parallel Remote Loopback** The parallel remote loopback mode allows the serial data input stream to pass through the clock and data recovery circuit and looped-back at the parallel interface to the serial output port. The 4-bit parallel transmit data input is ignored while the 4-bit parallel receive data output is maintained. "Low" = Disabled "High" = Parallel Remote Loopback Mode Enabled ***NOTE:*** *DLOOP and RLOOPS should be **disabled** when RLOOPP is enabled. The internal FIFO should also be flushed using FIFO_RST pin or register bit when parallel remote loopback is enabled/disabled.* This pin is provided with an internal pull-down.
DLOOP	LVTTL, LVCMOS	I	B6	**Digital Local Loopback** The digital local loopback mode interconnects the 4-bit parallel transmit data and parallel transmit clock input to the 4-bit parallel receive data and parallel receive clock output respectively while maintaining the transmit serial data output. If digital local loopback is enabled, the receive serial data input is ignored. "Low" = Disabled "High" = Digital Local Loopback Mode Enabled ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.* This pin is provided with an internal pull-down.

HARDWARE COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
LOOPTM_JA	LVTTL, LVCMOS	I	C6	**Loop Timing Mode With Jitter Attenuation** The LOOPTM_JA pin must be set "High" in order to select the recovered receive clock as the reference source for the de-jitter PLL. "Low" = Disabled "High" = Loop timing with de-jitter PLL Activated This pin is provided with an internal pull-down.
LOOPTM_NOJA	LVTTL, LVCMOS	I	P2	**Loop Timing Mode With No Jitter Attenuation** When the loop timing mode is activated, the external local reference clock input to the CMU is replaced with the 1/16th or 1/32nd of the high-speed recovered receive clock coming from the CDR. "Low" = Disabled "High" = Loop timing Activated This pin is provided with an internal pull-down.

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXDI0P TXDI0N TXDI1P TXDI1N TXDI2P TXDI2N TXDI3P TXDI3N	LVDS	I	H13 J13 K14 L14 K13 L13 M14 N14	**Transmit Parallel Data Input** The 622.08 Mbps 4-bit parallel transmit data input should be applied to the transmit parallel bus simultaneously to be sampled at the rising edge of the TXPCLKIP/N input. The 4-bit parallel interface is multiplexed into the transmit serial output interface MSB first (TXDI3P/N). ***NOTE:*** *The XRT91L80 can accept 666.51 Mbps 4-bit parallel transmit data input for Forward Error Correction (FEC) Applications.*
TXPCLKIP TXPCLKIN	LVDS	I	H14 J14	**Transmit Parallel Clock Input** 622.08 MHz clock input used to sample the 4-bit parallel transmit data input TXDI[3:0]P/N. ***NOTE:*** *The XRT91L80 can accept a 666.51 MHz transmit clock input for Forward Error Correction (FEC) Applications.*
TXOP TXON	CMLDIFF	O	K1 L1	**Transmit Serial Data Output** The transmit serial data output stream is generated by multiplexing the 4-bit parallel transmit data input into a 2.488 Gbps serial data output stream. In Forward Error Correction, the transmit serial data output stream is 2.666 Gbps.
REFCLKP REFCLKN	LVPECL	I	P6 N6	**Reference Clock Input** This differential clock input reference is used for the transmit clock multiplier unit (CMU) to provide the necessary high-speed clock reference for this device. Pin ALTFREQSEL determines the value used as the reference. See Pin ALTFREQSEL for more details.
VCXO_INP VCXO_INN	LVPECL	I	P4 N4	**Voltage Controled Oscillator Input** This differential clock input is used for the transmit PLL jitter attenuation. Pin ALTFREQSEL determines the value used as the reference. See Pin ALTFREQSEL for more details.

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
ALTFREQSEL	LVTTL, LVCMOS	I	P1	**Reference Clock Frequency Select** This pin is used to select the frequency of the REFCLKP/N clock input to the CMU. "Low" = 77.76 MHz (83.31 MHz for FEC) "High" = 155.52 MHz (166.63 MHz for FEC) This pin is provided with an internal pull-up.
VCXO_SEL	LVTTL, LVCMOS	I	M6	**De-Jitter VCXO Select Option** This pin selects either the normal REFCLKP/N or the de-jitter VCXO_INP/N pin as a reference clock to the CMU. "Low" = Normal REFCLKP/N reference clock "High" = De-Jitter VCXO_INP/N reference clock This pin is provided with an internal pull-down.
VCXO_LOCK	LVCMOS	O	N8	**De-Jitter PLL Lock Detect** If the de-jitter PLL lock detect is enabled with pin P3 and the de-jitter VCXO mode is selected by pin M6, this pin will assert "High" when the PLL is locked. "Low" = VCXO Out of Lock "High" = VCXO Locked
VCXO_LOCKEN	LVTTL, LVCMOS	I	P3	**De-Jitter PLL Lock Detect Enable** This pin enables the VCXO_INP/N lock detect circuit and VCXO_LOCK pin N8 to be active. "Low" = VCXO Lock Detect Disabled "High" = VCXO Lock Detect Enabled This pin is provided with an internal pull-down.
CPOUT	-	O	P8	**Charge Pump Output (for external VCXO)** The nominal output of the charge pump current is 250µA
LOOPBW	LVTTL, LVCMOS	I	M7	**CMU Loop Bandwidth Select** This pin is used to select the bandwidth of the clock multiplier unit of the transmit path to a narrow or wide band. Use Wide Band for clean reference signals and Narrow Band for noisy references. "Low" = Wide Band (4x) "High" = Narrow Band (1x) This pin is provided with an internal pull-down.
TXPCLKOP TXPCLKON	LVDS	O	P10 P11	**Transmit Parallel Clock Output** This 622.08 MHz clock can be used for the downstream device to generate the TXDI[3:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48/STM-16 transceiver to be in synchronization. ***NOTE:*** *The XRT91L80 can output a 666.51 MHz transmit clock output for Forward Error Correction (FEC).*

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXCLKO16P TXCLKO16N	LVDS	O	N10 N11	**Auxiliary Clock Output (155.52/166.63 MHz)** 155.52/166.63 MHz auxiliary clock derived from CMU output. This clock can also be used for the downstream device as a reference for generating the TXDI[3:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48/STM-16 transceiver to be in synchronization. The output of this pin is controlled by TXCLKO16DIS.
TXCLKO16DIS	LVTTL, LVCMOS	I	M12	**Auxiliary Clock Disable** This pin is used to control the activity of the auxiliary clock. "Low" = TXCLKO16P/N Enabled "High" = TXCLKO16P/N Disabled This pin is provided with an internal pull-down.
LOCKDET_CMU	LVCMOS	O	N2	**CMU Lock Detect** This pin is used to monitor the lock condition of the clock multiplier unit. "Low" = CMU Out of Lock "High" = CMU Locked
OVERFLOW	LVCMOS	O	M13	**Transmit FIFO Overflow** This pin is used to monitor the transmit FIFO status. "Low" = Normal Status "High" = Overflow Condition
FIFO_RST	LVTTL, LVCMOS	I	N13	**FIFO Control Reset** FIFO_RST should be held "High" for a minimum of 2 TXPCLKOP/N cycles after powering up and during manual FIFO reset. After the FIFO_RST pin is returned "Low," it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Upon an interrupt indication that the FIFO has an overflow condition, this pin is used to reset or flush out the FIFO. "Low" = Normal Operation "High" = Manual FIFO Reset ***NOTE:*** *To automatically reset the FIFO, see FIFO_AUTORST pin.* This pin is provided with an internal pull-down.
FIFO_AUTORST	LVTTL, LVCMOS	I	N12	**Automatic FIFO Overflow Reset** If this pin is set "High", the STS-48/STM-16 transceiver will automatically flush the FIFO upon an overflow condition. Upon power-up, the FIFO should be manually reset by setting FIFO_RST "High" for a minimum of 2 TXPCLKOP/N cycles. "Low" = Manual FIFO reset required for Overflow Conditions "High" = Automatically resets FIFO upon Overflow Detection This pin is provided with an internal pull-down.

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXDO0P RXDO0N RXDO1P RXDO1N RXDO2P RXDO2N RXDO3P RXDO3N	LVDS	O	E13 F13 C14 D14 C13 D13 A14 B14	**Receive Parallel Data Output** 622Mbps 4-bit parallel receive data output is updated simultaneously on the rising edge of the RXPCLKOP/N output. The 4-bit parallel interface is de-multiplexed from the receive serial data input MSB first (RXDO3P/N). ***NOTE:*** *The XRT91L80 can output 666.51 Mbps 4-bit parallel receive data output for Forward Error Correction (FEC) Applications.*
RXPCLKOP RXPCLKON	LVDS	O	E14 F14	**Receive Parallel Clock Output** 622.08 MHz parallel clock output used to update the 4-bit parallel receive data output RXDO[3:0]P/N at the rising edge of this clock.. ***NOTE:*** *The XRT91L80 can output a 666.51 MHz receive clock output for Forward Error Correction (FEC).*
DISRD	LVTTL LVCMOS	I	C12	**Parallel Receive Data Output Disable** This pin is used to disable the RXDO[3:0]P/N parallel receive data output bus asynchronously. "Low" = Normal Mode "High" = Forces RXDO[3:0]P/N to a logic state "0" This pin is provided with an internal pull-down.
RXIP RXIN	CMLDIFF	I	C1 D1	**Receive Serial Data Input** The receive serial data stream of 2.488 Gbps is applied to these input pins. In Forward Error Correction, the receive serial data stream is 2.666 Gbps.
XRES1P XRES1N	-	I	G1 F1	**External LVDS Biasing Resistors** A 402Ω resistor with +/-1% tolerance should be placed across these 2 pins for proper biasing.
RXCLKO16P RXCLKO16N	LVDS	O	A6 A7	**Auxiliary Clock Output (155.52/166.63 MHz)** 155.52/166.63 MHz auxiliary clock derived from divide-by-16 CDR recovered clock.
LOCKDET_CDR	LVCMOS	O	C7	**CDR Lock Detect** This pin is used to monitor the lock condition of the clock and data recovery unit. "Low" = CDR Out of Lock "High" = CDR Locked
SDEXT	LVTTL, LVCMOS	I	B5	**Signal Detect Input from Optical Module** **Hardware Mode** When inactive, it will immediately declare a Loss of Signal Detect (LOSD) condition and assert LOSDET output pin and control the activity of the RXDO[3:0]P/N parallel data output based on LOSDMUTE pin setting. **Host Mode** In addition to asserting LOSDET output pin, it will update the LOSD condition on the registers and control the activity of the RXDO[3:0]P/N parallel data output based on LOSDMUTE register bit setting. "Active" = Normal Operation "Inactive" = LOSD Condition (SDEXT detects signal absence) This pin is provided with an internal pull-down.

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
POLARITY	LVTTL, LVCMOS	I	C4	**Polarity for SDEXT Input** Controls the Signal Detect polarity convention of SDEXT. "Low" = SDEXT is active "Low." "High" = SDEXT is active "High." This pin is provided with an internal pull-down.
LOSDET	LVCMOS	O	C5	**LOS Detect Condition** Flags LOSD condition based on SDEXT signal coming from the optical module. "Low" = No Alarm "High" = A LOS condition is present
LOSDMUTE	LVTTL, LVCMOS	I	A3	**Parallel Receive Data Output Mute Upon LOSD** If this pin is asserted "High", the receive data output will automatically be forced to a logic state of "0" when an LOSD condition occurs. "Low" = Disabled "High" = Mute RXDO[3:0]P/N Data Upon LOSD Condition This pin is provided with an internal pull-down.

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
VDD3.3	PWR	A8, D9, D10, D11, E11, P13, P14	**CMOS Digital 3.3V I/O Power Supply** VDD3.3 should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDD3.3 power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_RX	PWR	D3, E3	**Analog 3.3V I/O Receiver Power Supply** AVDD3.3_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_RX power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_TX	PWR	P5, P9	**Analog 3.3V I/O Transmitter Power Supply** AVDD3.3_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_TX power supply pins should have bypass capacitors to the nearest ground.
VDD1.8	PWR	A13, B7, B13, D12, E12, K11, L9, L10, M9, M10, M11	**CMOS Digital 1.8V Core Power Supply** VDD1.8 should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDD1.8 power supply pins should have bypass capacitors to the nearest ground.
AVDD1.8_RX	PWR	D4, D5, D6, D8, F3, G3	**Analog 1.8V Core Receiver Power Supply** AVDD1.8_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD1.8_RX power supply pins should have bypass capacitors to the nearest ground.

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
AVDD1.8_TX	PWR	J1, J4, L6, L7, L8, M3, N9, M2	**Analog 1.8V Core Transmitter Power Supply** AVDD1.8_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD1.8_TX power supply pins should have bypass capacitors to the nearest ground.
DGND	GND	A5, A12, B3, B8, B12, F11, F12, G11, G12, G13, G14, H11, H12, J11, J12, K12, L3, L11, L12, P12	**Digital Ground for 3.3V I/O and 1.8V Core Digital Power Supplies** It is recommended that all ground pins of this device be tied together.
AGND_RX	GND	A1, B1, B2, C2, C3, D2, D7, E1, E2, E4, F2, F4, G2, G4, H1, H2, H3, H4	**Receiver Analog Ground for 3.3V I/O and 1.8V Core Analog Power Supplies** It is recommended that all ground pins of this device be tied together.
AGND_TX	GND	J2, J3, K2, K3, K4, L2, L4, L5, M1, M4, M5, N5, N7, P7	**Transmitter Analog Ground for 3.3V I/O and 1.8V Core Analog Power Supplies** It is recommended that all ground pins of this device be tied together.
TGND	GND	E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10	**Thermal Ground** It is recommended that all ground pins of this device be tied together.

NO CONNECTS

NAME	LEVEL	TYPE	PIN	DESCRIPTION
NC		NC	A4 B4	**No Connect** This pin can be left floating or tied to ground.

JTAG

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCK	N3	I	**Test clock:** Boundary Scan Clock Input.
TMS	N1	I	**Test Mode Select:** Boundary Scan Mode Select Input. JTAG is disabled by default. ***Note**: This input pin should be pulled "Low" for JTAG operation* This pin is provided with an internal pull-up.
TDI	M8	I	**Test Data In:** Boundary Scan Test Data Input This pin is provided with an internal pull-up.
TDO	B11	O	**Test Data Out:** Boundary Scan Test Data Output
TRST	A2	I	**JTAG Test Reset Input** ***Note**: This input pin should be pulled "Low" to reset JTAG* This pin is provided with an internal pull-up.

1.0 FUNCTIONAL DESCRIPTION

The XRT91L80 transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The transceiver converts 4-bit parallel data at 622.08/666.51 Mbps to a serial CML bit stream at 2.488/2.666 Gbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), and receive clock and data recovery (CDR) unit. The transceiver is divided into transmit and receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

1.1 Hardware Mode vs. Host Mode

Functionality of the STS-48/STM-16 transceiver can be configured by using either Host mode or Hardware mode. If Hardware mode is selected by pulling HOST/$\overline{HW}$ "Low" or leaving this pin unconnected, the functionality is controlled by the hardware pins described in the Hardware Pin Descriptions. However, if Host mode is selected by pulling HOST/$\overline{HW}$ "High", the functionality is controlled by programming internal R/W registers using the Serial Microprocessor interface. Whether using Host or Hardware mode, the functionality remains the same. Therefore, the following sections describe the functionality rather than how each function is controlled. The Hardware Pin Descriptions and the Register Bit Descriptions concentrate on configuring the device.

1.2 Clock Input Reference

The XRT91L80 can accept either a 77.76/83.3 MHz or 155.52/166.63 MHz clock input at REFCLKP/N as its internal timing reference for generating higher speed clocks. The reference clock can be provided with one of two frequencies chosen by ALTFREQSEL. The reference frequency options for the XRT91L80 are listed in Table 1.

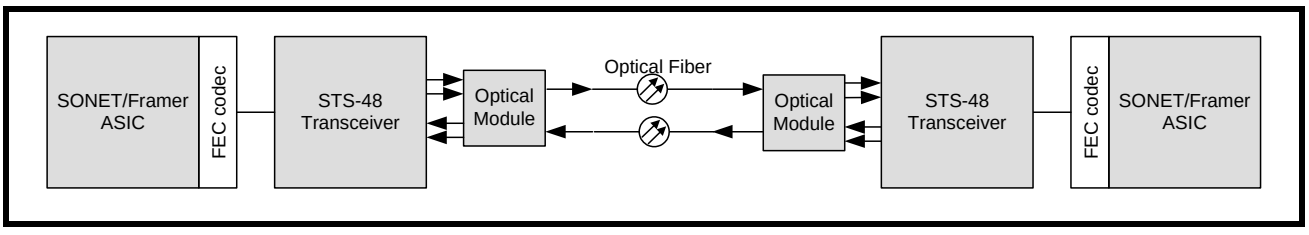
TABLE 1: REFERENCE FREQUENCY OPTIONS (NON-FEC AND FEC MODE)

ALTFREQSEL	REFERENCE CLOCK FREQUENCY	TRANSMIT/RECEIVE DATA RATE	OPERATING MODE
0	77.76/83.3 MHz	2.488/2.666 Gbps	STS-48/STM-16
1	155.52/166.63 MHz	2.488/2.666 Gbps	STS-48/STM-16

1.3 Forward Error Correction (FEC)

Forward Error Correction is used to control errors along a one-way path of communication. FEC sends extra information along with data which can be used by a receiver to check and correct the data without requesting re-transmission of the original information. It does so by introducing a known structure into a data sequence prior to transmission. The most common methods are to replace a 14-bit data packet with a 15-bit codeword structure, or to replace a 17-bit data packet with an 18-bit codeword structure. To maintain original bandwidth, a higher speed clock reference, derived by the ratio of 15/14 or 18/17 referenced to 77.76MHz or 155.52MHz is applied to the STS-48/STM-16 transceiver using an external crystal. The XRT91L80 supports FEC by accepting a clock input reference frequency of 83.31 MHz or 166.63 MHz. This allows the transmit 4-bit parallel data input to be applied to the STS-48/STM-16 transceiver at 666.51 Mbps which is converted to a 2.666 Gbps serial output stream to an optical module. A simplified block diagram of FEC is shown in Figure 3.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF FORWARD ERROR CORRECTION



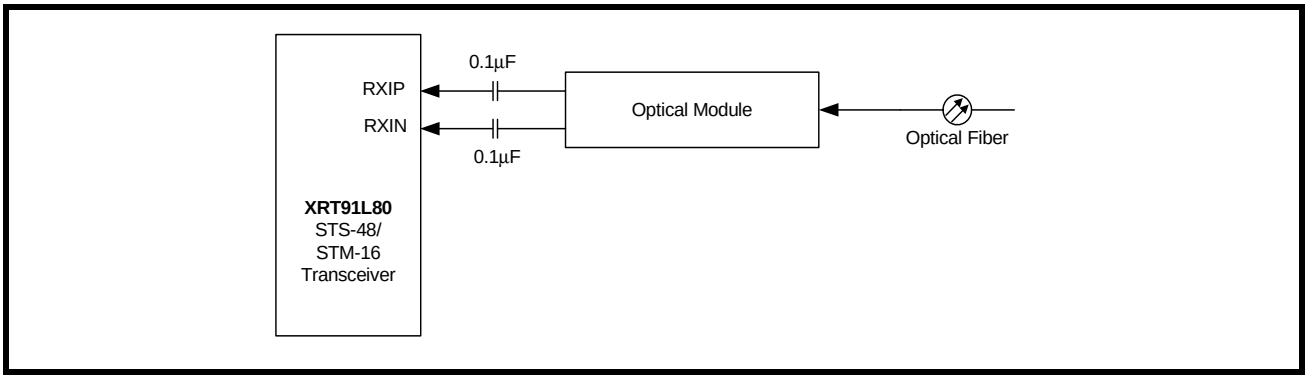
2.0 RECEIVE SECTION

The receive section of XRT91L80 includes the differential inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter (SIPO). The receiver accepts the high speed Non-Return to Zero (NRZ) serial data at 2.488/2.666 Gbps through the differential input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into 4-bit-wide 622.08/666.51 Mbps parallel data and presented to the RXD[3:0]P/N LVDS parallel interface. A divide-by-4 version of the high-speed recovered clock, RXPCLKOP/N, is used to synchronize the transfer of the 4-bit RXDO[3:0]P/N data with the receive portion of the upstream device. Upon initialization or loss of signal or loss of lock the 77.76/155.52 MHz (83.31/166.63 MHz) external local reference clock is used to start-up the clock recovery phase-locked loop for proper operation. A special loop-back feature can be configured when parallel remote loopback (RLOOPP) is used in conjunction with de-jittered loop-time mode that allows the re-transmitted data to comply with ITU and Bellcore jitter generation specifications.

2.1 Receive Serial Input

The receive serial CML inputs are applied to RXIP/N. The receive serial inputs can be AC or DC coupled to an optical module or an electrical interface. A simplified AC coupled block diagram is shown in Figure 4.

FIGURE 4. RECEIVE SERIAL INPUT INTERFACE BLOCK



NOTE: *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

The 2.488/2.666 Gbps high-speed differential CML RXIP/N input swing characteristics is shown in Table 2.

TABLE 2: DIFFERENTIAL CML INPUT SWING PARAMETERS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
ΔV_{INDIFF}	Differential Input Voltage Swing	200		1000	mV
ΔV_{INSE}	Single-Ended Input Voltage Swing	100		600	mV
ΔV_{INBIAS}	Input Bias Range (AC Coupled)	1.0		1.4	V
R_{DIFF}	Differential Input Resistance	75		125	Ω

2.2 Receive Clock and Data Recovery

The clock and data recovery unit accepts the high speed NRZ serial data from the differential CML receiver and generates a clock that is the same frequency as the incoming data. The clock recovery utilizes the REFCLKP/N to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the local reference clock within ±500 ppm. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock. When this condition occurs the PLL will declare Loss of Lock and the LOCKDET_CDR signal will be pulled "Low." Whenever a Loss of Lock/Loss of Signal Detection (LOSD) event occurs, the CDR will continue to supply a receive clock (based on the local reference clock) to the upstream framer device. A Loss of Lock condition will also be declared when the external SDEXT becomes inactive. When the SDEXT is de-asserted by the optical module and LOSDMUTE is enabled, receive parallel data output will be forced to a logic zero state for the entire duration that a LOSD condition is detected. This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. When SDEXT becomes active and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source, the clock recovery PLL will switch and lock back onto the incoming receive data stream and the lock detect output (LOCKDET_CDR) will go active. Table 3 specifies the Clock and Data Recovery Unit performance characteristics.

TABLE 3: CLOCK AND DATA RECOVERY UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	45		55	%
REF_{TOL}	Reference clock frequency tolerance[1]	-20		+20	ppm
$OCLK_{JIT}$	Clock output jitter generation with 77.76 MHz reference clock		3.5	5.0	mUI_{rms}
$OCLK_{JIT}$	Clock output jitter generation with 155.52 MHz reference clock		3.7	5.0	mUI_{rms}
TOL_{JIT}	Input jitter tolerance with 1 MHz < f < 20 MHz PRBS pattern	0.4	0.7		UI
$OCLK_{FREQ}$	Frequency output	2.488		2.667	GHz
$OCLK_{DUTY}$	Clock output duty cycle	45		55	%

Jitter specification is defined using a 12kHz to 20MHz appropriate SONET/SDH filter.

[1]Required to meet SONET output frequency stability requirements.

2.3 External Signal Detection

XRT91L80 supports external Signal Detection (SDEXT). The external Signal Detect function is supported by the SDEXT input. This input is coming from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices, the polarity of this signal can be either active "Low" or active "High." The SDEXT and POLARITY inputs are Exclusive OR’ed to generate the external LOSDET signal, internal Loss of Signal Detect (LOSD) declaration and Mute upon LOSD control signal. Whenever an external SD is absent, the XRT91L80 will automatically output a high level signal on the LOSDET output pin as well as update the control registers whenever the host mode serial microprocessor interface feature is active. If LOSDMUTE is enabled, it will force the receive parallel data output to a logic state "0" for the entire duration that a LOSD condition is declared. This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. Table 4 specifies SDEXT declaration polarity settings.

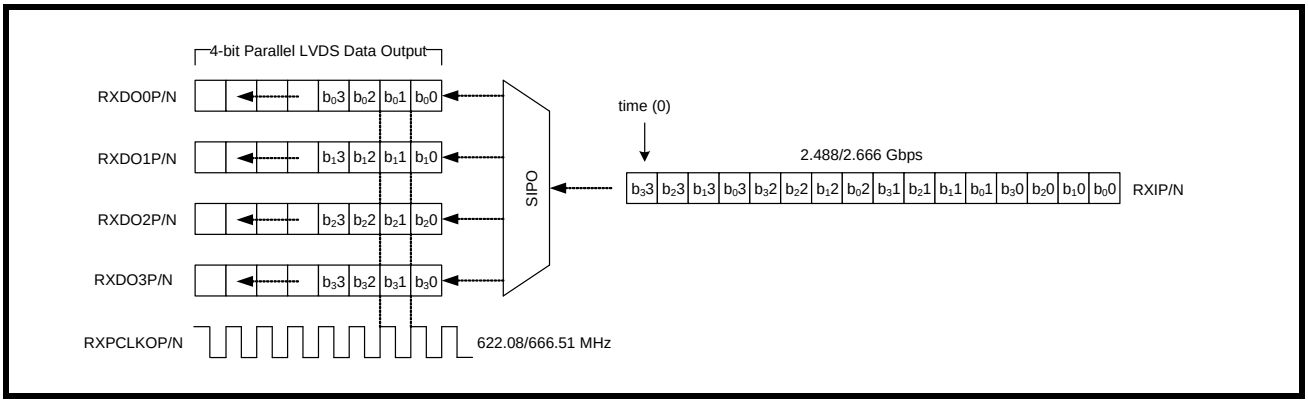
TABLE 4: LOSD DECLARATION POLARITY SETTING

SDEXT	POLARITY	LOSDMUTE	INTERNAL SIGNAL DETECT	LOSDET OUTPUT	RXDO[3:0]P/N	CDR PLL REFERENCE LOCK
0	**0**	**1**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module.	Low	Normal Operation	Hi-Spd Received Data
0	**1**	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module.	High **LOSD declared**	Muted	Local Reference Clock
1	**0**	**1**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module.	High **LOSD declared**	Muted	Local Reference Clock
1	**1**	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module.	Low	Normal Operation	Hi-Spd Received Data

2.4 Receive Serial Input to Parallel Output (SIPO)

The SIPO is used to convert the 2.488/2.666 Gbps serial data input to 622.08/666.51 Mbps parallel data output which can interface to a SONET Framer/ASIC. The SIPO bit de-interleaves the serial data input into a 4-bit parallel output to RXDO[3:0]P/N. A simplified block diagram is shown in Figure 5.

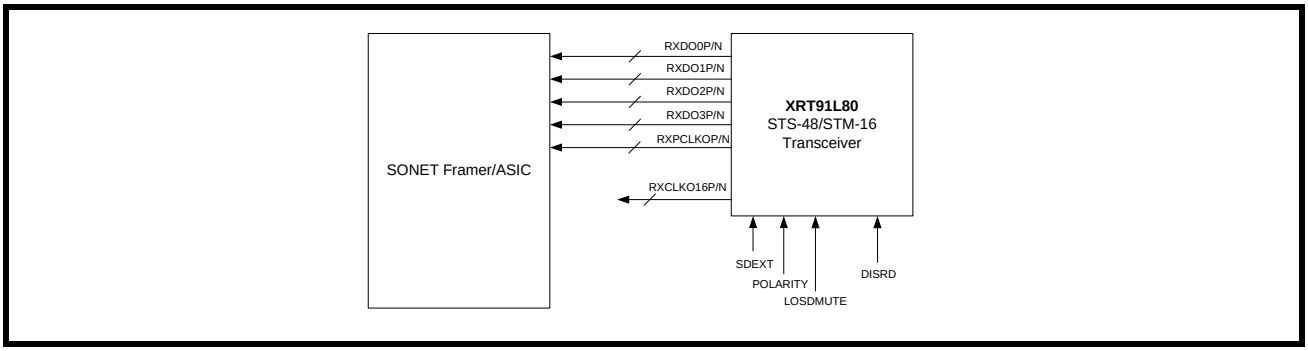
FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF SIPO



2.5 Receive Parallel Output Interface

The 4-bit LVDS 622.08/666.51 Mbps parallel data output of the receive path is used to interface to a SONET Framer/ASIC synchronized to the recovered clock. A simplified block diagram is shown in Figure 6.

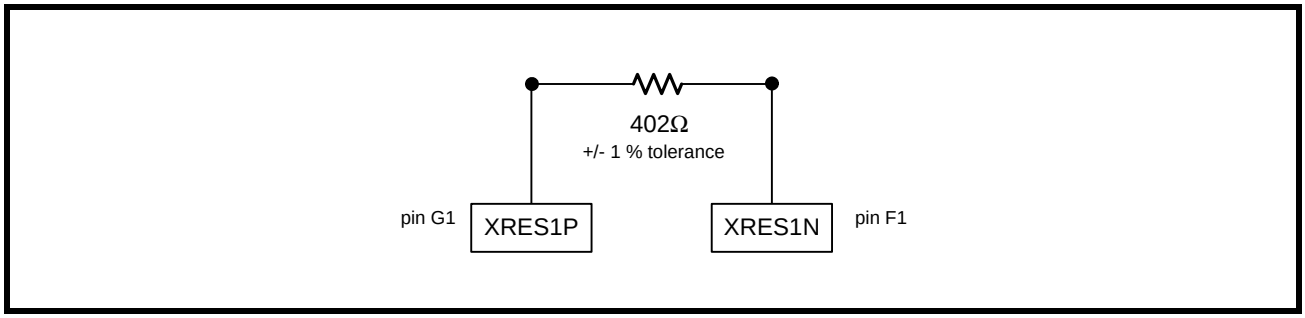
FIGURE 6. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK



2.6 Receive Parallel Interface LVDS Operation

When operating the 4-bit Differential bus in LVDS mode, a 402Ω external resistor is needed across XRES1P and XRES1N to properly bias the RXDO[3:0]P/N and RXPCLKOP/N pins. Figure 7 shows the proper biasing resistor installed.

FIGURE 7. LVDS EXTERNAL BIASING RESISTORS



2.7 Parallel Receive Data Output Mute Upon LOSD

The parallel receiver data outputs can be automatically forced "Low" during an LOSD condition to prevent data chattering. However, the user must select the proper SDEXT polarity for the optical module used. By asserting LOSDMUTE "High", the parallel receiver data outputs will be forced "Low" any time an LOSD condition occurs.

2.8 Parallel Receive Data Output Disable

Unlike LOSDMUTE, DISRD is used to asynchronously force the parallel receiver data outputs to zero, regardless of the data input stream. By asserting DISRD "High", the parallel receiver data outputs will immediately mute.

2.9 Receive Parallel Data Output Timing

The receive parallel data output from the STS-48/STM-16 receiver will adhere to the setup and hold times shown in Figure 8 and Table 5.

FIGURE 8. RECEIVE PARALLEL OUTPUT TIMING

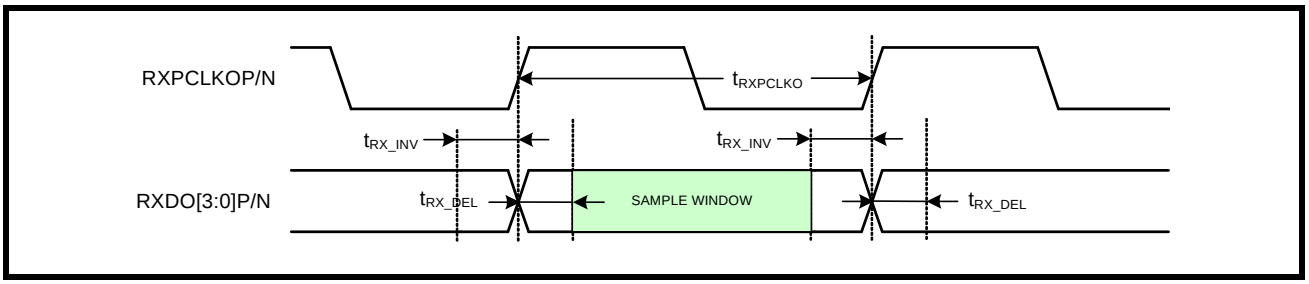


TABLE 5: RECEIVE PARALLEL DATA AND CLOCK OUTPUT TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{RXPCLKO}$	Receive parallel clock output period (622.08 MHz non-FEC rate)		1608		ps
$t_{RXPCLKO}$	Receive parallel clock output period (666.51 MHz FEC rate)		1500		ps
t_{RX_INV}	RXPCLKOP/N "High" to data invalid window			200	ps
t_{RX_DEL}	RXPCLKOP/N "High" to data delay			200	ps
RX_{DUTY}	RXPCLKOP/N Duty Cycle	45		55	%

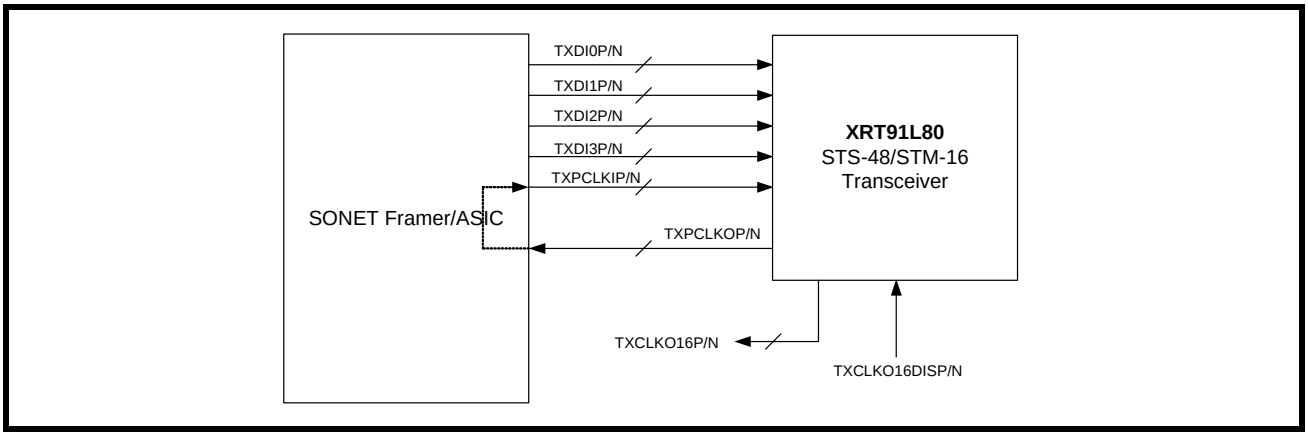
3.0 TRANSMIT SECTION

The transmit section of the XRT91L80 accepts 4-bit parallel LVDS data and converts it to serial CML data output intented to interface to an optical module. It consists of a 4-bit parallel LVDS interface, a 4x9 FIFO, Parallel-to-Serial Converter, a clock multiplier unit (CMU), a Current Mode Logic (CML) differential line driver, and Loop Timing modes. The CML serial data output rate is 2.488/2.666 Gbps for STS-48/STM-16 applications. The high frequency serial clock is synthesized by a PLL, which uses a low frequency clock as its input reference. In order to synchronize the data transfer process, the synthesized 2.488/2.666 GHz serial clock output is divided by four and the 622.08/666.51 MHz clock is presented to the upstream device to be used as its timing source.

3.1 Transmit Parallel Input Interface

The parallel data from an upstream device is presented to the XRT91L80 through a 4-bit LVDS parallel bus interface TXDI[3:0]P/N. The data is latched into a parallel input register on the rising edge of TXPCLKIP/N. If the SONET Framer/ASIC is synchronized to the same timing source as the XRT91L80, the transmit data and clock input can directly interface to the STS-48/STM-16 transceiver. However, if the SONET Framer/ASIC is synchronized to a separate crystal, the XRT91L80 has two clock output references that can be used to synchronize the SONET Framer/ASIC. TXPCLKOP/N is a 622.08/666.51 MHz LVDS clock output source that is derived from the CMU synthesized high-speed clock. TXCLKO16P/N is a 155.52/166.63 MHz LVDS auxiliary clock output source that is also derived from the CMU synthesized high-speed clock. Either of these two clock output sources can be used to synchronize the SONET Framer/ASIC to the XRT91L80. If the auxiliary clock source is not used, it can be disabled by pulling TXCLKO16DIS "High". A simplified block diagram of the parallel interface is shown in Figure 9.

FIGURE 9. TRANSMIT PARALLEL INPUT INTERFACE BLOCK



3.2 Transmit Parallel Data Input Timing

When applying parallel data input to the transmitter, the setup and hold times should be followed as shown in Figure 10 and Table 6.

FIGURE 10. TRANSMIT PARALLEL INPUT TIMING

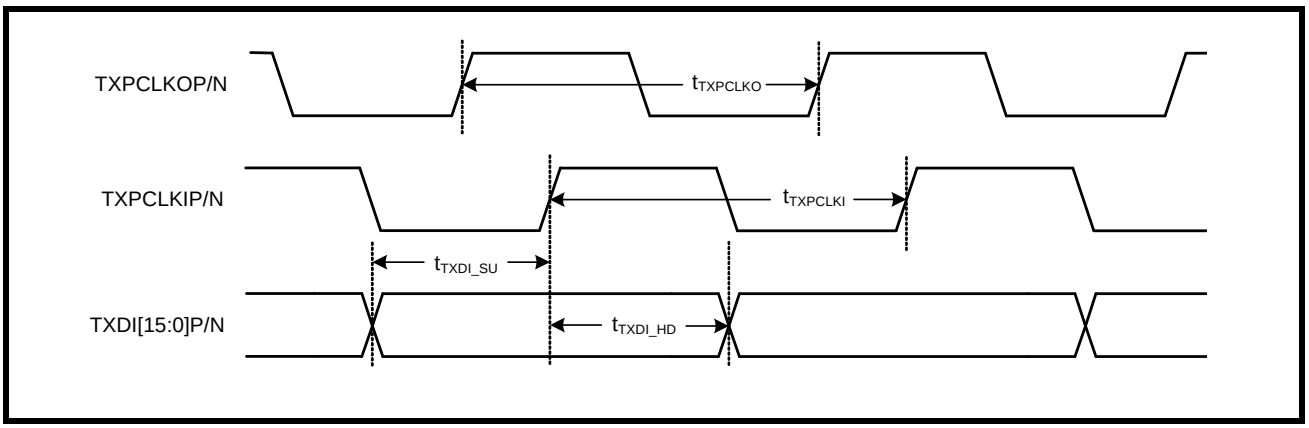


TABLE 6: TRANSMIT PARALLEL DATA AND CLOCK INPUT TIMING SPECIFICATION

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{TXPCLKI}$	Transmit parallel clock input period (622.08 MHz non-FEC rate)		1608		ps
$t_{TXPCLKI}$	Transmit parallel clock input period (666.51 MHz FEC rate)		1500		ps
t_{TXDI_SU}	TXPCLKIP/N "High" to data setup time	300			ps
t_{TXDI_HD}	TXPCLKIP/N "High" to data hold time	300			ps
TX_{DUTY}	TXPCLKIP/N Duty Cycle	40		60	%

TABLE 7: TRANSMIT PARALLEL CLOCK OUTPUT TIMING SPECIFICATION

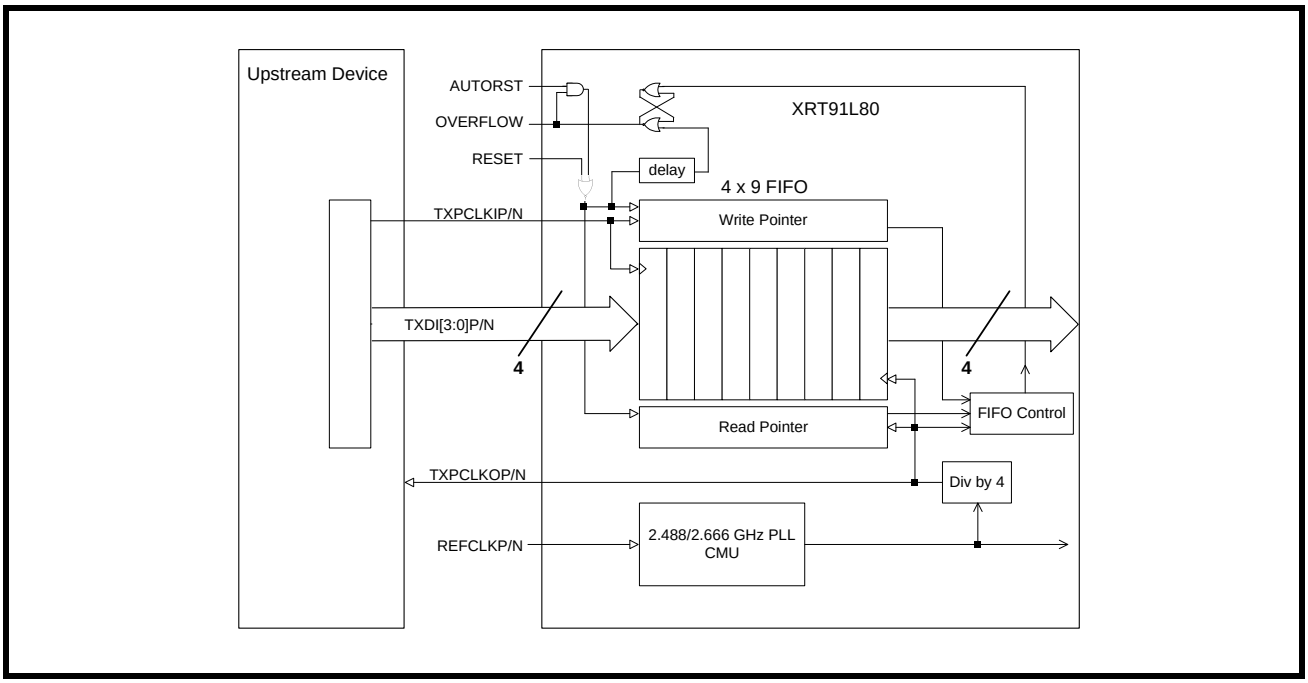
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{TXPCLKO}$	Transmit parallel clock output period (622.08 MHz non-FEC rate)		1608		ps
$t_{TXPCLKO}$	Transmit parallel clock output period (666.51 MHz FEC rate)		1500		ps
TX_{DUTY}	TXPCLKOP/N Duty Cycle	45		55	%

3.3 Transmit FIFO

The parallel interface also includes a 4x9 FIFO that can be used to eliminate difficult timing issues between the input transmit clock and the clock derived from the CMU. The use of the FIFO permits the system to tolerate an arbitrary amount of delay and jitter between TXPCLKOP/N and TXPCLKIP/N. The FIFO can be initialized when FIFO_RST is asserted and held "High" for 2 cycles of the TXPCLKOP/N clock. When the FIFO_RST is de-asserted, it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Once the FIFO is centered, the delay between TXPCLKOP/N and TXPCLKIP/N can decrease or increase up to two periods of the low-speed clock. Should the delay exceed this amount, the read and write pointers will point to the same Nibble in the FIFO resulting in a loss of transmitted data (FIFO overflow). In the event of a FIFO overflow, the FIFO control logic will initiate an OVERFLOW signal that can be used by an external controller to issue a FIFO RESET signal. The device under the control of the FIFO_AUTORST pin can automatically recover from an overflow condition. When the FIFO_AUTORST input is set to a "High" level, once an overflow condition is detected, the

device will set the OVERFLOW pin to a "High" level and will automatically reset and center the FIFO. Figure 11 provides a detailed overview of the transmit FIFO in a system interface.

FIGURE 11. TRANSMIT FIFO AND SYSTEM INTERFACE



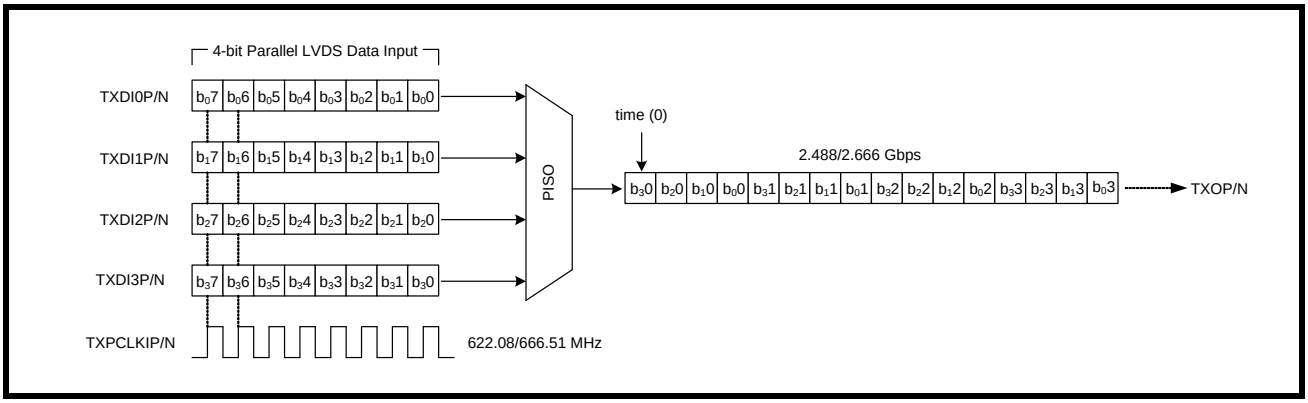
3.4 FIFO Calibration Upon Power Up

It is required that the FIFO_RST pin be pulled "High" for 2 TXPCLKOP/N cycles to flush out the FIFO after the device is powered on. If the FIFO experiences an Overflow condition, FIFO_RST can be used to manually reset the FIFO. However, the STS-48/STM-16 transceiver has an automatic reset pin that will allow the FIFO to automatically reset upon an Overflow condition. FIFO_AUTORST should be pulled "High" to enable the automatic FIFO reset function.

3.5 Transmit Parallel Input to Serial Output (PISO)

The PISO is used to convert 622.08/666.51 MHz parallel data input to 2.488/2.666 Gbps serial data output which can interface to an optical module. The PISO bit interleaves parallel data input into a serial bit stream taking the first bit from TXDI3P/N, then the first bit from TXDI2P/N, and so on as shown in Figure 12.

FIGURE 12. SIMPLIFIED BLOCK DIAGRAM OF PISO



3.6 Clock Multiplier Unit (CMU) and Re-Timer

The high-speed serial clock synthesized by the CMU is divided by 4, and is presented to the upstream device as TXPCLKOP/N clock . The upstream device should use TXPCLKOP/N as its timing source. The upstream device then generates the TXPCLKIP/N clock that is phase aligned with the transmit data and provides it to the parallel interface of the transmitter. The data must meet setup and hold times with respect to TXPCLKIP/N. The XRT91L80 will latch TXDI[3:0]P/N on the rising edge of TXPCLKIP/N. The clock synthesizer uses a PLL to lock to the differential input reference clock REFCLKP/N. It will then use this reference clock to generate the 2.488/2.666 GHz STS-48/STM-16 serial clock and in addition feed this high-speed synthesized clock to the PISO. The Retimer will then align the transmit serial data from the PISO with this 2.488/2.666 GHz synthesized clock to generate the output TXOP/N. REFCLKP/N input can accept a clock from a differential LVPECL crystal oscillator that has a frequency accuracy better than 20ppm in order for the high-speed transmit serial clock frequency to have the accuracy required for SONET systems. Table 8 specifies the Clock Multiplier Unit performance characteristics.

The CMU can also be driven by an optional external VCXO for loop timed or local reference de-jitter applications. VCXO_INP/N can be connected to the output of a VCXO that can be configured to clean up the recovered received clock coming from CP_OUT in loop timing mode before being applied to the input of the transmit CMU as a reference clock. In addition, the internal phase/frequency detector and charge pump, combined with an external VCXO can alternately be used as a jitter attenuator to de-jitter a noisy system reference clock such as REFCLKP/N prior to it being used to time the CMU. The following Section 3.7, “Loop Timing and Clock Control,” on page 21 illustrate the use of this method.

TABLE 8: CLOCK MULTIPLIER UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	45		55	%
REF_{TOL}	Reference clock frequency tolerance[1]	-20		+20	ppm
REF_{STS48}	Reference clock jitter limits from 12 KHz to 20 MHz			-61	dB_C
$OCLK_{JIT}$	Clock output jitter generation with 77.76 MHz reference clock		3.1	4.0	mUI_{rms}
$OCLK_{JIT}$	Clock output jitter generation with 155.52 MHz reference clock		2.5	3.0	mUI_{rms}
$OCLK_{FREQ}$	Frequency output	2.488		2.667	GHz
$OCLK_{DUTY}$	Clock output duty cycle	45		55	%

Jitter specification is defined using a 12kHz to 20MHz appropriate SONET/SDH filter.

[1]Required to meet SONET output frequency stability requirements.

3.7 Loop Timing and Clock Control

Two types of loop timing are possible in the XRT91L80.

In the regular loop timing mode (without an external VCXO), loop timing is controlled by the LOOPTM_NOJA pin. This mode is selected by asserting the LOOPTM_NOJA signal to a "High" level. When the loop timing mode is activated, the external local reference clock to the input of the CMU is replaced with the 1/16th or the 1/32nd of the high-speed recovered receive clock coming from the CDR. Under this condition both the transmit and receive sections are synchronized to the recovered receive clock. The normal looptime mode directly locks the CMU to the recovered receive clock with no external de-jittering.

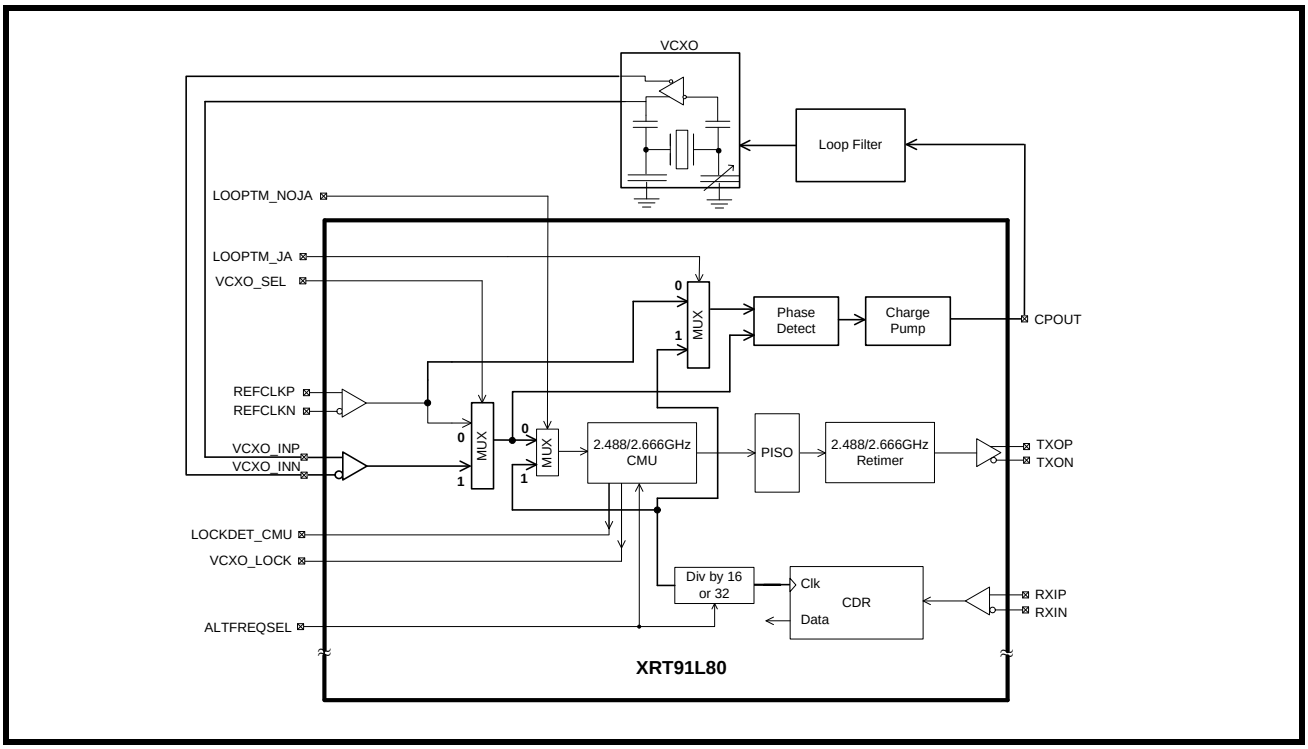
Loop timing performance can be further improved using an external VCXO-based PLL to clean up the jitter of the recovered receive clock. In this case the VCXO_SEL pin should be set "High." By doing so, the CMU receives its reference clock signal from an external VCXO connected to the VCXO_INP/N inputs. The LOOPTM_JA pin must also be set "High" in order to select the recovered receive clock as the reference source for the de-jitter PLL. In this state, the VCXO will be phase locked to the recovered receive clock through a narrowband loop filter. The use of the on-chip phase/frequency detector with charge pump and an external VCXO to remove the transmit jitter due to jitter in the recovered clock is shown in Figure 13.

The on-chip phase/frequency detector can also be used to remove the jitter from a noisy reference signal that is applied to the REFCLKP/N inputs. In this case, the LOOPTM_NOJA pin should be set "Low", the VCXO_SEL set "High", and the LOOPTM_JA pin set "Low". In this configuration, the REFCLKP/N signal is used as the reference to the de-jitter PLL and the de-jittered output of the phase locked VCXO is used as the timing reference to the CMU. Table 9 provides configuration for selecting the loop timing and reference de-jitter modes.

TABLE 9: LOOP TIMING AND REFERENCE DE-JITTER CONFIGURATIONS

VCXO_SEL	LOOPTM_JA	LOOPTM_NOJA	ACTION
0	**0**	**0**	Normal mode
0	**0**	**1**	Loop timing without de-jitter VCXO
1	**0**	**0**	REFCLKP/N reference de-jitter VCXO
1	**1**	**0**	Loop timing with de-jitter VCXO

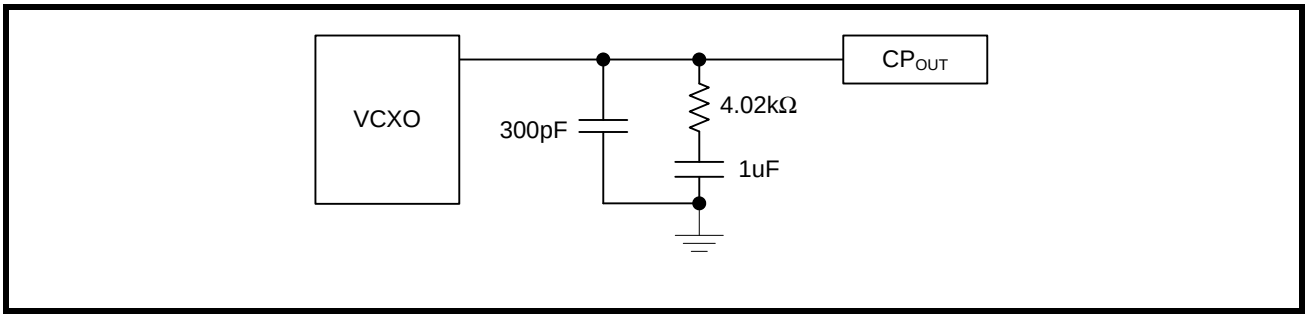
FIGURE 13. LOOP TIMING MODE USING AN EXTERNAL CLEANUP VCXO



3.8 External Loop Filter

As shown in Figure 13, there is an internal charge pump used to drive an external loop filter and external VCXO. The charge pump current is fixed at 250uA. Figure 14 is a simplified block diagram of the external loop filter and recommended values.

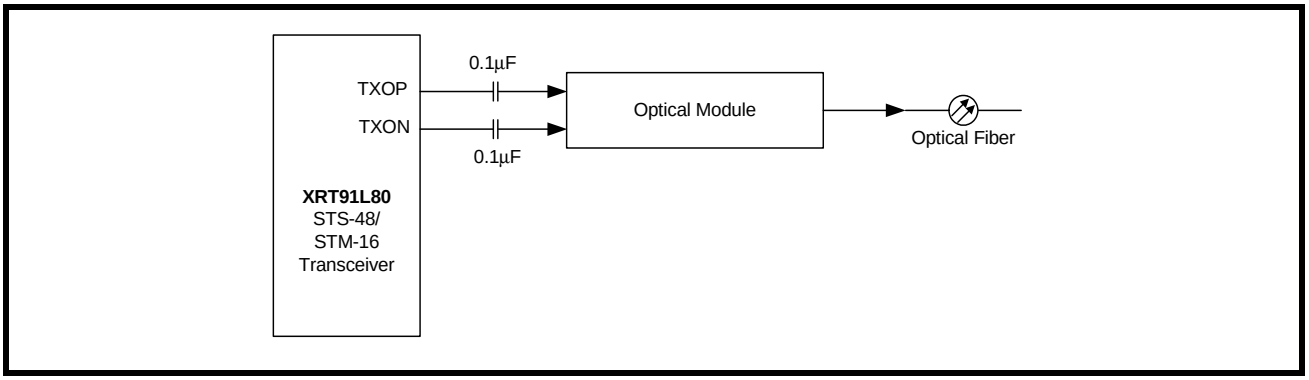
FIGURE 14. SIMPLIFIED DIAGRAM OF THE EXTERNAL LOOP FILTER



3.9 Transmit Serial Output Control

The 2.488/2.666 Gbps transmit serial output is avaliable on TXOP/N pins. The transmit serial output can be AC or DC coupled to an optical module or electrical interface. A simplified AC coupling block diagram is shown in Figure 15.

FIGURE 15. TRANSMIT SERIAL OUTPUT INTERFACE BLOCK



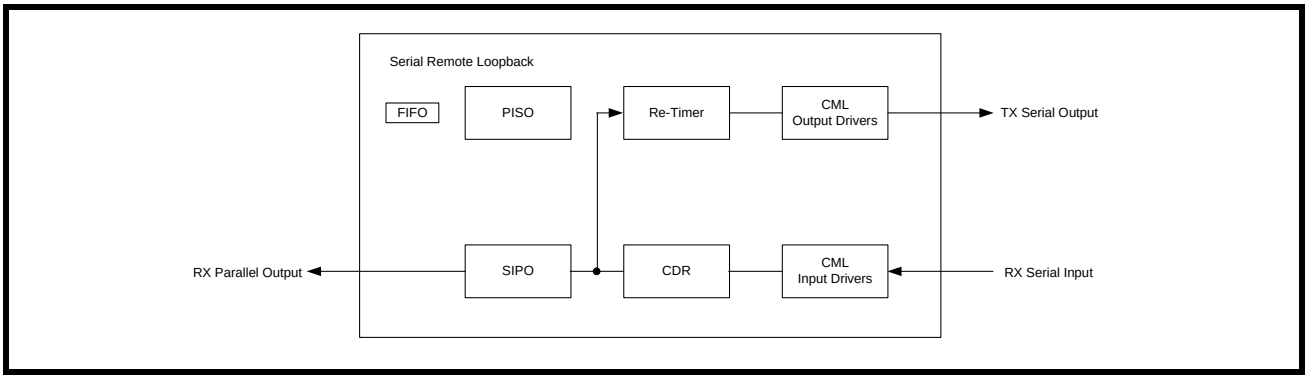
NOTE: *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

4.0 DIAGNOSTIC FEATURES

4.1 Serial Remote Loopback

The serial remote loopback function is activated by setting RLOOPS "High". When serial remote loopback is activated, the high-speed serial receive data from RXIP/N is presented at the high-speed transmit output TXOP/N, and the high-speed recovered clock is selected and presented to the high-speed transmit clock input of the Retimer. During serial remote loopback, the high-speed receive data (RXIP/N) is also converted to parallel data and presented at the low-speed receive parallel interface RXDO[3:0]P/N. The recovered receive clock is also divided by 4 and presented at the low-speed clock output RXPCLKOP/N to synchronize the transfer of the 4-bit received parallel data. A simplified block diagram of serial remote loopback is shown in Figure 16.

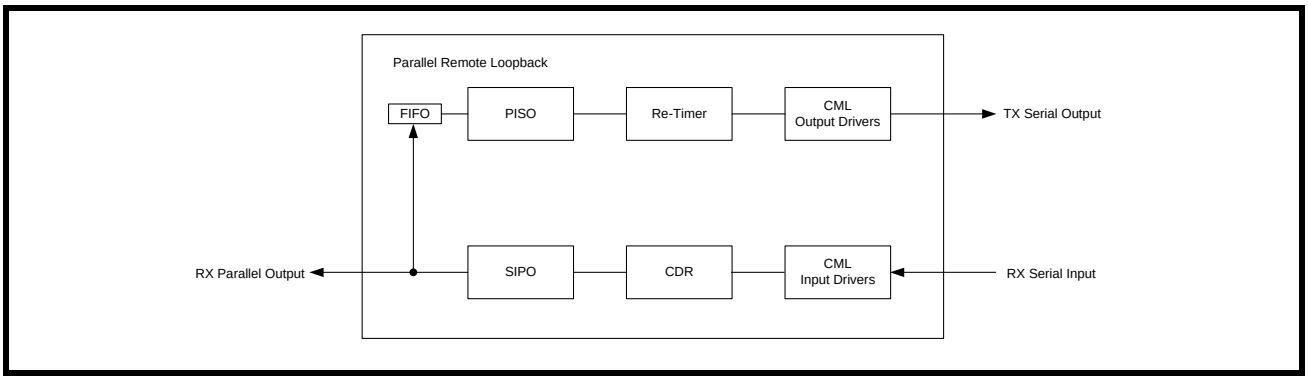
FIGURE 16. SERIAL REMOTE LOOPBACK



4.2 Parallel Remote Loopback

RLOOPP controls a more comprehensive version of remote loop-back that can also be used in conjunction with the de-jitter PLL that is phase locked to the recovered receive clock. In this mode, the received signal is processed by the CDR, and is sent through the serial to parallel converter. At this point, the 4-bit parallel data and clock are looped back to the transmit FIFO. Concurrently, if receive clock jitter attenuation is also employed, the received clock is divided down in frequency and presented to the input of the integrated phase/ frequency detector and is compared to the frequency of a VCXO that is connected to the VCXO_INP/N inputs. With the LOOPTM_JA configured to use the recovered receive clock as the reference and VCXO_SEL asserted, the VCXO is phase locked to the recovered receive clock. The de-jittered clock is then used to retime the transmitter, resulting in the re-transmission of the de-jittered received data out of TXOP/N. A FIFO reset using FIFO_RST should follow immediately after enabling/disabling parallel remote loopback. A simplified block diagram of parallel remote loopback is shown in Figure 17.

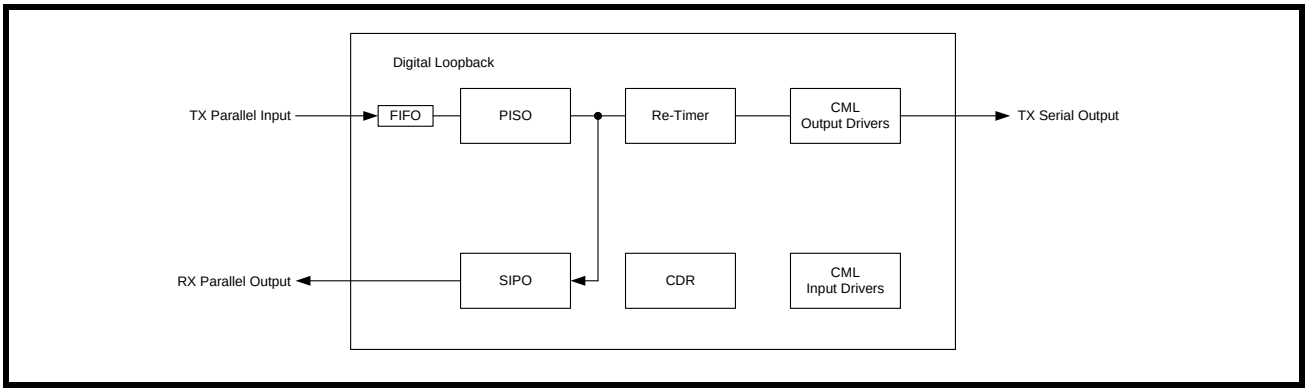
FIGURE 17. PARALLEL REMOTE LOOPBACK



4.3 Digital Local Loopback

The digital local loopback is activated when the DLOOP signal is set "High." When digital local loopback is activated, the high-speed data from the output of the parallel to serial converter is looped back and presented to the high-speed input of the receiver serial to parallel converter. The CMU output is also looped back to the receive section and is used to synchronize the transfer of the data through the receiver. In Digital loopback mode, the transmit data from the transmit parallel interface TXDI[3:0]P/N is serialized and presented to the high-speed transmit output TXOP/N using the high-speed 2.488/2.666 GHz transmit clock which is generated from the clock multiplier unit and presented to the input of the Retimer and SIPO. A simplified block diagram of digital loopback is shown in Figure 18.

FIGURE 18. DIGITAL LOOPBACK



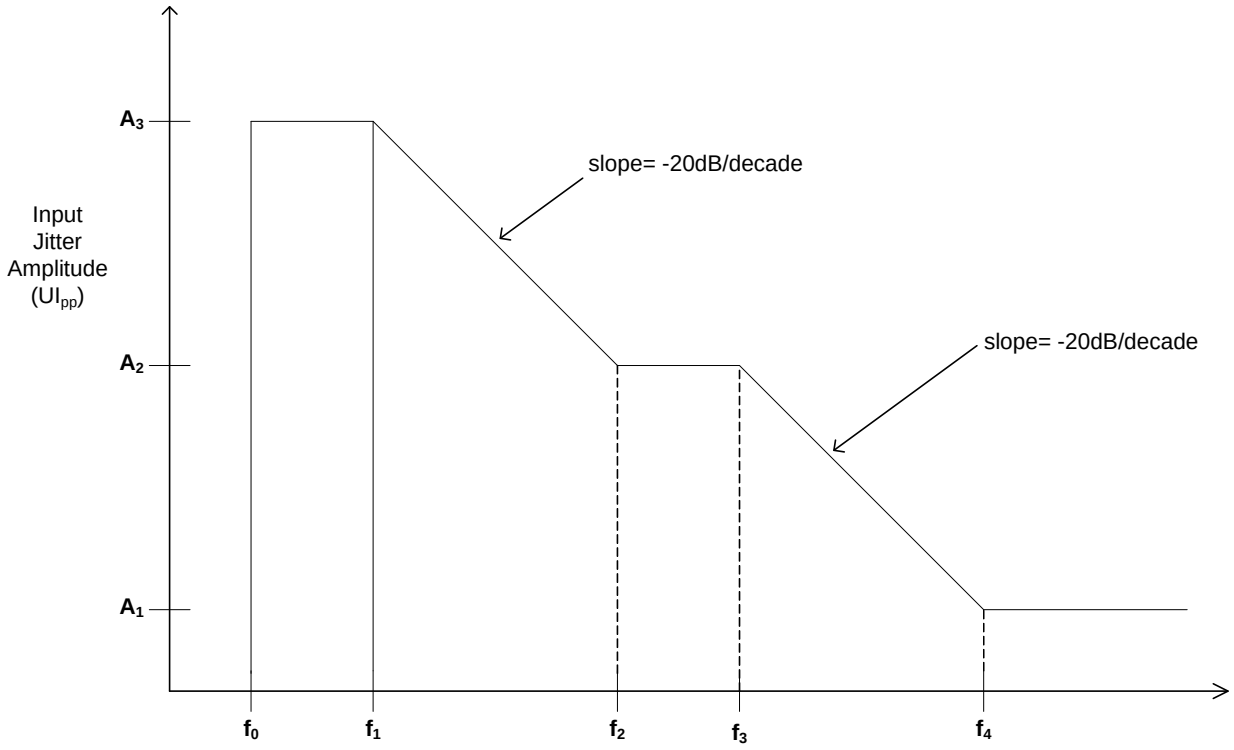
4.4 SONET Jitter Requirements

SONET equipment jitter requirements are specified for the following three types of jitter. The definitions of each of these types of jitter are given below. SONET equipment jitter requirements are specified for the following three types of jitter.

4.4.1 Jitter Tolerance:

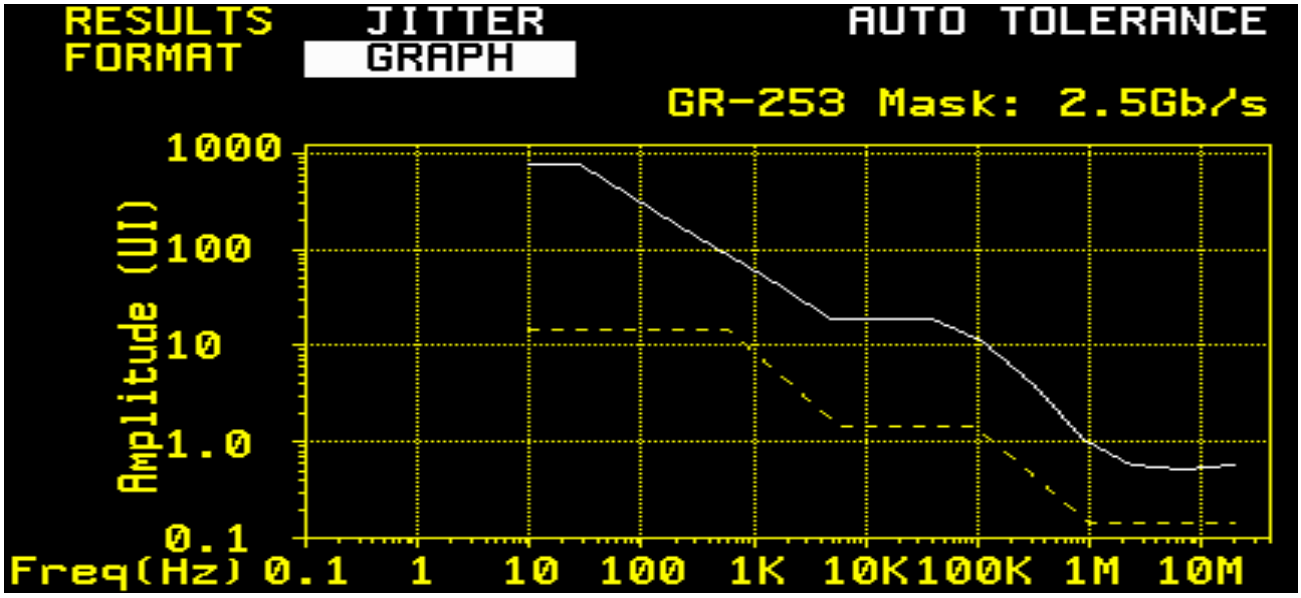
Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input OC-N equipment interface that causes an equivalent 1dB optical power penalty. OC-1/STS-1, OC-3/STS-3, OC-12/ STS-12 and OC-48/STS-48 category II SONET interfaces should tolerate, the input jitter applied according to the mask of Figure 19, with the corresponding parameters specified in the figure.

FIGURE 19. JITTER TOLERANCE MASK



OC-N/STS-N LEVEL	F0 (HZ)	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (HZ)	A1 (UIPP)	A2 (UIPP)	A3 (UIPP)
1	10	30	300	2K	20K	0.15	1.5	15
3	10	30	300	6.5K	65K	0.15	1.5	15
12	10	30	300	25K	250K	0.15	1.5	15
48	10	600	6000	100K	1000K	0.15	1.5	15

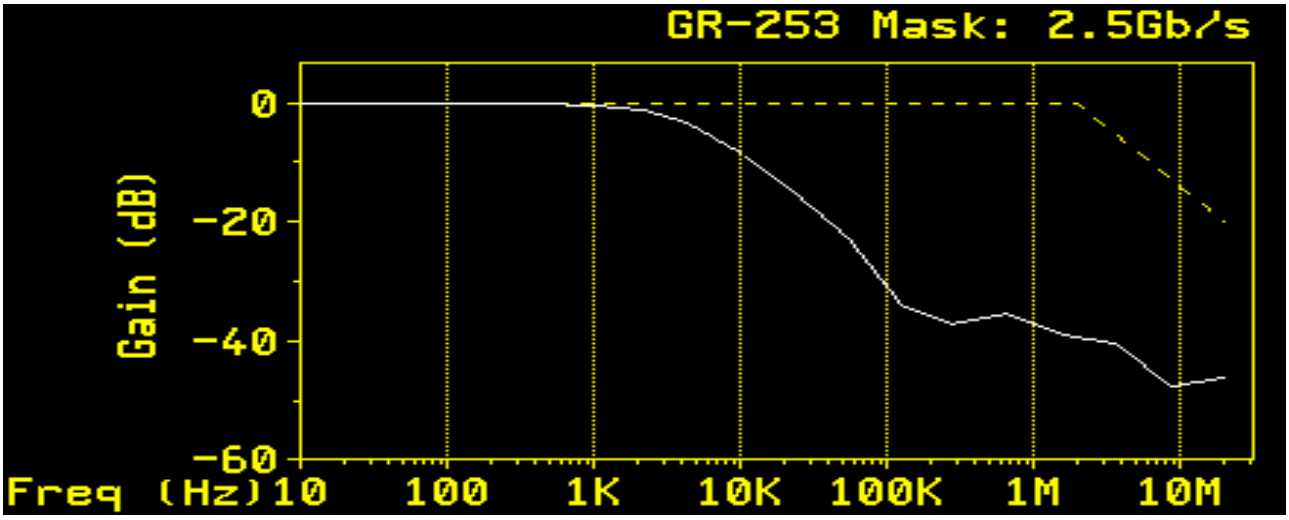
FIGURE 20. 91L80 MEASURED JITTER TOLERANCE WITH EXTERNAL JITTER ATTENUATION ENABLED IN LOOPTIMING AT 2.488 GBPS IN STS-48.



4.4.2 Jitter Transfer

Jitter transfer is defined as the ratio of the jitter on the output of STS-N to the jitter applied on the input of STS-N versus frequency. Jitter transfer is important in applications where the system is utilized in the loop-timed mode, where the recovered clock is used as the source of the transmit clock.

FIGURE 21. 91L80 MEASURED JITTER TRANSFER WITH EXTERNAL JITTER ATTENUATION ENABLED IN LOOPTIMING AT 2.488 GBPS IN STS-48.



4.4.3 Jitter Generation

Jitter generation is defined as the amount of jitter at the STS-N output in the absence of applied input jitter. The Bellcore and ITU requirement for this type jitter is 0.01UI rms measured with a specific band-pass filter.

FIGURE 22. 91L80 MEASURED ELECTRICAL PHASE NOISE TRANSMIT JITTER GENERATION AT 2.488 GBPS

Wide-band filter used in this test case.

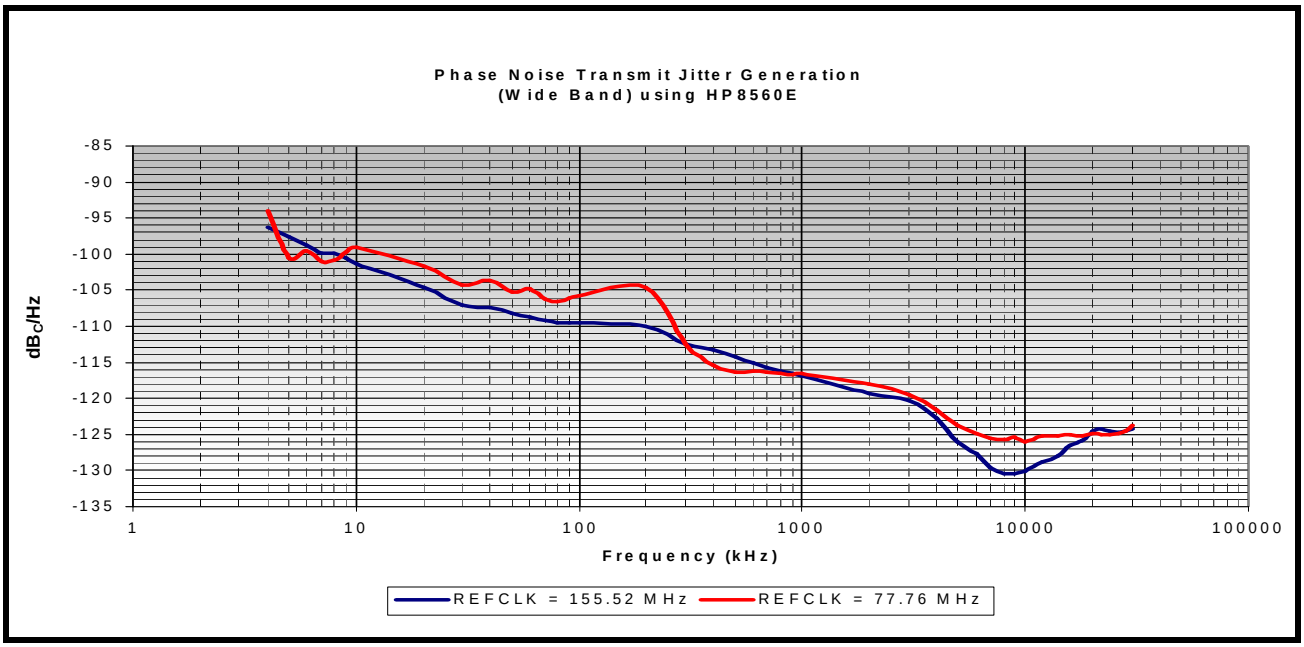
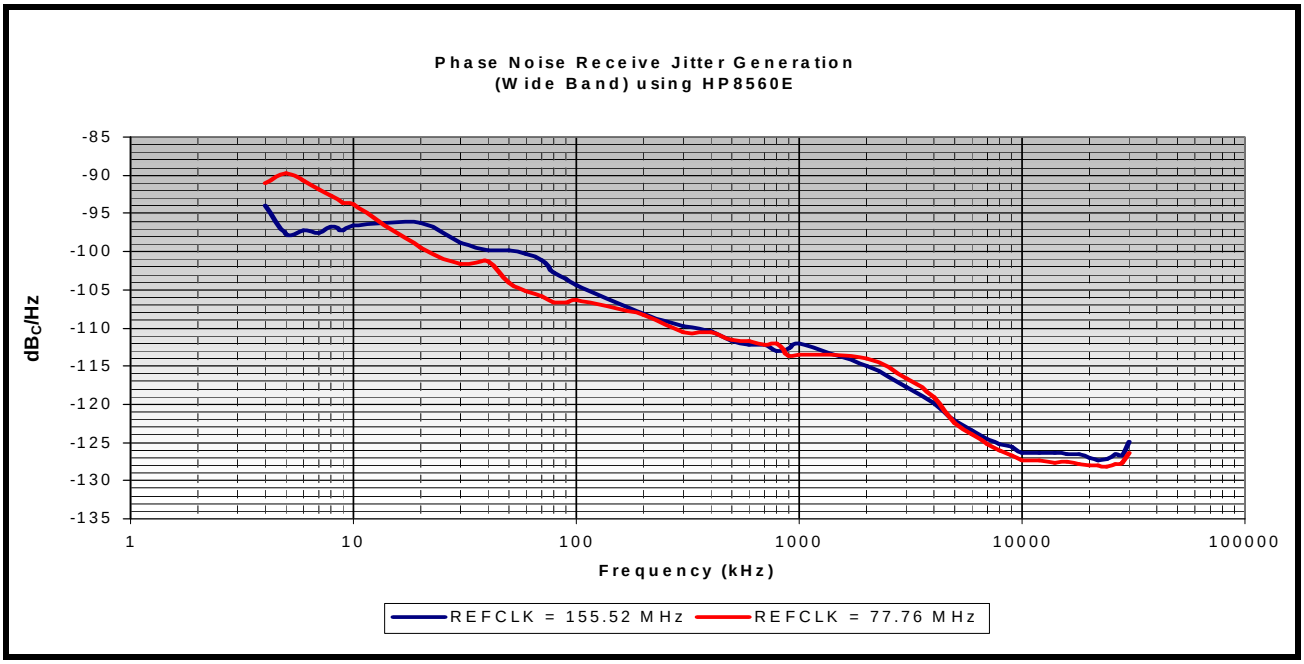


FIGURE 23. 91L80 MEASURED ELECTRICAL PHASE NOISE RECEIVE JITTER GENERATION AT 2.488 GBPS

Wide-band filter used in this test case.

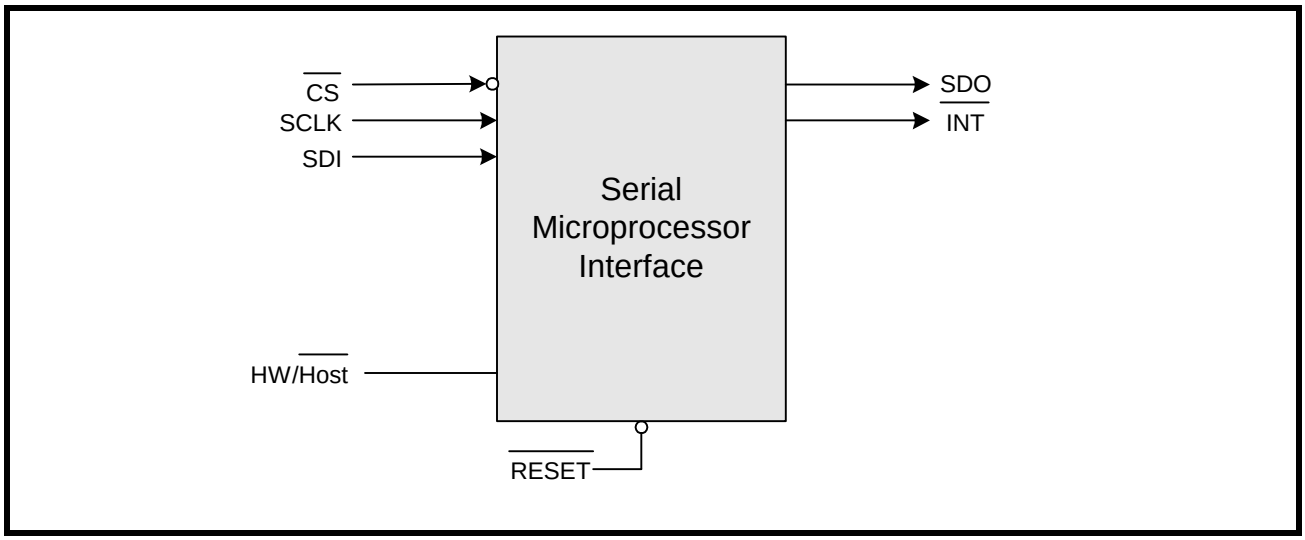


For more information on these specifications refer to Bellcore TR-NWT-000253 sections 5.6.2-5 and GR-253-CORE section 5.6.

5.0 SERIAL MICROPROCESSOR INTERFACE BLOCK

The serial microprocessor uses a standard 3-pin serial port with $\overline{CS}$, SCLK, and SDI for programming the transceiver. Optional pins such as SDO, $\overline{INT}$, and $\overline{RESET}$ allow the ability to read back contents of the registers, monitor the transceiver via an interrupt pin, and reset the transceiver to its default configuration by pulling reset "Low" for more than 10ms. A simplified block diagram of the Serial Microprocessor is shown in Figure 24.

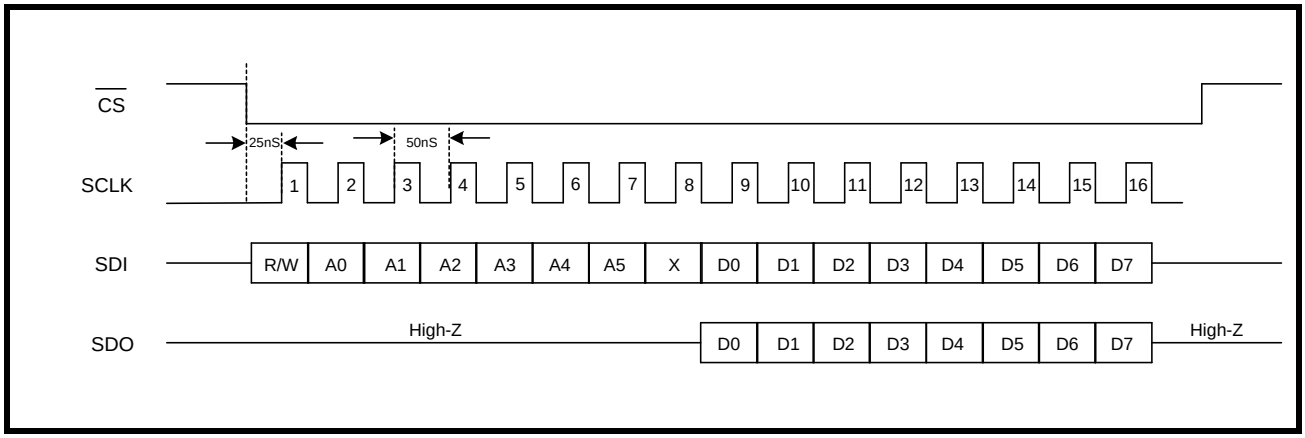
FIGURE 24. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



5.1 SERIAL TIMING INFORMATION

The serial port requires 16 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 16 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in Figure 25.

FIGURE 25. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



NOTE: *The serial microprocessor interface does **NOT** support "burst write" or "burst read" operations. Chip Select (active "Low") **must be de-asserted** at the end of every single write or single read operation.*

5.2 16-BIT SERIAL DATA INPUT DESCRITPTION

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the transceiver LSB first. The 16 bits of serial data are described below.

5.2.1 R/W (SCLK1)

The first serial bit applied to the transceiver informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to “0”, the microprocessor is configured for a Write operation. If the R/W bit is set to “1”, the microprocessor is configured for a Read operation.

5.2.2 A[5:0] (SCLK2 - SCLK7)

The next 6 SCLK cycles are used to provide the address to which a Read or Write operation will occur. A0 (LSB) must be sent to the transceiver first followed by A1 and so forth until all 6 address bits have been sampled by SCLK.

5.2.3 X (Dummy Bit SCLK8)

The dummy bit sampled by SCLK8 is used to allow sufficient time for the serial data output pin to update data if the readback mode is selected by setting R/W = “1”. Therefore, the state of this bit is ignored and can hold either “0” or “1” during both Read and Write operations.

5.2.4 D[7:0] (SCLK9 - SCLK16)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. D0 (LSB) must be sent to the transceiver first followed by D1 and so forth until all 8 data bits have been sampled by SCLK. Once 16 SCLK cycles have been complete, the transceiver holds the data until $\overline{CS}$ is pulled “High” whereby, the serial microprocessor latches the data into the selected internal register.

5.3 8-BIT SERIAL DATA OUTPUT DESCRIPTION

The serial data output is updated on the falling edge of SCLK9 - SCLK16 if R/W is set to “1”. D0 (LSB) is provided on SCLK9 to the SDO pin first followed by D1 and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

6.0 REGISTER MAP AND BIT DESCRIPTIONS

TABLE 10: MICROPROCESSOR REGISTER MAP

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Channel 0 Control Register (0x00h - 0x05h)										
0	0x00	R/W	Reserved	Reserved	Reserved	VCXOIE	LOSIE	CDRIE	CMUIE	FIFOIE
1	0x01	RUR	Reserved	Reserved	Reserved	VCXOIS	LOSIS	CDRIS	CMUIS	FIFOIS
2	0x02	RO	Reserved	Reserved	Reserved	VCXOD	LOSD	CDRD	CMUD	FIFOD
3	0x03	R/W	Reserved	ALTFREQSEL	Reserved	LOOPBW	VCXO_SEL	TXCLK016DIS	FIFO_AUTO-RST	FIFORST
4	0x04	R/W	Reserved	POLARITY	LOOPTM_JA	LOOPTM_NOJA	LOSDMUTE	DISRD	Reserved	VCXOLKEN
5	0x05	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	DLOOP	RLOOPS	RLOOPP
0x06 - 0x3D		R/W	**Reserved**							
62	0x3E	RO	**Device ID (See Bit Description)**							
63	0x3F	RO	**Revision ID (See Bit Description)**							

TABLE 11: MICROPROCESSOR REGISTER 0X00H BIT DESCRIPTION

INTERRUPT ENABLE CONTROL REGISTER (0X00H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	Reserved	This Register Bit is Not Used	X	X
D4	VCXOIE	**Voltage Controlled External Oscillator Lock Interrupt Enable** "0" = Masks the VCXO Lock interrupt generation "1" = Enables Interrupt generation ***NOTE:*** *VCXOLKEN must be enabled for this bit to have functional meaning.*	R/W	0
D3	LOSIE	**Loss of Signal Interrupt Enable** "0" = Masks the LOS interrupt generation "1" = Enables Interrupt generation	R/W	0
D2	CDRIE	**Clock and Data Recovery Lock Interrupt Enable** "0" = Masks the CDR Lock interrupt generation "1" = Enables Interrupt generation	R/W	0
D1	CMUIE	**Clock Multiplier Unit Lock Interrupt Enable** "0" = Masks the CMU Lock interrupt generation "1" = Enables Interrupt generation	R/W	0
D0	FIFOIE	**FIFO Overflow Interrupt Enable** "0" = Masks the FIFO Overflow interrupt generation "1" = Enables Interrupt generation	R/W	0

TABLE 12: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION

INTERRUPT STATUS CONTROL REGISTER (0X01H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	Reserved	This Register Bit is Not Used	X	X
D4	VCXOIS	**Voltage Controlled External Oscillator Lock Interrupt Status** An external interrupt will not occur unless the VCXOIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in VCXO Lock Status Occurred ***NOTE:*** *VCXOLKEN must be enabled for this bit to have functional meaning.*	RUR	0
D3	LOSIS	**Loss of Signal Interrupt Status** An external interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in LOS Status Occurred	RUR	0
D2	CDRIS	**Clock and Data Recovery Lock Interrupt Status** An external interrupt will not occur unless the CDRIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in CDR Lock Status Occurred	RUR	0
D1	CMUIS	**Clock Multiplier Unit Lock Interrupt Status** An external interrupt will not occur unless the CMUIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in CMU Lock Status Occurred	RUR	0
D0	FIFOIS	**FIFO Overflow Interrupt Status** An external interrupt will not occur unless the FIFOIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in FIFO Overflow Status Occurred	RUR	0

TABLE 13: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

STATUS CONTROL REGISTER (0X02H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X

STATUS CONTROL REGISTER (0X02H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D5	Reserved	This Register Bit is Not Used	X	X
D4	VCXOD	**Voltage Controlled External Oscillator Lock Detection** The VCXOD is used to indicate whether the internal clock reference is locked to an external VCO. "0" = VCXO currently not Locked "1" = VCXO Locked ***NOTE:*** *VCXOLKEN must be enabled for this bit to have functional meaning.*	RO	0
D3	LOSD	**Loss of Signal Detection** The LOSD indicates the LOS activity. "0" = No Alarm "1" = A LOS condition is present	RO	0
D2	CDRD	**Clock and Data Recovery Lock Detection** The CDRD is used to indicate that the CDR is locked. "0" = CDR Out of Lock "1" = CDR Locked	RO	0
D1	CMUD	**Clock Multiplier Unit Lock Detection** The CMUD is used to indicate that the CMU is locked. "0" = CMU Out of Lock "1" = CMU Locked	RO	0
D0	FIFOD	**FIFO Overflow Detection** The FIFOD indicates that the FIFO is experiencing an overflow condition. "0" = No Alarm "1" = A FIFO Overflow condition is present	RO	0

TABLE 14: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

CONFIGURATION 0 CONTROL REGISTER (0X03H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D7	Reserved	Reserved - Set to 0	R/W	0
D6	ALTFREQSEL	**Input Reference Frequency Select** This bit is used to select the clock input reference. "0" = 77.76/83.3 MHz "1"= 155.52/166 MHz	R/W	1
D5	Reserved	Reserved - Set to 0	R/W	0

TABLE 14: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

CONFIGURATION 0 CONTROL REGISTER (0X03H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D4	LOOPBW	**CMU Loop Band Width Select** This bit is used to select the bandwidth of the clock multiplier unit of the transmit path to a narrow or wide band. Use Wide Band for clean reference signals and Narrow Band for noisy references. "0" = Wide Band (4x) "1" = Narrow Band (1x)	R/W	0
D3	VCXO_SEL	**VCXO De-Jitter Select** This bit selects either the normal REFCLKP/N or the de-jitter VCXO_INP/N as a reference clock. "0" = Normal REFCLKP/N Mode "1" = De-Jitter VCXO Mode	R/W	0
D2	TXCLKO16DIS	**Auxiliary Clock Disable** This bit is used to control the activity of the auxiliary clock. "0" = TXCLKO16P/N Enabled "1" = TXCLKO16P/N Disabled	R/W	0
D1	FIFO_ AUTORST	**Automatic FIFO Overflow Reset** If this bit is set to "1", the STS-48/STM-16 transceiver will automatically flush the FIFO upon an overflow condition. Upon power-up, the FIFO should be manually reset by setting FIFO_RST to "1" for a minimum of 2 TXPCLKOP/N cycles. "0" = Manual FIFO reset required for Overflow Conditions "1" = Automatically resets FIFO upon Overflow Detection	R/W	0
D0	FIFO_RST	**Manual FIFO Reset** FIFORST should be set to "1" for a minimum of 2 TXPCLKOP/N cycles after powering up and during manual FIFO reset. After the FIFO_RST bit is returned "Low," it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Upon an interrupt indication that the FIFO has an overflow condition, this bit is used to reset or flush out the FIFO. "0" = Normal Operation "1" = Manual FIFO Reset ***NOTE:*** *To automatically reset the FIFO, see the FIFO_AUTORST bit.*	R/W	0

TABLE 15: MICROPROCESSOR REGISTER 0X04H BIT DESCRIPTION

CONFIGURATION 1 CONTROL REGISTER (0X04H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	POLARITY	**Polarity for SDEXT Input** Controls the Signal Detect polarity convention of SDEXT. "0" = SDEXT is active "Low" "1" = SDEXT is active "High"	R/W	0
D5	LOOPTM_JA	**Loop Timing With Jitter Attenuation** The LOOPTM_JA bit must be set to "1" in order to select the recovered receive clock as the reference source for the de-jitter PLL. "0" = Disabled "1" = Loop timing with de-jitter PLL Activated	R/W	0
D4	LOOPTM_ NOJA	**Loop Timing With No Jitter Attenuation** When the loop timing mode is activated, the external local reference clock input to the CMU is replaced with the 1/16th or 1/32nd of the high-speed recovered receive clock coming from the CDR. "0" = Disabled "1" = Loop timing Activated	R/W	0
D3	LOSDMUTE	**Parallel Receive Data Output Mute Upon LOSD** If this bit is set to "1", the receive data output will automatically be forced to a logic state of "0" when an LOSD condition occurs. "0" = Disabled "1" = Mute RXDO[3:0]P/N Data Upon LOSD Condition	R/W	0
D2	DISRD	**Parallel Receive Data Output Disable** This bit is used to disable the RXDO[3:0]P/N parallel receive data output bus asynchronously. "0" = Normal Mode "1" = Forces RXDO[3:0]P/N to a logic state "0"	R/W	0
D1	Reserved	Reserved - Set to 0	R/W	0
D0	VCXOLKEN	**De-Jitter PLL Lock Detect Enable** This bit enables the VCXO_INP/N lock detect circuit to be active. "0" = VCXO Lock Detect Disabled "1" = VCXO Lock Detect Enabled	R/W	0

TABLE 16: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

DIAGNOSTIC CONTROL REGISTER (0X05H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X

DIAGNOSTIC CONTROL REGISTER (0X05H)				
BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D5	Reserved	This Register Bit is Not Used	X	X
D4	Reserved	This Register Bit is Not Used	X	X
D3	Reserved	This Register Bit is Not Used	X	X
D2	DLOOP	**Digital Local Loopback** Digital local loopback allows the transmit input pins to be looped back to the receive output pins for local diagnostics. The transmit serial data output is valid during the digital loopback. "0" = Disabled "1" = Enable Digital Local Loopback ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*	R/W	0
D1	RLOOPS	**Serial Remote Loopback** Serial remote loopback allows the receive serial input pins to be looped back to the transmit serial output pins for remote diagnostics. The receive data output is valid during a serial remote loopback. "0" = Disabled "1" = Enable Remote Serial Loopback ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*	R/W	0
D0	RLOOPP	**Parallel Remote Loopback** Parallel remote loopback has the same affect as the serial remote loopback, except that the data input is allowed to pass through the SIPO before it's looped back to the transmit path, wherein it passes through the transmit FIFO, through the PISO, and back out the transmit serial output. The receive data output is valid during a parallel remote loopback. "0" = Disabled "1" = Enable Remote Parallel Loopback ***NOTE:*** *DLOOP and RLOOPS should be **disabled** when RLOOPP is enabled. The internal FIFO should also be flushed using FIFO_RST when parallel remote loopback is enabled/ disabled.*	R/W	0

TABLE 17: MICROPROCESSOR REGISTER 0X3EH BIT DESCRIPTION

DEVICE "ID" REGISTER (0X3EH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Device "ID"	The device "ID" of the XRT91L80 LIU is 0xC0h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	1
D6				1
D5				0
D4				0
D3				0
D2				0
D1				0
D0				0

TABLE 18: MICROPROCESSOR REGISTER 0X3FH BIT DESCRIPTION

REVISION "ID" REGISTER (0X3FH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Revision "ID"	The revision "ID" of the XRT91L80 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon (Revision A) will be 0x01h.	RO	This byte shows the revision of the device.
D6				
D5				
D4				
D3				
D2				
D1				
D0				

7.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Thermal Resistance of STBGA Package....Θ_{jA} = 44°C/W		Operating Temperature Range.....-40°C t o 85°C
Thermal Resistance of STBGA Package....Θ_{jC} = 12°C/W		Case Temperature under bias.....-55°C to 125°C
ESD Protection (HBM).....>2000V		Storage Temperature .....-65°C to 150°C

ABSOLUTE MAXIMUM POWER AND INPUT/OUTPUT RATINGS

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS
$VDD_{1.8}$		1.8V Digital Core Power Supplies	-0.5		3.6	V
$AVDD_{1.8}$		1.8V Analog Core Power Supplies	-0.5		3.6	V
VDD_{IO}		3.3V Digital I/O and Power Supply	-0.5		6.0	V
$AVDD_{IO}$		3.3V Analog I/O and Power Supply	-0.5		6.0	V
	LVPECL	DC logic signal input voltage	-0.5		VDD_{IO} +0.5	V
	LVDS	DC logic signal input voltage	-0.5		VDD_{IO} +0.5	V
	LVTTL/ LVCMOS	DC logic signal input voltage	-0.5		5.5	V
	LVDS	DC logic signal output voltage	-0.5		VDD_{O} +0.5	V
	LVCMOS	DC logic signal output voltage	-0.5		VDD_{O} +0.5	V
	LVPECL	Input current	-100		100	mA
	LVDS	Input current	-100		100	mA
	LVTTL/ LVCMOS	Input current	-100		100	mA

NOTE: *Stresses listed under Absolute Maximum Power and I/O ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods will severely affect device reliability.*

POWER AND CURRENT DC ELECTRICAL CHARACTERISTICS

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$VDD_{1.8}$		CML and CMOS Core Power Supply Voltage	1.710	1.8	1.890	V	
$AVDD_{1.8\_TX}$		Analog Transmit CML and LVDS Power Supply Voltage (AVDD1.8_TX)	1.710	1.8	1.890	V	
$AVDD_{1.8\_RX}$		Analog Receive CML and LVDS Power Supply Voltage (AVDD1.8_RX)	1.710	1.8	1.890	V	
$VDD_{3.3}$		LVPECL and Digital I/O Power Supply Voltage	3.135	3.3	3.465	V	

POWER AND CURRENT DC ELECTRICAL CHARACTERISTICS

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$AVDD_{3.3\_TX}$		Analog Transmit I/O Power Supply Voltage (AVDD3.3_TX)	3.135	3.3	3.465	V	
$AVDD_{3.3\_RX}$		Analog Receive I/O Power Supply Voltage (AVDD3.3_RX)	3.135	3.3	3.465	V	
$I_{DD\_1.8}$		1.8V Total Power Supply Current		262		mA	
I_{DD_IO}		3.3V Total Power Supply Current		5		mA	
P_{LVDS}		Total Power Dissipation		490	650	mW	LVDS Mode

COMMON MODE LOGIC SIGNAL DC ELECTRICAL CHARACTERISTICS

Test Condition: $VDD_{1.8}$ = 1.8V ± 5%, $VDD_{\_IO}$ = 3.3V ± 5% unless otherwise specified

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{ODIFF}	CML	Output Differential Voltage	800		1200	mV	Differential Mode.
V_{IDIFF}	CML	Input Differential Voltage	200		1000	mV	Differential Mode.
$V_{ISINGLE}$	CML	Input Single-Ended Voltage Swing	100		600	mV	Differential Mode.
V_{IBIAS}	CML	Input Bias Range (AC Coupled)	1.0		1.4	V	Differential Mode.
R_{DIFF}	CML	Input Differential Resistance	75		125	Ω	

LVPECL LOGIC SIGNAL DC ELECTRICAL CHARACTERISTICS

Test Condition: $VDD_{1.8}$ = 1.8V ± 5%, $VDD_{\_IO}$ = 3.3V ± 5% unless otherwise specified

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	LVPECL	Input High Voltage	$VDD_{\_IO}$ - 1.2		$VDD_{\_IO}$ - 0.7	V	Differential
V_{IL}	LVPECL	Input Low Voltage	$VDD_{\_IO}$ - 2.0		$VDD_{\_IO}$ - 1.4	V	Differential
V_{IDIFF}	LVPECL	Input Differential Voltage	0.4		2.4	V	Differential Mode.
$V_{ISINGLE}$	LVPECL	Input Single-Ended Voltage Swing	0.2		1.2	V	Differential Mode.

LVDS LOGIC SIGNAL DC ELECTRICAL CHARACTERISTICS

Test Condition: $VDD_{1.8}$ = 1.8V ± 5%, VDD_IO = 3.3V ± 5% unless otherwise specified							
SYMBOL	**TYPE**	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
V_{OH}	LVDS	Output High Voltage			1480	mV	100 Ω line - line
V_{OL}	LVDS	Output Low Voltage	1020			mV	100 Ω line - line
V_{ODIFF}	LVDS	Output Differential Voltage Swing	250		400	mV	100 Ω line - line
$V_{OSINGLE}$	LVDS	Output Single-Ended Voltage Swing	125		200	mV	100 Ω line - line
V_{IH}	LVDS	Input High Voltage			1400	mV	
V_{IL}	LVDS	Input Low Voltage	800			mV	
V_{IDIFF}	LVDS	Input Differential Voltage Swing	200			mV	
$V_{ISINGLE}$	LVDS	Input Single-Ended Voltage Swing	100			mV	

LVTTL/LVCMOS SIGNAL DC ELECTRICAL CHARACTERISTICS

Test Condition: $VDD_{1.8}$ = 1.8V ± 5%, VDD_IO = 3.3V ± 5% unless otherwise specified							
SYMBOL	**TYPE**	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
V_{OH}	LVCMOS	Output High Voltage			2.4	V	I_{OH} = -1.0mA
V_{OL}	LVCMOS	Output Low Voltage	0.4			V	I_{OH} = 1.0mA
V_{IH}	LVTTL/ LVCMOS	Input High Voltage			2.0	V	
V_{IL}	LVTTL/ LVCMOS	Input Low Voltage	0.8			V	
I_{LEAK}	LVTTL/ LVCMOS	Input Leakage Current	-10		10	µA	V_{IN} = VDD_IO or V_{IN} = 0
I_{LEAK_PU}	LVTTL/ LVCMOS	Input Leakage Current with Pull-Up Resistor	38	52	65	µA	V_{IN} = 0
I_{LEAK_PD}	LVTTL/ LVCMOS	Input Leakage Current with Pull-Down Resistor	32	43	55	µA	V_{IN} = VDD_IO

NOTE: *All input control pins are LVCMOS and LVTTL compatible. All output control pins are LVCMOS compatible only.*

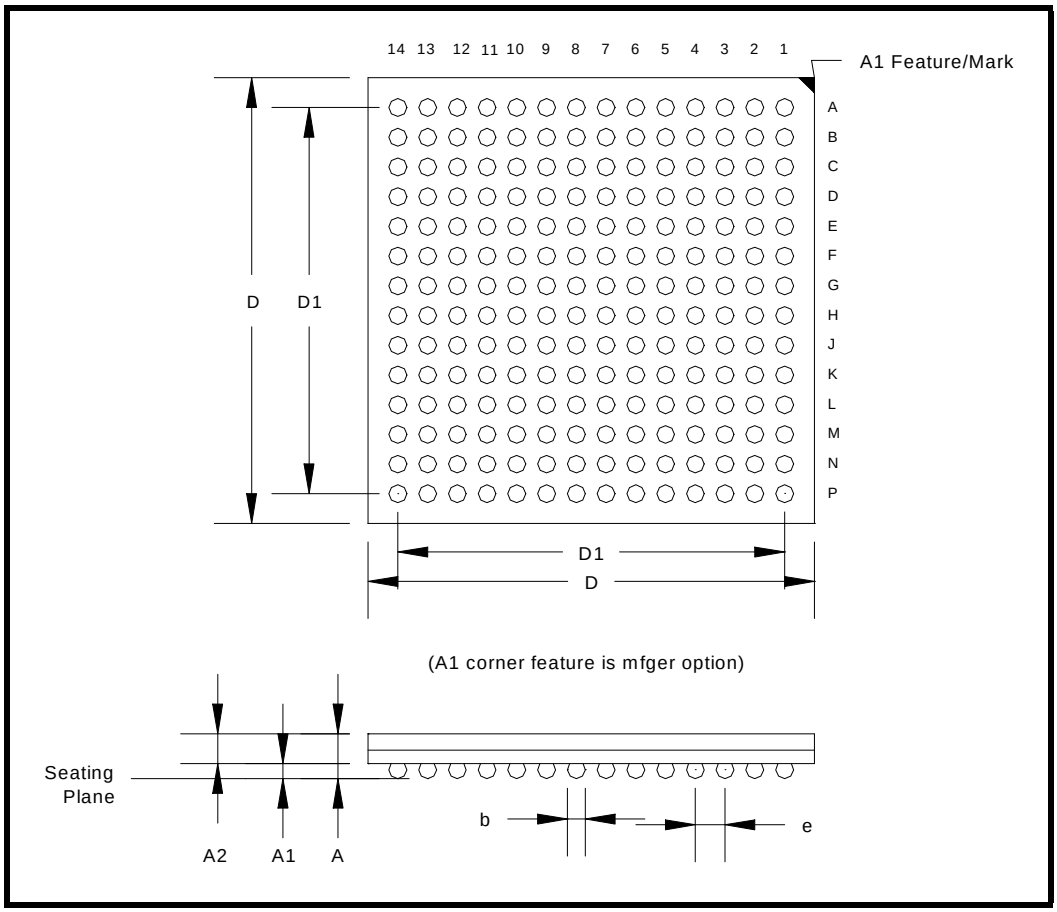
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L80IB	196 Shrink Thin Ball Grid Array (12.0 mm x 12.0 mm, STBGA)	-40°C to +85°C

196 SHRINK THIN BALL GRID ARRAY

(12.0 MM X 12.0 MM, STBGA)

REV. 1.00



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.067	1.35	1.70
A1	0.010	0.022	0.25	0.55
A2	0.033	0.052	0.85	1.31
D	0.465	0.480	11.80	12.20
D1	0.409 BSC		10.40 BSC	
b	0.018	0.022	0.45	0.55
e	0.031 BSC		0.80 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	October 2004	1st release of the XRT91L80 product brief
P1.0.1	October 2004	Fixed typos throughout document
P1.0.2	October 2004	Fixed typos throughout document
P1.0.3	January 2005	Added jitter transfer and tolerance mask test results and phase noise transmit jitter generation results, added $\overline{CS}$ de-assertion note on section 5.1, fixed register 0x02, 0x04, 0x05 microprocessor bit descriptions, updated pin descriptions, corrected 'falling edge' typo in section 3.6 to 'rising edge', and enhanced receive and transmit interface block diagrams.
P1.0.4	March 2005	Remove 'RXSEL' reference on the RXIP/N pin description. Minor edit in receive section 2.0. FIFO_RST corrected for active High in section 3.4. Removed unsupported note for transparent mode FIFO operation in section 3.3.
P1.0.5	April 2005	1.Design change: Renamed DISRD, TRIRXD, and TRITXCLKO16P/N to LOSDMUTE, DISRD, and TXCLKO16DIS respectively. Corrected and redefined pin definitions for LOSDMUTE, DISRD, and TXCLKO16DIS. 2.Renamed LOSEXT, REFFREQSEL, TXCLKIP/N, RXCLKP/N, RXD[3:0]P/N, RXCLK16P/N, LPTIME_JA, LPTIME_NO_JA, RXP/N to SDEXT, ALTFREQSEL, TXPCLKIP/N, RXPCLKOP/N, RXDO[3:0]P/N, RXCLKO16P/N, LOOPTM_JA, LOOPTM_NOJA, XRES1P/N respectively. 3.Updated STBGA pinout names to include above mentioned changes. 4.Corrected LOOPBW and RLOOPP pin descriptions. 5.Corrected RXDO[3:0]P/N description error from 'updated on rising edge' to 'updated on falling edge' of RXPCLKOP/N. 5.Updated and improved all pin list decriptions and formatted table headers. 6.Added JTAG input pin pull-up and pull-down descriptions. 7.Removed unsupported note for transparent mode FIFO operation in section 3.3 and enhanced and corrected FIFO reset operation description. 8.Moved FIFO Figure 11 from sect 3.6 to section 3.3. 9.Corrected Figure 13, "Loop Timing Mode Using an External Cleanup VCXO. 10.Corrected Loopback definition errors in Section 4.0. 11.Significantly enhanced Sec. 2.3 "LOS" to "External Signal Detection, Sec. 3.3 Transmit FIFO, and Sec. 3.6 CMU and Retimer, and Sec. 3.7 Loop timing and Clock Control. 12.Enhanced Transmit/Receive Parallel Data and Clock Input/Output timing diagram and tables. 13.Added CMU and CDR performace tables. 14.Added CML input swing characteristics table. 15.Added LOSD declaration polarity setting tables. 16.Added LVDS biasing resistor diagram. 17.Reformatted and Enhanced AC/DC electrical characteristics tables. 18.Change MHz to Mbps to reflect Parallel data I/O and Serial I/O more accurately. Corrected and enhanced PISO and SIPO diagrams. 19.Removed all reference to "differential limiting amplifier" and TXO2P/N pins. 20.Updated Microprocessor Register Bits and Descriptions to reflect changes. 21.Added Microprocessor Register Names. 22.Retouched 91L80 Block Diagram. 23.Changed OC-48 name to STS-48. 24.Minor edits and spelling and grammatical corrections.

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.6	July 2005	1.Updated CML input swing characteristics table. 2.Updated CDR and CMU jitter performance parameters. 3.Updated Intrinsic Transmit and Receive Phase Noise performance plots. 4.Updated AC/DC electrical characteristics tables.
P1.1.0	July 2005	1.Revision E silicon: CMOS Digital 1.8V power pins P13 and P14 changed to 3.3V. 2.Revision E silicon: ALTFREQSEL default clock selection changed to 155.52 MHz.

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Datasheet July 2005.