

W83194R-630



166MHZ CLOCK FOR SIS CHIPSET

1. GENERAL DESCRIPTION

The W83194R-630 is a Clock Synthesizer for SiS 540/630 chipset. W83194R-630 provides all clocks required for high-speed RISC or CISC microprocessor such as AMD, Cyrix, Intel Pentium, Pentium II and also provides 16 different frequencies of CPU clocks frequency setting. All clocks are externally selectable with smooth transitions. The W83194R-630 makes SDRAM in synchronous or asynchronous frequency with CPU clocks.

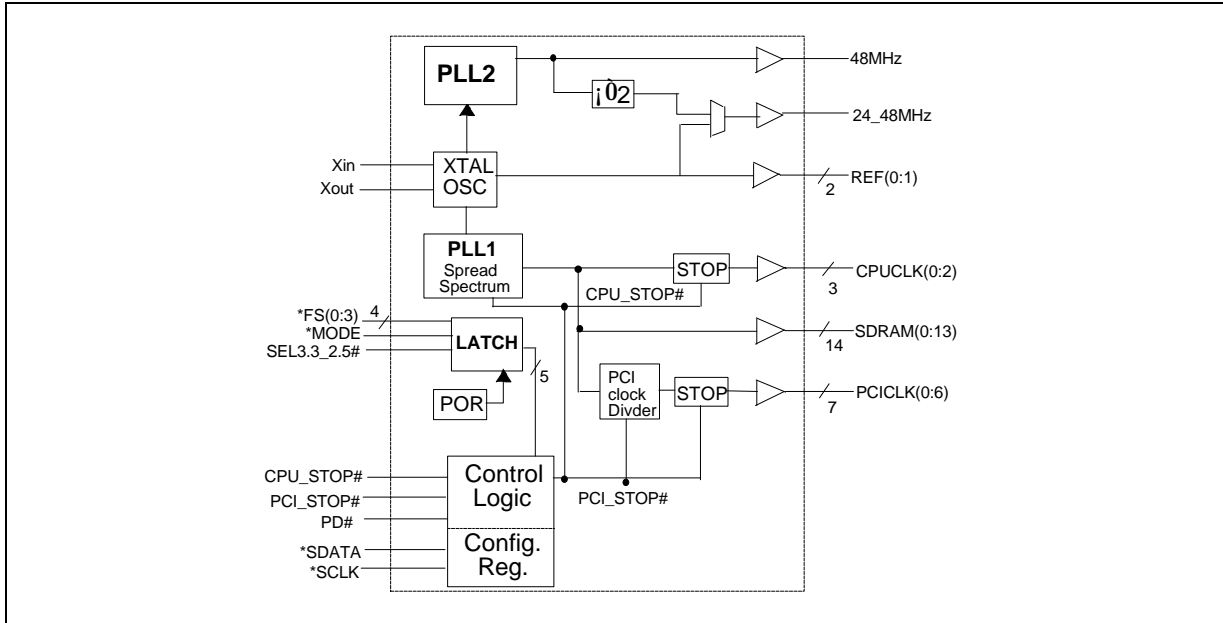
The W83194R-630 provides I²C serial bus interface to program the registers to enable or disable each clock outputs and W83194R-630 provides the 0.5%, 0.75% center type and 0~0.5% down type spread spectrum to reduce EMI.

The W83194R-630 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V/ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V/ns slew rate.

2. PRODUCT FEATURES

- Supports Pentium™, Pentium™ II, AMD and Cyrix CPUs with I²C.
- 3 CPU clocks
- 14 SDRAM clocks for 3 DIMMs
- 7 PCI synchronous clocks.
- Optional single or mixed supply:
(All Vdd = 3.3V) or (Other s Vdd = 3.3V, VddLCPU=2.5V)
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- SDRAM frequency synchronous or asynchronous to CPU clocks
- Smooth frequency switch with selections from 66 to 166mhz
- I²C 2-Wire serial interface and I²C read back
- **0.5%, 0.75%center type, 0~0.5% down type spread spectrum to reduce EMI**
- Programmable registers to enable/stop each output and select modes
(mode as Tri-state or Normal)
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 48-pin SSOP

3. BLOCK DIAGRAM



4. PIN CONFIGURATION

Vdd	1	48	REF1
REF0X2/ *FS3	2	47	VddLPCPU
Vss	3	46	CPUCLK_F
Xin	4	45	CPUCLK0
Xout	5	44	Vss
VddP	6	43	CPUCLK1
PCICLK_F/ *FS1	7	42	VddSD
PCICLK1/ *FS2	8	41	SDRAM12
PCICLK2/*MODE	9	40	SDRAM_F
Vss	10	39	Vss
PCICLK3	11	38	SDRAM11
PCICLK4	12	37	SDRAM 10
PCICLK5	13	36	VddSD
PCICLK6	14	35	SDRAM 9
VddP	15	34	SDRAM 8
Vss	16	33	Vss
SDRAM 0/CPU_STOP#	17	32	SDRAM 7
SDRAM 1/PCI_STOP#	18	31	SDRAM 6
VddSD	19	30	VddSD
SDRAM 2/PD#	20	29	SDRAM 5
SDRAM 3	21	28	SDRAM 4
Vss	22	27	VddSD
*SDATA	23	26	48MHz/*FS0
*SDCLK	24	25	24_48MHz/SEL2.5_3.3#



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5. PIN DESCRIPTION

- IN - Input
- OUT - Output
- I/O - Bi-directional Pin
- # - Active Low
- * - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

5.2 CPU, SDRAM, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK_F	46	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. VddLCPU is the supply voltage for these outputs. This pin will not be stopped by CPU_STOP#
CPUCLK [0:1]	45,43	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. VddLCPU is the supply voltage for these outputs.
SDRAM_F	40	OUT	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. This pin will not be stopped by CPU_STOP#
SDRAM0/CPU_STOP#	17	I/O	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. CPU_STOP# input pin when MODE=0.
SDRAM1/PCI_STOP#	18	I/O	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. PCI_STOP# input pin when MODE=0.
SDRAM2/PD#	20	I/O	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks. PD# input pin when MODE=0.
SDRAM[3:12]	21,28,29,31,32,34,35,37,38,41	OUT	SDRAM clock outputs which have syn. or asyn. frequencies as CPU clocks.
PCICLK_F/ *FS1	7	I/O	Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.



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			PCI free-running clock during normal operation.
PCICLK 1/ *FS2	8	I/O	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. PCI clock during normal operation.
PCICLK 2/ *MODE	9	I/O	Latched input for MODE at initial power up for input selection of CPU_STOP#, PCI_STOP# and PD#. When MODE=1, the above pins are SDRAM clock outputs. When MODE=0, the pins are inputs ACPI pins. PCI clock during normal operation.
PCICLK [3:6]	11,12,13,14	OUT	Low skew (< 250ps) PCI clock outputs.

5.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	23	I/O	Serial data of I ² C 2-wire control interface
*SDCLK	24	IN	Serial clock of I ² C 2-wire control interface

5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0X2 / *FS3	2	I/O	3.3V, 14.318MHz reference clock output . Internal 250kΩ pull-up. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
REF1	48	I/O	3.3V or 2.5V by VddLCP, 14.318MHz reference clock output.
24_48MHz/ SEL2.5_3.3#	25	I/O	SEL2.5_3.3# controls the Vdd of CPU. If logic 0 at power on, VddLCP=3.3V. If logic 1, VddLCP=2.5V. 24MHz or 48MHz selected by I2C for Super I/O.
48MHz / *FS0	26	I/O	Internal 250kΩ pull-up. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. 48MHz output for USB during normal operation.



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5.5 Power Pins

SYMBOL	PIN	FUNCTION
Vdd	1	Power supply for REF0 crystal and core logic.
VddLCPU	47	Power supply for REF1, CPUCLK_F and CPUCLK[0:1], either 2.5V or 3.3V.
VddP	6,15	Power supply for PCI outputs.
VddSD	19,27,30,36,42	Power supply for SDRAM and 48/24MHz outputs.
Vss	3,10,16,22,33,39,44	Circuit Ground.

6. FREQUENCY SELECTION BY HARDWARE

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz) IOAPIC
0	0	0	0	66.8	100.2	33.4	14.318
0	0	0	1	100.2	100.2	33.4	14.318
0	0	1	0	122	122	30.5	14.318
0	0	1	1	133.6	100.2	33.4	14.318
0	1	0	0	66.8	116.9	33.4	14.318
0	1	0	1	100.2	133.6	33.4	14.318
0	1	1	0	100.2	150.3	33.4	14.318
0	1	1	1	133.6	133.6	33.4	14.318
1	0	0	0	66.8	66.8	33.4	14.318
1	0	0	1	97	97	32.3	14.318
1	0	1	0	97	129.3	32.3	14.318
1	0	1	1	95.2	95.2	31.7	14.318
1	1	0	0	95.2	126.6	31.7	14.318
1	1	0	1	112	112	37.3	14.318
1	1	1	0	96.2	96.2	32.1	14.318
1	1	1	1	166	166	33.3	14.318

7. SEL3.3_2.5# BUFFER SELECTION

SEL3.3_2.5# (Pin 25) Input Level	CPU Operate at
1	VDDL CPU = 2.5V
0	VDDL CPU = 3.3V



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8. FUNCTION DESCRIPTION

8.1 2-WIRE I²C CONTROL INTERFACE

The clock generator is a slave I2C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194R-630 initializes with default register settings, and then it optional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I²C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I²C controller :

Clock Address A(6:0) & R/W	Ack	8 bits dummy Command code	Ack	8 bits dummy Byte count	Ack	Byte0,1,2... until Stop
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Set R/W to 1 when read back the data sequence is as follows, [1101 0011] :

Clock Address A(6:0) & R/W	Ack	Byte 0	Ack	Byte 1	Ack	Byte2, 3, 4... until Stop
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8.2 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2,) will be valid and acknowledged.

Frequency table by I2C

SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz) IOAPIC
0	0	0	0	66.8	100.2	33.4	14.318
0	0	0	1	100.2	100.2	33.4	14.318
0	0	1	0	122	122	30.5	14.318
0	0	1	1	133.6	100.2	33.4	14.318
0	1	0	0	66.8	116.9	33.4	14.318
0	1	0	1	100.2	133.6	33.4	14.318
0	1	1	0	100.2	150.3	33.4	14.318
0	1	1	1	133.6	133.6	33.4	14.318
1	0	0	0	66.8	66.8	33.4	14.318
1	0	0	1	97	97	32.3	14.318
1	0	1	0	97	129.3	32.3	14.318
1	0	1	1	95.2	95.2	31.7	14.318
1	1	0	0	95.2	126.6	31.7	14.318
1	1	0	1	112	112	37.3	14.318
1	1	1	0	96.2	96.2	32.1	14.318
1	1	1	1	166	166	33.3	14.318

8.2.1 Register 0: CPU Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	0 = $\pm 0.5\%$ Center type Spread Spectrum Modulation 1 = $\pm 0.75\%$ Center type Spread Spectrum Modulation
6	0	-	SSEL2 (for frequency table selection by software via I ² C)
5	0	-	SSEL1 (for frequency table selection by software via I ² C)
4	0	-	SSEL0 (for frequency table selection by software via I ² C)
3	0	-	0 = Selection by hardware 1 = Selection by software I ² C - Bit 2, 6:4
2	0	-	SSEL3 (for frequency table selection by software via I ² C)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs



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8.2.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	x	-	Latched FS2#
6	1	-	Reserved
5	1	-	0 = 0.5% down type spread, overrides Byte0-bit7. 1= Center type spread.
4	1	-	Reserved
3	1	43	CPUCLK2 (Active / Inactive)
2	1	45	CPUCLK1 (Active / Inactive)
1	1	46	CPUCLK0 (Active / Inactive)
0	1	-	Reserved

8.2.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	14	PCICLK6 (Active / Inactive)
5	1	13	PCICLK5 (Active / Inactive)
4	1	12	PCICLK4 (Active / Inactive)
3	1	11	PCICLK3 (Active / Inactive)
2	1	9	PCICLK2 (Active / Inactive)
1	1	8	PCICLK1 (Active / Inactive)
0	1	7	PCICLK0 (Active / Inactive)

8.2.4 Register 3: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	1 Pin25 24_48MHz = 24MHz 0 Pin25 24_48MHz = 48MHz
6	x	-	Latched FS0#
5	1	26	48MHz (Active / Inactive)
4	1	25	24-48MHz (Active / Inactive)
3	1	-	Reserved
2	1	-	Reserved
1	1	48	REF1 (Active / Inactive)
0	1	2	REF0X2 (Active / Inactive)



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8.2.5 Register 4: SDRAM Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	41	SDRAM13 (Active / Inactive)
6	1	40	SDRAM12 (Active / Inactive)
5	1	38	SDRAM11 (Active / Inactive)
4	1	37	SDRAM10 (Active / Inactive)
3	x	X	Latched FS1#
2	1	35	SDRAM9 (Active / Inactive)
1	x	X	Latched FS3#
0	1	34	SDRAM8 (Active / Inactive)

8.2.6 Register 5: SDRAM Register(1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	32	SDRAM7 (Active / Inactive)
6	1	31	SDRAM6 (Active / Inactive)
5	1	29	SDRAM5 (Active / Inactive)
4	1	28	SDRAM4 (Active / Inactive)
3	1	21	SDRAM3 (Active / Inactive)
2	1	20	SDRAM2 (Active / Inactive)
1	1	18	SDRAM1 (Active / Inactive)
0	1	17	SDRAM0 (Active / Inactive)

8.2.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	1	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	1	-	Winbond Chip ID

9.0 SPECIFICATIONS

9.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V _{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T _{STG}	Storage Temperature	- 65°C to + 150°C
T _B	Ambient Temperature	- 55°C to + 125°C
T _A	Operating Temperature	0°C to + 70°C

9.2 Electrical Characteristics---Input/Output

Vddq1=Vddq2 = Vddq3 = Vddq4 =3.3V, VddL1 =VddL2= 2.5V , T _A = 0° C to +70° C						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Low Voltage	V _{IL}	Vss-0.3		0.8	V _{dc}	
Input High Voltage	V _{IH}	2.0		Vdd+0.3	V _{dc}	
Input Low Current	I _{IL}	-5			μA	No pull-up resistors
Input Low Current	I _{IL}	-200			μA	Pull-up resistors
Input High Current	I _{IH}	-5		5	μA	
Input Capacitance	C _{IN}			5	pF	Logic inputs
	C _{OUT}			6	pF	Output capacitance
	C _{INX}	27		45	pF	Xin and Xout
Operating Supply Current	I _{dd3}			100	mA	CPU = 66.6 MHz PCI = 33.3 Mhz with load
Power Down Supply Current	I _{dd2}			600	μA	
Settling Time	T _s			3	mS	From first crossing to 1% target freq.



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Skew	$T_{\text{CPU-PCI}}$	1		4	nS	$V_T=1.5V$
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9.3 Electrical Characteristics of CPU Clock

$V_{\text{dd}}=2.5V \pm 5\%$; $C_L=10\text{-}20\text{pF}$

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R_{DSP}	13.5		30	Ohm	
Output Impedance	R_{DSN}	13.5		30	Ohm	
Output Low Voltage	V_{OL}			0.4	V	$I_{\text{OL}}=1\text{mA}$
Output High Voltage	V_{OH}	2.0			V	$I_{\text{OH}}=-1\text{mA}$
Output Low Current	I_{OL}	19			MA	
Output High Current	I_{OH}			-27	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{\text{RF(min)}}$	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{\text{RF(max)}}$			2.0	ns	20pF Load
Duty Cycle	Dt	45		55	%	$V_T=1.25V$
Skew	T_{SK}			175	ps	$V_T=1.25V$
Jitter	$T_{\text{SC-C}}$			250	ps	$V_T=1.25V$

9.4 Electrical Characteristics of SDRAM Clock

$V_{\text{dd}}=3.3V \pm 5\%$; $C_L=20\text{-}30\text{pF}$

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R_{DSP}	11		30	Ohm	
Output Impedance	R_{DSN}	11		30	Ohm	
Output Low Voltage	V_{OL}			0.45	V	$I_{\text{OL}}=1\text{mA}$
Output High Voltage	V_{OH}	2.4			V	$I_{\text{OH}}=-1\text{mA}$
Output Low Current	I_{OL}	35			MA	
Output High Current	I_{OH}			-45	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{\text{RF(min)}}$	0.5			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{\text{RF(max)}}$			2.0	ns	20pF Load
Duty Cycle	Dt	45		55	%	$V_T=1.5V$
Skew	T_{SK}			250	ps	$V_T=1.5V$
Jitter	$T_{\text{SC-C}}$			250	ps	$V_T=1.5V$

9.5 Electrical Characteristics of PCI Clock

V_{dd}=3.3V +/- 5%; C_L=10-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	15		55	Ohm	
Output Impedance	R _{DSN}	15		55	Ohm	
Output Low Voltage	V _{OL}			0.5	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} =-1mA
Output Low Current	I _{OL}	30			MA	
Output High Current	I _{OH}			-33	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T _{RF(min)}	0.5			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T _{RF(max)}			2.0	ns	20pF Load
Duty Cycle	Dt	45		55	%	V _T =1.5V
Skew	T _{SK}			500	ps	V _T =1.5V
Jitter	T _{SC-C}			500	ps	V _T =1.5V

9.6 Electrical Characteristics of 24/48MHz, REF Clock

V_{dd}=3.3V +/- 5%; C_L=20pF

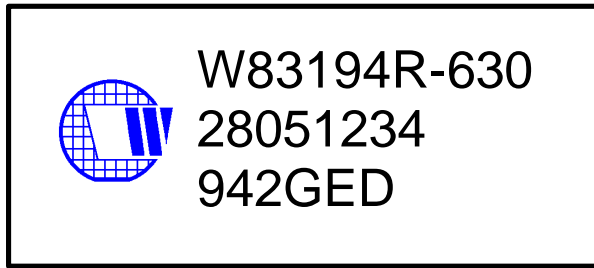
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	20		55	Ohm	
Output Impedance	R _{DSN}	20		55	Ohm	
Output Low Voltage	V _{OL}			0.4	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} =-1mA
Output Low Current	I _{OL}	10			MA	
Output High Current	I _{OH}			-23	MA	
RiseTime	T _R		1.8	4	ns	10pF Load
Fall Time	T _F		1.7	4	ns	20pF Load
Duty Cycle	Dt	45		55	%	V _T =1.5V
Skew	T _{SK}			500	ps	V _T =1.5V
Jitter	T _{SC-C}			1000	ps	V _T =1.5V

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10. ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194R-630	48 PIN SSOP	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194R-630

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 942 G E D

942: packages made in '99, week 42

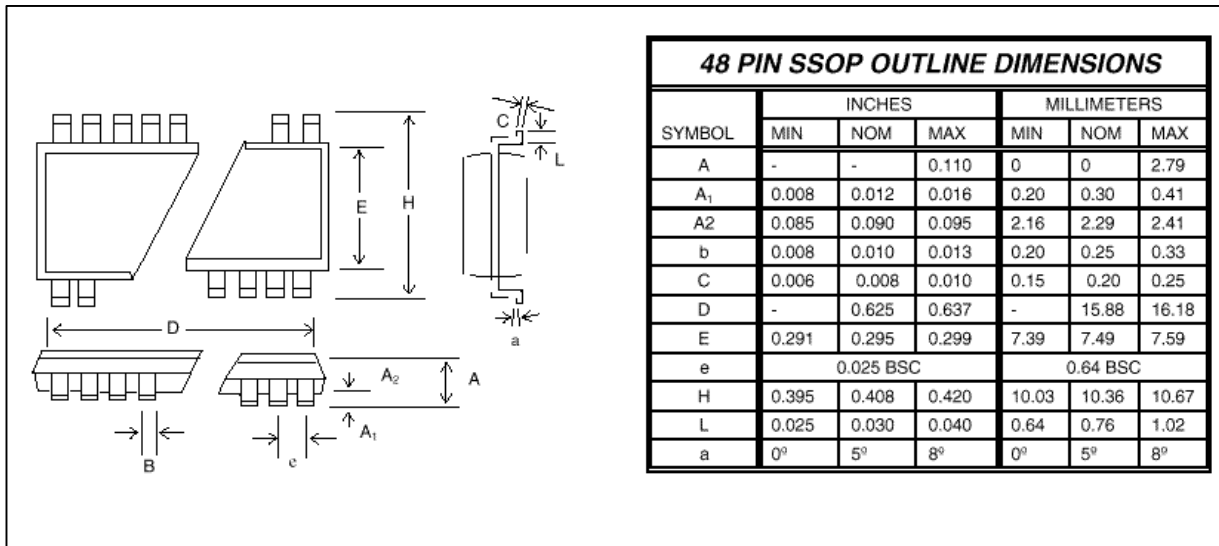
G: assembly house ID; O means OSE, G means GR

E: Internal use code

D: IC revision

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12. PACKAGE DRAWING AND DIMENSIONS



Headquarters
 No. 4, Creation Rd. III
 Science-Based Industrial Park
 Hsinchu, Taiwan
 TEL: 886-35-770066
 FAX: 886-35-789467
 www: <http://www.winbond.com.tw/>

Taipei Office
 11F, No. 115, Sec. 3, Min-Sheng East Rd.
 Taipei, Taiwan
 TEL: 886-2-7190505
 FAX: 886-2-7197502
 TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
 Rm. 803, World Trade Square, Tower II
 123 Hoi Bun Rd., Kwun Tong
 Kowloon, Hong Kong
 TEL: 852-27516023-7
 FAX: 852-27552064

**Winbond Electronics
 (North America) Corp.**
 2730 Orchard Parkway
 San Jose, CA 95134 U.S.A.
 TEL: 1-408-9436666
 FAX: 1-408-9436668

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