NEC
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CMOS-8
5-VOLT, 0.6-MICRON
CMOS GATE ARRAYS

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Description

NEC's 5-volt CMOS-8 family are high performance, sub-micron gate arrays, targeted for applications requiring extensive integration and high speeds. The device processing includes 0.6-micron (drawn) silicon-gate CMOS technology and two or three-layer metallization. This technology features channelless (sea-of-gates) architecture with an internal gate delay of 145 ps (F/O=1; L=0 mm). Output drive is variable up to 24 mA in one I/O slot. Slew-rate buffers are also available for low noise applications. High performance I/O macros including GTL and PCI are also supported.

The μPD65800 series of 5-volt devices consists of eleven masters, offered in densities of 11.7K gates to 233.3K gates. Usable gates range from 7K to 163.3K gates. They are ideal for applications such as engineering workstations, high-end PCs and LAN products, where extensive integration and high speed are primary design goals.

CMOS-8 products are fully supported by NEC's advanced ASIC design technology. NEC's OpenCAD® integration system lets the designer choose the most powerful design tools and services available. The CMOS-8 macro cell (block) library is upwardly compatible with the powerful CMOS-8L and CMOS-9 block libraries.

Figure 1. Sample CMOS-8 Packages

Optionally these devices can be powered at 3.3V ± 0.3V. Also available are 5V libraries characterized at commercial conditions of 5V ± 5% and T_j = 0-100°C (CMOS-8T).

NEC offers advanced packaging solutions including BGA, PQFP, and TQFP. These packages give CMOS-8 devices the performance edge in high-integration applications.

Table 1. CMOS-8 Series Features and Benefits

CMOS-8 Series Features	CMOS-8 Series Benefits
• 0.6-micron (drawn), 2 and 3 level metal CMOS sea-of-gates	• Fastest, lowest power 5V technology
• 11 base arrays with raw gates from 12K to 233K	• Variety of arrays provide optimal fit for required gates
• Utilization rates of 60% for 2LM, 75% for 3LM	• Highest % for 5V gate array – allows small die size
• Two rows of fine-pitch, staggered I/O pads	• Provides smallest die size for high pin count needs
• Pad counts from 172 to 676 pads	• Delivers high pad counts for pad-intensive designs
• CMOS, TTL buffers at 3, 6, 9, 12, 18, 24 mA	• Provides buffers for standard interface types
• Slew-rate-controlled buffers	• Delivers low noise interface
• Power consumption of 1.47 μW/MHz/gate	• Lowest power of any 5V gate array
• High-speed RAM compiler	• Optimize RAM area for user-defined configuration
• TQFP and LQFP packages	• Thin packages for portable and PCMCIA applications
• BGA packages in pin counts from 169 to 672	• Delivers high pin count, high yield BGA packages
• Supported on NEC's OpenCAD® system	• Integrated system of 3rd party and proprietary tools

* OpenCAD is a registered trademark of NEC Electronics Inc.

Circuit Architecture

CMOS-8 products are built with NEC's 0.6-micron (drawn) channelless gate array architecture. As shown in figure 2, CMOS gate array chips are divided into I/O and internal cell areas. The I/O cell area contains input and output buffers that isolate the internal cells from high-energy external signals. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel MOS transistors, as well as four additional n-channel MOS transistors for compact RAM design.

Output Slew-Rate Selection

Fast rise and fall times of CMOS output buffers can cause system noise and signal overshoot. When an unterminated line is being driven by a buffer, the maximum line length is determined by the rise and fall time of the output buffers and the round-trip signal delay of the line.

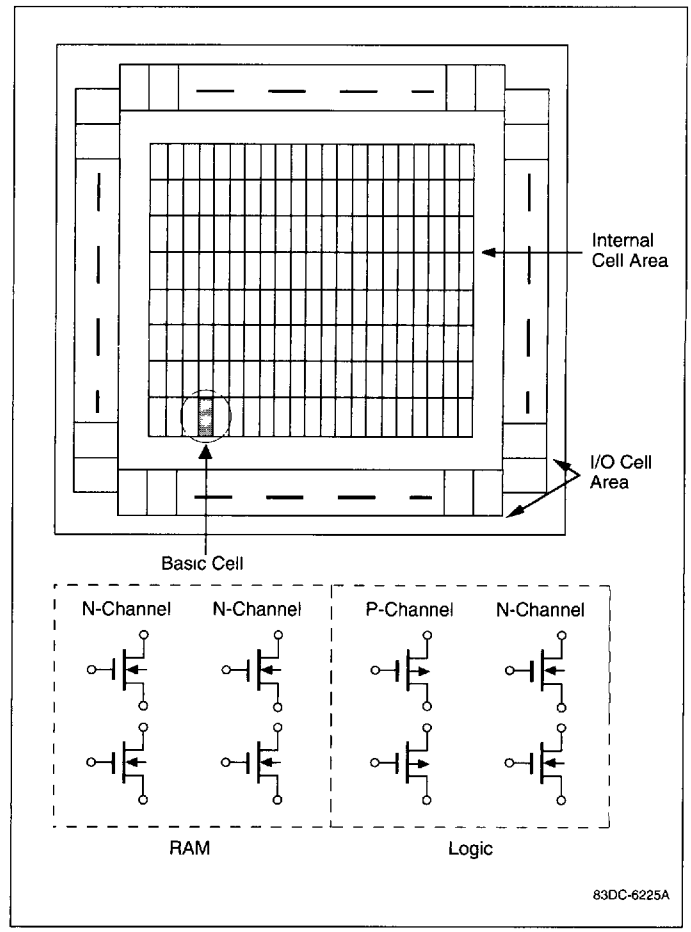
As a general rule, the round-trip delay of the line should not exceed the rise or fall time of the driving signal. Transmission lines that are longer than those determined by this rule can degrade system performance due to reflections and ringing. One benefit of slew-rate output buffers is that longer interconnections on a PC board and routing flexibility are possible.

Gate Array Sizes

Device	Available Gates	Usable Gates	Total Pads	Metal Layers
μPD65800	11,712	7,027	172	2
μPD65801	21,504	12,902	228	2
μPD65802	32,000	19,200	268	2
μPD65803	42,688	25,612	308	2
μPD65804	42,688	32,016	308	3
μPD65806	58,752	44,064	356	3
μPD65808	82,432	61,824	420	3
μPD65810	103,680	77,760	468	3
μPD65811	138,776	104,087	524	3
μPD65812	176,720	132,540	588	3
μPD65813	233,280	174,960	676	3

Actual gate utilitization varies depending on circuit implementation. Utilization is 75% for three-layer metal; 60% for two-layer metal. Depending on package and circuit specification, some pads are used for V_{DD} and GND and are not available as signal pads.

Figure 2. Chip Layout and Internal Cell Configuration



ASIC designers, therefore, can slow down the output edge-rate by using a slew-rate output buffer and thus accommodate longer transmission lines on PC boards.

Slew-rate buffers also inject less noise into the internal power and ground busses of the device, than their non-slew-rate counterparts. As a consequence, slew-rate buffers require fewer power/ground pairs for simultaneous switching outputs.

Publications

This data sheet contains specifications, package information, and operational data for the CMOS-8 gate array families. Additional design information is available in NEC's CMOS-8 Block Library and CMOS-8 Design Manual. Contact your local NEC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +6.0 V
Input/output voltage, V_I / V_O	–0.5 V to V_{DD} + 0.5 V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note:
(1) Values include package pin capacitance.

Power Consumption

Description	Limits	Unit
Internal cell	1.47	μW/MHz
Input block	32	μW/MHz
Output block	405	μW/MHz

Recommended Operating Conditions

Parameter	Symbol	CMOS Level		TTL Level		3.3V Level		5V PCI Level		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	3.0	3.6	4.5	5.5	V
Ambient temperature	T_A	–40	+85	0	+70	–40	+85	–40	+125	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	0	0.8	0	0.2 V_{DD}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	2.2	V_{DD}	0.8 V_{DD}	V_{DD}	2.0	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	0	200	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	0	200 ns	—	—	ms
Positive Schmitt-trigger voltage	V_P	1.8	4.0	1.2	2.4	1.28	2.58	—	—	V
Negative Schmitt-trigger voltage	V_N	0.6	3.1	0.6	1.8	0.48	2.0	—	—	V
Hysteresis voltage	V_H	0.3	1.5	0.3	1.5	0.1	0.93	—	—	V

AC Characteristics

$V_{DD} = 5$ V ± 10%; T_J = –40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}			274	MHz	D-F/F; F/O = 1; L = 0 mm
Delay time, 2-input NAND gate						
Standard gate (F302)	t_{PD}		145		ps	F/O = 1; L = 0 mm
			260		ps	F/O = 2; L = 1 mm
Low power gate (L302)	t_{PD}		174		ps	F/O = 1; L = 0 mm
			388		ps	F/O = 2; L = 1 mm
Delay time, buffer						
Input (FI01)	t_{PD}		360		ps	F/O = 2; L = 2 mm
Output (FO01 - 24mA)	t_{PD}		173		ps	C_L = 15 pF
Output rise time (FO01)	t_R		1.80		ns	C_L = 15 pF
Output fall time (FO01)	t_F		1.63		ns	C_L = 15 pF

DC Characteristics

V_{DD} = 5 V ± 10%; T_J = −40 to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (Note 1)	I_L		1.0	200	µA	$V_I = V_{DD}$ or GND
Input leakage current (Note 2)						
Regular	I_I		$\pm10^{-5}$	±10	µA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I	−45.0	−131	−320.0	µA	V_I = GND
5 kΩ pull-up	I_I	−0.35	−1.0	−2.20	mA	V_I = GND
50 kΩ pull-down	I_I	45	131	320	µA	$V_I = V_{DD}$
Off-state output leakage current	I_{OZ}			±10	µA	$V_O = V_{DD}$ or GND
Input clamp voltage	V_{IC}	−1.2			V	I_I = 18 mA
Output short circuit current (Note 3)	I_{OS}			−250	mA	V_O = 0 V
Low-level output current (CMOS)						
3 mA (Note 4)	I_{OL}	3		10	mA	V_{OL} = 0.4 V
6 mA (Note 4)	I_{OL}	6		15	mA	V_{OL} = 0.4 V
9 mA (Note 4)	I_{OL}	9		20	mA	V_{OL} = 0.4 V
12 mA (Note 4)	I_{OL}	12		30	mA	V_{OL} = 0.4 V
18 mA (Note 4)	I_{OL}	18		40	mA	V_{OL} = 0.4 V
24 mA (Note 4)	I_{OL}	24		60	mA	V_{OL} = 0.4 V
High-level output current (CMOS)						
3 mA (Note 4)	I_{OH}	−1.5			mA	$V_{OH} = V_{DD}$ − 0.4 V
6 mA (Note 4)	I_{OH}	−3			mA	$V_{OH} = V_{DD}$ − 0.4 V
9 mA (Note 4)	I_{OH}	−4.5			mA	$V_{OH} = V_{DD}$ − 0.4 V
12 mA (Note 4)	I_{OH}	−6			mA	$V_{OH} = V_{DD}$ − 0.4 V
18 mA (Note 4)	I_{OH}	−9			mA	$V_{OH} = V_{DD}$ − 0.4 V
24 mA (Note 4)	I_{OH}	−12			mA	$V_{OH} = V_{DD}$ − 0.4 V
Low-level output current (TTL)						
9 mA (Note 5)	I_{OL}	9			mA	V_{OL} = 0.4 V
18 mA (Note 5)	I_{OL}	18			mA	V_{OL} = 0.4 V
High-level output current (TTL)						
9 mA (Note 5)	I_{OH}			−0.5	mA	V_{OH} = 2.4 V
18 mA (Note 5)	I_{OH}			−1.0	mA	V_{OH} = 2.4 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage (CMOS) (Note 4)	V_{OH}	V_{DD}−0.1			V	I_{OH} = 0 mA
High-level output voltage (TTL) (Note 5)	V_{OH}	2.6	3.4		V	I_{OH} = 0 mA

Notes:

(1) The static current consumption increases if an I/O block with on-chip pull-up/pull-down resistor or an oscillator is used. Contact an NEC ASIC Design Center for assistance in calculation.

(2) Leakage current is limited by tester capabilities. The specification listed represents this measurement limitation. Actual values will be significantly lower.

(3) Rating is for only one output operating in this mode for less than 1 second.

(4) CMOS-level output buffer (V_{DD} = 5 V ± 10%, T_A = −40 to +85°C).

(5) TTL-level output buffer (V_{DD} = 5 V ± 5%, T_A = 0 to +70°C).