HYM532410A M-Series

4M x 32-bit CMOS DRAM MODULE

DESCRIPTION

The HYM532410A is a 4M x 32-bit Fast page mode CMOS DRAM module consisting of eight HY5117400A in 24/26 pin SOJ or TSOPII on a 72 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.
The HYM532410AM/ASLM/ATM/ASLTM are Tin-Lead plated and HYM532410AMG/ASLMG/ATMG/ASLTMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- **Low power dissipation**
  Max. self-refresh 13.2mW (SL-part)
  Max. battery back-up 22.0mW (SL-part)
  Max. CMOS standby 17.6mW (SL-part)
  44.0mW
  Max. TTL standby 88.0mW
  Max. operating

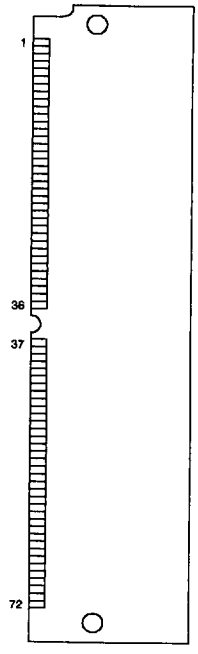
Speed	Power
50	6.38W
60	5.28W
70	4.40W

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tPC
50	50ns	15ns	40ns
60	60ns	18ns	45ns
70	70ns	20ns	50ns

- **Fast page mode operation**
- **$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, $\overline{\text{RAS}}$-only, Hidden refresh and Self-Refresh**
- **2048 refresh cycles / 256ms (SL-part)**
  2048 refresh cycles / 32ms

PIN CONNECTION



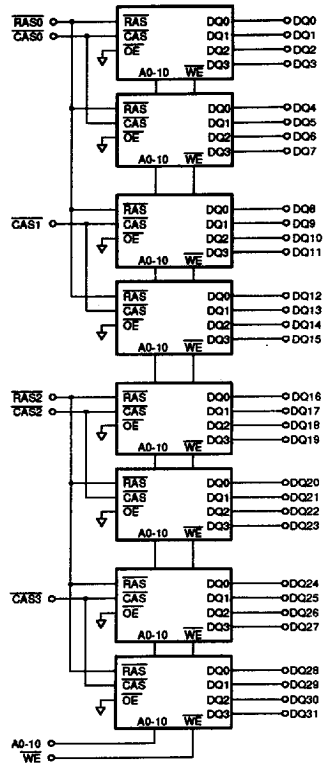
PIN DESCRIPTION

$\overline{\text{RAS0}}$	Row Address Strobe
$\overline{\text{CAS0}}$-$\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
A0-A10	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ17	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ18	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ19	45	NC
10	Vcc	46	NC
11	PD5	47	$\overline{WE}$
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	Vcc	66	PD EDO
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	PD REF.
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PIN

PIN	-50	-60	-70
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	Vss	NC	Vss
PD4	Vss	NC	NC
PD5	NC	NC	NC.

PIN	PD EDO	PD REF.
Vss	-	-
NC	Fast Page	Standard

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	–1.0 to 7.0	V
V_{CC}	Voltage on Vcc Relative to Vss	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	8.16	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	Vcc+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$+ 1.0, All other pins not under test= V_{SS}		-80	80	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	Vcc Supply Current, Operating	t_{RC}= t_{RC} (min.)	50 60 70	- - -	1160 960 800	mA	1,2,3
I_{CC2}	Vcc Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}		-	16	mA	
I_{CC3}	Vcc Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	50 60 70	- - -	1160 960 800	mA	1,3
I_{CC4}	Vcc Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	50 60 70	- - -	720 640 560	mA	1,2,3
I_{CC5}	Vcc Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ Vcc–0.2V	 SL-part	- -	8 3.2	mA	 5
I_{CC6}	Vcc Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	50 60 70	- - -	1160 960 800	mA	1,3
I_{CC7}	Vcc Supply Current, Battery Back Up (SL-part only)	t_{RC}= 125µs, $\overline{CAS}$= CBR cycling or 0.2V $\overline{WE}$= Vcc–0.2V A0-A10= Vcc–0.2V or 0.2V DQ0-DQ31= Vcc–0.2V, 0.2V, or open	$t_{RAS} \le$ 300ns $t_{RAS} \le$ 1µs	-	2.4 4.0	mA	1,4,5
I_{CC8}	Vcc Supply Current Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V $\overline{OE}$ & $\overline{WE}$ & A0-A10= Vcc-0.2V or 0.2V DQ0-DQ31= Vcc - 0.2V, 0.2V or open			2.4	mA	5
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
3. Icc is specified as average current. For I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$= V_{IL}. For I_{CC4}, address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only t_{RAS}(max.)= 1µs is applied to refresh of battery backup but t_{RAS}(max.)= 10µs is applied to normal functional operation.
5. I_{CC5}(max.)= 3.2mA, I_{CC7} and I_{CC8} are applied to SL-part only (HYM532410ASLM/ASLTM/ASLMG/ASLTMG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532410A M-series						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tRHCP	Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	5,10,11
6	tCAC	Access Time from $\overline{CAS}$	-	13	-	15	-	18	ns	5,10
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	5,10,11
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	ns	5
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	5
10	tOFF	Output Buffer Turn-off Delay	0	10	0	13	0	15	ns	6
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4
12	tRP	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	13	-	15	-	18	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	50	-	60	-	70	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	13	10K	15	10K	18	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	37	20	45	20	52	ns	10
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	11
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	8	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	50	-	55	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	7
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	7
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	45	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	13	-	15	-	18	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	13	-	15	-	18	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	8
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	8
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	50	-	50	-	55	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0		0	-	0	-	ns	9

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM532410A M-Series						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	
44	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRASS	$\overline{RAS}$ Pulse (Self Refresh)	100	-	100	-	100	-	ns	
47	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh)	90	-	110	-	130	-	ns	
48	tCHS	$\overline{CAS}$ Hold Time from $\overline{RAS}$ (Self Refresh)	-50	-	-50	-	-50	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS}$= Vss during power-up, the HYM532410A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition time is measured between VIH and VIL and assumed to be 5ns for all inputs.
4. Refer to the HY5117400A and data sheet for detailed information.
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. tOFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
9. tWCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If tWCS≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
10. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
11. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
12. tREF(max.)= 256ms is applied to SL-part only (HYM532410ASLM/ASLTM/ASLMG/ASLTMG).

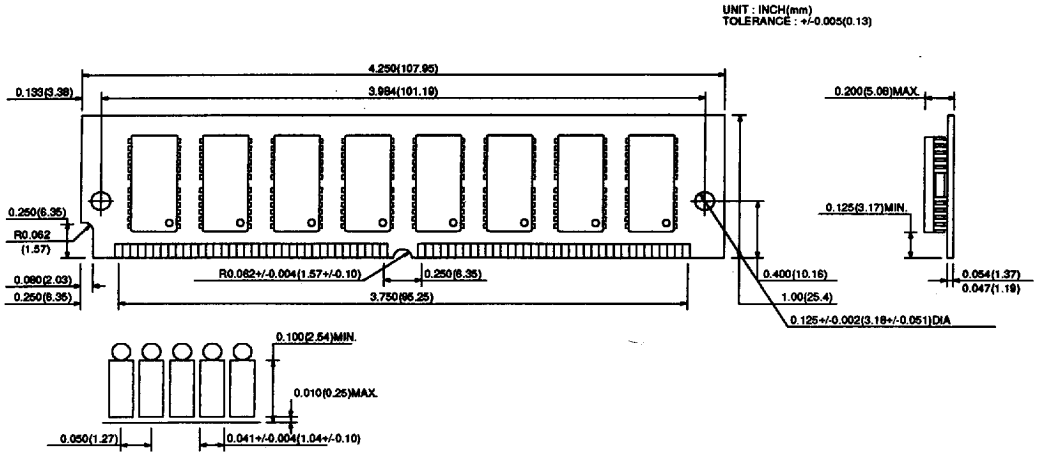
CAPACITANCE

(TA= 25°C, Vcc= 5V± 10%, Vss= 0V, f= 1MHz, unless otherwise noted.)

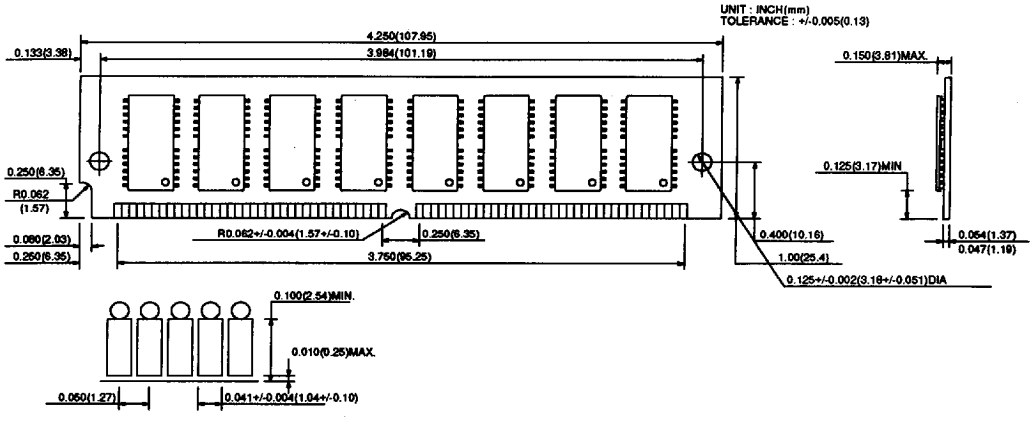
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	64	pF
CIN2	Input Capacitance ($\overline{WE}$)	-	70	pF
CIN3	Input Capacitance ($\overline{RAS0}$)	-	80	pF
CIN4	Input Capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	-	46	pF
CDQ	Data Input/Output Capacitance (DQ0-31)	-	29	pF

PACKAGE INFORMATION

72 pin Single In-line Memory (M ; Tin-Lead plated, MG ; Gold plated)
HYM532410A/AL (SOJ Mounted)



HYM532410AT/ALT (TSOPII Mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532410AM	50/60/70		SIMM	Tin-Lead
HYM532410ASLM	50/60/70	SL-part	SIMM	Tin-Lead
HYM532410ATM	50/60/70		SIMM	Tin-Lead
HYM532410ASLTM	50/60/70	SL-part	SIMM	Tin-Lead
HYM532410AMG	50/60/70		SIMM	Gold
HYM532410ASLMG	50/60/70	SL-part	SIMM	Gold
HYM532410ATMG	50/60/70		SIMM	Gold
HYM532410ASLTMG	50/60/70	SL-part	SIMM	Gold