1st Generation

DESCRIPTION

This family is a 64M bit dynamic RAM organized 16,777,216 x 4-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode offers high speed of random access memory within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60 or 70ns) and refresh cycle(8K ref. or 4K ref.) and package(SOJ or TSOP-II) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Fast Page operation
- Read-modify-write capability
- Multi-bit parallel test capability
- LVTTL(3.3V) compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- JEDEC standard pinout
  32-pin plastic SOJ/TSOP-II (400mil)
- Single power supply of 3.3 ± 0.3V
- Early write or output enable controlled write

- Max. Active power dissipation

Speed	8K refresh	4K refresh
60	396mW	540mW
70	324mW	468mW

- Fast access time and cycle time

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Refresh cycle

Part number	Refresh	Normal	L-part
HY51V64400[1)]	8K	64ms	128ms
HY51V65400[2)]	4K		

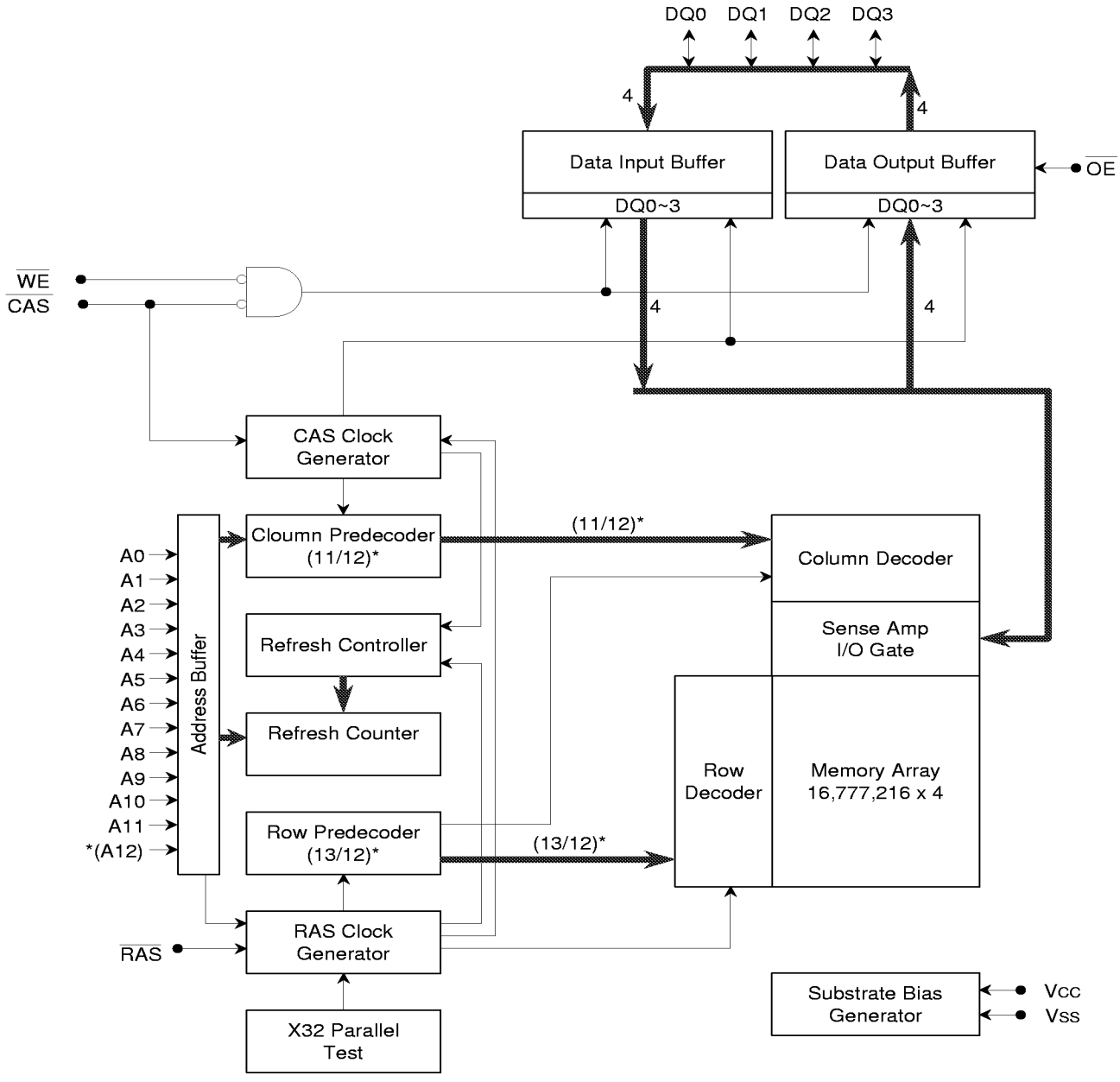
1) Normal read / write, /RAS only refresh : 8K cycles / 64ms
   /CAS-before-/RAS, Hidden refresh : 4K cycles / 64ms
2) Normal read / write, /RAS only refresh : 4K cycles / 64ms
   /CAS-before-/RAS, Hidden refresh : 4K cycles / 64ms

ORDERING INFORMATION

Part Name	Refresh	Power	Package
HY51V64400JC/TC	8K		32Pin SOJ/TSOP-II
HY51V64400LJC/TC	8K	L-part	32Pin SOJ/TSOP-II
HY51V64400SLJC/TC	8K	*SL-part	32Pin SOJ/TSOP-II
HY51V65400JC/TC	4K		32Pin SOJ/TSOP-II
HY51V65400LJC/TC	4K	L-part	32Pin SOJ/TSOP-II
HY51V65400SLJC/TC	4K	*SL-part	32Pin SOJ/TSOP-II

*SL : Self refresh with low power.

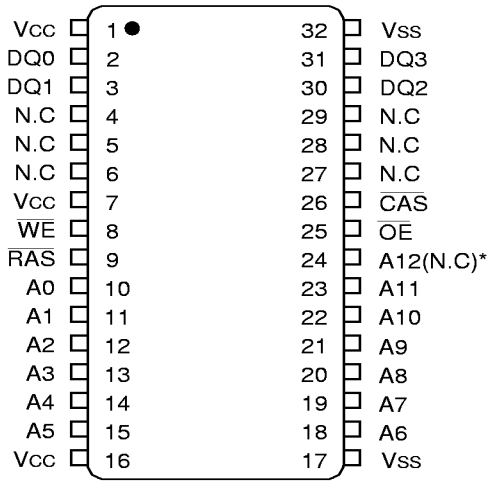
FUNCTIONAL BLOCK DIAGRAM



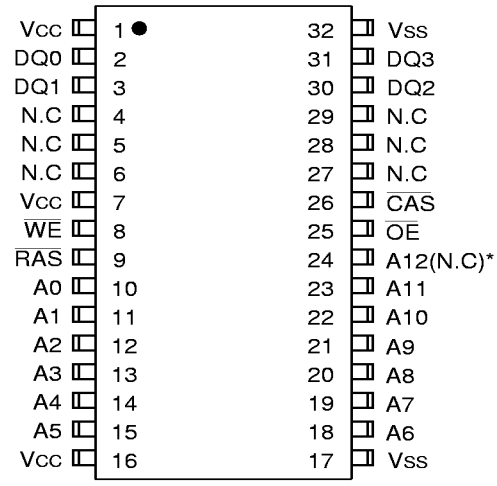
*(A12) for 8K refresh part

(8K Refresh / 4K Refresh)*

PIN CONFIGURATION (Top Side)



32Pin Plastic SOJ (400mil)



32Pin Plastic TSOP-II (400mil)

A12(N.C)* : For 4K refresh product

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A12	Address Input (8K Refresh Product)
A0~A11	Address Input (4K Refresh Product)
DQ0~DQ3	Data In/Out
Vcc	Power (3.3V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings could adversely affect device reliability and cause permanent damage.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3[1)]	V
V_{IL}	Input Low Voltage	-0.3[2)]	-	0.8	V

Note : All voltages are referenced to V_{SS}.

1) 6.0V at pulse width 10ns which is measured at V_{CC}.

2) -1.0V at pulse width 10ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Min	Max	Unit
I_{LI}	Input Leakage Current (Any input)	$V_{SS} \le V_{IN} \le V_{CC}$ + 0.3 All other pins not under test = V_{SS}	-5	5	µA
I_{LO}	Output Leakage Current (Any input)	$V_{SS} \le V_{OUT} \le V_{CC}$ /RAS&/CAS at V_{IH}	-5	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -2.0mA	2.4	-	V

DC CHARACTERISTICS

(T_A = 0°C to 70°C , V_{CC} = 3.3 ± 0.3V , V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max. Current		Unit
				8K refresh	4K refresh	
I_{CC1}	Operating Current	/RAS, /CAS Cycling t_{RC} = $t_{RC(min.)}$	60 70	110 90	150 130	mA
I_{CC2}	LVTTL Standby Current	/RAS, /CAS ≥ V_{IH} Other inputs ≥ V_{SS}		1	1	mA
I_{CC3}	/RAS-only Refresh Current	/RAS Cycling,/CAS = V_{IH} t_{RC} = $t_{RC(min.)}$	60 70	110 90	150 130	mA
I_{CC4}	Fast Page mode Current	/CAS Cycling, /RAS = V_{IL} t_{PC} = $t_{PC(min.)}$	60 70	80 70	80 70	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V_{CC} - 0.2V	 L-part	500 300	500 300	µA
I_{CC6}	/CAS-before-/RAS Refresh Current	t_{RC} = $t_{RC(min.)}$	60 70	150 130	150 130	mA
I_{CC7}	Battery Back-up Current (L-part)	V_{IH} = V_{CC} - 0.2V, V_{IL} = 0.2V /CAS = CBR cycling or 0.2V /OE&/WE = V_{IH} = V_{CC} - 0.2V Address = Don't care, t_{RC} = 31.25uS DQ0~DQ15 = Open, t_{RAS} ≤ 300ns		700	700	µA
I_{CC8}	Self Refresh Current (L-part)	/RAS&/CAS = 0.2V Other pins are same as I_{CC7}		700	700	µA

Note

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(t_{RC} and t_{PC}).
2. Specified values are obtained with output unloaded.
3. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} withen one Fast Page mode cycle time t_{PC}.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 3.3 ± 0.3V , V_{SS} = 0V, unless otherwise noted.)

#	Symbol	Parameter	60ns		70ns		Unit	Note
			Min	Max	Min	Max		
1	tRC	Random read or write cycle time	110	-	130	-	ns	
2	tRWC	Read-modify-write cycle time	140	-	170	-	ns	
3	tPC	Fast Page mode cycle time	40	-	45	-	ns	
4	tPRWC	Fast Page mode read-modify-write cycle time	70	-	80	-	ns	
5	tRAC	Access time from /RAS	-	60	-	70	ns	4,5,9,10
6	tCAC	Access time from /CAS	-	15	-	20	ns	4,5,9
7	tAA	Access time from column address	-	30	-	35	ns	4,5,10
8	tCPA	Access time from /CAS precharge	-	35	-	40	ns	4
9	tCLZ	/CAS to output low impedance	0	-	0	-	ns	3
10	tOFF	Output buffer turn-off delay from /CAS	0	13	0	15	ns	
11	tT	Transition time(rise and fall)	2	50	2	50	ns	4
12	tRP	/RAS precharge time	40	-	50	-	ns	
13	tRAS	/RAS pulse width	60	10K	70	10K	ns	
14	tRASP	/RAS pulse width(Fast Page mode)	60	100K	70	100K	ns	
15	tRSH	/RAS hold time	15	-	20	-	ns	
16	tCSH	/CAS hold time	55	-	65	-	ns	
17	tCAS	/CAS pulse width	15	10K	20	10K	ns	
18	tRCD	/RAS to /CAS delay time	20	45	20	50	ns	9
19	tRAD	/RAS to column address delay time	15	30	15	35	ns	10
20	tCRP	/CAS to /RAS precharge time	5	-	5	-	ns	
21	tCP	/CAS precharge time	10	-	10	-	ns	14
22	tASR	Row address set-up time	0	-	0	-	ns	
23	tRAH	Row address hold time	10	-	10	-	ns	
24	tASC	Column address set-up time	0	-	0	-	ns	13
25	tCAH	Column address hold time	10	-	15	-	ns	13
26	tAR	Column address hold time from /RAS	50	-	55	-	ns	
27	tRAL	Column address to /RAS lead time	30	-	35	-	ns	
28	tRCS	Read command set-up time	0	-	0	-	ns	
29	tRCH	Read command hold time referenced to /CAS	0	-	0	-	ns	6
30	tRRH	Read command hold time referenced to /RAS	0	-	0	-	ns	6
31	tWCH	Write command hold time	10	-	10	-	ns	

AC CHARACTERISTICS

Continued

#	Symbol	Parameter	60ns		70ns		Unit	Note
			Min	Max	Min	Max		
32	tWCR	Write command hold time from /RAS	45	-	50	-	ns	
33	tWP	Write command pulse width	10	-	10	-	ns	
34	tRWL	Write command to /RAS lead time	15	-	20	-	ns	
35	tCWL	Write command to /CAS lead time	10	-	15	-	ns	16
36	tDS	Data-in set-up time	0	-	0	-	ns	7,19
37	tDH	Data-in hold time	10	-	10	-	ns	7,19
38	tDHR	Data-in hold time referenced to /RAS	45	-	50	-	ns	
39	tREF	Refresh period(8192 cycles)	-	64	-	64	ms	11,12
		Refresh period(4096 cycles)	-	64	-	64	ms	11
		Refresh period(SL-part)	-	128	-	128	ms	11,12
40	tWCS	Write command set-up time	0	-	0	-	ns	8
41	tCWD	/CAS to /WE delay time	35	-	45	-	ns	8,15
42	tRWD	/RAS to /WE delay time	80	-	95	-	ns	8
43	tAWD	Column address to /WE delay time	50	-	60	-	ns	8
44	tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	ns	17
45	tCHR	/CAS hold time(CBR cycle)	10	-	10	-	ns	18
46	tRPC	/RAS to /CAS precharge time	5	-	5	-	ns	
47	tCPT	/CAS precharge time(CBR counter test)	30	-	35	-	ns	
48	tROH	/RAS hold time referenced to /OE	0	-	0	-	ns	
49	tOEA	/OE access time	-	15	-	20	ns	
50	tOED	/OE to data delay	15	-	20	-	ns	
51	tOEZ	Output buffer turn-off delay time from /OE	0	15	0	15	ns	6
52	tOEH	/OE command hold time	15	-	15	-	ns	
53	tCPWD	/WE delay time from /CAS precharge	55	-	65	-	ns	8
54	tRHCP	/RAS hold time from /CAS precharge	35	-	40	-	ns	
55	tWRP	/WE to /RAS precharge time(CBR cycle)	10	-	10	-	ns	
56	tWRH	/WE to /RAS hold time(CBR cycle)	10	-	10	-	ns	
57	tWTS	Write command set-up time(test mode in)	10	-	10	-	ns	
58	tWTH	Write command hold time(test mode in)	10	-	10	-	ns	
59	tRASS	/RAS pulse width(self refresh)	100K	-	100K	-	ns	
60	tRPS	/RAS precharge time(self refresh)	110	-	130	-	ns	
61	tCHS	/CAS hold time(self refresh)	-50	-	-50	-	ns	

TEST MODE

#	Symbol	Parameter	60ns		70ns		Unit	Note
			Min	Max	Min	Max		
1	tRC	Random read or write cycle time	115	-	135	-	ns	
2	tRWC	Read-modify-write cycle time	145	-	175	-	ns	
3	tPC	Fast Page mode cycle time	40	-	45	-	ns	
4	tHPRWC	Fast Page mode read-modify-write cycle time	75	-	85	-	ns	
5	tRAC	Access time from /RAS	-	65	-	75	ns	4,5,9,10
6	tCAC	Access time from /CAS	-	20	-	25	ns	4,5,9
7	tAA	Access time from column address	-	35	-	40	ns	4,5,10
8	tCPA	Access time from /CAS precharge	-	40	-	45	ns	4
13	tRAS	/RAS pulse width	65	10K	75	10K	ns	
14	tRASP	/RAS pulse width(Fast Page mode)	65	100K	75	100K	ns	
15	tRSH	/RAS hold time	20	-	25	-	ns	4
16	tCSH	/CAS hold time	60	-	70	-	ns	
17	tCAS	/CAS pulse width	20	10K	25	10K	ns	
27	tRAL	Column address to /RAS lead time	35	-	40	-	ns	
41	tCWD	/CAS to /WE delay time	40	-	50	-	ns	15
42	tRWD	/RAS to /WE delay time	85	-	100	-	ns	
43	tAWD	Column address to /WE delay time	55	-	65	-	ns	8
49	tOEA	/OE access time	-	20	-	25	ns	
50	tOED	/OE to data delay	20	-	25	-	ns	
52	tOEH	/OE command hold time	20	-	25	-	ns	
53	tCPWD	/WE delay time from /CAS precharge	60	-	70	-	ns	8

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS-only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS- before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit parallel test mode during initialization.
2. If /RAS=V_{SS} during power-up, the HY51V64400, HY51V65400 could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up.
3. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
4. $V_{IH(min.)}$ and $V_{IL(max.)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min.)}$ and $V_{IL(max.)}$, and are assumed to be 5ns for all inputs.
5. Measured at V_{OH}=2.0V and VOL=0.8V with a load equivalent to 1TTL loads and 100pF.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles and late write cycle.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPWD} \geq t_{CPWD(min.)}$, the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the $t_{RCD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
11. $t_{REF(max)}$=128ms is applied to L-parts and SL-parts.
12. A burst of 8192 /RAS-only refresh cycles must be executed within 64ms (128ms for L-parts) after exiting self refresh. (CBR refresh & Hidden refresh : 4K cycle/64ms)
13. t_{ASC},t_{CAH} are referenced to the earlier /CAS falling edge.
14. t_{CP} is specified from the last /CAS rising edge in the previous to the first /CAS falling edge in the next cycle.
15. t_{CWD} is referenced to the later /CAS falling edge at word read-modifiy-write cycle.
16. t_{CWL} is specified from /WE falling edge to the earlier /CAS rising edge.
17. t_{CSR} is referenced to the earlier /CAS falling before /RAS transition low.
18. t_{CHR} is referenced to the later /CAS rising high after /RAS transition low.
19. t_{DS} is specified for the earlier /CAS falling edge and t_{DH} is specified by the later /CAS falling edge in early write cycle.

CAPACITANCE

(T_A = 0°C to 70°C , V_{CC} = 3.3 ± 0.3V, V_{SS} = 0V, f = 1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Input Capacitance (A0~A12)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input / Output Capacitance (DQ0~DQ3)	-	7	pF