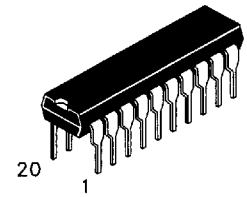
Available Q2, 1995

Octal 3-State Inverting Transparent Latch

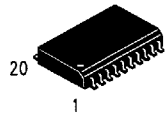
DV74HC533
DV74HCT533

The latches in this device appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is High. When Latch Enable is Low, data meeting the set-up and hold times becomes latched. The state of the latch is not affected by the Output Enable. Therefore, data may be latched even when the outputs are not enabled. Outputs are inverted from inputs.

- **Output Drive Capability: 15 LSTTL Loads**
- **Outputs Directly Interface to CMOS, NMOS, and TTL**
- **Operating Voltage Range: 2 to 6 V**
- **Low Input Current: 1 μA**
- **DC, AC parameters guaranteed from -55°C to 125°C**



N Suffix
Plastic DIP
AVG-005 Case



D Suffix
Plastic SOP
AVG-006 Case

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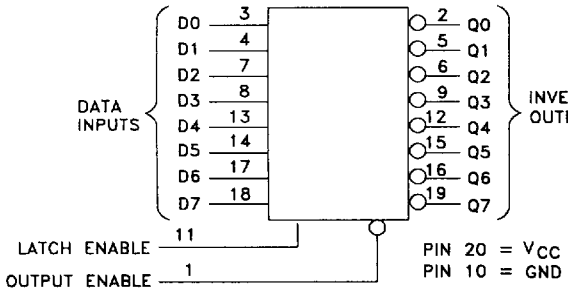
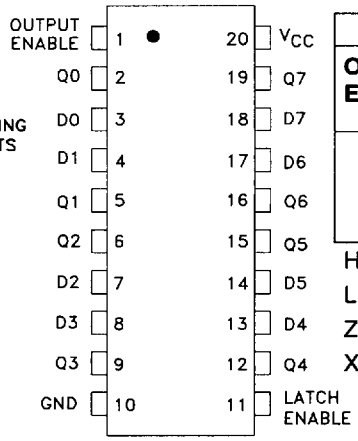


PIN ASSIGNMENT



TRUTH TABLE

Inputs			Output
Output Enable	**Latch Enable**	**D**	**Q**
L	H	H	L
L	H	L	H
L	L	X	no change
H	X	X	Z

H = High Logic Level
L = Low Logic Level
Z=High Impedance
X=Don't Care

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	–1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic DIP SOP Package	750 500	mW
T_{STG}	Storage Temperature Range	–65 to +150	°C
TL	Lead Temperature, 1mm from Case for 10 Seconds	260	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Ambient Temperature	–55	+125	°C

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Symbol	Parameter		Min	Max	Unit
t_r, t_f	Input Rise and Fall Time:	HC: V_{CC}=2.0V HCT: V_{CC}=5.5V / HC: V_{CC}=4.5V HC: V_{CC}=6.0V	0 0 0	1000 500 400	ns

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} V	Guaranteed Limits			Unit
				25°C to –55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT} =0.1 V, $\|I_{OUT}\| \leq 20\mu A$ or $V_{OUT} = V_{CC}-0.1V$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low- Level Input Voltage	V_{OUT} =0.1 V, $\|I_{OUT}\| \leq 20\mu A$ or $V_{OUT} = V_{CC}-0.1V$	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 6.0mA$ $\|I_{OUT}\| \leq 7.8\ mA$	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 6.0mA$ $\|I_{OUT}\| \leq 7.8mA$	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum Three-State Leakage Current	Output in High Impedance State $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $\|I_{OUT}\| = 0\ \mu A$ (Per Package)	6.0	8.0	80	160	µA

AC ELECTRICAL CHARACTERISTICS over full operating conditions (C_L=50pF, Input t_f=t_r=6ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to –55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Input D to Q	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Latch Enable to Q	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay Time, Output Disable to Q	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay Time, Output Enable to Q	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time Any Output	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns

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C_{IN}	Maximum Input Capacitance	—	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output High-Impedance)	—	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Latch) Used to determine the no-load dynamic power consumption $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	**Typical @ 25°C, V_{CC} = 5 V** 41	pF

TIMING REQUIREMENTS (Input t_r=t_f=6 ns)

Symbol	Parameter	V_{CC}	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125 °C	
t_{su}	Minimum Setup Time, Data to Clock	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t_h	Minimum Hold Time, Clock to Data	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Clock	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} V	Guaranteed Limits			Unit
				25°C to –55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT} =0.1 V, $\|I_{OUT}\| \leq 20\mu A$ or $V_{OUT} = V_{CC}$–0.1V	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low- Level Input Voltage	V_{OUT} =0.1 V, $\|I_{OUT}\| \leq 20\mu A$ or $V_{OUT} = V_{CC}$–0.1V	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 6.0mA$	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \leq 6.0mA$	4.5	0.26	0.33	0.40	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5	±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum Three-State Leakage Current	Output in High Impedance State $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	±0.5	±5.0	±10.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $\|I_{OUT}\|$= 0 µA (Per Package)	5.5	8.0	80	160	µA

ΔI_{CC}	Additional Quiescent Supply Current	V_{IN}=2.4V, Any One Input V_{IN}=V_{CC} or GND, Other Inputs I_{OUT}=0µA	5.5	≥ –55°C 2.9	25°C to 125°C 2.4	mA

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AC ELECTRICAL CHARACTERISTICS over full operating conditions (C_L=50pF, Input t_f=t_r=6ns)

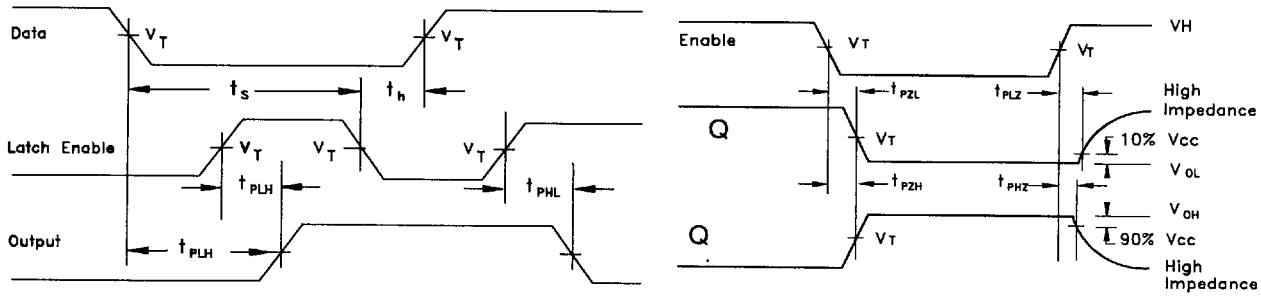
Symbol	Parameter	Vcc V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Input D to Q	5.0 ±10%	35	44	53	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time, Latch Enable to Q		35	44	53	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay Time, Output Disable to Q		35	44	53	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay Time, Output Enable to Q	5.0 ±10%	35	44	53	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		12	15	18	ns
C_{IN}	Maximum Input Capacitance	—	10	10	10	pF
C_{OUT}	Maximum 3-State Output Capacitance (Output High-Impedance)	—	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, Vcc = 5 V 65	pF

TIMING REQUIREMENTS (Input t_r=t_f=6 ns)

Sym-bol	Parameter	Vcc	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125 °C	
t_{su}	Minimum Setup Time, Data to Latch Enable	5.0V ±10%	20	25	30	ns
t_h	Minimum Hold Time, Latch Enable to Data		5	6	8	ns
t_w	Minimum Pulse Width, Clock		16	20	24	ns

SWITCHING WAVEFORMS



Input and Output Threshold Voltage:
V_T=50% V_{CC} for HC; 1.3V for HCT
V_H=V_{CC} for HC, 3V for HCT

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