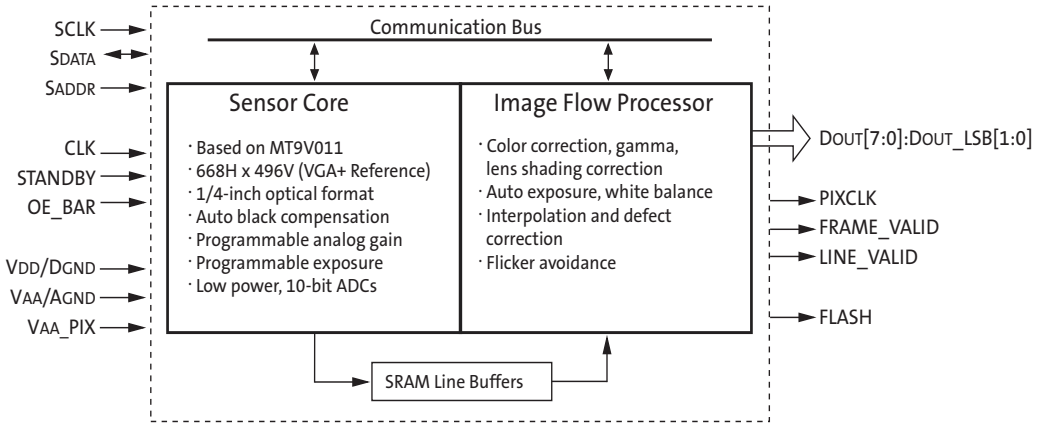
General Description

This SOC VGA CMOS image sensor features DigitalClarity—Aptina's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The MT9V131 is a fully-automatic, single-chip camera, requiring only a power supply, lens, and clock source for basic operation. Output video is streamed through a parallel 8-bit DOUT port, as shown in Figure 1. The output pixel clock is used to latch the data, while FRAME_VALID (FV) and LINE_VALID (LV) signals indicate the active video. The sensor can be put in an ultra-low power sleep mode by asserting the STANDBY pin. Output signals can also be tri-stated by de-asserting the OE_BAR pin. The MT9V131 internal registers can be configured using a two-wire serial interface.

The MT9V131 can be programmed to output progressive scan images up to 30 fps in an 8-bit ITU_R BT.656 (YCbCr) formerly CCIR656, YUV, 565RGB, 555RGB, or 444RGB formats. 10-bit raw Bayer data output can also be selected. The FV and LV signals are output on dedicated pins, along with a pixel clock (PIXCLK) that is synchronous with valid data.

Figure 1: Chip Block Diagram

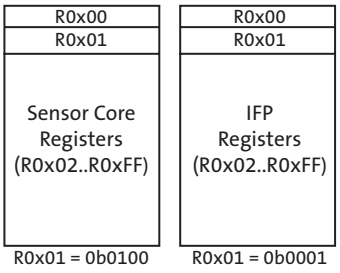


The MT9V131 can accept an input clock of up to 27 MHz, delivering 30 fps. With power-on defaults (see Appendix B on page 28 for recommended defaults), the camera is configured to deliver 15 fps at 12 MHz and automatically slows down the frame rate in low-light conditions to achieve longer exposures and better image quality.

Internally, the MT9V131 consists of a sensor core and an image flow processor (IFP). The sensor core functions to capture raw Bayer-encoded images that are input into the IFP as shown in Figure 1. The IFP processes the incoming stream to create interpolated, color-corrected output and controls the sensor core to maintain the desirable exposure and color balance.

Sensor core and IFP registers are grouped into two separate address spaces, as shown in Figure 2 on page 6. The internal registers can be accessed through the two-wire serial interface. Selecting the desired address space can be accomplished by programming register R0x01, which remains present in both register sets.

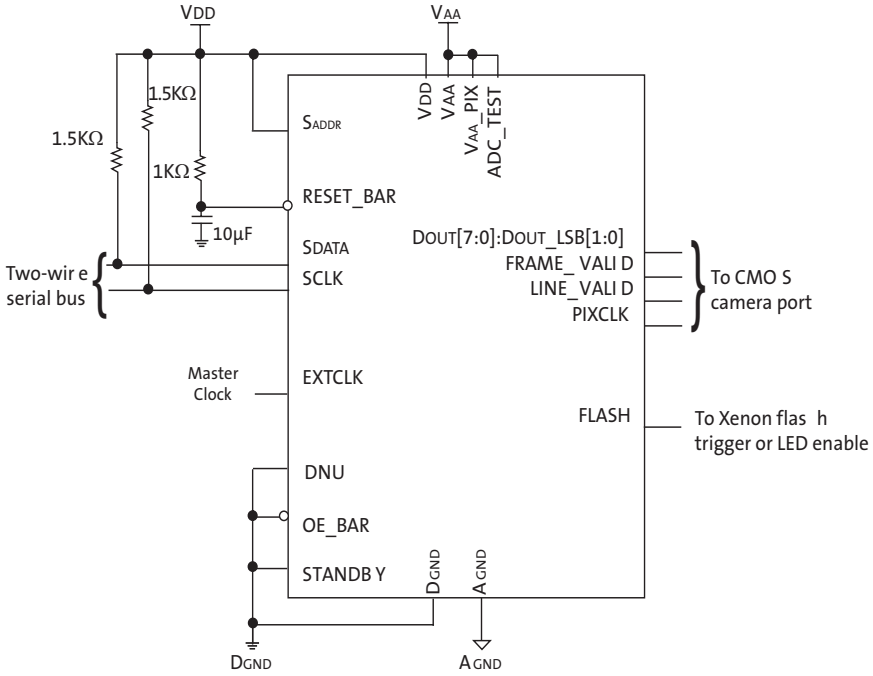
Figure 2: Internal Register Grouping



Note: Program R0x01 to select the desired space (0b0100 = sensor core registers, 0b0001 = IFP/SOC registers).

Figure 3 shows MT9V131 typical connections. For low-noise operation, the MT9V131 requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together right next to the die. Both power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

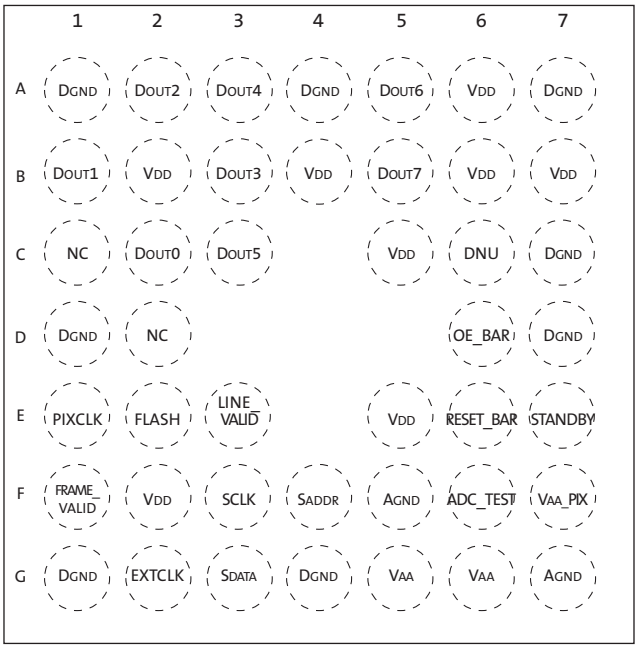
Figure 3: Typical Configuration (Connection)



Note: Aptina recommends a 1.5KΩ resistor value, but it may be greater for slower two-wire speed.

Ball Assignment

Figure 4: 44-Ball ICSP Pinout Diagram



Top View
(Ball Down)

Figure 5: 48-Pin CLCC Pinout Diagram

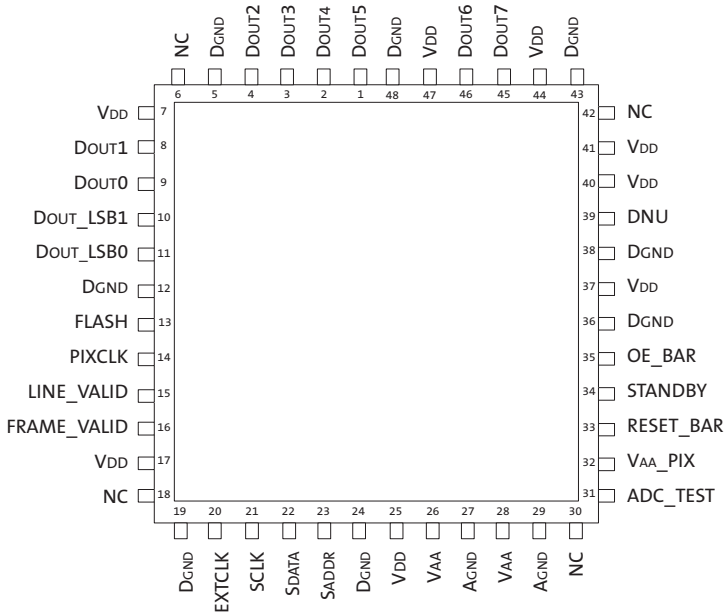


Table 3: Ball Description for ICSP Package

Ball Numbers	Name	Type	Description
G2	EXTCLK	Input	Master clock into sensor. Default is 12 MHz (27 MHz maximum).
F3	SCLK	Input	Serial clock.
F4	SADDR	Input	Serial interface address select: R0xB8 when HIGH (default). R0x90 when LOW.
F6	ADC_TEST	Input	Tie to Vaa_PIX (factory use only).
E6	RESET_BAR	Input	Asynchronous reset of sensor when LOW. All registers assume factory defaults.
E7	STANDBY	Input	When HIGH, puts the imager in ultra-low power standby mode.
D6	OE_BAR	Input	Output_Enable pin. When HIGH, tri-state all outputs except SDATA (tie LOW for normal operation).
C6	DNU	Input	Tie to digital ground.
G3	SDATA	I/O	Serial data I/O.
E2	FLASH	Output	Flash strobe.
E1	PIXCLK	Output	Pixel clock out. Pixel data output are valid during rising edge of this clock. IFP R0x08 [9] inverts polarity. Frequency = Master clock.
E3	LINE_VALID	Output	Active HIGH during line of selectable valid pixel data.
F1	FRAME_VALID	Output	Active HIGH during frame of valid pixel data.
B5	DOUT7	Output	ITU_R BT.656/RGB data bit 7 (MSB).
A5	DOUT6	Output	ITU_R BT.656/RGB data bit 6.
C3	DOUT5	Output	ITU_R BT.656/RGB data bit 5.
A3	DOUT4	Output	ITU_R BT.656/RGB data bit 4.
B3	DOUT3	Output	ITU_R BT.656/RGB data bit 3.
A2	DOUT2	Output	ITU_R BT.656/RGB data bit 2.
B1	DOUT1	Output	ITU_R BT.656/RGB data bit 1.
C2	DOUT0	Output	ITU_R BT.656/RGB data bit 0 (LSB).
A6, B2, B4, B6, B7, C5, E5, F2	VDD	Supply	Digital power (2.8V).
G5, G6	VAA	Supply	Analog power (2.8V).
F7	VAA_PIX	Supply	Pixel array power (2.8V).
F5, G7	AGND	Supply	Analog ground.
A1, D1, A4, A7, C7, D7, G1, G4	DGND	Supply	Digital ground.
C1, D2	NC	–	No connect.

Table 4: Pin Description for the CLCC Package

Pin Number	Pin Name	Type	Description
20	EXTCLK	Input	Master clock into sensor. Default is 12 MHz (27 MHz maximum).
21	SCLK	Input	Serial clock.
23	SADDR	Input	Serial interface address select: R0xB8 when HIGH (default). R0x90 when LOW.
31	ADC_TEST	Input	Tie to Vaa_PIX (factory use only).
33	RESET_BAR	Input	Asynchronous reset of sensor when LOW. All registers assume factory defaults.
34	STANDBY	Input	When HIGH, puts the imager in ultra-low power standby mode.
35	OE_BAR	Input	Output_Enable pin. When HIGH, tri-state all outputs except SDATA (tie LOW for normal operation).
39	DNU	Input	Tie to digital ground.
22	SDATA	I/O	Serial data I/O.
13	FLASH	Output	Flash strobe.
14	PIXCLK	Output	Pixel clock out. Pixel data output are valid during rising edge of this clock. IFP R0x08 [9] inverts polarity. Frequency = Master clock.
15	LINE_VALID	Output	Active HIGH during line of selectable valid pixel data.
16	FRAME_VALID	Output	Active HIGH during frame of valid pixel data.
45	DOUT7	Output	ITU_R BT.656/RGB data bit 7 (MSB).
46	DOUT6	Output	ITU_R BT.656/RGB data bit 6.
1	DOUT5	Output	ITU_R BT.656/RGB data bit 5.
2	DOUT4	Output	ITU_R BT.656/RGB data bit 4.
3	DOUT3	Output	ITU_R BT.656/RGB data bit 3.
4	DOUT2	Output	ITU_R BT.656/RGB data bit 2.
8	DOUT1	Output	ITU_R BT.656/RGB data bit 1.
9	DOUT0	Output	ITU_R BT.656/RGB data bit 0 (LSB).
10	DOUT_LSB1	Output	Raw Bayer 10-bit output.
11	DOUT_LSB0	Output	Raw Bayer 10-bit output (LSB).
7, 17, 25, 37, 40, 41, 44, 47	VDD	Supply	Digital power (2.8V).
26, 28	VAA	Supply	Analog power (2.8V).
32	VAA_PIX	Supply	Pixel array power (2.8V).
27, 29	AGND	Supply	Analog ground.
5, 12, 19, 24, 36, 38, 43, 48	DGND	Supply	Digital ground.
6, 18, 30, 42	NC	–	No connect.

Image Flow Processor

Overview of Architecture

The IFP consists of a color processing pipeline and a measurement and control logic block, as shown in Figure 6 on page 11. The stream of raw data from the sensor enters the pipeline and undergoes a number of transformations. Image stream processing starts from conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens. Next, the data is interpolated to recover missing color components for each pixel and defective pixels are corrected. The resulting interpolated RGB data passes through the current color correction matrix (CCM), gamma, and saturation corrections and is formatted for final output.

The measurement and control logic continuously accumulates statistics about image brightness and color. Indoor 50/60 Hz flicker is detected and automatically updated when possible. Based on these measurements, the IFP calculates updated values for exposure time and sensor analog gains, which are sent to the sensor core through the communication bus.

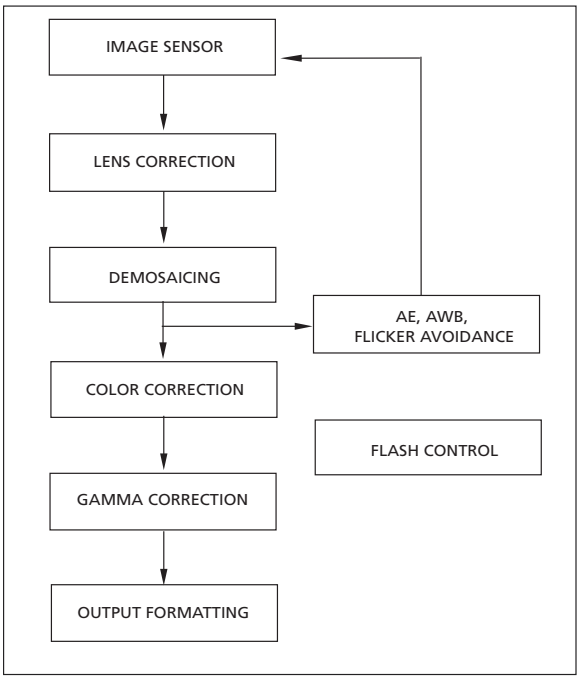
Color correction is achieved through a linear transformation of the image with a 3 x 3 color correction matrix. Color saturation can be adjusted in the range from zero (black and white) to 1.25 (125% of full color saturation).

Gamma correction compensates for nonlinear dependence of the display device output versus driving signal (monitor brightness versus CRT voltage).

Output and Formatting

Processed video can be output in the form of a progressive ITU_R BT.656 or RGB stream. The ITU_R BT.656 (default) stream contains 4:2:2 data with optional embedded synchronization codes. This kind of output is typically suitable for subsequent display by standard video equipment. For JPEG/MPEG compression, YUV/ encoding is suitable. RGB functionality is provided to support LCD devices. The MT9V131 can be configured to output 16-bit RGB (565RGB) and 15-bit RGB (555RGB), as well as two types of 12-bit RGB (444RGB). The user can configure internal registers to swap odd and even bytes, chrominance channels, and luminance and chrominance components to facilitate interfacing to application processors.

Figure 6: Image Flow Processor Block Diagram



The MT9V131 features smooth, continuous zoom and pan. This functionality is available when the IFP output is downsized in the decimation block. The decimation block can downsize the original VGA image to any integer size, including QVGA, QQVGA, CIF, and QCIF with no loss to the field of view. The user can program the desired size of the output image in terms of horizontal and vertical pixel count. In addition, the user can program the size of a region for downsizing. Continuous zoom is achieved every time the region of interest is less than the entire VGA image. The maximum zoom factor is equal to the ratio of VGA to the size of the region of interest. For example, an image rendered on a 160 x 120 display can be zoomed by 640/160 = 480/120 = 4 times. Continuous pan is achieved by adjusting the starting coordinates of the region of interest.

Also, a fixed 2X up-zoom is implemented by means of windowing down the sensor core. In this mode, the IFP receives a QVGA-sized input data and outputs a VGA-size image. The sub-window can be panned both vertically and horizontally by programming sensor core registers.

The MT9V131 supports both LED and xenon-type flash light sources using a dedicated output pad. For xenon devices, the signal generates a strobe to fire when the imager's shutter is fully open. For LED, the signal can be asserted or de-asserted asynchronously. Flash modes are configured and engaged over the two-wire serial interface using IFP R0x98.

Output Data Ordering

In YCbCr the first and second bytes can be swapped. Luma/chroma bytes can be swapped as well. R and B channels are bit-wise swapped when chroma swap is enabled. See IFP R0x3A for channel swapping configuration.

Table 5: YUV/YCbCr Output Data Ordering

Mode	1st Byte	2nd Byte	3rd Byte	4th Byte
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CrCb	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CrCb, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

Table 6: RGB Output Data Ordering in Default Mode

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
565RGB	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
555RGB	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G4	G3	G2	B7	B6	B5	B4	B3
444xRGB	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
x444RGB	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

A bypass mode is available whereby raw Bayer 10-bits data is output as two bytes. See IFP R0x08[7].

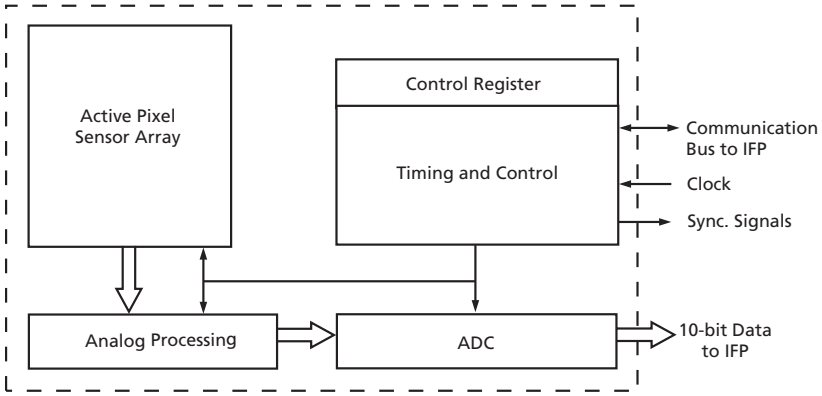
Table 7: Byte Ordering in 8 + 2 Bypass Mode

Byte Ordering									
8+2 Bypass	First	D9	D8	D7	D6	D5	D4	D3	D2
	Second	0	0	0	0	0	0	D1	D0

Sensor Core Overview

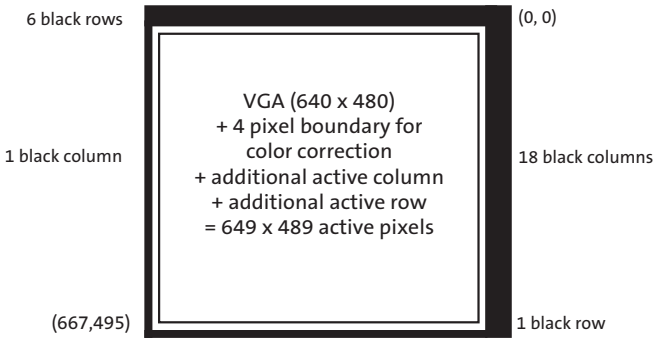
The sensor consists of a pixel array of 668 x 496 total, analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

Figure 7: Sensor Core Block Diagram



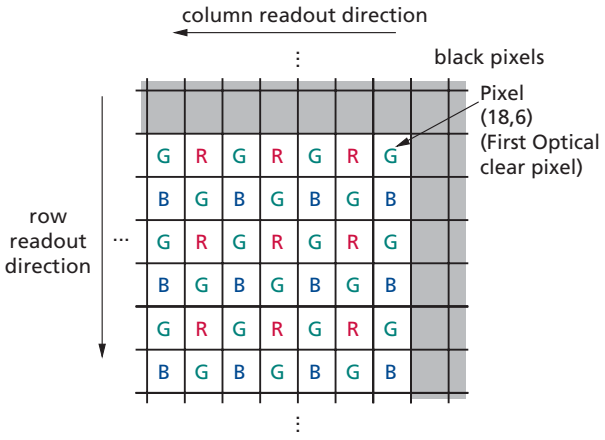
The sensor core's pixel array is configured as 668 columns by 496 rows (shown in Figure 8). The first 18 columns and the first 6 rows of pixels are optically black and can be used to monitor the black level. The last column and the last row of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. There are 649 columns by 489 rows of optically active pixels, which provides a four-pixel boundary around the VGA (640 x 480) image to avoid boundary affects during color interpolation and correction. The additional active column and additional active row are used to allow horizontally and vertically mirrored readout to also start on the same color pixel, as shown in Figure 8.

Figure 8: Pixel Array Description



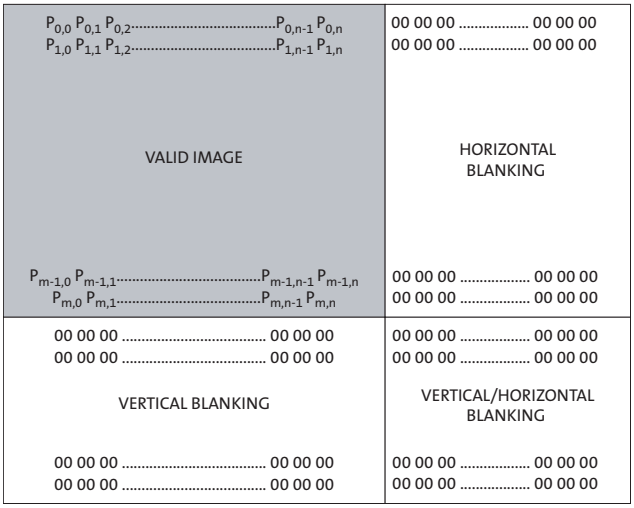
The sensor core uses the RGB Bayer color pattern (shown in Figure 9 on page 14). Even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. Even-numbered columns contain green and blue color pixels; odd- numbered columns contain red and green color pixels.

Figure 9: Pixel Color Pattern Detail (Top Right Corner)



The sensor core image data is read-out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 10. The amount of horizontal and vertical blanking is programmable through the sensor core registers R0x05 and R0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. See "Appendix A – Sensor Timing" on page 21 for the description of FRAME_VALID timing.

Figure 10: Spatial Illustration of Image Readout



Notes:
1. Do not change these registers. Contact Aptina support for settings different from defaults.
2. IFP controls these registers when AE, AWB, or flicker avoidance are enabled.

Electrical Specifications

The recommended operating temperature ranges from –20°C to +70°C. The sensor image quality may degrade above +40°C.

Table 8: DC Electrical Characteristics
$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Definition	Symbol	Condition	Min	Typ	Max	Unit
Input high voltage	V_{IH}		V_{DD} - 0.25		V_{DD} + 0.25	V
Input low voltage	V_{IL}		–0.3		0.8	V
Input leakage current	I_{IN}	No pull-up resistor; $V_{IN} = V_{DD}$ or DGND	–5.0		5.0	µA
Output high voltage	V_{OH}		V_{DD} - 0.2			V
Output low voltage	V_{OL}				0.2	V
Output high current	I_{OH}				15.0	mA
Output low current	I_{OL}				20.0	mA
Tri-state output leakage current	I_{OZ}				5.0	µA
Analog operating supply current	I_{AA}	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 10.0 10.0	 20.0 20.0	 25.0 25.0	mA
Digital operating supply current	I_{DD}	Default settings, C_{LOAD} = 10pF CLKIN = 12 MHz CLKIN = 27 MHz	 5.0 10.0	 8.0 15.0	 20.0 20.0	mA
Analog standby supply current	I_{AA} Standby	STDBY = V_{DD}	0.0	2.5	5.0	µA
Digital standby supply current	I_{DD} Standby	STDBY = V_{DD}	0.0	2.5	5.0	µA

Notes:
1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.
2. When STANDBY is de-asserted, standby mode is exited immediately (within several master clocks), but the current frame and the next two frames will be invalid. The fourth frame will contain a valid image.

Table 9: AC Electrical Characteristics

$V_{DD} = V_{AA} = 2.8 \pm 0.25V$; $T_A = 25°C$

Definition		Symbol	Condition	Min	Typ	Max	Unit	Notes
Input clock frequency		^{f}CLKIN		10	12	27	MHz	
Clock duty cycle			50:50	45	50	55	%	1
Input clock rise time		^{t}R		1	2	5	ns	
Input clock fall time		^{t}F		1	2	5	ns	
CLKIN to PIXCLK propagation delay	LOW-to-HIGH	$^{t}PLH_P$	C_{LOAD} = 10pF	6	12	14	ns	3
	HIGH-to-LOW	$^{t}PHL_P$		6	10	14	ns	
PIXCLK to DOUT[7:0] at 27 MHz	Setup time	^{t}DSETUP	C_{LOAD} = 10pF	11	18	–	ns	2
	Hold time	^{t}DHOLD		11	18	–	ns	
PIXCLK to FRAME_VALID and LINE_VALID propagation delay	LOW-to-HIGH	$^{t}PLH_{F,L}$	C_{LOAD} = 10pF	4	9.0	13	ns	
	HIGH-to-LOW	$^{t}PHL_{F,L}$		4	7.5	13	ns	
Output rise time		$^{t}OUT_R$	C_{LOAD} = 10pF	5	7.0	15	ns	
Output fall time		$^{t}OUT_F$	C_{LOAD} = 10pF	5	9.0	15	ns	

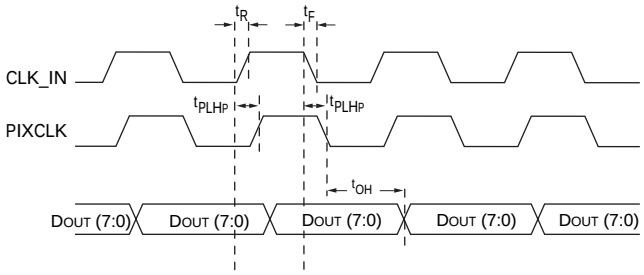
Notes:
1. For 30 fps operation with a 27 MHz clock, the user must have a precise duty cycle equal to 50%. With a slower frame rate and a slower clock, the clock duty cycle can be relaxed.
2. Typical is 1/2 of CLKIN period.
3. PIXCLK can be programmed to be inverted or non-inverted.

Propagation Delays

Propagation Delays for PIXCLK and Data Out Signals

The output PIXCLK delay, relative to the master clock (CLKIN), is typically 10–12ns. Note that the data outputs change on the rising edge of the master clock (CLKIN) as shown in in Figure 11. PIXCLK by default is inverted from CLKIN but can be programmed to be non-inverted.

Figure 11: Propagation Delays for PIXCLK and Data Out Signals

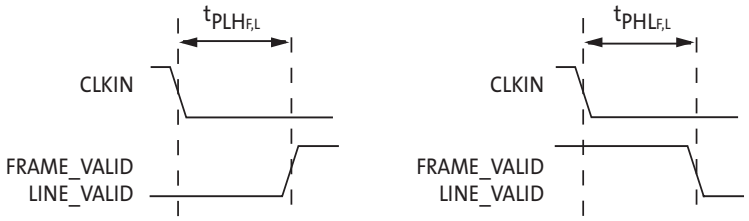


Note: Default condition of the IPA register R0x08[9] = 0.

Propagation Delays for FRAME_VALID and LINE_VALID Signals

The LINE_VALID and FRAME_VALID signals change on the same clock edge as the data output. The LINE_VALID goes HIGH on the same falling master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock falling edge as the end of the output of the last valid pixel's data. The default timing of PIXCLK with respect to LINE_VALID and FRAME_VALID is shown in Figure 12.

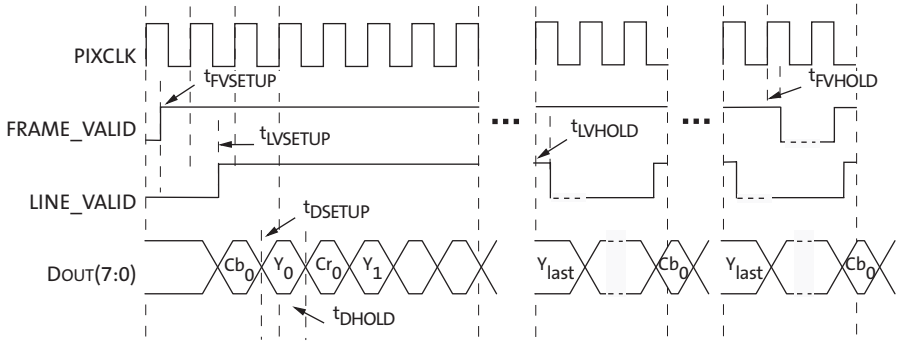
Figure 12: Propagation Delays for FRAME_VALID and LINE_VALID Signals



Output Data Timing

As shown in Figure 13, FRAME_VALID goes HIGH 6 pixel clocks prior to the time that the first LINE_VALID goes HIGH. It returns LOW at a time corresponding to 6 pixel clocks after the last LINE_VALID goes LOW.

Figure 13: Data Output Timing Diagram



Notes:
1. PIXCLK = 27 MHz (MAX)
2. ^{t}FVSETUP = / setup time for FRAME_VALID before falling edge of PIXCLK / = 18ns
3. ^{t}FVHOLD = / hold time for FRAME_VALID after falling edge of PIXCLK / = 18ns
4. ^{t}LVSETUP = / setup time for LINE_VALID before falling edge of PIXCLK / = 18ns
5. ^{t}LVHOLD = / hold time for LINE_VALID after falling edge of PIXCLK / = 18ns
6. ^{t}DSETUP = / setup time for DOUT before falling edge of PIXCLK / = 18ns
7. ^{t}DHOLD = / hold time for DOUT after falling edge of PIXCLK / = 18ns
   Frame start: FF00 00A0
   Line start: FF00 0080
   Line end: FF00 0090
   Frame end: FF00 00B0
8. Drawing shown has R0x08[9] = 1

Figure 14: Typical Spectral Characteristics

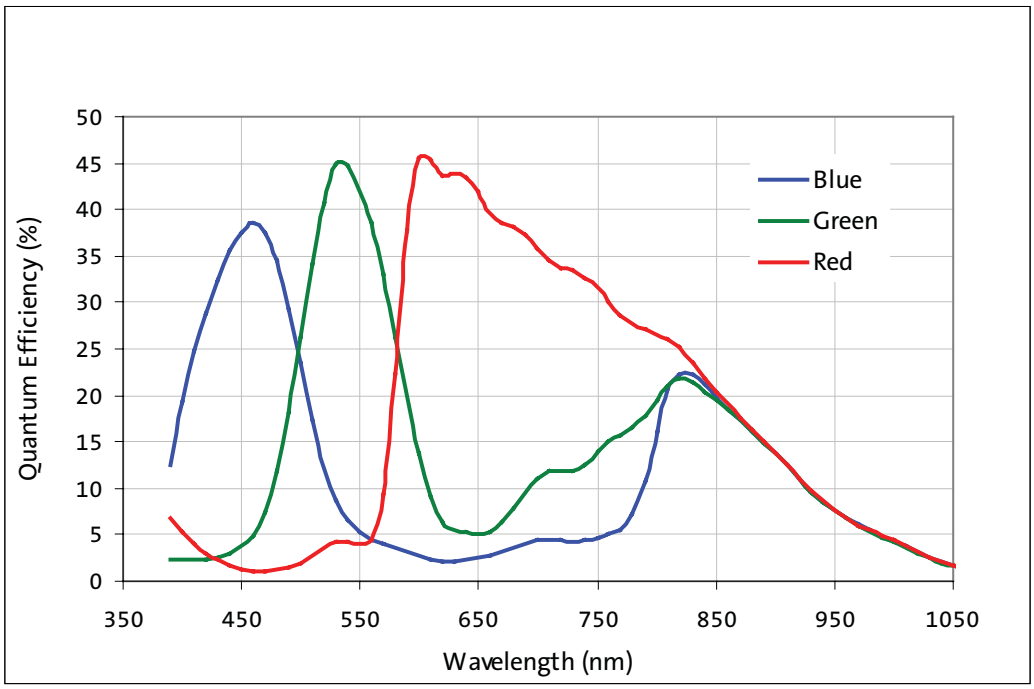
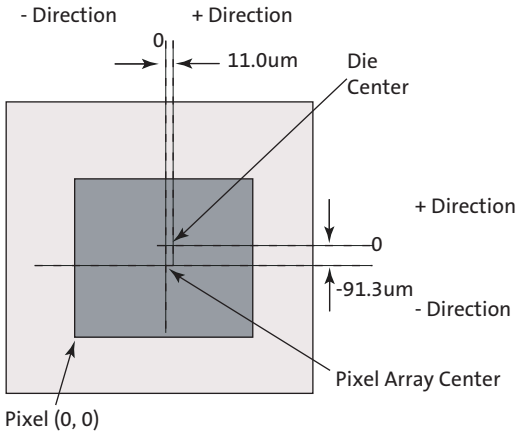
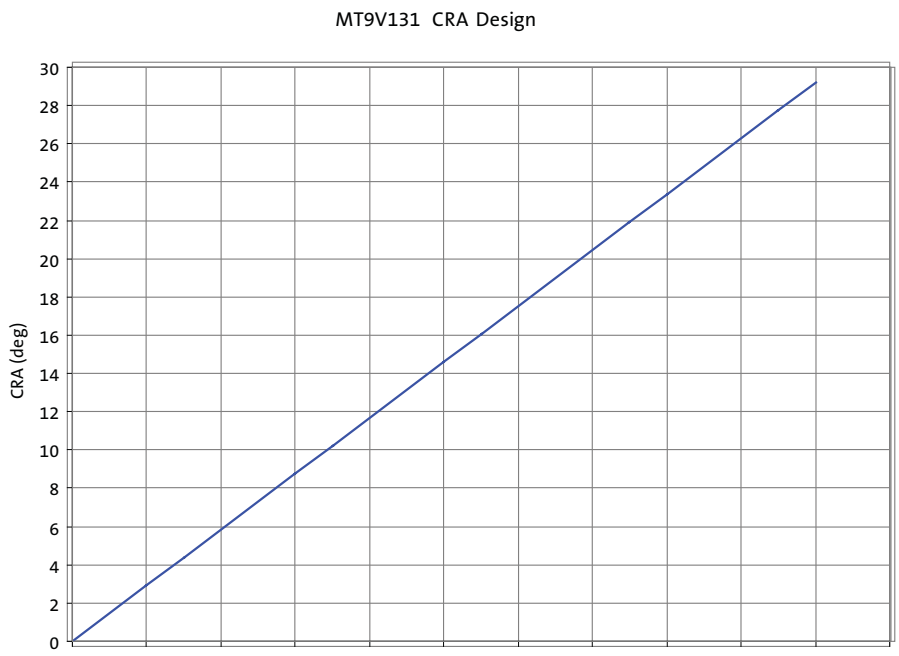


Figure 15: Die Center – Image Center Offset



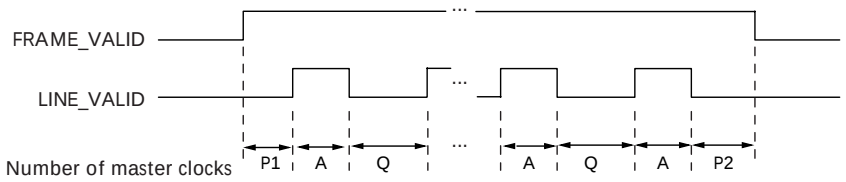
Note: Not to scale.

Figure 16: Chief Ray Angle (CRA) vs. Image Height

CRA vs. Image Height Plot	Image Height		CRA (Deg)
	(%)	(mm)	
	0	0	0
	5	0.112	1.46
	10	0.224	2.92
	15	0.336	4.38
	20	0.448	5.84
	25	0.560	7.30
	30	0.672	8.75
	35	0.784	10.21
	40	0.896	11.67
	45	1.008	13.13
	50	1.120	14.59
	55	1.232	16.05
	60	1.344	17.51
	65	1.456	18.97
	70	1.568	20.43
	75	1.680	21.89
	80	1.792	23.34
	85	1.904	24.80
	90	2.016	26/26
	95	2.128	27.72
	100	2.240	29.18

Appendix A – Sensor Timing

Figure 17: Row Timing and FRAME_VALID/LINE_VALID Signals



Note: The signals in Figure 17 are defined in Table 10.

Table 10: Frame Time

Parameter	Name	Equation (Master Clocks)	Default Timing At 12 MHz
A	Active data time	(R0x04 - 7) x 2	= 1,280 pixel clocks = 1,280 master clocks = 106.7µs
P1	Frame start blanking	(R0x05 + 112) x 2	= 300 pixel clocks = 300 master clocks = 25.0µs
P2	Frame end blanking	14 CLKS	= 14 pixel clocks = 14 master clocks = 1.17µs
Q	Horizontal blanking	(R0x05 + 121) x 2 (MIN R0x05 value = 9)	= 318 pixel clocks = 318 master clocks = 26.5µs
A + Q	Row time	(R0x04 + R0x05 +114) x 2	= 1,598 pixel clocks = 1,598 master clocks = 133.2µs
V	Vertical blanking	(R0x06 + 9) x (A + Q) + (Q - P1 - P2)	= 20,778 pixel clocks = 20,778 master clocks = 1.73ms
Nrows x (A + Q)	Frame valid time	(R0x03 - 7) x (A + Q) - (Q - P1 - P2)	= 767,036 pixel clocks = 767,036 master clocks = 63.92ms
F	Total frame time	(R0x03 + R0x06 + 2) x (A + Q)	= 787,814 pixel clocks = 787,814 master clocks = 65.65ms

Note: In order to avoid flicker, frame time is 65.65ms.

Sensor timing is shown above in terms of master clock cycle. The vertical blanking and total frame time equations assume that the number of integration rows (bits 11 through 0 of R0x09) is less than the number of active row plus blanking rows (R0x03 + 1 + R0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 11.

Table 11: Frame Time – Larger than One Frame

Parameter	Name	Equation (Master Clocks)	Default Timing
V'	Vertical blanking (long integration time)	(R0x09 - R0x03) x (A + Q)	–
F'	Total Frame Time (long integration time)	(R0x09 + 1) x (A + Q)	–

Serial Bus Description

Registers are written to and read from the MT9V131 through the two-wire serial interface bus. The sensor is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9V131 through the serial data (SDATA) line. The SDATA line is pulled up to 2.8V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time. The registers are 16 bits wide and can be accessed through 16-bit or 8-bit two-wire serial bus sequences.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device eight-bit address. SADDR is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xB8.
- an acknowledge or a no-acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a “0” indicates a write and a “1” indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The MT9V131 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

The MT9V131 allows for 8-bit data transfers through the two-wire serial interface by writing (or reading) the most significant 8 bits to the register and then writing (or reading) the least significant 8 bits to R0x7F (127).

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the least significant bit (LSB) of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xB8, while the read address is 0xB9; this only applies when SADDR is set HIGH.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the serial clock—it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

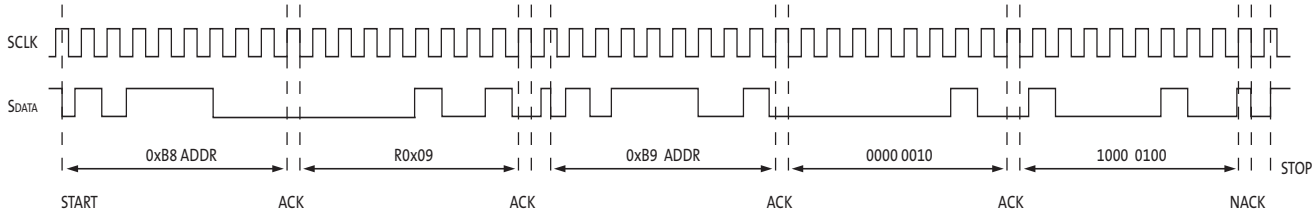
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences (with SADDR = 1)

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 18. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bits, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

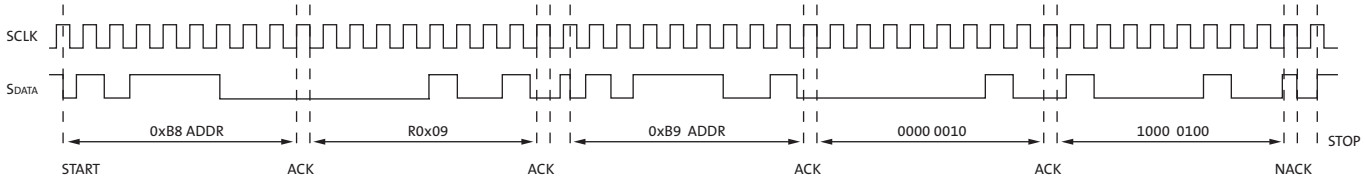
Figure 18: Timing Diagram Showing a Write to R0x09 with Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 19. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 19: Timing Diagram Showing a Read from R0x09; Returned Value 0x0284

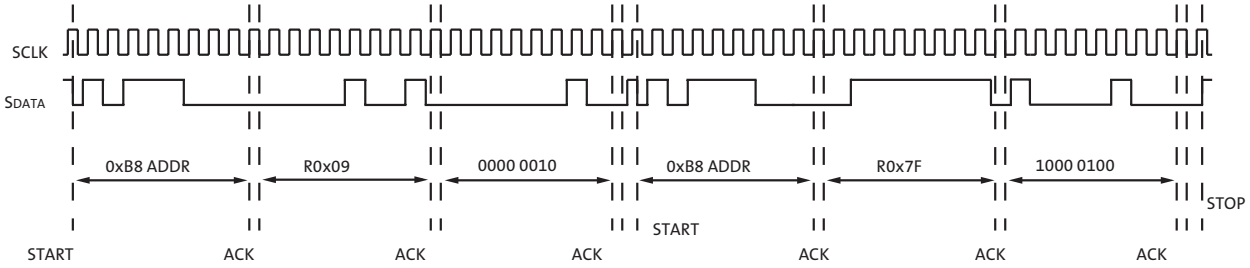


8-Bit Write Sequence

All registers in the camera are treated and accessed as 16-bit, even when some registers do not have all 16-bits used. However, certain hosts only support 8-bit serial communication access. The camera provides a special accommodation for these hosts.

To be able to write one byte at a time to the register a special register address is added. The 8-bit write is done by first writing the upper 8 bits to the desired register and then writing the lower 8 bits to the special register address (R0x7F). The register is not updated until all 16 bits have been written. It is not possible to just update half of a register. In Figure 20, a typical sequence for 8-bit writing is shown. The second byte is written to the special register (R0x7F).

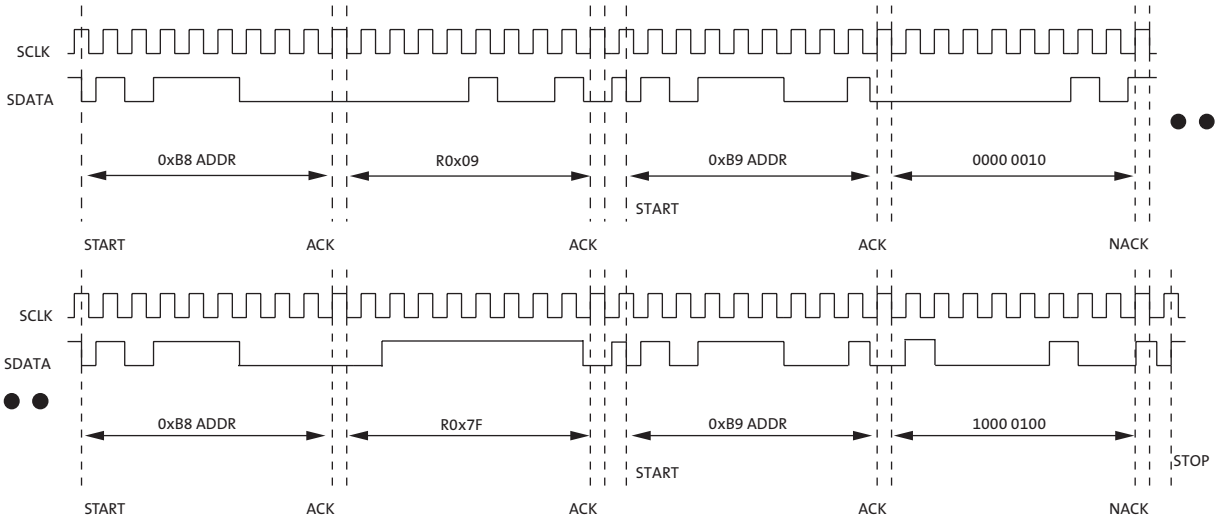
Figure 20: Timing Diagram Showing a Bytewise Write to R0x09 with Value 0x0284



8-Bit Read Sequence

To read 1 byte at a time, the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a read from the special register (R0x7F) the lower 8 bits are accessed, as shown in Figure 21 The master sets the no-acknowledge bits.

Figure 21: Timing Diagram Showing a Bytewise Read from R0x09; Returned Value 0x0284



Two-Wire Serial Bus Timing

The two-wire serial interface operation requires a certain minimum of master clock cycles between transitions. These are specified below in master clock cycles.

Figure 22: Serial Host Interface Start Condition Timing

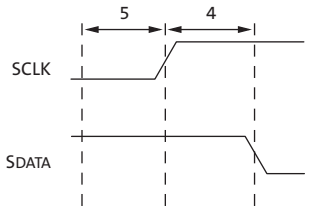
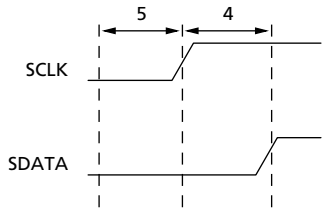
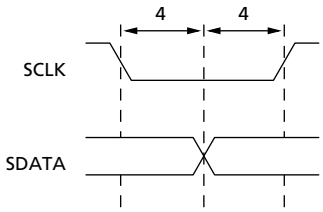


Figure 23: Serial Host Interface Stop Condition Timing



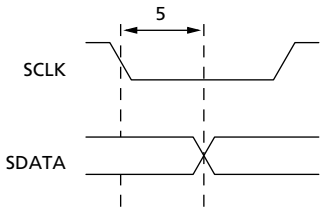
Note: All timing are in units of master clock cycle.

Figure 24: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 25: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 26: Acknowledge Signal Timing After an 8-bit Write to the Sensor

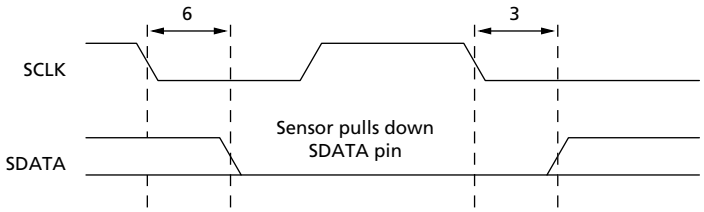
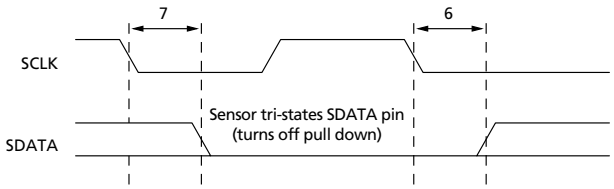


Figure 27: Acknowledge Signal Timing After an 8-bit Read from the Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Appendix B – Overview of Programming

Default Sensor Configuration

In its default configuration, the sensor outputs up to 15 fps at 12 MHz master clock frequency. Auto exposure, automatic white balance, 60Hz flicker avoidance, defect correction, and automatic noise suppression in low-light conditions are enabled. The frame rate is controlled by AE and can be slowed down to 5 fps in low light. Lens shading correction is disabled. Gamma correction uses gamma = 0.6. Image data are output in progressive YCbCr ITU_R.BT.656 VGA format, with Y, Cb, and Cr values ranging from 16 to 240.

The use of the non-default register settings shown in Table 12 are recommended to optimize sensor performance in the above configuration.

Table 12: Non-Default Register Settings Optimizing 15 fps at 12 MHz Operation

Core:	R0x5 = 0x2E, R0x7[4] = 0, R0x21 = 0xE401, R0x2F = 0xF7B6
IFP:	R0x33 = 0x1411, R0x38 = 0x878, R0x39 = 0x122, R0x3B = 0x42C, R0x3E = 0xFFF, R0x40 = 0x0E10, R0x41 = 0x1417, R0x42 = 0x1213, R0x43 = 0x1112, R0x44 = 0x7110, R0x45 = 0x7473

Note: Non-default register settings required for an optimal 30 fps, 27 MHz operation are shown in Table 13.

Table 13: Non-Default Register Settings Optimizing 30 fps at 27 MHz Operation

Core:	R0x05 = 0x84, R0x06 = 0xA, R0x07[4] = 0, R0x21 = 0xE401
IFP:	R0x33 = 0x1411, R0x39 = 0x122, R0x3B = 0x42C, R0x3E = 0xFFF, R0x59 = 0x1F8, R0x5A = 0x25D, R0x 5C = 0x201E, R0x5D = 0x2725, R0x64 = 0x117D

Note: To obtain register settings for other frame rates and clock speeds, contact a Aptina FAE.

Auto Exposure

Target image brightness and accuracy of AE are set by IFP R0x2E[7:0] and R0x2E[15:8], respectively. For example, to overexpose images, set IFP R0x2E[7:0] = 0x78. To change image brightness on LCD in RGB preview mode, use IFP R0x34[15:8]. AE logic can be programmed to keep the frame rate constant or vary it within certain range, by writing to IFP R0x37[9:5] one of the values tabulated in Table 14. Current and time-averaged luma values can be read in IFP R0x4C and R0x4D, respectively.

Table 14: Relation Between IFP R0x37[9:5] Setting and Frame Rate Range

Minimum Frame Rate	Maximum Frame Rate = 15 fps	Maximum Frame Rate = 30 fps
30 fps	N/A	4
15 fps	8	8
7.5 fps	16	16
5 fps	24	24

The speed of AE is set using IFP R0x2F. The speed should be higher for preview modes and lower for video output to avoid sudden changes in brightness between frames.

Auto exposure is disabled by setting IFP R0x06[14] = 0. When AE, AWB, and flicker avoidance are all disabled (IFP R0x06[14] = 0, IFP R0x06[1] = 0, and IFP R8[11] = 0), exposure and analog gains can be adjusted manually (see core registers R0x09, R0x0C, and R0x2B through R0x2E).

Automatic White Balance

AWB can be disabled by setting IFP R0x06[1] = 0. Use IFP R0x25[2:0] and R0x25[6:3] to speed up AWB response. Note that speeding AWB up may result in color oscillation. If necessary, AWB range can be restricted by changing the upper limit in IFP R0x25[14:8] and lower limit in IFP R0x25[6:0].

Flicker Avoidance

Use IFP R0x5B to choose automatic/manual, 50Hz/60Hz flicker avoidance and IFP R0x08[11] = 0 to disable this feature.

Flash

For flash programming, see IFP R0x98 description.

Decimation, Zoom, and Pan

For output decimation programming, see IFP R0xA5 description. Table 15 provides some examples.

Table 15: Decimation, Zoom, and Pan

IFP Registers	CIF Output (Correct Aspect Ratio)	QVGA Output 2:1 Zoom	QVGA Output 1:1 Zoom
R0xA5	26	160	0
R0xA6	586	320	640
R0xA7	352	320	320
R0xA8	0	120	0
R0xA9	480	240	480
R0xAA	288	240	240

Note: For fixed 2x upsize zoom, set core R0x1E[0] = 1.

Interpolation

Use IFP R0x05[2:0] to adjust image sharpness. By default, sharpness is automatically reduced in low-light conditions (see IFP R0x5[3]). For 565RGB 16-bit capture, set IFP R0x06[12] = 0 and IFP R0x05[3] = 0 to avoid contouring.

Special Effects

To switch from color to gray scale output, set IFP R0x08[5] = 1.

Image Mirroring

To mirror images horizontally, set core R0x20[14] = 1 and IFP R0x08[0] = 1. To flip images vertically, set core R0x20[15] = 1 and IFP R0x08[1] = 1.

Test Pattern

See IFP R0x48 and IFP R0x35[5:3] description.

Gamma Correction

See Table 16 and Table 17 for register settings required to setup non-default gamma correction. Note that these settings determine output signal range. Use YCbCr settings with ITU_R BTU-compatible devices. Use YUV settings for JPEG capture and RGB preview; switching to YUV mode requires setting IFP R0x34 = 0 and IFP R0x35 = 0xFF01.

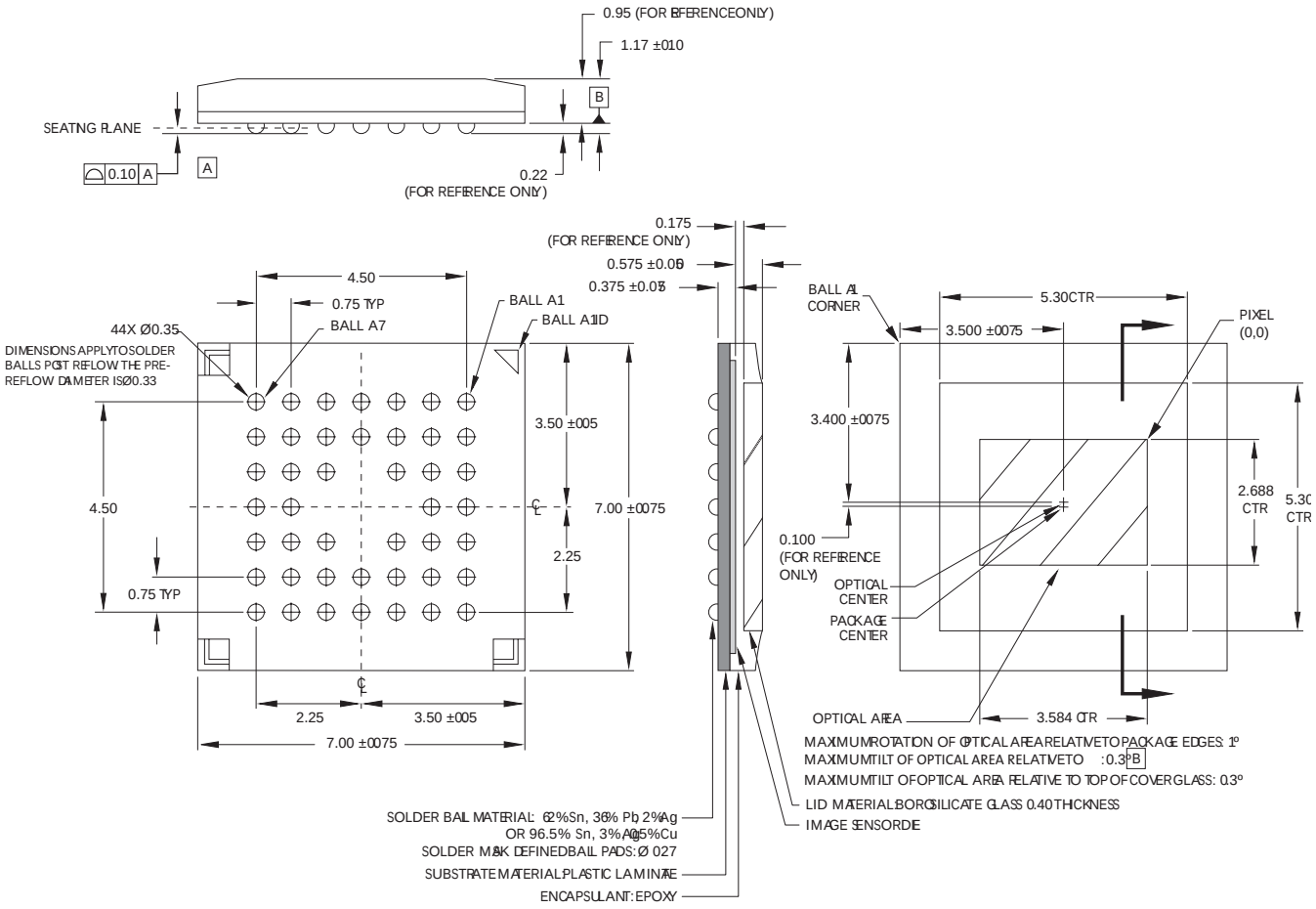
Table 16: YCbCr Settings

Gamma	0.45	0.5	0.55	0.6 (Default)	0.7	1.0
IFP R0x53	0x3224	0x2A1D	0x2318	0x1E14	0x150D	0x804
IFP R0x54	0x5D44	0x543B	0x4C34	0x452D	0x3923	0x2010
IFP R0x55	0x987F	0x9277	0x8C70	0x8669	0x785D	0x6040
IFP R0x56	0xC0AE	0xBDA9	0xBAA4	0xB7A0	0xB097	0xA080
IFP R0x57	0xE0D0	0xE0CF	0xE0CD	0xE0CC	0xE0C9	0xE0C0

Table 17: YUV Settings

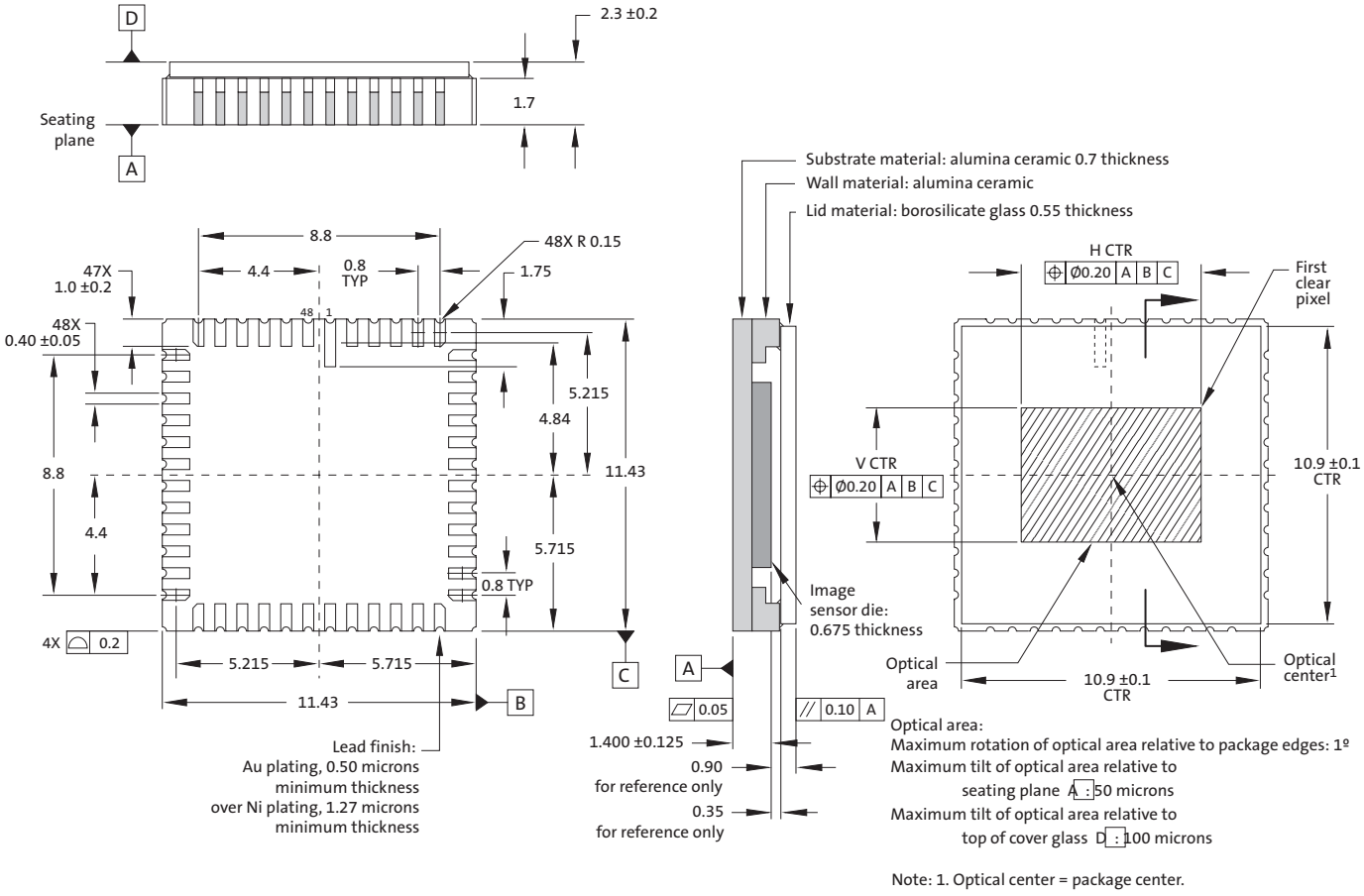
Gamma	0.45	0.5	0.55	0.6	0.7	1.0
IFP R0x53	0x3829	0x3021	0x281B	0x2216	0x180F	0x0904
IFP R0x54	0x3021	0x6043	0x573B	0x4F34	0x4128	0x2412
IFP R0x55	0xAD90	0xA687	0x9F7F	0x9877	0x8C69	0x6C48
IFP R0x56	0xDAC5	0xD6C0	0xD3BA	0xCFB5	0xC8AB	0xB591
IFP R0x57	0xFEEC	0xFEEB	0xFEE9	0xFEE7	0xFEE4	0xFED9

Figure 28: 44-Ball ICSP Package Outline



Notes:
1. All dimensions in millimeters.
2. ICSP package information is preliminary.

Figure 29: 48-Pin CLCC Package Outline



Note: All dimensions in millimeters.

Revision History

Rev. E 6/2/10

- Updated to non-confidential

Rev. D 5/6/10

- Updated to Aptina template

Rev. C 2/1/08

- Changed operating temperature on Table 1 on page 1 from –20°C to +60°C to –20°C to +70°C.
- Changed register description for registers 48, 49, 50, 76, and 77 in Table 8 (on page 14).
- Added registers R0x1F, R0x20, R0x24, R0x2A, R0x30, R0x31, R0x32, R0x36, R0x37, r0x39, R0x3C, R0x3D, R0x3E, R0x46, R0x4C, R0x4D, R0x59, R0x5A, R0x5C, R0x5D, R0x80, R0x81, R0x82, R0x83, R0x84, R0x85, R0x86, R0x87, R0x88, R0x89, R0x8A, R0x8B, R0x8C, R0x8D, R0x8E, R0x8F, R0x90, R0x91, R0x92, R0x93, R0x94, and R0x95 to Table 9, IFP Register Description.
- Updated Figure 14: “Typical Spectral Characteristics,” on page 19.
- Added Figure 16: “Chief Ray Angle (CRA) vs. Image Height,” on page 20.
- Added last sentence of first paragraph in “Auto Exposure” on page 28.
- Updated signal names to new standard:
  - Changed OE# to OE_BAR
  - Changed RESET# to RESET_BAR
  - Changed VAAPIX to VAA_PIX

Rev. B 3/5/07

- Fixed typos.
- Updated document with hexadecimal format for registers.
- Added Table 4 on page 9 for CLCC package.
- Added Figure 29 on page 32 for CLCC package.
- Updated Figure 11 on page 17, Table 9 on page 16, and Figure 13 on page 18.
- Updated Figure 14 on page 19.
- Updated Figure 18 on page 24.

Rev. A 5/06

- Initial release.

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