MRF24J40
Data Sheet

IEEE 802.15.4™ 2.4 GHz RF Transceiver

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MRF24J40

IEEE 802.15.4™ 2.4 GHz RF Transceiver

Devices Included:

- MRF24J40

Features:

- Complete IEEE 802.15.4 Specification Compliant
- Supports MiWi™, ZigBee™ and Proprietary Protocols
- Simple, 4-Wire SPI Interface
- Integrated 20 MHz and 32.768 kHz Oscillator Drive
- 20 MHz Reference Clock Output:
  - Available to drive microcontroller oscillator
- Supports Power-Saving mode
- Low-Current Consumption, Typical 18 mA in RX mode and 22 mA in TX mode
- Typical 2 μA Sleep mode
- Small, 40-Pin Leadless QFN 6x6 mm^2 Package

RF/Analog Features:

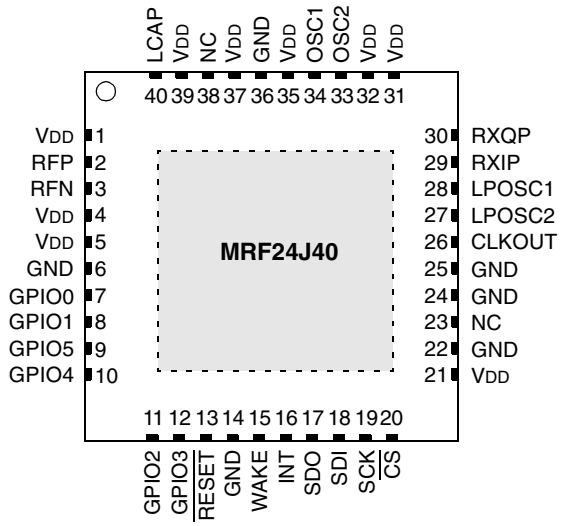
- ISM Band 2.405-2.48 GHz Operation
- -91 dBm Typical Sensitivity and +5 dBm Maximum Input Level
- +0 dBm Typical Output Power and 38.75 dB TX Power Control Range
- Differential RF Input/Output and Integrated TX/RX Switch
- Integrated Low Phase Noise VCO, Frequency Synthesizer and PLL Loop Filter
- Digital VCO and Filter Calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High Receiver and RSSI Dynamic Range

MAC/Baseband Features:

- Hardware CSMA-CA Mechanism, Automatic ACK Response and FCS Check
- Independent Beacon, Transmit and GTS FIFO
- Hardware Security Engine (AES-128) with CTR, CCM and CBC-MAC modes
- Supports all CCA modes and RSS/LQI
- Automatic Packet Retransmit Capability
- Supports In-Line or Stand-Alone modes for both Encryption and Decryption

Pin Diagram:

40-Pin QFN



Note: Backside center pad is GND.

Table of Contents

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1.0 OVERVIEW

The MRF24J40 is an IEEE 802.15.4-2003 compliant transceiver supporting MiWi™, ZigBee™ and other proprietary protocols. The MRF24J40 integrates wireless RF, PHY layer baseband and MAC layer architectures that can be combined with a simple microprocessor to apply low data rate to a multitude of applications that include home automation, consumer electronics, PC peripherals, toys, industrial automation and more. The MRF24J40 device integrates a receiver, transmitter, VCO and PLL into a single integrated circuit. It uses advanced radio architecture to minimize external part count and power consumption. The MRF24J40 MAC/baseband provides hardware architecture for both IEEE 802.15.4 MAC and PHY layers. It mainly consists of TX/RX FIFOs, a CSMA-CA controller, superframe constructor, receive frame filter, security engine and digital signal processing module. The MRF24J40 is fabricated by advanced 0.18 μm CMOS process and is offered in a 40-pin QFN 6x6 mm^2 package.

Features are summarized in Table 1-1 and the pinout for this device is listed in Table 1-2.

The MRF24J40 consists of four major functional blocks:

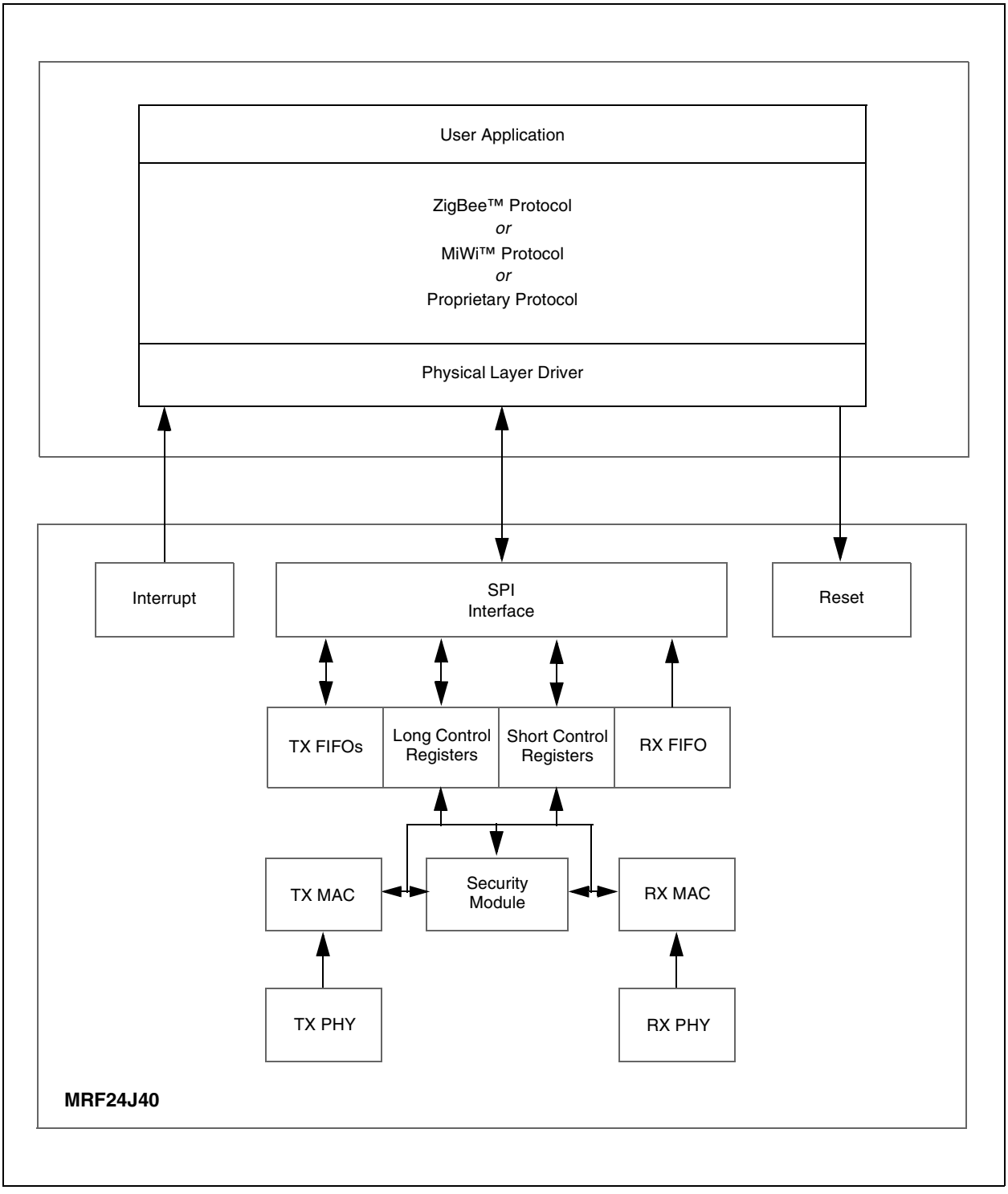
1. An SPI interface that serves as a communication channel between the host controller and the MRF24J40.
2. Control registers which are used to control and monitor the MRF24J40.
3. The MAC (Medium Access Control) module that implements IEEE 802.3™ compliant MAC logic.
4. The PHY (Physical Layer) driver that encodes and decodes the analog data.

The device also contains other support blocks, such as the on-chip voltage regulator, security module and system control logic.

TABLE 1-1: DEVICE FEATURES FOR THE MRF24J40 (40-PIN DEVICE)

Features	MRF24J40
IEEE 802.15.4™ Specification Compliant	Yes
Integrated Oscillator Drive	20 MHz and 32.768 kHz
Reference Clock Output	20 MHz
Power-Saving Mode Support	Yes
Current Consumption	Typical 18 mA in RX and 22 mA in TX
Sleep Mode	2 μA Typical
Serial Communications	SPI (4-wire)
Packages	40-Pin Leadless QFN 6x6 mm^2

FIGURE 1-1: MRF24J40 ARCHITECTURE BLOCK DIAGRAM



1.1 Pin Descriptions

TABLE 1-2: MRF24J40 PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
2	RFP	AIO	Differential RF input/output (+).
3	RFN	AIO	Differential RF input/output (-).
4	VDD	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
5	VDD	Power	Guard ring power supply. Bypass with a capacitor as close to the pin as possible.
6	GND	Ground	Guard ring ground.
7	GPIO0	DIO	General purpose digital I/O, also used as external PA enable.
8	GPIO1	DIO	General purpose digital I/O, also used as external TX/RX switch control.
9	GPIO5	DIO	General purpose digital I/O.
10	GPIO4	DIO	General purpose digital I/O.
11	GPIO2	DIO	General purpose digital I/O, also used as external TX/RX switch control.
12	GPIO3	DIO	General purpose digital I/O.
13	$\overline{\text{RESET}}$	DI	Global hardware Reset pin active-low.
14	GND	Ground	Ground for digital circuit.
15	WAKE	DI	External wake-up trigger.
16	INT	DO	Interrupt pin to microcontroller.
17	SDO	DIO	Serial interface data output from MRF24J40.
18	SDI	DIO	Serial interface data input to MRF24J40.
19	SCK	DI	Serial interface clock.
20	$\overline{\text{CS}}$	DI	Serial interface enable.
21	VDD	Power	Digital circuit power supply. Bypass with a capacitor as close to the pin as possible.
22	GND	Ground	Ground for digital circuit.
23	NC	—	No Connection, do not connect anything to this pin.
24	GND	Ground	Ground for digital circuit.
25	GND	Ground	Ground for digital circuit.
26	CLKOUT	DIO	20/10/5/2.5 MHz clock output.
27	LPOSC2	AI	32 kHz crystal input (-).
28	LPOSC1	AI	32 kHz crystal input (+).
29	RXIP	AO	Analog RX I channel output (+).
30	RXQP	AO	Analog RX Q channel output (+).
31	VDD	Power	Power supply for band gap reference circuit. Bypass with a capacitor as close to the pin as possible.
32	VDD	Power	Power supply for analog circuit. Bypass with a capacitor as close to the pin as possible.
33	OSC2	AI	20 MHz crystal input (-).
34	OSC1	AI	20 MHz crystal input (+).
35	VDD	Power	PLL power supply. Bypass with a capacitor as close to the pin as possible.
36	GND	Ground	Ground for PLL.
37	VDD	Power	Charge pump power supply. Bypass with a capacitor as close to the pin as possible.
38	NC	—	No Connection.
39	VDD	Power	VCO supply. Bypass with a capacitor as close to the pin as possible.
40	LCAP	—	PLL loop filter external capacitor. Connected to external 180 pF capacitor.

Legend: A = Analog, D = Digital, I = Input, O = Output

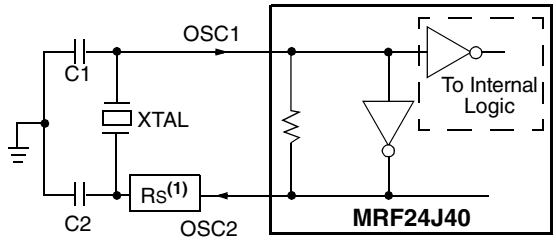
NOTES:

2.0 EXTERNAL CONNECTIONS

2.1 Oscillator

The MRF24J40 is designed to operate at 20 MHz with a crystal connected to the OSC1 and OSC2 pins. A typical oscillator circuit is shown in Figure 2-1.

FIGURE 2-1: CRYSTAL OSCILLATOR OPERATION



Note 1: A series resistor (RS) may be required for AT strip cut crystals.

2.2 Oscillator Start-up

The MRF24J40 PHY has an internal PLL that must lock before the device is capable of transmitting or receiving packets. After a full Power-on Reset, the device requires 2 ms to lock. During this delay, all registers and buffer memory may still be read and written to through the SPI bus. However, software should not attempt to transmit any packets (set the TXRTS (TXNMTRIG<0>)), or access any MAC or PHY registers during this period.

2.3 CLKOUT Pin

The clock out pin is provided to the system designer for use as the host controller clock or as a clock source for other devices in the system. The CLKOUT has an internal prescaler which can divide the output by 1, 2, 4 or 8. The CLKOUT function is enabled via the CLKCTRL register (Register 2-1) and the prescaler is selected via the RFCTRL7 register (Register 2-2).

REGISTER 2-1: CLKCTRL: DIVIDED SLEEP CLOCK (50 kHz) SELECTION REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	—	$\overline{\text{CLKOEN}}$	SCLKDIV<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Maintain as '0'

bit 6 **Unimplemented:** Read as '0'

bit 5 **$\overline{\text{CLKOEN}}$:** 20 MHz Clock Output Enable bit
1 = Disable
0 = Enable

bit 4-0 **SCLKDIV4:SCLKDIV0:** Divided SLPCLK Selection bits
Divided by 2^n.

REGISTER 2-2: RFCTRL7: RF CONTROL REGISTER 7

R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
SLPCLK<7:6>		—	—	—	—	CLKDIV<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SLPCLK7:SLPCLK6:** Sleep Clock Selection bits
00 = None
01 = External crystal
10 = Internal ring oscillator
11 = Reserved

bit 5-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKDIV1:CLKDIV0:** MRF24J40 Clock Output Frequency bits
00 = 2.5 MHz
01 = 5 MHz
10 = 10 MHz
11 = 20 MHz

To create a clean clock signal, the CLKOUT pin is held low for a period when power is first applied. After the Power-on Reset ends, the Oscillator Start-up Timer (OST) will begin counting. When the OST expires, the CLKOUT pin will begin outputting its default frequency of 2.5 MHz (main clock divided by 8).

2.4 RF Output

RFP and RFN are the differential RF input/output pins. These pins are connected to the antenna of the system, as seen in the example circuit diagram in Figure A-1. L5 is an RF choke. This inductor filters out non 2.4 GHz voltages. L3, L4, C37 and C43 act as a balun. The balun converts a differential unbalanced input and converts it to a balanced singled-ended output and visa versa. L1, C23 and C38 form a pi-type matching circuit to match the impedance of the balun to the impedance of the antenna. This circuit is not required if the impedance of the balun matches the antenna impedance. Refer to **Appendix A.1 "Layout Considerations and RF Measurements"** for more details about board layout and part selection concerning the RF output pins.

3.0 MEMORY ORGANIZATION

All memory in the MRF24J40 is implemented as static RAM. There are five types of memory in the MRF24J40:

- Short Address Control Registers
- Long Address Control Registers
- Transmit Buffers
- Receive Buffers
- Security Buffer

The control registers, both long and short, are used for configuration, control, and status retrieval of the MRF24J40. The control registers are directly read and written to by the SPI interface. The transmit and receive buffers contain transmit and receive memory used by the controller to transmit and receive data.

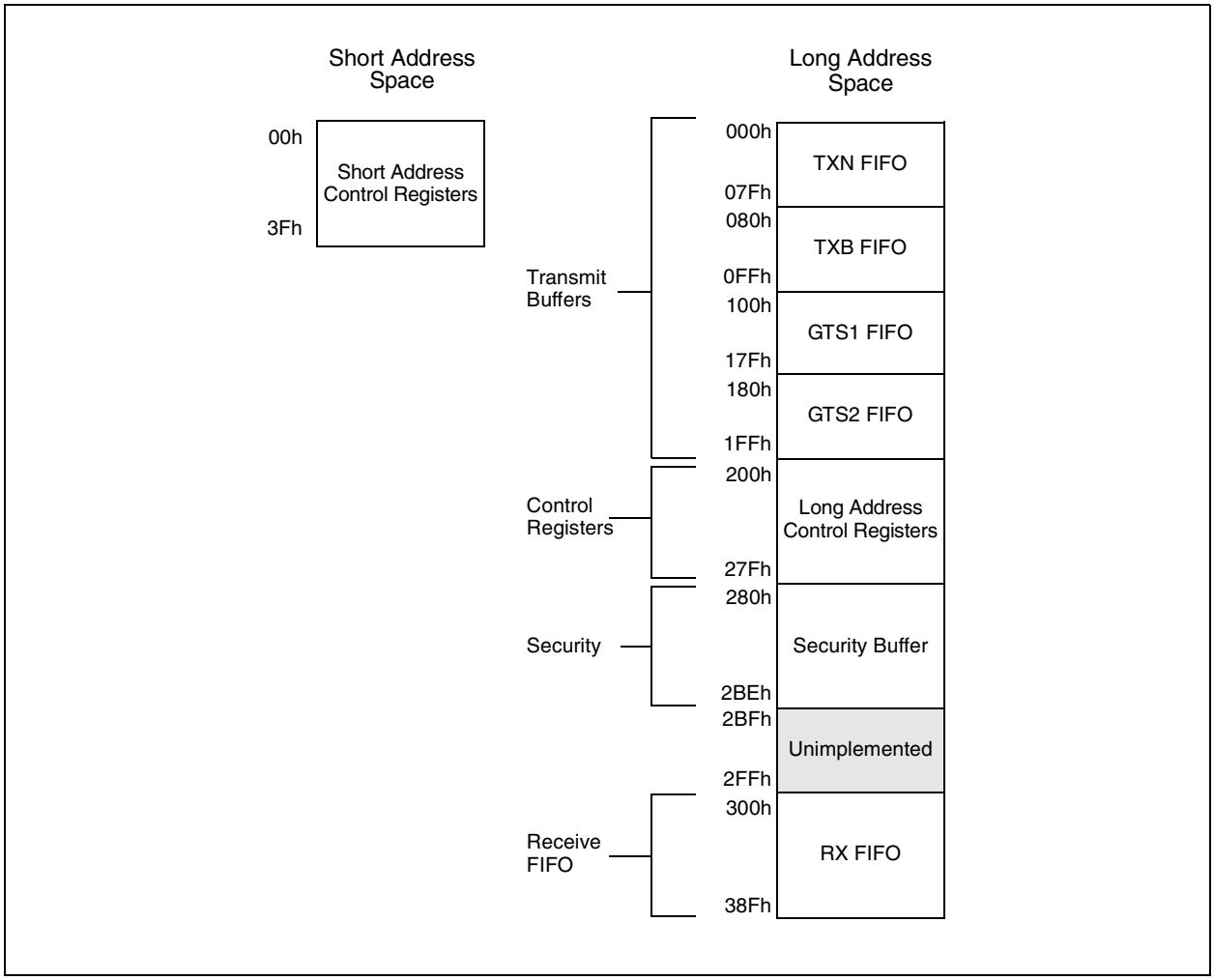
The security buffer provides an engine for the MRF24J40 MAC, which is compatible with the IEEE 802.15.4 LR-WPAN (ZigBee). The security buffer contains the following features:

- Transmit encryption and receive decryption.
- Seven-mode security suite.
- 64 x 8-bit security RAM for security suite storing; one receive key and three transmit keys for TX FIFOs. Beacon FIFO and GTS2 FIFO share the same key space since they will not conflict with each other. Normal FIFO and GTS1 FIFO both have their own transmit key.
- Security of APL and NWK layers can be achieved using the same engine. The upper layer security function is compliant to the ZigBee V1.0 and ZigBee 2006 specifications.

The SPI interface used to write and read these registers is described in **Section 4.0 "Serial Peripheral Interface (SPI)"**.

Figure 3-1 shows the data memory organization for the MRF24J40.

FIGURE 3-1: MRF24J40 MEMORY SPACE



3.1 Control Registers

The control registers provide the main interface between the host controller and the on-chip RF controller logic. Writing to these registers controls the operation of the interface, while reading the registers allows the host controller to monitor operations.

The control register memory is partitioned into the short address control register section and the long address control register section.

All reserved registers may be read but their contents must not be changed. When reading and writing to registers which contain reserved bits, any rules stated in the register definition should be observed.

FIGURE 3-2: MRF24J40 SHORT ADDRESS CONTROL REGISTER MAPPING

00h	RXMCR	10h	—	20h	—	30h	—
01h	PANIDL	11h	—	21h	—	31h	ISRSTS
02h	PANIDH	12h	—	22h	—	32h	INTMSK
03h	SADRL	13h	—	23h	—	33h	GPIO
04h	SADRH	14h	—	24h	TXSR	34h	TRISGPIO
05h	EADR0	15h	—	25h	—	35h	—
06h	EADR1	16h	—	26h	—	36h	RFCTL
07h	EADR2	17h	—	27h	—	37h	—
08h	EADR3	18h	—	28h	—	38h	—
09h	EADR4	19h	—	29h	—	39h	—
0Ah	EADR5	1Ah	—	2Ah	—	3Ah	BBREG2
0Bh	EADR6	1Bh	TXNMTRIG	2Bh	—	3Bh	—
0Ch	EADR7	1Ch	—	2Ch	—	3Ch	—
0Dh	RXFLUSH	1Dh	—	2Dh	—	3Dh	—
0Eh	—	1Eh	—	2Eh	—	3Eh	BBREG6
0Fh	—	1Fh	—	2Fh	—	3Fh	RSSITHCCA

FIGURE 3-3: MRF24J40 LONG ADDRESS CONTROL REGISTER MAPPING

200h	RFCTRL0	210h	—	220h	CLKCTRL	230h	—	240h	—
201h	—	211h	CLKINTCR	221h	—	231h	—	241h	—
202h	RFCTRL2	212h	—	222h	—	232h	—	242h	—
203h	RFCTRL3	213h	—	223h	—	233h	—	243h	—
204h	—	214h	—	224h	—	234h	—	244h	—
205h	—	215h	—	225h	—	235h	—	245h	—
206h	RFCTRL6	216h	—	226h	—	236h	—	246h	—
207h	RFCTRL7	217h	—	227h	—	237h	—	247h	—
208h	RFCTRL8	218h	—	228h	—	238h	—	248h	—
209h	—	219h	—	229h	—	239h	—	249h	—
20Ah	—	21Ah	—	22Ah	—	23Ah	—	24Ah	—
20Bh	—	21Bh	—	22Bh	—	23Bh	—	24Bh	—
20Ch	—	21Ch	—	22Ch	—	23Ch	—	24Ch	—
20Dh	—	21Dh	—	22Dh	—	23Dh	—		
20Eh	—	21Eh	—	22Eh	—	23Eh	—		
20Fh	—	21Fh	—	22Fh	—	23Fh	—		

3.2 MRF24J40 Address Summary

TABLE 3-1: REGISTER FILE SHORT ADDRESS SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on page:
RXMCR	$\overline{\text{TXCRCEN}}$	BBLPBK	$\overline{\text{ACKEN}}$	MACLPBK	PANCOORD	COORD	$\overline{\text{RXCRCEN}}$	PROMI	0000 0000	21
PANIDL	MAC PAN Low Byte (PANL<7:0>)								0000 0000	26
PANIDH	MAC PAN High Byte (PANH<15:8>)								0000 0000	26
SADRL	MAC Short Address Low Byte (SADDRL<7:0>)								0000 0000	27
SADRH	MAC Short Address High Byte (SADDRH<15:8>)								0000 0000	27
EADR0	LSB of EUI (EADR0<7:0>)								0000 0000	26
EADR1	Byte 2 of EUI (EADR1<15:8>)								0000 0000	26
EADR2	Byte 3 of EUI (EADR2<23:16>)								0000 0000	26
EADR3	Byte 4 of EUI (EADR3<31:24>)								0000 0000	26
EADR4	Byte 5 of EUI (EADR4<39:32>)								0000 0000	26
EADR5	Byte 6 of EUI (EADR5<47:40>)								0000 0000	26
EADR6	Byte 7 of EUI (EADR6<55:48>)								0000 0000	26
EADR7	MSB of EUI (EADR7<63:56>)								0000 0000	26
RXFLUSH	—	r	r	$\overline{\text{RXWRTBLK}}$	CMDONLY	DATAONLY	BCNONLY	RXFLUSH	-000 0000	34
TXNMTRIG	—	—	—	PENDACK	INDIRECT	ACKREQ	SECEN	TXRTS	---0 0000	30
TXSR	TXRETRY<7:6>		CCAFAIL	r	r	r	r	r	0000 0000	31
ISRSTS	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	GTS2TXIF	GTS1TXIF	TXIF	0000 0000	36
INTMSK	SLPMSK	WAKEMSK	HSYMTMRMSK	SECMSK	RXMSK	GTS2TXMSK	GTS1TXMSK	TXMSK	1111 1111	37
GPIO	—	—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	--00 0000	39
TRISGPIO	—	—	TRISGP5	TRISGP4	TRISGP3	TRISGP2	TRISGP1	TRISGP0	--00 0000	40
RFCTL	r	—	—	r	r	RFRST	r	r	0--0 0000	24
BBREG2	CCAMODE<7:6>		CCATHRES<5:2>				—	—	0000 00--	25
BBREG6	RSSIREQ	RXRSSI	r	r	r	r	r	RSSIRDY	0000 0001	25
RSSITHCCA	RSSITHRES<7:0>								0000 0000	23

Legend: - = unimplemented, r = reserved. Shaded cells are unimplemented, read as '0'.

TABLE 3-2: REGISTER FILE LONG ADDRESS SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Details on page:
RFCTRL0	CHANNEL<7:4>				—	—	—	—	0000 ----	24
RFCTRL2	RFPLL	r	r	r	r	—	—	—	0000 0---	22
RFCTRL3	TXPOWER<7:3>					—	—	—	0000 0---	22
RFCTRL6	TXFIL	—	r	r	BATMONEN	—	—	—	0-00 0---	23
RFCTRL7	SLPCLK<7:6>		—	—	—	—	CLKDIV<1:0>		00-- --00	8
RFCTRL8	—	—	—	RF_VCO	—	—	—	SLPCLKOUT	---0 ---0	23
CLKINTCR	—	—	—	—	—	—	INTEDGE	$\overline{\text{SLPCLKEN}}$	---- --00	38
CLKCTRL	r	—	$\overline{\text{CLKOEN}}$	SCLKDIV<4:0>					0-00 0000	7

Legend: - = unimplemented, r = reserved. Shaded cells are unimplemented, read as '0'.

NOTES:

4.0 SERIAL PERIPHERAL INTERFACE (SPI)

4.1 Overview

The MRF24J40 is designed to interface directly with the Serial Peripheral Interface (SPI) port available on many microcontrollers. The implementation used on this device supports SPI mode 0,0 only. In addition, the SPI port requires that SCK be Idle in a low state; selectable clock polarity is not supported.

Commands and data are sent to the device via the SDI pin, with data being clocked in on the rising edge of SCK. Data is driven out by the MRF24J40 on the SDO line, on the falling edge of SCK. The $\overline{CS}$ pin must be held low while any operation is performed and returned high when finished.

The MRF24J40 accesses the short and long RAM banks in a slightly different manner. The following sections describe the required waveforms in order to read and write from both short and long RAM addresses.

FIGURE 4-1: SPI INPUT TIMING

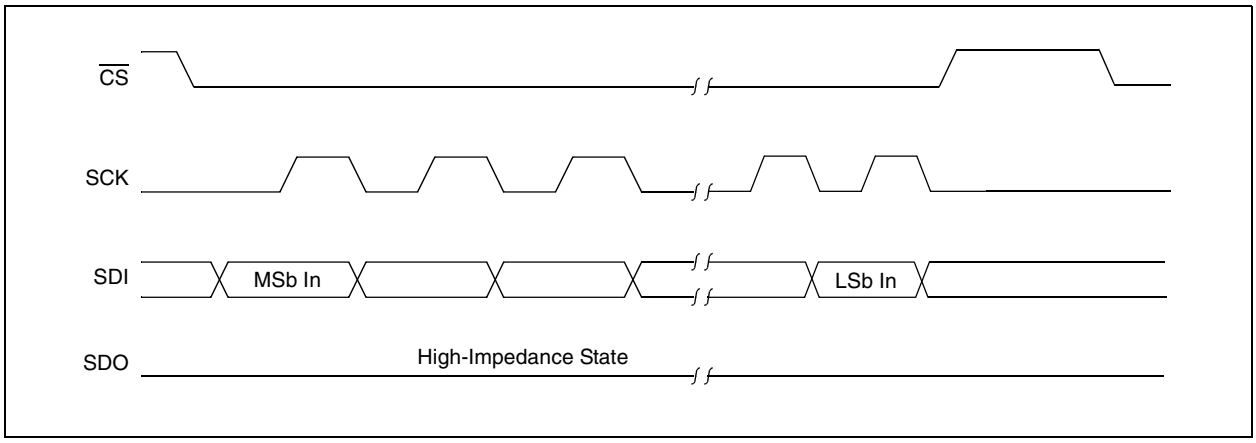
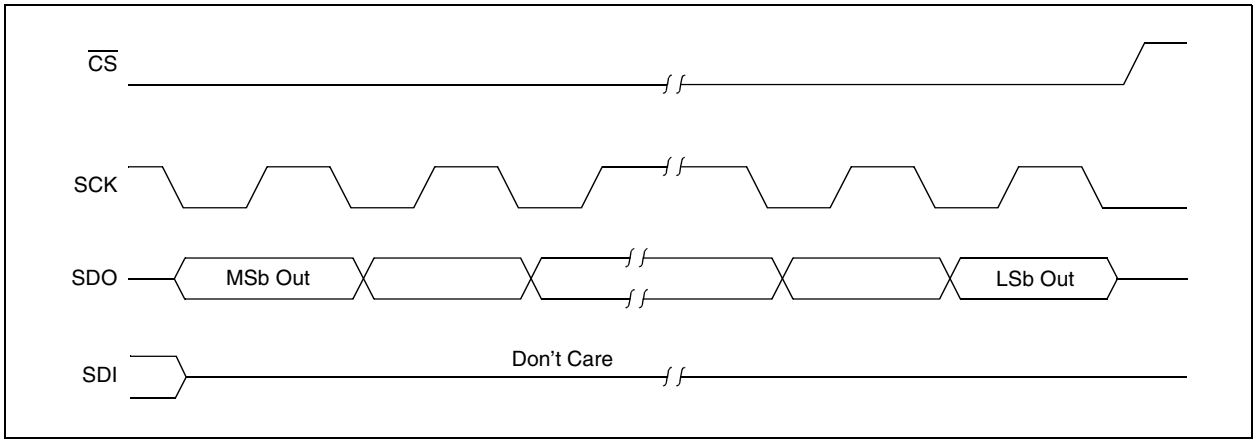


FIGURE 4-2: SPI OUTPUT TIMING

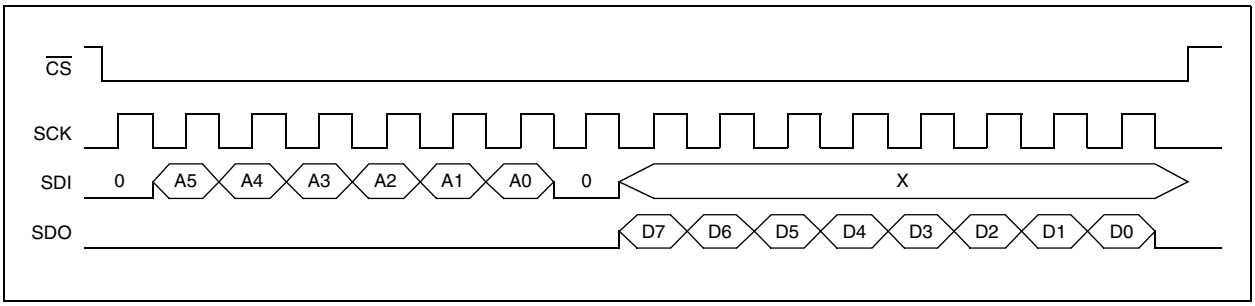


4.2 Short Address Register Interface

4.2.1 READING SHORT ADDRESS REGISTERS

The short address space is accessed by sending a '0' as the first bit of the SPI transfer. The following 6 bits are the address of the target register. The final bit of the first byte is a '0' to indicate that the command is a read. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

FIGURE 4-3: SHORT ADDRESS READ



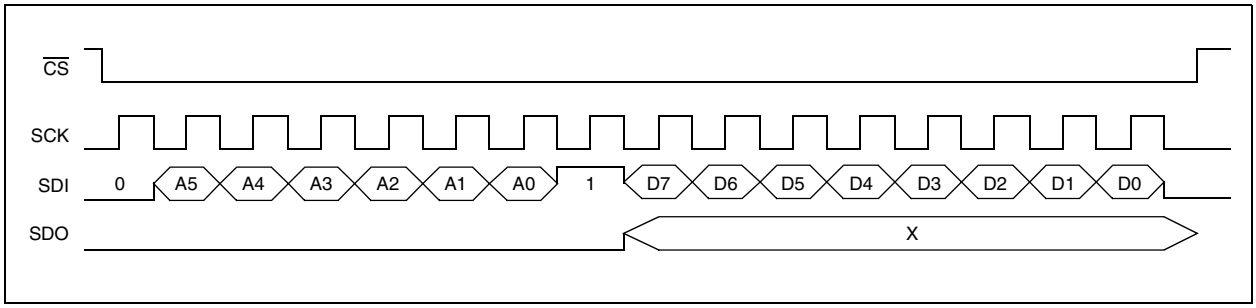
EXAMPLE 4-1: SHORT ADDRESS READ EXAMPLE

```
BYTE GetShortRAMAddress(BYTE address)
{
       BYTE toReturn;
       CSn = 0;
       SPIPut((address<<1)&0b01111110);
       toReturn = SPIGet();
       CSn = 1;
       return toReturn;
}
```


4.2.2 WRITING SHORT ADDRESS REGISTERS

The short address space is accessed by sending a '0' as the first bit of the SPI transfer. The following 6 bits are the address of the target register. The final bit of the first byte is a '1' to indicate that the command is a write. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

FIGURE 4-4: SHORT ADDRESS WRITE



EXAMPLE 4-2: SHORT ADDRESS WRITE EXAMPLE

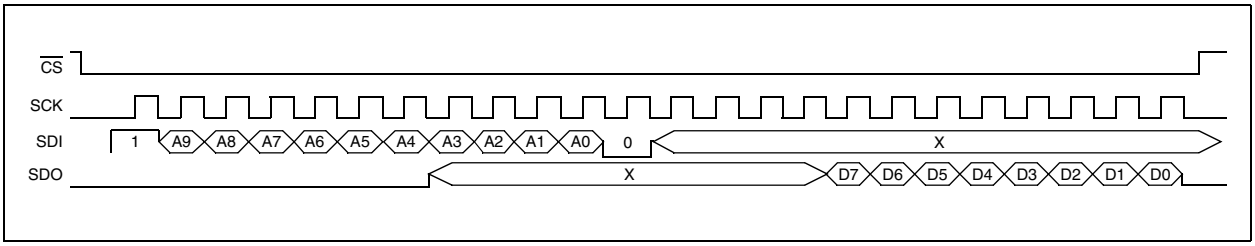
```
void SetShortRAMAddress(BYTE address, BYTE value)
{
       CSn = 0;
       SPIPut(((address<<1)&0b01111111)|0x01);
       SPIPut(value);
       CSn = 1;
}
```

4.3 Long Address Register Interface

4.3.1 READING LONG ADDRESS REGISTERS

The long address space is accessed by sending a '1' as the first bit of the SPI transfer. The following 10 bits are the address of the target register. The final bit is a '0' to indicate that the command is a read. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

FIGURE 4-5: LONG ADDRESS READ



EXAMPLE 4-3: LONG ADDRESS READ EXAMPLE

```
BYTE GetLongRAMAddress(WORD address)
{
       BYTE toReturn;
       CSn = 0;
       SPIPut(((address>>3)&0b01111111)|0x80);
       SPIPut(((address<<5)&0b11100000));
       toReturn = SPIGet();
       CSn = 1;
       return toReturn;
}
```

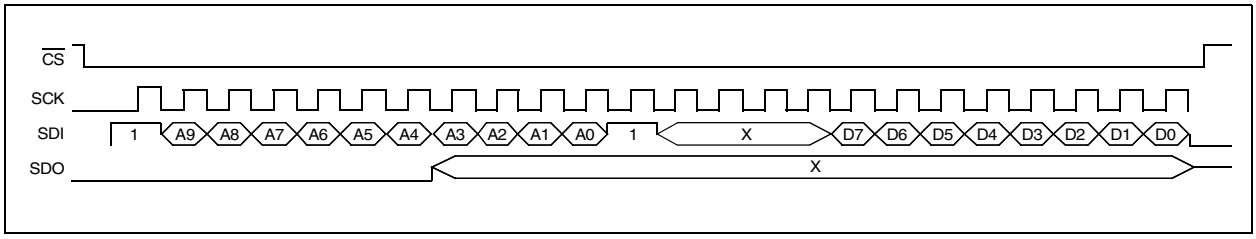

4.3.2 WRITING LONG ADDRESS REGISTERS

The long address space is accessed by sending a '1 ' as the first bit of the SPI transfer. The following 10 bits are the address of the target register. The final bit is a '1 ' to indicate that the command is a write. On the next clock edge of SCK, the Most Significant bit of the register will shift out, followed by the rest of the bits.

4.4 Buffer Interface

The receive and transmit buffers in the MRF24J40 are located in the long RAM address space. These buffers are accessed using the same process as accessing the long RAM control addresses. The received buffer is read-only and should not be written to. The use of these buffers is described in **Section 7.0 "Transmitting and Receiving Packets"**.

FIGURE 4-6: LONG ADDRESS WRITE



EXAMPLE 4-4: LONG ADDRESS WRITE EXAMPLE

```
void SetLongRAMAddress(WORD address, BYTE value)
{
       CSn = 0;
       SPIPut((((BYTE)(address>>3))&0b01111111)|0x80);
       SPIPut((((BYTE)(address<<5))&0b11100000)|0x10);
       SPIPut(value);
       CSn = 1;
}
```

NOTES:

5.0 IEEE 802.15.4™-2003

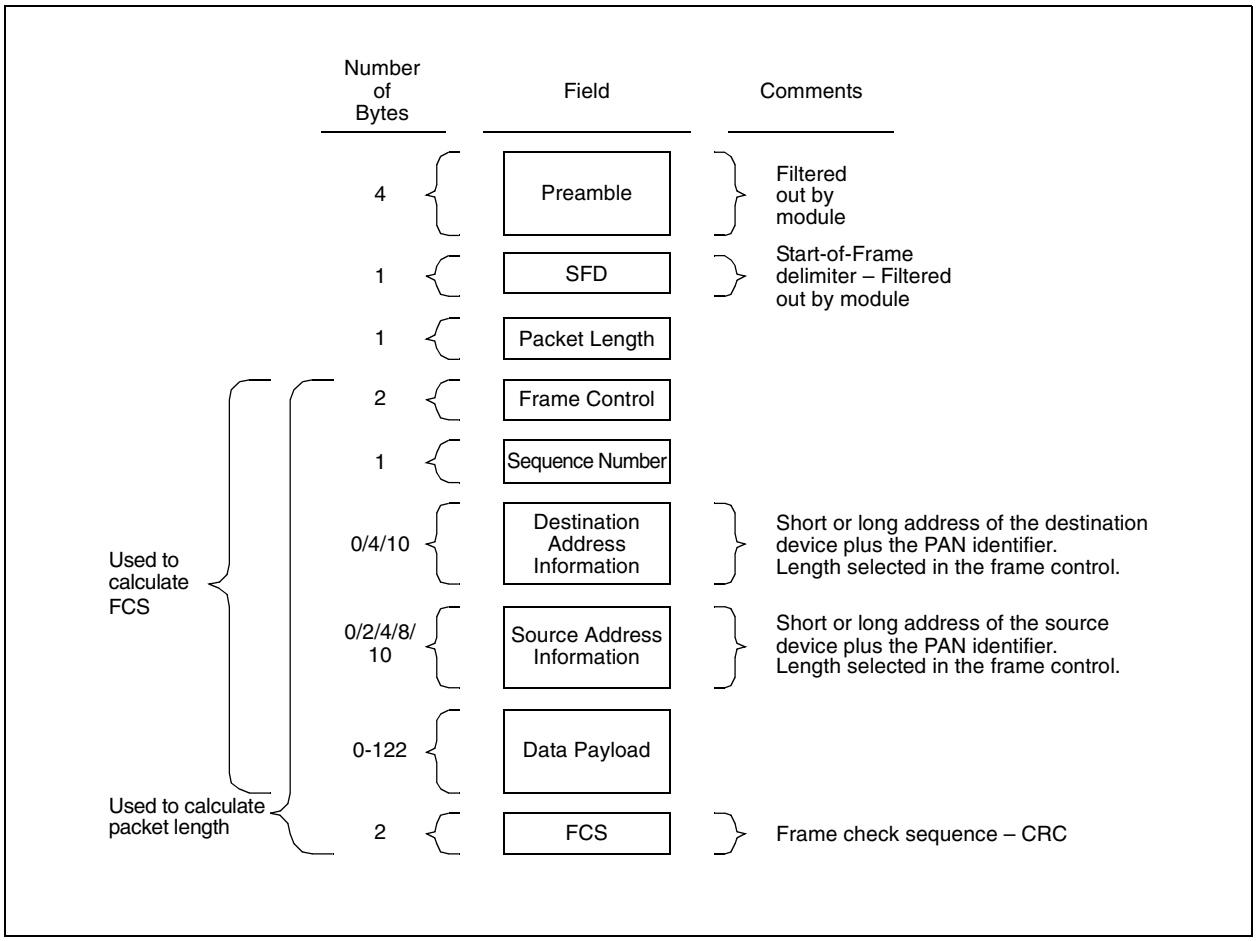
5.1 Overview

Before discussing the use of the MRF24J40, it may be helpful to review the structure of a typical data frame. Users requiring more information should refer to the IEEE 802.15.4 Standard.

5.2 Packet Format

Normal IEEE 802.15.4 compliant packets are between 5 and 127 bytes long. They are made up of several possible fields: destination address information, source address information, a length field, data payload and a Cyclic Redundancy Check (CRC). Additionally, a 4-byte preamble field and Start-of-Frame Delimiter (SFD) byte are appended to the beginning of the packet. Thus, traffic seen on the air will appear as shown in Figure 5-1.

FIGURE 5-1: PACKET FORMAT



5.2.1 PREAMBLE/START-OF-FRAME DELIMITER

When transmitting and receiving data with the MRF24J40, the preamble and Start-of-Frame delimiter bytes will automatically be generated or stripped from the packets when they are transmitted or received. The host controller does not need to concern itself with them. Normally, the host controller will also not need to concern itself with the CRC, which the MRF24J40 will also be able to automatically generate when transmitting and verify when receiving. The CRC fields will, however, be written into the receive buffer when packets arrive, so they may be evaluated by the host controller if needed.

5.2.2 LENGTH

The length field is a 1-byte field which defines the size of the packet excluding itself, the preamble and SFD, but including all other bytes of the packet, including FCS.

5.2.3 FRAME CONTROL

The frame control field describes the format of this packet. It defines the type of packet (beacon, data, ACK, etc.) the addressing modes used, if the packet is encrypted or not, if the packet requires an ACK and if the packet is an intra-PAN network. This information is used by the host controller to determine how to decipher the data that follows the frame control field.

5.2.4 SEQUENCE NUMBER

The sequence number field is a 1-byte sequence number that distinguishes packets. The sequence number field is used in the Acknowledgement process. An ACK packet contains no addressing information, so the uniqueness of the sequence number is the sole determining factor for verifying that a packet reached its destination. The MRF24J40 has an Auto-Acknowledgement feature that is described in **Section 7.1 "Transmitting Packets"**.

5.2.5 DESTINATION ADDRESS INFORMATION

The destination address fields of an IEEE 802.15.4 packet can change depending on the frame control field of that packet. The frame control field can specify that no destination address is present, or can specify that the short address (2 bytes) or long address (8 bytes) is present. In all cases where an address is specified, the destination PAN identifier will also be included. On incoming packets, the MRF24J40 will filter out packets that do not match the preconfigured addressing information for that radio. This eliminates any software intervention for packets that do not meet the addressing requirements. When transmitting the host controller is required to write the appropriate destination address into the transmit buffer.

5.2.6 SOURCE ADDRESS INFORMATION

The source address fields of an IEEE 802.15.4 packet can change depending on the frame control field of that packet. The frame control field can specify that no destination address is present, or can specify that the short address (2 bytes) or long address (8 bytes) is present. The frame control can also specify, by using the intra-PAN bit, that the source PAN matches the destination PAN and is thus, not included in the packet.

Long addresses consist of two portions. The first three bytes are known as the Extended Organizationally Unique Identifier (EUI). EUIs are distributed by the IEEE 802.15.4. The last five bytes are address bytes which can contain the needed requirements at the discretion of the company that purchased the EUI.

When transmitting packets, the assigned source long or short address, depending on the setting of the frame control field, must be written into the transmit buffer by the host controller. The MRF24J40 will not automatically include the source address information.

5.2.7 DATA

The data section of the packet can vary in length from 0 bytes to 122 bytes. Packets that exceed 127 bytes, including the frame control, source addressing, destination addressing, data and FCS fields, will be filtered out by the MRF24J40.

5.2.8 FCS

The FCS field is a 2-byte field which contains an industry standard, 16-bit CRC calculated with the data from the frame control, sequence number, destination, source, and data fields. When receiving packets, the MRF24J40 will check the CRC of each incoming packet. If the $\overline{\text{RXCRCEN}}$ bit (RXMCR<1>) is cleared, packets with invalid CRCs will automatically be discarded. If $\overline{\text{RXCRCEN}}$ is set, and the packet meets all other receive filtering criteria, the packet will be written into the receive buffer and the host controller will be able to determine if the CRC was valid by reading the receive status vector (see **Section 7.3 "Receiving Packets"**).

When transmitting packets, the MRF24J40 will automatically generate a valid CRC and transmit it attached to the end of the packet if the $\overline{\text{TXCRCEN}}$ bit (RXMCR<7>) is cleared.

6.0 INITIALIZATION

6.1 Overview

Before the MRF24J40 can be used to transmit and receive packets, certain device settings must be initialized. Depending on the application, some configuration options may need to be changed. Normally, these tasks may be accomplished once after Reset and do not need to be changed thereafter.

6.2 Receive Filters

To minimize the processing requirements of the host controller, the MRF24J40 incorporates several different receive filters which can automatically reject packets which are not needed. These options are controlled through the RXMCR register.

REGISTER 6-1: RXMCR: RECEIVE FILTER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
$\overline{\text{TXCRCEN}}$	r	$\overline{\text{ACKEN}}$	r	PANCOORD	COORD	$\overline{\text{RXCRCEN}}$	PROMI
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{TXCRCEN}}$:** No CRC Data with Normal FIFO bit
1 = CRC is disabled for the TX FIFO
0 = CRC is enabled for the TX FIFO

bit 6 **Reserved:** Maintain as '0'

bit 5 **$\overline{\text{ACKEN}}$:** No ACK Respond in Any Case bit
1 = ACK response is always disabled
0 = ACK response enabled. ACKs are returned when they are requested.

bit 4 **Reserved:** Maintain as '0'

bit 3 **PANCOORD:** PAN Coordinator bit
1 = Set as PAN coordinator
0 = Not set as PAN coordinator

bit 2 **COORD:** Coordinator bit
1 = Set as coordinator
0 = Not set as coordinator

bit 1 **$\overline{\text{RXCRCEN}}$:** Error Report bit
1 = RX all kinds of PKT (including CRC error)
0 = Only RX PKT (CRC ok)

bit 0 **PROMI:** RX All Kinds of PKT bit (CRC ok)
1 = RX all kinds of PKT (CRC ok)
0 = Discard PKT when there is a MAC address mismatch, illegal frame type, dPAN/sPAN or MAC short address mismatch

6.3 PHY Initialization

The physical layer of the MRF24J40 controls the current levels going to different sections of the device, as well as thresholds and controls used in packet reception and transmission. There are several registers that may require modification in order to operate in the application's intended mode.

Note:	The RSSI threshold defaults to '0', however, it can be set to a user-defined RSSI threshold limit. Please note, any RSSI value resulting from a CCA request that is below the RSSI threshold limit will result in a failure.

REGISTER 6-2: RFCTRL2: RF CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
RFPLL(1)	r	r	r	r	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **RFPLL:** RF-PLL Control bit(1)
1 = PLL enabled
0 = PLL disabled

bit 6-3 **Reserved:** Maintain as '0'

bit 2-0 **Unimplemented:** Read as '0'

Note 1: PLL must be enabled for RF reception or transmission.

REGISTER 6-3: RFCTRL3: RF CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
TXPOWER<7:3>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **TXPOWER7:TXPOWER3:** Small Scale Control for TX Power in dB bits
00000 = 0 dB
00001 = -1.25 dB
00010 = -2.5 dB
00011 = -3.75 dB
00100 = -5 dB
00101 = -6.25 dB
00110 = -7.5 dB
00111 = -8.75 dB
…
11111 = -38.75 dB

bit 2-0 **Unimplemented:** Read as '0'

REGISTER 6-4: RFCTRL6: RF CONTROL REGISTER 6

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
TXFIL	—	r	r	BATMONEN	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TXFIL:** TX Filter Control bit
Recommended value: '1'.

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **Reserved:** Maintain as '0'

bit 3 **BATMONEN:** Battery Monitor Enable bit
1 = Enabled
0 = Disabled

bit 2-0 **Unimplemented:** Read as '0'

REGISTER 6-5: RFCTRL8: RF CONTROL REGISTER 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
—	—	—	RF_VCO	—	—	—	SLPCLKOUT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **RF_VCO:** VCO Control bit
1 = Enhanced VCO (recommended)
0 = Normal VCO

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SLPCLKOUT:** 20 MHz Reference Output Clock Source bit
1 = Stabilize CLKOUT while recovering from Sleep
0 = Stabilize CLKOUT after a wake from Sleep

REGISTER 6-6: RSSITHCCA: RSSI THRESHOLD FOR CCA REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSSITHRES<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **RSSITHRES7:RSSITHRES0:** RSSI Threshold for CCA/ED Mode bits

6.4 MAC Initialization

The medium access control layer of the MRF24J40 consists of several registers that define how this device operates on an IEEE 802.15.4 network.

6.4.1 DEVICE CONFIGURATION

The RXMCR, described in **Section 6.2 "Receive Filters"**, should be set to the appropriate value for the intended device operation. If the device is operating as a PAN coordinator, the PANCOORD bit should be set. If the device is operating as a coordinator, then the COORD bit should be set.

6.4.2 CHANNEL SELECTION

The operational channel is selected using the RFCTRL0 register.

REGISTER 6-7: RFCTRL0: RF CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
CHANNEL<7:4>				—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CHANNEL7:CHANNEL4:** Channel Number bits
`00000` = Channel 11
`00001` = Channel 12
`00010` = Channel 13
…
`11111` = Channel 26

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 6-8: RFCTL: RF MODE CONTROL REGISTER

W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
r	—	—	r	r	RFRST	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Reserved:** Maintain as '0'

bit 6-5 **Unimplemented:** Read as '0'

bit 4-3 **Reserved:** Maintain as '0'

bit 2 **RFRST:** RF Reset bit
`1` = Reset RF (turn off RF)
`0` = Normal operation

bit 1-0 **Reserved:** Maintain as '0'

REGISTER 6-9: BBREG2: BASEBAND CCA/RSSI MODE REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
CCAMODE<7:6>		CCATHRES<5:2>				—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **CCAMODE7:CCAMODE6:** CCA Mode bits
00 = Reserved
01 = CCA Mode 1, carrier sense only
10 = CCA Mode 2, energy above threshold
11 = CCA Mode 3, carrier sense with energy above threshold

bit 5-2 **CCATHRES5:CCATHRES2:** CCA Carrier Sense Threshold bits
CCA/CS value set to 0xE or '1110'.

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 6-10: BBREG6: BASEBAND RSSI MODE REGISTER 6

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1
RSSIREQ	RXRSSI	r	r	r	r	r	RSSIRDY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **RSSIREQ:** RSSI Mode 1 bit
1 = Initiate an RSSI calculation (write back to '0' when complete)
0 = Otherwise

bit 6 **RXRSSI:** RSSI Mode 2 bit
1 = Calculating RSSI for RX packet
0 = No calculating RSSI for RX packet

bit 5-1 **Reserved:** Maintain as '0'

bit 0 **RSSIRDY:** RSSI Ready Signal Firmware Request bit
1 = RSSI value ready
0 = Otherwise

6.4.3 LONG ADDRESSES

Every device in the world has a unique long address. Long addresses are described in more detail in **Section 5.2.5 "Destination Address Information"** and **Section 5.2.6 "Source Address Information"**. EADR0-EADR7 are eight short RAM address registers in the MRF24J40 that are used to define the device's long address. These addresses should be loaded into the device during the device configuration. The MRF24J40 will automatically filter out any long address packets that do not match the contents of EADR0-EADR7.

6.4.4 SHORT ADDRESS AND PAN ID

The device's short address and PAN ID are programmed into the MRF24J40 through the SADRL, SADRH, PANIDL and PANIDH registers. These registers are located in the short RAM address space. The MRF24J40 automatically filters out packets that are specified as short address destinations with addresses that do not match these registers. The exception to this rule is packets with the broadcast short address (FFFFh) and/or the broadcast PAN ID (FFFFh). Packets that match the short address and have the broadcast PAN ID will be accepted, as well as packets with the broadcast short address that match the PAN ID. A true broadcast packet will have both the short address and PAN ID set to the broadcast address. The MRF24J40 will also receive these packets no matter what the setting of the short address and PAN ID registers.

Example 6-1 shows how to initialize the MRF24J40.

REGISTER 6-11: PANIDL: MAC PAN LOW BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MAC PAN Low Byte (PANL<7:0>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PANL7:PANL0:** Lower Byte of PAN Address bits

REGISTER 6-12: PANIDH: MAC PAN HIGH BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MAC PAN High Byte (PANH<15:8>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PANH15:PANH8:** Higher Byte of PAN Address bits

REGISTER 6-13: SADRL: MAC SHORT ADDRESS LOW BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MAC Short Address Low Byte (SADDRL<7:0>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SADDRL7:SADDRL0:** Lower Byte of Short Address bits

REGISTER 6-14: SADRH: MAC SHORT ADDRESS HIGH BYTE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MAC Short Address High Byte (SADDRH<15:8>)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SADDRH15:SADDRH8:** Higher Byte of Short Address bits

EXAMPLE 6-1: INITIALIZING THE MRF24J40

```
void MRF24J40Init(void)
{
    BYTE i;
    WORD j;

    /* place the device in hardware reset */
    RESETn = 0;
    for(j=0;j<(WORD)300;j++){}

    /* remove the device from hardware reset */
    RESETn = 1;
    for(j=0;j<(WORD)300;j++){}

    /* reset the RF module */
    SetShortRAMAddr(RFCTL,0x04);
    /* remove the RF module from reset */
    SetShortRAMAddr(RFCTL,0x00);

    /* flush the RX fifo */
    SetShortRAMAddr(WRITE_RXFLUSH,0x01);

    /* Program the short MAC Address, 0xffff */
    SetShortRAMAddr(SADRL,0xFF);
    SetShortRAMAddr(SADRH,0xFF);
    SetShortRAMAddr(PANIDL,0xFF);
    SetShortRAMAddr(PANIDH,0xFF);

    /* Program Long MAC Address*/
    for(i=0;i<(BYTE)8;i++)
    {
        SetShortRAMAddr(EADR0+i*2,myLongAddress[i]);
    }

    /* enable the RF-PLL */
    SetLongRAMAddr(RFCTRL2,0x80);

    /* set TX for max output power */
    SetLongRAMAddr(RFCTRL3,0x00);

    /* enabled TX filter control */
    SetLongRAMAddr(RFCTRL6,0x80);

    SetLongRAMAddr(RFCTRL8,0b00010000);

    /* Program CCA mode using RSSI */
    SetShortRAMAddr(BBREG2,0x78);
    /* Enable the packet RSSI */
    SetShortRAMAddr(BBREG6,0x40);

    /* Program CCA, RSSI threshold values */
    SetShortRAMAddr(RSSITHCCA,0x00);

    SetLongRAMAddr(RFCTRL0,0x00); //channel 11

    SetShortRAMAddr(RFCTL,0x04);  //reset the RF module with new settings
    SetShortRAMAddr(RFCTL,0x00);
}
```


7.0 TRANSMITTING AND RECEIVING PACKETS

7.1 Transmitting Packets

The MAC inside the MRF24J40 will automatically generate the preamble and Start-of-Frame delimiter fields when transmitting. Additionally, the MAC can generate any padding (if needed), and the CRC, if configured to do so. The host controller must generate and write all other frame fields into the buffer memory for transmission. Before transmitting packets, the MAC registers, which alter the transmission characteristics, should be initialized as documented in **Section 6.0 "Initialization"**.

7.2 TX FIFO Format

The TX MAC performs three major tasks conforming to IEEE 802.15.4:

- TX FIFO Control
- Automatic CSMA-CA and Timing Alignments
- Hardware Superframe Handling

For TX FIFO control function, TX MAC controls 4 FIFOs, including beacon, normal and 2 GTS FIFOs. When each FIFO is triggered, TX MAC performs a CSMA-CA algorithm, sends a packet to the Transmit Baseband (TXBB) at the right time, handles the retransmission if an ACK is required but not received and generates FCS bytes automatically.

The automatic CSMA-CA algorithm performs timing alignments, such as LIFS, SIFS and ACK turnaround time. The user can simply program parameters for the CSMA-CA algorithm. The TX MAC will perform automatically according these parameters.

For hardware superframe handling, TX MAC builds up the timing frame of a superframe. It includes CAP, CFP, INACTIVE and each time slot. TX MAC sends beacon, normal and GTS FIFOs at the right time, automatically, at each transmission. This largely reduces the complexity of the Beacon Enable mode of IEEE 802.15.4.

FIGURE 7-1: TRANSMIT PACKET LAYOUT

Address	Memory	Description
0x000	Header Length	Length of the header. This field is described in more detail in the security section of this document.
0x001	Packet Length (m + 3)	The length of the packet, not including the length or FCS.
0x002-0x003	Frame Control	The frame control field describing how this packet should behave.
0x004	Sequence Number	The sequence number distinguishing this packet.
0x005	Data[0]	The destination and source addressing information, as well as any application data.
	Data[...]	
0x005 + (m – 1)	Data[m – 1]	
0x006 + m	FCS[0]	The CRC value for the packet; written by hardware.
0x007 + m	FCS[1]	

7.2.1 TRIGGER PACKET TRANSMISSION

The MRF24J40 handles the Clear Channel Assessment (CCA) and Carrier Sense Multiple Access Collision Avoidance (CSMA-CA) algorithms in hardware. The MRF24J40 also handles automatic retransmission of packets that require an ACK. If the frame control field of the packet requires an ACK, the ACKREQ bit (TXNMTRIG<2>) needs to be set before transmission. Once the TX FIFO is loaded with the data to transmit the TXRTS bit (TXNMTRIG<0>) is used to transmit the packet.

REGISTER 7-1: TXNMTRIG: TRIGGER AND SETTING FOR NORMAL FRAME (CAP) REGISTER

U-0	U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	W-0
—	—	—	PENDACK	INDIRECT(1)	ACKREQ(1)	SECEN(1)	TXRTS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **PENDACK:** Data Pending Status in ACK bit

Status of the data pending bit in ACK from previous transmission. This bit is reset by hardware on the next transmission.

1 = Data pending bit was set

0 = Data pending bit was cleared

bit 3 **INDIRECT:** Activate Indirect Transmission bit(1)

1 = Indirect transmission enabled

0 = Indirect transmission disabled

bit 2 **ACKREQ:** TX Packet in TXN FIFO needs ACK Response bit(1)

1 = ACK requested

0 = No ACK requested

bit 1 **SECEN:** Secure Current TX Packet bit(1)

1 = Secure packet

0 = Send packet without securing it

bit 0 **TXRTS:** Trigger TX MAC to Send the Packet in TX FIFO bit

1 = Send the packet in the TX FIFO, automatically cleared by hardware

Note 1: This bit is cleared at the next triggering of TXN FIFO.

7.2.2 TRANSMISSION STATUS

When a transmission completes, the TXIF flag of the ISRSTS register will become set. Once the TXIF bit is set, the status of the transmission is located in the TXSR register.

REGISTER 7-2: TXSR: TX MAC STATUS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TXRETRY<7:6>		CCAFAIL	r	r	r	r	r
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TXRETRY7:TXRETRY6:** Retry Times bits
Defines the retry times of the most recent TXN FIFO transmission.

bit 5 **CCAFAIL:** Clear Channel Assessment (CCA) Status of Last Transmission bit
1 = CCA failed
0 = CCA passed

bit 4-0 **Reserved:** Maintain as '0'

7.3 Receiving Packets

The following section details the reception of a non-secured frame. When the MRF24J40 receives a packet that passes the MAC layer addressing, threshold and packet type filters, it will indicate the reception of this packet to the host controller by setting the RXIF bit (ISRSTS<3>). The packet will remain in the buffer until the host frees the buffer. No other packets can be received while the buffer is holding a packet.

7.4 RX MAC

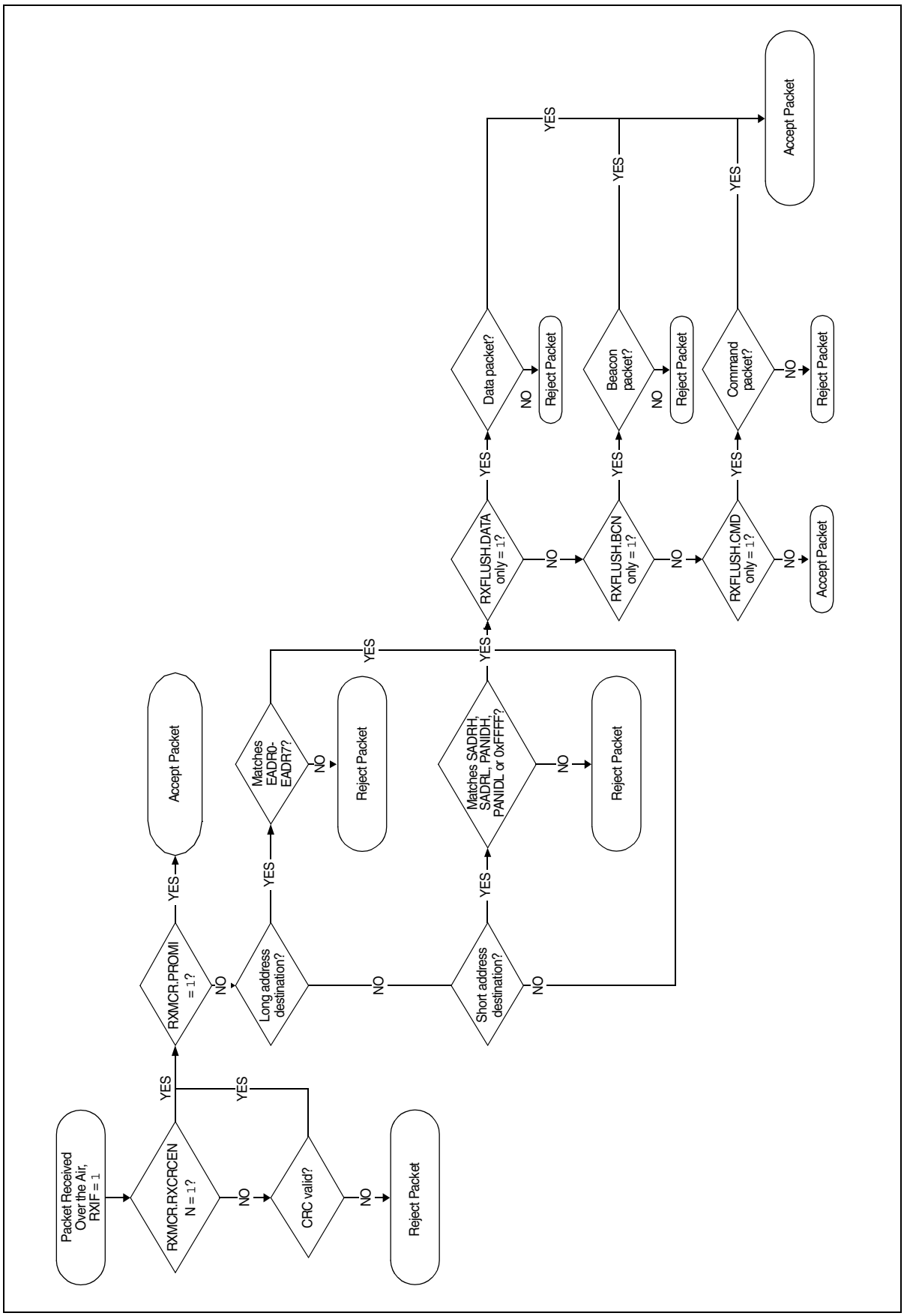
The RX MAC block will do CRC checking, parse the received frame type and address recognition, then store the received frame into RX FIFO. In addition to the IEEE 802.15.4 packet, there are also 2 bytes of information that are appended to the end of the packet after the FCS field: LQI and RSSI.

The behavior of RX FIFO follows a certain rule. When a received packet is not filtered or dropped, a received interrupt/status will be issued. The interrupt is read-to-clear to save host operation time. However, the RX FIFO is flushed only using the following three methods:

- The host reads the first byte and the last byte to the packet
- The host issues RX flush
- A software is reset

For RX filter function, the Promiscuous mode is supported to receive all FCS-ok packets. An Error mode is supported to receive all packets that successfully correlated PHY level preamble and delimiter.

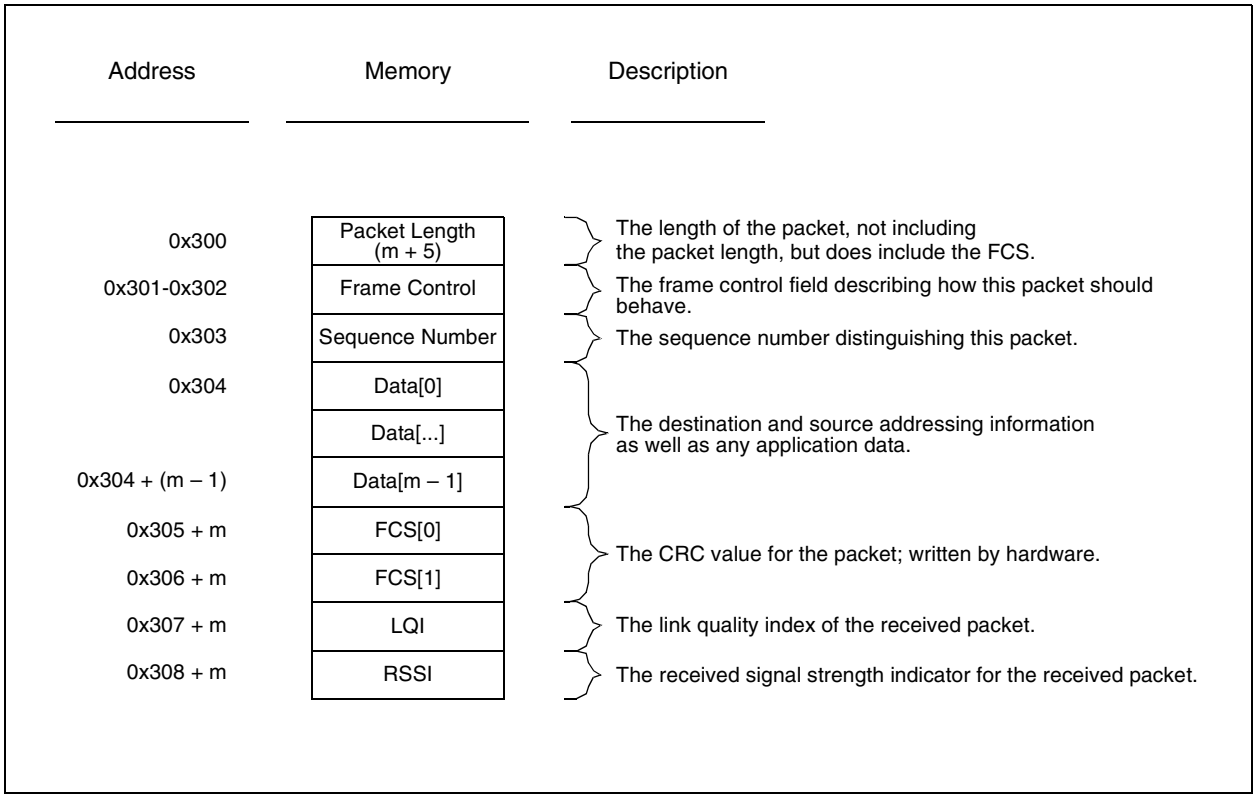
FIGURE 7-2: RECEIVE PROCESS



7.4.1 RECEIVE PACKET LAYOUT

When a packet passes all of the enabled filters, it is placed in the receive FIFO in the following format.

FIGURE 7-3: RECEIVE PACKET LAYOUT.



7.4.2 FREEING RECEIVE BUFFER SPACE

The RX buffer is cleared when the length byte of the packet and the last byte of the FCS are read. Once both of these values are read from the RX buffer, the buffer will enable itself to receive another packet. Because the LQI and RSSI values are appended to the end of the packet after the FCS, it may be advisable to read these values out of the RX buffer before reading the FCS.

Alternatively, it is possible to clear the RX buffer by flushing it. This is done through the RXFLUSH register.

REGISTER 7-3: RXFLUSH: RECEIVE FIFO FLUSH REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	W-0
—	r	r	$\overline{\text{RXWRTBLK}}$	CMDONLY	DATAONLY	BCNONLY	RXFLUSH
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-5 **Reserved:** Maintain as '0'

bit 4 **$\overline{\text{RXWRTBLK}}$:** Software Write to RX FIFO Address bit
1 = Writing to any RX FIFO address is enabled
0 = Writing to any RX FIFO address is disabled

bit 3 **CMDONLY:** Command Packet Receive bit
1 = Only command packets are received, all other packets are filtered out
0 = All valid packets are received

bit 2 **DATAONLY:** Data Packet Receive bit
1 = Only data packets are received, all other packets are filtered out
0 = All valid packets are received

bit 1 **BCNONLY:** Beacon Packet Receive bit
1 = Only beacon packets are received, all other packets are filtered out
0 = All valid packets are received

bit 0 **RXFLUSH:** Flush RX FIFO Address bit
1 = Flush the RX FIFO. Cleared by hardware.
0 = Previous flush complete

7.5 Transceiver

The MRF24J40 receiver features a low IF architecture and consists of an LNA, a pair of down conversion mixers, polyphase channel filters, baseband limiter amplifiers and RSSI technology. An ADC is used to sample the RSSI value and the sampled data is stored in a register from which the data can be read out via the SPI bus. The local oscillator generation circuits (VCO, PLL and buffers) are shared with the receiver and transmitter. The Low Noise Amplifier (LNA) features a differential input for high performance. The RX/TX switch is integrated and LNA input and Power Amplifier (PA) output share the same pins. A common external matching network and single-ended to differential conversion is required. The transmitter features a direct conversion architecture and has a 0 to -38.75 dBm output power. The output power adjustment is in 1.25 dB step. The TX gain is programmed by the SPI bus.

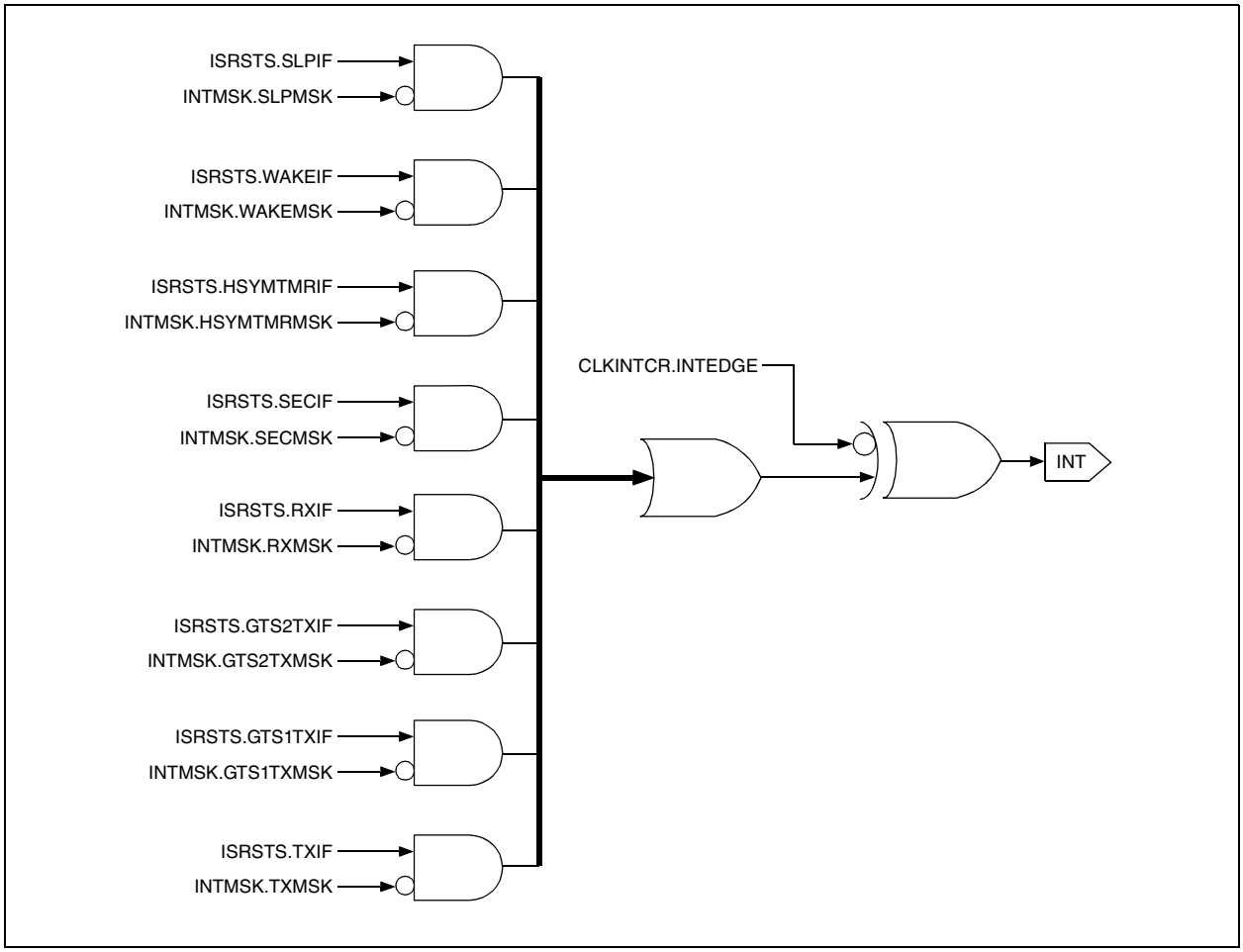
8.0 INTERRUPTS

The MRF24J40 has a simple interrupt structure. There is one interrupt pin that signals all of the possible events. The ISRSTS register is a read-to-clear register that specifies which interrupt(s) caused the interrupt. The INTMSK register is used to block unwanted interrupt sources from generating interrupts. The INTEDGE bit (CLKINTCR<1>) controls the polarity of the interrupt pin. Once ISRSTS is read by the host controller, the interrupt flags are cleared. The host controller should make certain to handle all returned flags each time the ISRSTS register is read.

8.1 Interrupt Structure

When an enabled interrupt occurs, the interrupt pin will remain at its interrupt state, as determined by the INTEDGE bit, until all of the flags which are causing the interrupt are cleared or masked off (the mask bits are set) by the host controller. If more than one interrupt source is enabled, the host controller must poll each flag in the ISRSTS register to determine the source(s) of the interrupt.

FIGURE 8-1: MRF24J40 INTERRUPT LOGIC



8.1.1 INT INTERRUPT STATUS REGISTERS

The registers associated with the INT interrupts are shown in Register 8-1, Register 8-2 and Register 8-3.

REGISTER 8-1: ISRSTS: INTERRUPT STATUS REGISTER

RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0
SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	GTS2TXIF	GTS1TXIF	TXIF
bit 7							bit 0

Legend:	RC = Read to clear		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SLPIF:** Sleep Alert Interrupt bit
1 = Sleep alert interrupt occurred
0 = Otherwise

bit 6 **WAKEIF:** Wake-up Alert Interrupt bit
1 = Wake-up interrupt occurred
0 = Otherwise

bit 5 **HSYMTMRIF:** Half Symbol Timer Interrupt bit
1 = Half symbol timer interrupt occurred
0 = Otherwise

bit 4 **SECIF:** Security Key Request Interrupt bit
1 = Security key request interrupt occurred
0 = Otherwise

bit 3 **RXIF:** RX OK Interrupt bit
1 = RX OK interrupt occurred
0 = Otherwise

bit 2 **GTS2TXIF:** GTS FIFO 2 Release Interrupt bit
1 = GTS2 transmission interrupt occurred
0 = Otherwise

bit 1 **GTS1TXIF:** GTS FIFO 1 Release Interrupt bit
1 = GTS1 transmission interrupt occurred
0 = Otherwise

bit 0 **TXIF:** TX FIFO Release Interrupt bit
1 = TX FIFO transmission interrupt occurred
0 = Otherwise

REGISTER 8-2: INTMSK: INTERRUPT MASK REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
SLPMSK	WAKEMSK	HSYMTMRMSK	SECMSK	RXMSK	GTS2TXMSK	GTS1TXMSK	TXMSK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SLPMSK:** Sleep Alert Mask bit
0 = Enable Sleep interrupt
1 = Otherwise

bit 6 **WAKEMSK:** Wake-up Alert Mask bit
0 = Enable Wake interrupt
1 = Otherwise

bit 5 **HSYMTMRMSK:** Half Symbol Timer Mask bit
0 = Enable half symbol timer interrupt
1 = Otherwise

bit 4 **SECMSK:** Security Interrupt Mask bit
0 = Enable security interrupt
1 = Otherwise

bit 3 **RXMSK:** RX OK Mask bit
0 = Enable receive interrupt
1 = Otherwise

bit 2 **GTS2TXMSK:** GTS FIFO 2 IRQ Mask bit
0 = Enable GTS FIFO 2 transmit interrupt
1 = Otherwise

bit 1 **GTS1TXMSK:** GTS FIFO 1 IRQ Mask bit
0 = Enable GTS FIFO 1 transmit interrupt
1 = Otherwise

bit 0 **TXMSK:** TX Normal FIFO IRQ Mask bit
0 = Enable normal FIFO transmit interrupt
1 = Otherwise

REGISTER 8-3: CLKINTCR: SLPCLK ON/OFF AND INTERRUPT POLARITY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	INTEDGE	$\overline{\text{SLPCLKEN}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **INTEDGE:** Interrupt Edge Polarity bit
1 = Rising edge
0 = Falling edge

bit 0 **$\overline{\text{SLPCLKEN}}$:** Sleep Clock Enable bit
1 = Disabled
0 = Enabled

9.0 GENERAL PURPOSE I/O

9.1 GPIO Registers

The MRF24J40 has 6 available, general purpose I/O pins. These pins are interfaced through the GPIO and TRISGPIO registers.

REGISTER 9-1: GPIO: GPIO PORT REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **GPIO5:** General Purpose I/O GPIO5 bit

bit 4 **GPIO4:** General Purpose I/O GPIO4 bit

bit 3 **GPIO3:** General Purpose I/O GPIO3 bit

bit 2 **GPIO2:** General Purpose I/O GPIO2 bit

bit 1 **GPIO1:** General Purpose I/O GPIO1 bit

bit 0 **GPIO0:** General Purpose I/O GPIO0 bit

EXAMPLE 9-1: READ/WRITE EXAMPLE

```
SetShortAddress(TRISGPIO,0x03);  //set GPIO5-2 to output, and GPIO 1-0 as input
SetShortAddress(GPIO,0x01);      //set GPIO0 high and GPIO1 as low.
```

REGISTER 9-2: TRISGPIO: GPIO PIN DIRECTION AND SPI MODE REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TRISGP5	TRISGP4	TRISGP3	TRISGP2	TRISGP1	TRISGP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **TRISGP5:** General Purpose I/O GPIO5 Direction bit
1 = Output
0 = Input

bit 4 **TRISGP4:** General Purpose I/O GPIO4 Direction bit
1 = Output
0 = Input

bit 3 **TRISGP3:** General Purpose I/O GPIO3 Direction bit
1 = Output
0 = Input

bit 2 **TRISGP2:** General Purpose I/O GPIO2 Direction bit
1 = Output
0 = Input

bit 1 **TRISGP1:** General Purpose I/O GPIO1 Direction bit
1 = Output
0 = Input

bit 0 **TRISGP0:** General Purpose I/O GPIO0 Direction bit
1 = Output
0 = Input

10.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on any combined digital and analog pin with respect to V_{SS} (except V_{DD}) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to 3.6V
Total power dissipation **(Note 1)** 1.0W
Maximum output current sunk by GPIO1-GPIO5 pins ..... 1 mA
Maximum output current sourced by GPIO1-GPIO5 pins ..... 1 mA
Maximum output current sunk by GPIO0 pin ..... 4 mA
Maximum output current sourced by GPIO0 pin ..... 4 mA

Note 1: Power dissipation is calculated as follows:
$Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 10-1: RECOMMENDED OPERATING CONDITIONS

Parameters	Min	Typ	Max	Units
Ambient Operating Temperature	-40	—	+85	°C
Supply Voltage for RF, Analog and Digital Circuits	2.4	—	3.6	V
Supply Voltage for Digital I/O	2.4	3.3	3.6	V
Input High Voltage (V_{IH})	0.5 x V_{DD}	—	V_{DD} + 0.3	V
Input Low Voltage (V_{IL})	-0.3	—	0.2 x V_{DD}	V

TABLE 10-2: CURRENT CONSUMPTION

Typical Values: T_A = 25°C, V_{DD} = 3.3V

Chip Mode	Condition	Min	Typ	Max	Units
Sleep		—	2	TBD	µA
TX	At maximum output power	—	22	TBD	mA
RX		—	18	TBD	mA

Legend: TBD = To Be Determined

TABLE 10-3: RECEIVER AC CHARACTERISTICS

Typical Values: T_A = 25°C, V_{DD} = 3.3V, LO Frequency = 2.445 GHz

Parameters	Condition	Min	Typ	Max	Units
RF Input Frequency		2.4	—	2.483	GHz
RF Sensitivity	At antenna input with O-QPSK signal and 3.5 dB front end loss is assumed	—	-91	—	dBm
Maximum RF Input	LNA at high gain	+5	—	—	dBm
LO Leakage	Measured at balun matching network input at frequency 2.405-2.48 GHz	—	-60	—	dBm
Input Return Loss	Externally matched to 50 source by a balun matching network	-12	-20	—	dB
Noise Figure (including matching)		—	8	—	dB
Adjacent Channel Rejection	@ +/- 5 MHz	30	—	—	dB
Alternate Channel Rejection	@ +/- 10 MHz	40	—	—	dB
RSSI Range		—	50	—	dB
RSSI Error		-5	—	5	dB

TABLE 10-4: TRANSMITTER AC CHARACTERISTICS

Typical Values: T_A = 25°C, V_{DD} = 3.3V, LO Frequency = 2.445 GHz

Parameters	Condition	Min	Typ	Max	Units
RF Carrier Frequency		2.4	—	2.483	GHz
Maximum RF Output Power		—	0	—	dBm
RF Output Power Control Range		—	38.75	—	dB
TX Gain Control Resolution	Programmed by register	—	1.25	—	dB
Carrier Suppression		—	-30	—	dBc
TX Spectrum Mask for O-QPSK Signal	Offset frequency > 3.5 MHz, at 0 dBm output power	-33	—	—	dBm
TX EVM		—	—	25	%
TX Noise Floor		—	—	-126	dBm/Hz

FIGURE 10-1: EXAMPLE SPI SLAVE MODE TIMING

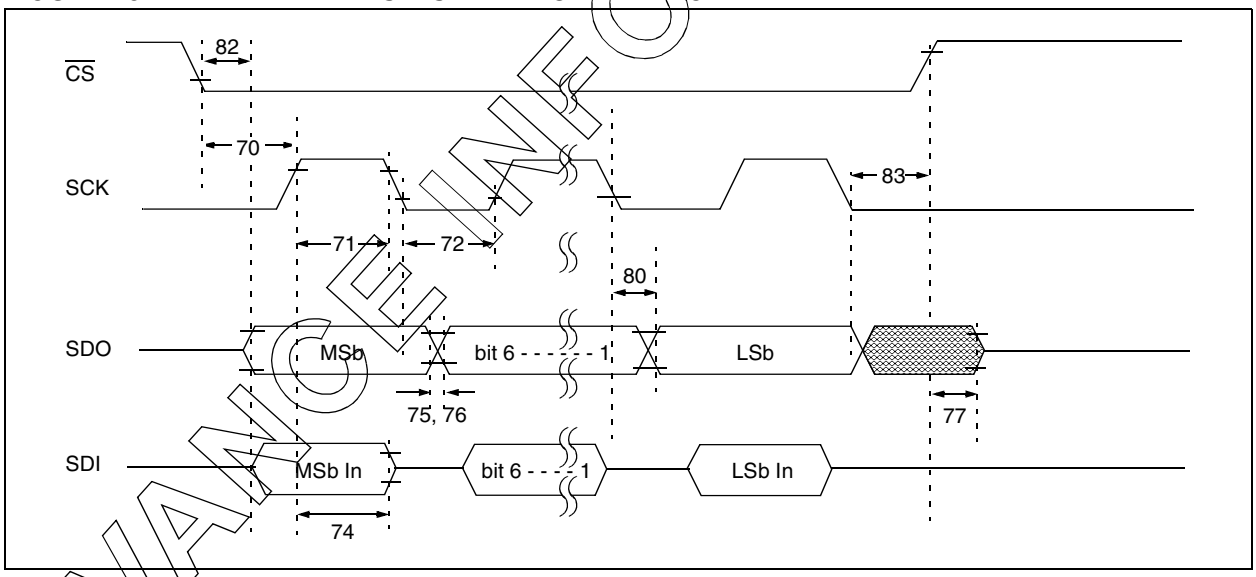


TABLE 10-5: EXAMPLE SPI SLAVE MODE REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH	$\overline{CS}$ ↓ to SCK ↑ Input		50	—	ns	
71	TscH	SCK Input High Time	Single Byte	50	—	ns	
72	TscL	SCK Input Low Time	Single Byte	50	—	ns	
74	TscH2diL	Hold Time of SDI Data Input to SCK Edge		25	—	ns	
75	TdoR	SDO Data Output Rise Time		—	25	ns	
76	TdoF	SDO Data Output Fall Time		—	25	ns	
78	TscR	SCK Output Rise Time (Master mode)		—	25	ns	
80	TscH2doV, TscL2doV	SDO Data Output Valid after SCK Edge		TBD	—	ns	
82	TssL2doV	SDO Data Output Valid after $\overline{CS}$ ↓ Edge		TBD	—	ns	
83	TscL2ssH	$\overline{CS}$ ↑ after SCK Edge		50	—	ns	

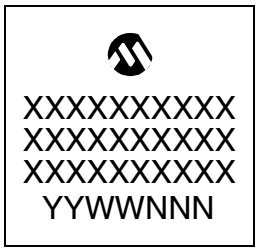
Legend: TBD = To Be Determined

NOTES:

11.0 PACKAGING INFORMATION

11.1 Package Marking Information

40-Lead QFN



Example

Legend:	XX...X	Product-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

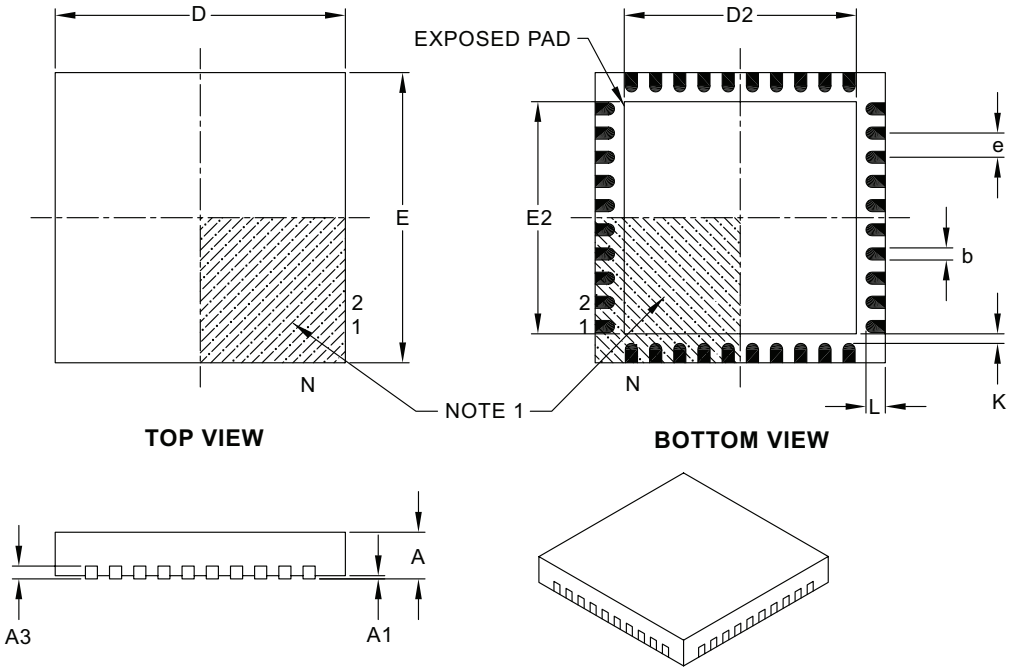
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

11.2 Package Details

The following sections give the technical details of the packages.

40-Lead Plastic Quad Flat, No Lead Package (MM) 6x6x0.9 mm Body [QFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.00	4.37	4.75
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.00	4.37	4.75
Contact Width	b	0.18	0.25	0.30
Contact Length §	L	0.30	0.40	0.50
Contact-to-Exposed Pad §	K	0.20	—	—

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04–118, 09/15/06

APPENDIX A: LAYOUT AND PART SELECTION

A.1 Layout Considerations and RF Measurements

Below is an example of the circuit diagram of a balun. A balun is the impedance transformer from unbalanced input of the PCB antenna and the balanced input of the RF transceiver (pins RFP and RFN).

Figure A-2 shows the measured impedance of the balun where the center of the band is very close to 50Ω. When using low tolerance components (i.e., ±5%) along with an appropriate ground, the impedance will remain close to the 50Ω measurement. Figure A-3 shows the measured impedance of the PCB antenna using a logarithmic scale magnitude. Figure A-4 shows the same impedance using a Smith Chart diagram and Figure A-5 using a voltage standing wave ratio.

FIGURE A-1: EXAMPLE CIRCUIT DIAGRAM

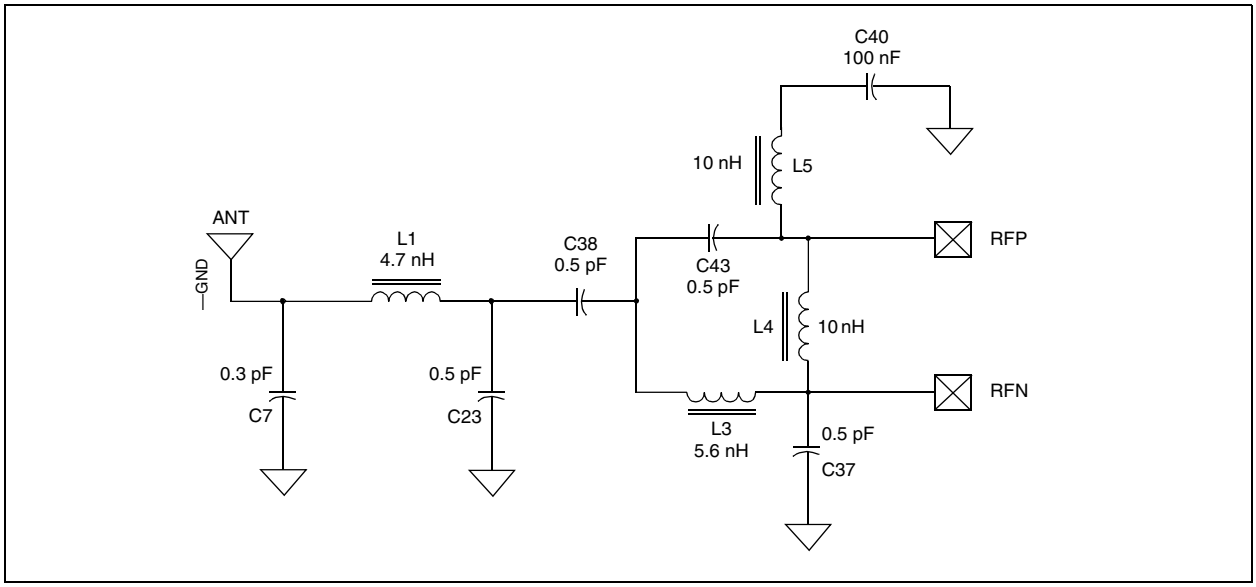


FIGURE A-2: MEASURED IMPEDANCE

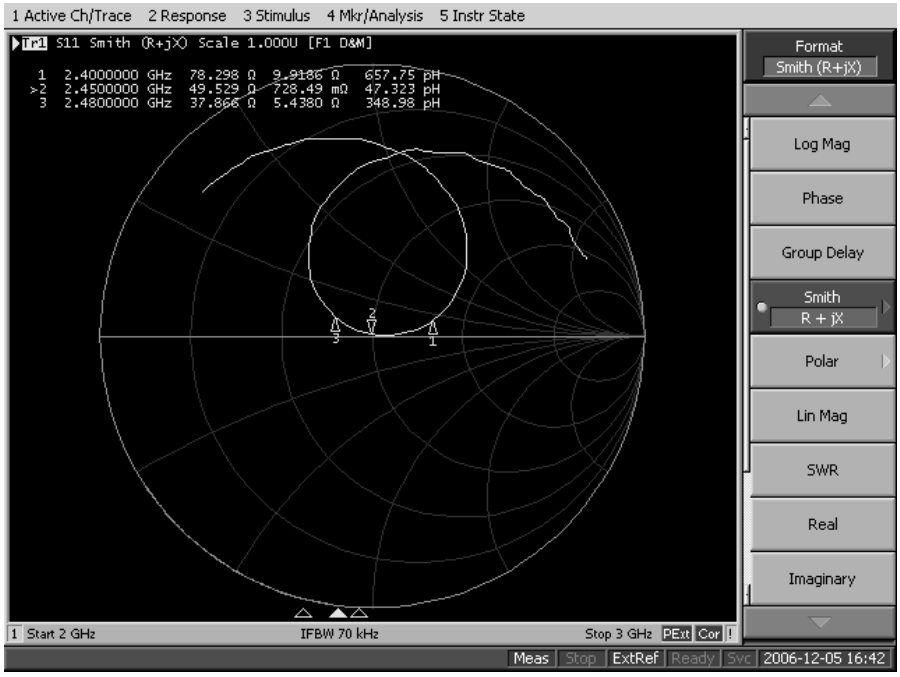


FIGURE A-3: IMPEDANCE OF THE PCB ANTENNA

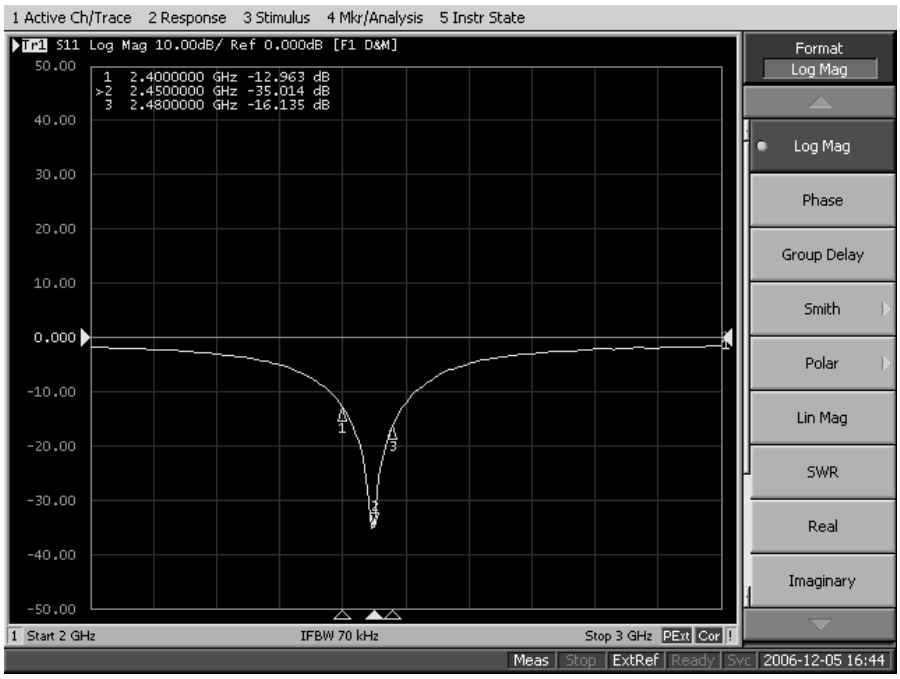


FIGURE A-4: IMPEDANCE OF THE PCB ANTENNA IN SMITH CHART

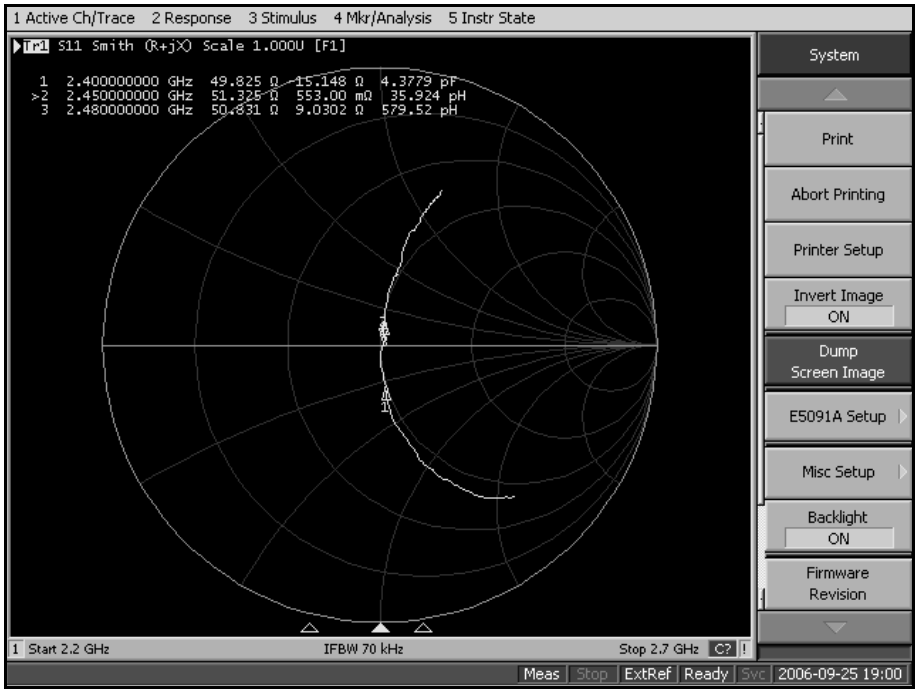
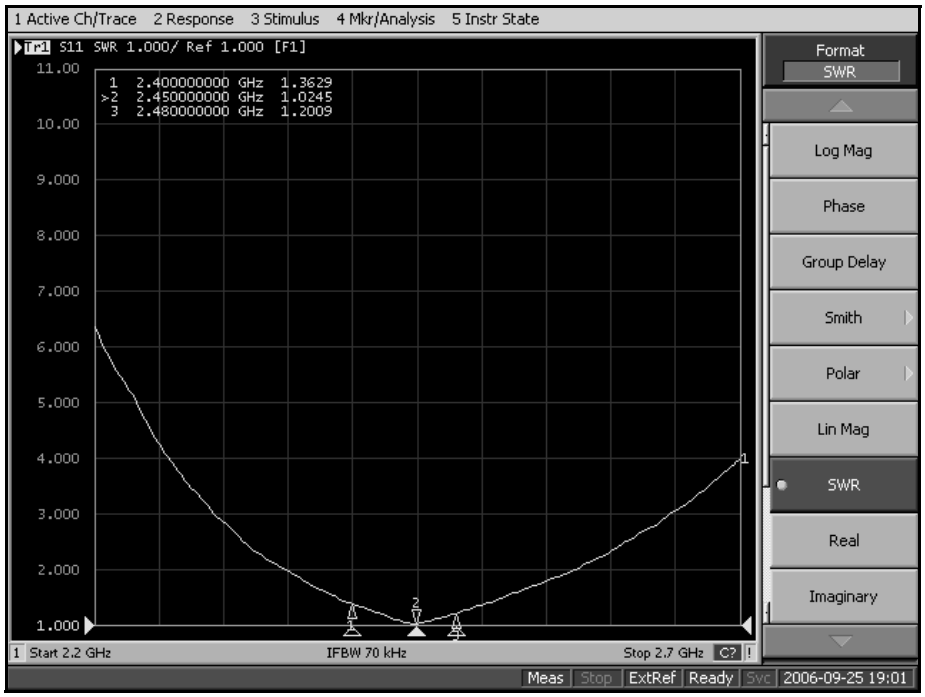


FIGURE A-5: IMPEDANCE OF THE PCB ANTENNA WITH VOLTAGE STANDING WAVE RATIO



The most critical part of maintaining proper impedance is adhering to the specified dimensions of the printed circuit board antenna (see Figure A-6). The antenna dimensions, if altered, will change the specified impedance. As an example, a 1 mm variance will shift the impedance by 5-10 MHz.

Note: This part has been simulated using a HFSS™ simulator provided by Ansoft Corporation.

FIGURE A-6: PRINTED CIRCUIT BOARD ANTENNA DIMENSIONS

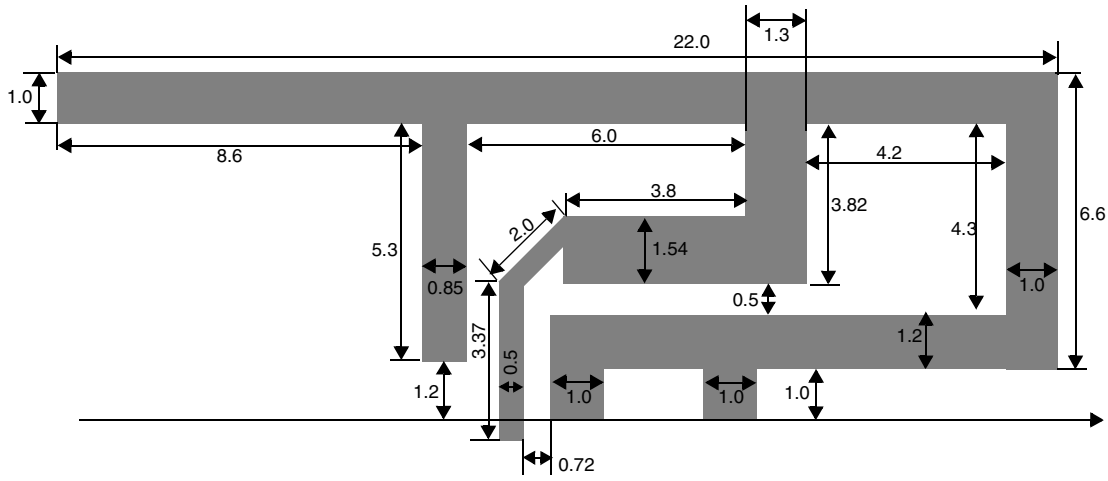


Figure A-7 and Figure A-8 illustrate simulation results of this PCB antenna. Note the simulation results are very close to the measurements.

FIGURE A-7: SIMULATED PCB ANTENNA IMPEDANCE, XY PLOT

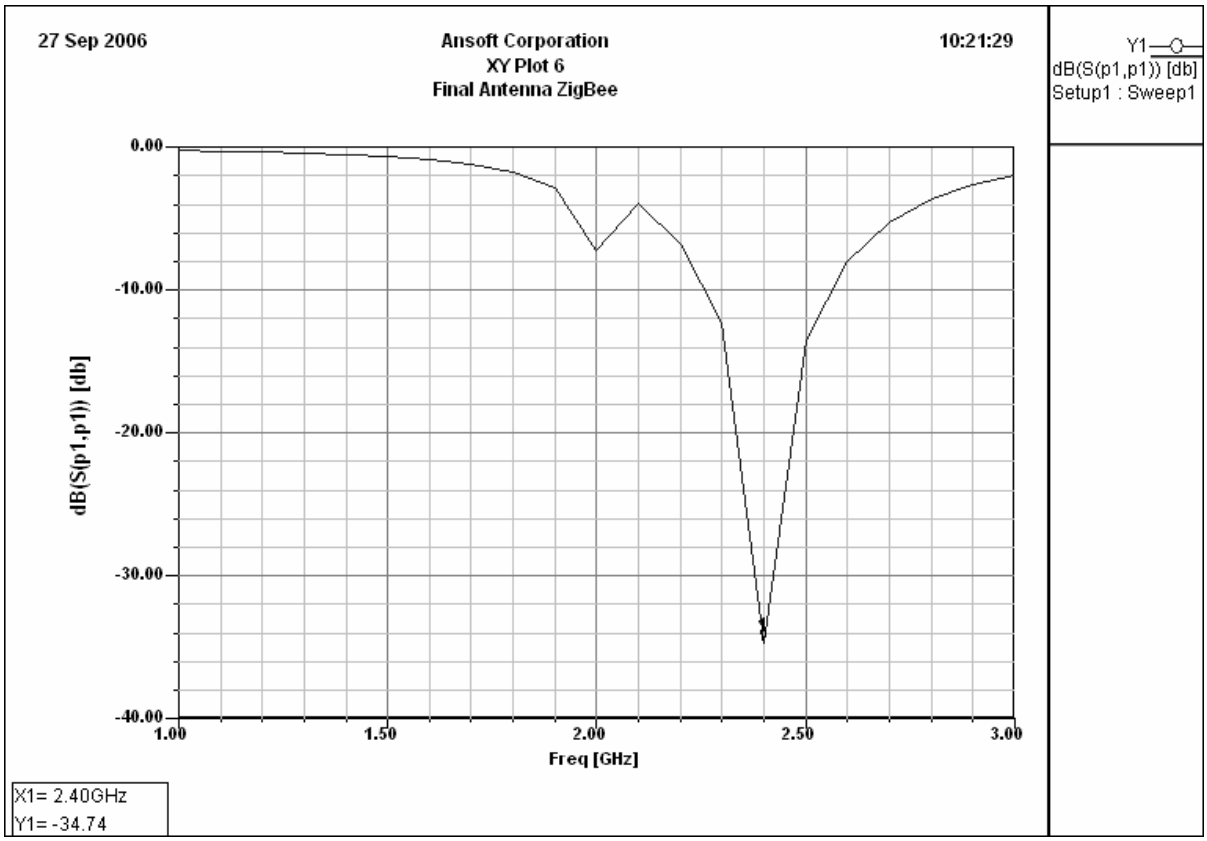
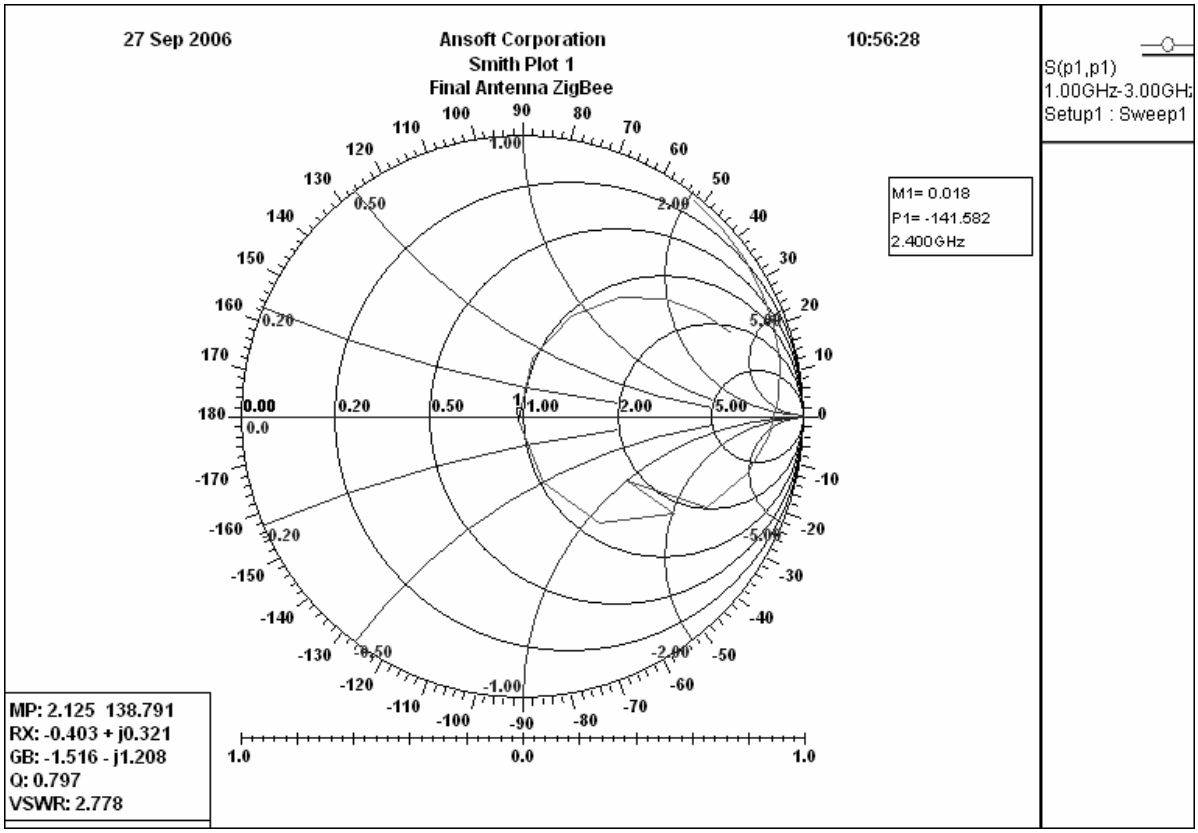


FIGURE A-8: SIMULATED PCB ANTENNA IMPEDANCE, SMITH PLOT

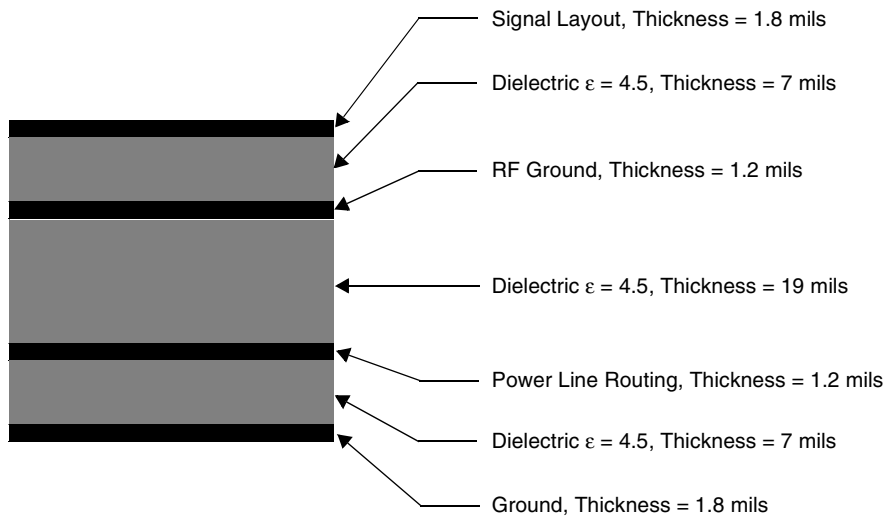


A.2 PCB Layout Design

The following guidelines are intended to aid users who are not experienced in high-frequency PCB layout design.

The printed circuit board is comprised of four basic FR4 layers: signal layout, RF ground, power line routing and ground (see Figure A-9). The guidelines will explain the requirements of these layers.

FIGURE A-9: FOUR BASIC COPPER FR4 LAYERS

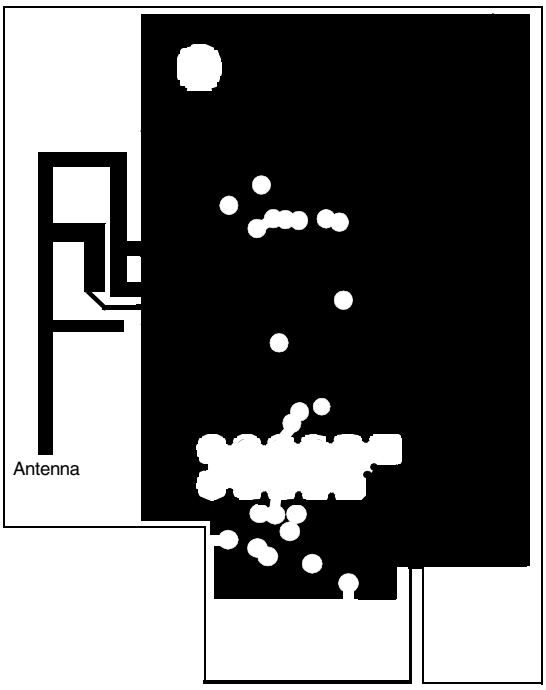


Note: Care should be taken with all ground lines to prevent breakage.

- It is important to keep the original PCB thickness since any change will affect antenna performance (see total thickness of dielectric) or microstrip lines characteristic impedance.
- The first layer width of a 50Ω characteristic impedance microstrip line is 12 mils.
- Avoid having microstrip lines longer than 2.5 cm, since that line might get very close to a quarter wave length of the working frequency of the board which is 3.0 cm, and start behaving as an antenna.
- Except for the antenna layout, avoid sharp corners since they can act as an antenna. Round corners will eliminate possible future EMI problems.
- Digital lines by definition are prone to be very noisy when handling periodic waveforms and fast clock/switching rates. Avoid laying out a RF signal close to any digital lines.
- A via filled ground patch underneath the IC transceiver is mandatory.
- A power supply must be distributed to each pin in a star topology and low-ESR capacitors must be placed at each pin for proper decoupling noise.
- Decoupling each power pin is a tedious task, especially when the noise is affecting the performance of the transceiver in a specific bandwidth. Usually, low value caps (15-27 pF) combined with large value caps (100 nF) will cover a large spectrum of frequency.
- Passive components (inductors) must be in the high-frequency category and the SRF (Self-Resonant Frequency) should be at least two times higher than the operating frequency.

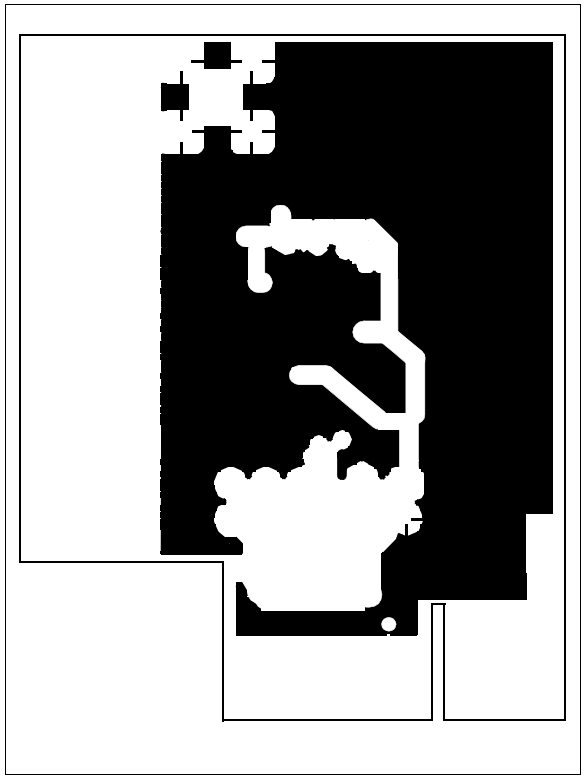
Figure A-10 and Figure A-11 illustrate the ground and power plane for the RF board.

FIGURE A-10: GROUND PLANE



Note: See Figure A-6 for antenna dimensions

FIGURE A-11: POWER GROUND PLANE

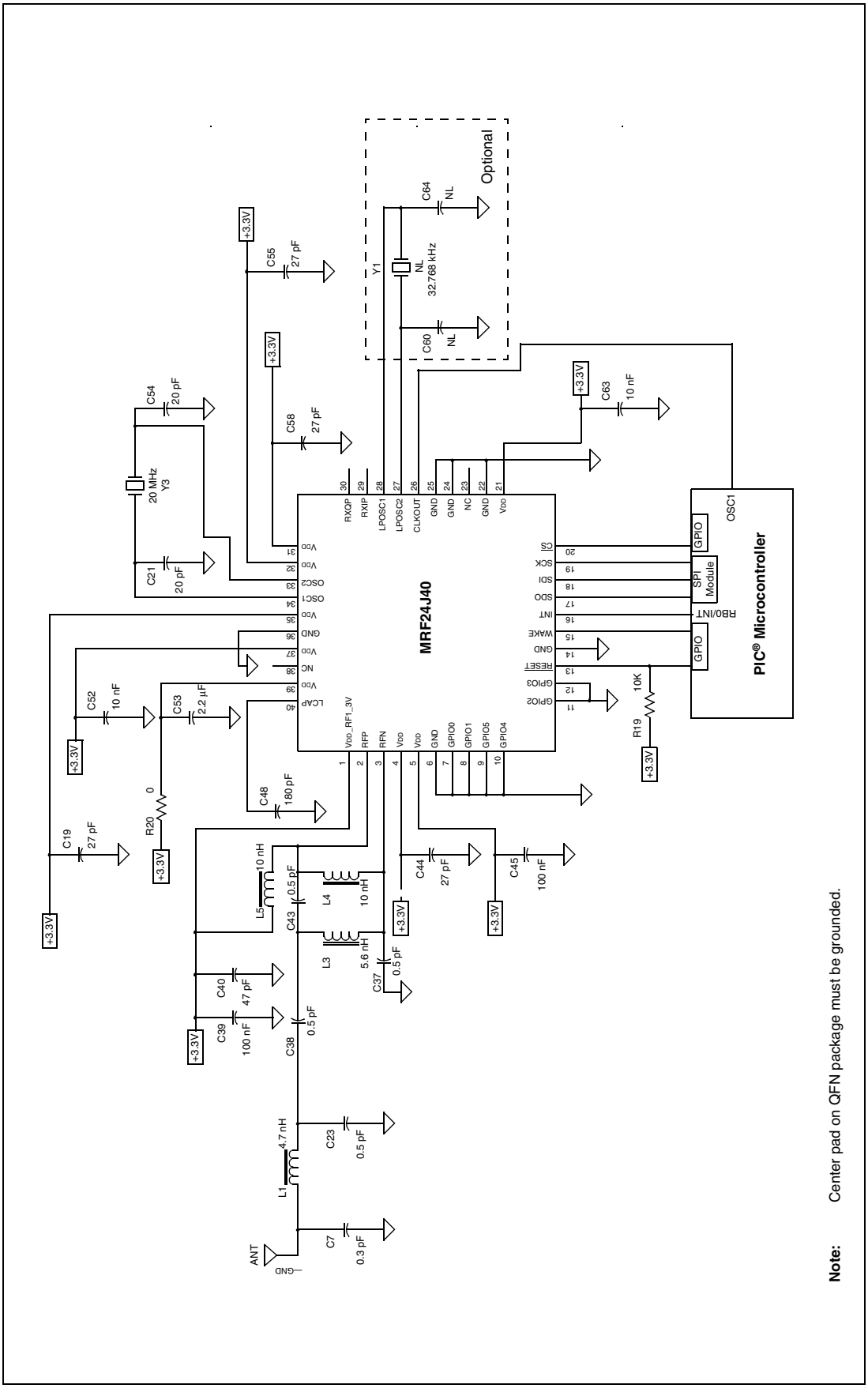


NOTES:

APPENDIX B: MRF24J40 SCHEMATIC AND BILL OF MATERIALS

B.1 Schematic

FIGURE B-1: MRF24J40 SCHEMATIC



Note: Center pad on QFN package must be grounded.

B.2 Bill of Materials

TABLE B-1: MRF24J40 DAUGHTER CARD BILL OF MATERIALS

Quantity	Component Name	Reference Description	Value	Description	Vendor	Vendor #
1	CAP3528	C1	2.2 µF_Tant	Capacitor TANT, 2.2 µF, 25V, 10%, SMD	Kemet	T491B225K025AT
4	CAP0402	C23, C37, C38, C43	0.5 pF	CAP, Ceramic, 0.5 pF, 50V, NP0, 0402	Yageo America	0402CG508C9B200
2	CAP0402	C21, C54	20 pF	CAP, Ceramic, 20 pF, 50V, 5%, C0G, 0402	Murata Electronics	GRM1555C1H200JZ01D
4	CAP0402	C19, C44, C55, C58	27 pF	CAP, Ceramic, 27 pF, 50V, 0402, SMD	Panasonic - ECG	ECJ-0EC1H270J
1	CAP0402	C40	47 pF	CAP, Ceramic, 47 pF, 50V, C0G, 5%, 0402	TDK Corporation	C1005C0G1H470J
2	CAP0402	C52, C63	10 nF	CAP, Ceramic, 10000 pF, 16V, X7R, 0402	Kemet	C0402C103K4RACTU
2	CAP0402	C39, C45	100 nF	C0402C104K8PACTU	Kemet	C0402C104K8PACTU
1	CAP0402	C48	180 pF	CAP, Ceramic, 180 pF, 50V, C0G, 5%, 0402	TDK Corporation	C1005C0G1H181J
1	CAP0603	C53	2.2 µF	CAP, Ceramic, 2.2 µF, 10V, Y5V, 0603	Taiyo Yuden	LMK107F225ZA-T
1	CRYSTAL_ABM8	Y3	20 MHz	Crystal, 20.000 MHz, 18 pF, FUND, SMD	Abracon Corporation	ABM8-20.000MHZ-B2-T
1	MRF24J40_QLP40	U1		MRF24J40, Single Chip Transceiver	Microchip	MRF24J40-I/ML
1	IND0402	L1	4.7 nH	Inductor Multilayer, 4.7 nH, 0402	TDK Corporation	MLK1005S4N7S
1	IND0402	L3	5.6 nH	Inductor Multilayer, 5.6 nH, 0402	TDK Corporation	MLK1005S5N6D
2	IND0402	L4, L5	10 nH	Inductor Multilayer, 10 nH, 0402	TDK Corporation	MLK1005S10NJ
2	RES0402	R20, R22	0Ω	RES, 0Ω, 1/16W, 5%, 0402, SMD	Panasonic - ECG	ERJ-2GE0R00X
1	RES0402	R19	10K	RES, 10 kΩ, 1/16W, 5%, 0402, SMD	Yageo America	RC0402JR-0710KL
1	HDR6X2	J2		.100" Socket/Terminal	Samtec	LST-106-07-F-D

B.3 REVISION HISTORY

Revision A (December 2006)

Original data sheet for the MRF24J40 device.

NOTES:

INDEX

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Temperature Range	I = -40°C to +85°C (Industrial)
Package	MM = QFN (Plastic Quad Flat, No Lead)

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