Document Title

512Kx36 & 256Kx72 DLW(Double Late Write) RAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial document.	Feb. 10, 2003	Preliminary
0.1	1. Correct the ZQ to programmable.	Mar. 8, 2003	Preliminary

512Kx36 & 256Kx72-Bit DLW(Dobule Late Write) RAM

FEATURES

• Double Late Write mode , Pipelined Read mode.
• Compatible with Double Late Write Sigma RAM^{TM} x36/x72.
• 1.8V+150/-100 mV Power Supply.
• I/O Supply Voltage 1.5V+0.1V/-0.1V for 1.5V I/O
• HSTL I/O
• Byte Writable Function.
• Single READ/WRITE control pin.
• Self-Timed Write Cycle.
• Complement echo clock outputs
• Programmable impedance output buffer(ZQ)
• 2 User programmable chip enable inputs for easy depth
  expansion.(EP2, EP3)
• Supports linear burst mode only.
• Slow Down Function.($\overline{SD}$)
• IEEE 1149.1 JTAG Compatible Boundary Scan
• 209 bump, 14mm x 22mm, 1mm bump pitch BGA package
• 209BGA(11x19 Ball Grid Array Package).

GENERAL DESCRIPTION

The K7Z163688B & K7Z167288B is 18,874,368-bits Synchro-
nous Static SRAMs.
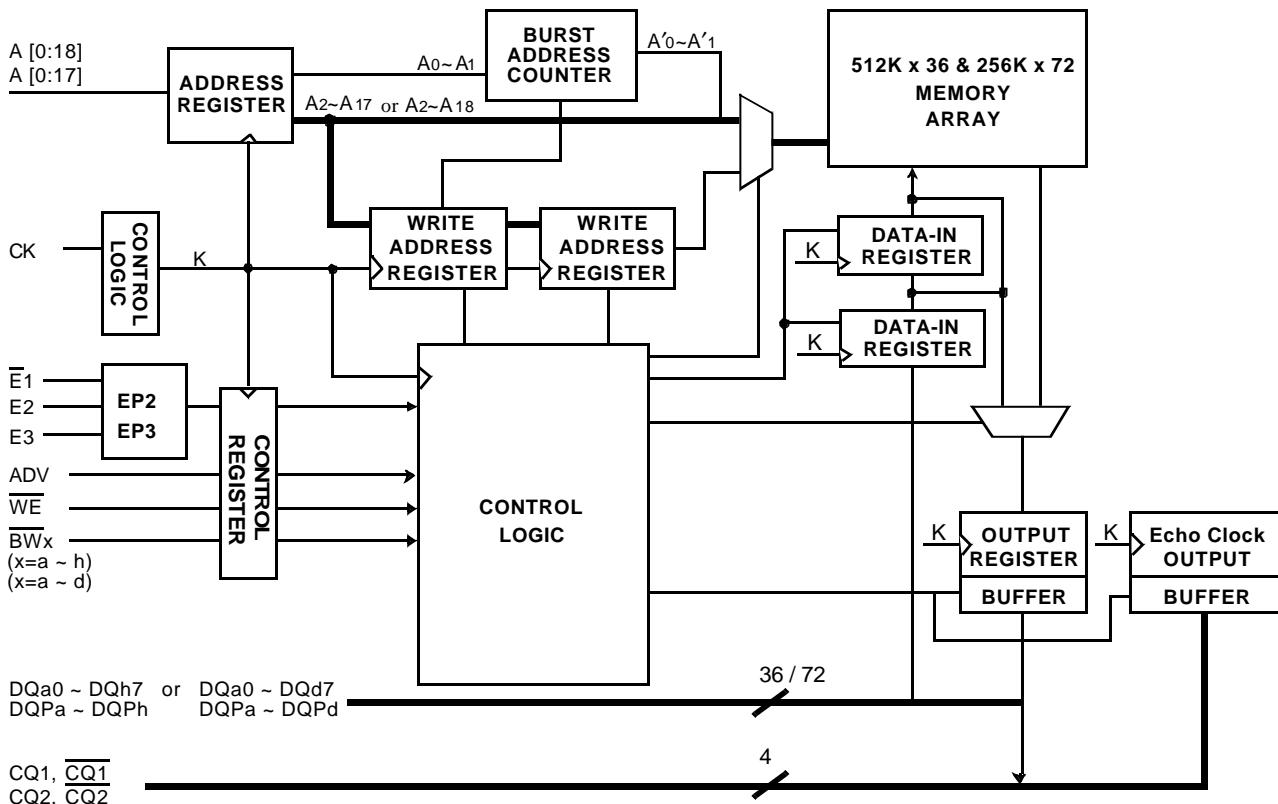
The Double Late Write RAM utilizes all the bandwidth in any com-
bination of operating cycles.

Address, data inputs, and all control signals except EP2, EP3,
and $\overline{SD}$ are synchronized to input clock.

Write cycles are internally self-timed and initiated by the rising
edge of the clock input. This feature eliminates complex off-chip
write pulse generation and provides increased timing flexibility for
incoming signals.

For read cycles,the SRAM output data is temporarily stored by an
edge triggered output register and then released to the output
buffers at the next rising edge of clock.

The K7Z163688B & K7Z167288B are implemented with SAM-
SUNG′s high performance CMOS technology and is available in
209BGA packages. Multiple power and ground pins   minimize
ground bounce.

FAST ACCESS TIMES

PARAMETER	Symbol	-35	Unit
Cycle Time	t_{CYC}	2.85	ns
Clock Access Time	t_{CD}	1.7	ns

LOGIC BLOCK DIAGRAM

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209BGA PACKAGE PIN CONFIGURATIONS (TOP VIEW)

512Kx36 Common I/O-Top View

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E 2	A	ADV	A	E3	A	DQb	DQb
B	NC	NC	$\overline{BW}c$	NC	A	$\overline{WE}$	A	$\overline{BW}b$	NC	DQb	DQb
C	NC	NC	NC	$\overline{BW}d$	NC(128M)	$\overline{E1}$	NC	NC	$\overline{BW}a$	DQb	DQb
D	NC	NC	Vss	Vref	NC	MCL	NC	Vref	Vss	DQb	DQb
E	NC	DQPc	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	NC	DQPb
F	DQc	DQc	Vss	Vss	Vss	ZQ	Vss	Vss	Vss	NC	NC
G	DQc	DQc	VDDQ	VDDQ	VDD	EP2	VDD	VDDQ	VDDQ	NC	NC
H	DQc	DQc	Vss	Vss	Vss	EP3	Vss	Vss	Vss	NC	NC
J	DQc	DQc	VDDQ	VDDQ	VDD	MCH	VDD	VDDQ	VDDQ	NC	NC
K	CQ2	$\overline{CQ2}$	CK	Vref	Vss	MCL	Vss	NC	NC	$\overline{CQ1}$	CQ1
L	NC	NC	VDDQ	VDDQ	VDD	MCH	VDD	VDDQ	VDDQ	DQa	DQa
M	NC	NC	Vss	Vss	Vss	MCL	Vss	Vss	Vss	DQa	DQa
N	NC	NC	VDDQ	VDDQ	VDD	$\overline{SD}$	VDD	VDDQ	VDDQ	DQa	DQa
P	NC	NC	Vss	Vss	Vss	MCL	Vss	Vss	Vss	DQa	DQa
R	DQPd	NC	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQPa	NC
T	DQd	DQd	Vss	Vref	NC	MCL	NC	Vref	Vss	NC	NC
U	DQd	DQd	NC	A	NC(64M)	A	NC(32M)	A	NC	NC	NC
V	DQd	DQd	A	A	A	A1	A	A	A	NC	NC
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

K7Z167288B
K7Z163688B
512Kx36 & 256Kx72 DLW(Double Late Write) RAM

209BGA PACKAGE PIN CONFIGURATIONS (TOP VIEW)

256Kx72 Common I/O-Top View

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	E2	A	ADV	A	E3	A	DQb	DQb
B	DQg	DQg	$\overline{BW}$c	$\overline{BW}$g	NC	$\overline{WE}$	A	$\overline{BW}$b	$\overline{BW}$f	DQb	DQb
C	DQg	DQg	$\overline{BW}$h	$\overline{BW}$d	NC(128M)	$\overline{E1}$	NC	$\overline{BW}$e	$\overline{BW}$a	DQb	DQb
D	DQg	DQg	Vss	Vref	NC	MCL	NC	Vref	Vss	DQb	DQb
E	DQPg	DQPc	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQPf	DQPb
F	DQc	DQc	Vss	Vss	Vss	ZQ	Vss	Vss	Vss	DQf	DQf
G	DQc	DQc	VDDQ	VDDQ	VDD	EP2	VDD	VDDQ	VDDQ	DQf	DQf
H	DQc	DQc	Vss	Vss	Vss	EP3	Vss	Vss	Vss	DQf	DQf
J	DQc	DQc	VDDQ	VDDQ	VDD	MCH	VDD	VDDQ	VDDQ	DQf	DQf
K	CQ2	$\overline{CQ2}$	CK	Vref	Vss	MCL	Vss	NC	NC	$\overline{CQ1}$	CQ1
L	DQh	DQh	VDDQ	VDDQ	VDD	MCH	VDD	VDDQ	VDDQ	DQa	DQa
M	DQh	DQh	Vss	Vss	Vss	MCL	Vss	Vss	Vss	DQa	DQa
N	DQh	DQh	VDDQ	VDDQ	VDD	$\overline{SD}$	VDD	VDDQ	VDDQ	DQa	DQa
P	DQh	DQh	Vss	Vss	Vss	MCL	Vss	Vss	Vss	DQa	DQa
R	DQPd	DQPh	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQPa	DQPe
T	DQd	DQd	Vss	Vref	NC	MCL	NC	Vref	Vss	DQe	DQe
U	DQd	DQd	NC	A	NC(64M)	A	NC(32M)	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Pin Description Table

Pin Name	Description	Type	Comments
A	Address	Input	-
ADV	Advance	Input	Active High
$\overline{BW}$x(x=a~h or a~d)	Byte Write Enable	Input	Active Low
CK	Clock	Input	Active High
DQ	Data I/O	Input/Output	-
CQ	Echo Clock Outputs	Output	Active High
$\overline{CQ}$	Echo Clock Outputs	Output	Active Low
$\overline{E1}$	Chip Enable	Input	Active Low
E2 & E3	Chip Enable	Input	Programmable Active High or Low
EP2 & EP3	Chip Enable Program Pin	Input	-
$\overline{SD}$	Slow Down Input	Input	Active Low
TCK	Test Clock	Input	Active High
TDI	Test Data In	Input	-
TDO	Test Data Out	Output	-
TMS	Test Mode Select	Input	-
MCH	Must Connect High	Input	Active High
MCL	Must Connect Low	Input	Active Low
NC	No Connect	-	Not connected to die
$\overline{WE}$	Write	Input	Active Low
VDD	Core Power Supply	Input	1.8V
VDDQ	Output Driver Power Supply	Input	1.5V
Vss	Ground	Input	-
ZQ	Output Impedance Control	Input	Programmable ZQ
Vref	Input Reference Voltage	Input	-

FUNCTION DESCRIPTION

The K7Z163688B & K7Z167288B are Double Late Write RAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
Because a Double Late Write RAM is a synchronous device, address, data Inputs, and read/write control inputs are captured on the rising edge of the input clock. EP2 , EP3 and $\overline{SD}$ are asynchronous control input.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, all three chip enables($\overline{E1}$, E2, E3) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low.The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the out-put register. At the second clock edge the data is driven out of the SRAM.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$x[h:a] can be used for byte write operation.
The Double Late Write RAM uses a double-late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

Double Late Write RAM supports linear burst sequence only.

BURST SEQUENCE TABLE (Linear Burst Order)

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Slow Down Function

$\overline{SD}$ is helpful to prevent to bus contention in read operation after write operation , especially high frequency application.
When $\overline{SD}$ is Low, the SRAM is operated in a slow down mode. In a slow down mode, the enable/disable timings of output data become slower , which are defined as tKHQV,tKHQZ,tKHQX,tKHQX1/tKHCH and tKLCL.
The valid data window in slow down mode is same with normal operation mode , so it will be helpful in read operation after write operation
When $\overline{SD}$ is High , the SRAM returns to normal operation node.
The state of $\overline{SD}$ must be fixed before operation , and it can not be changed during operation.

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Programmable Enables

Double Late Write RAM features two user programmable chip enable inputs, E2 and E3. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP2 and E P3. For example, if EP2 is held at V_{DD}, E2 functions as an active high enable. If EP2 is held to VSS, E2 functions as an active low chip enable input.
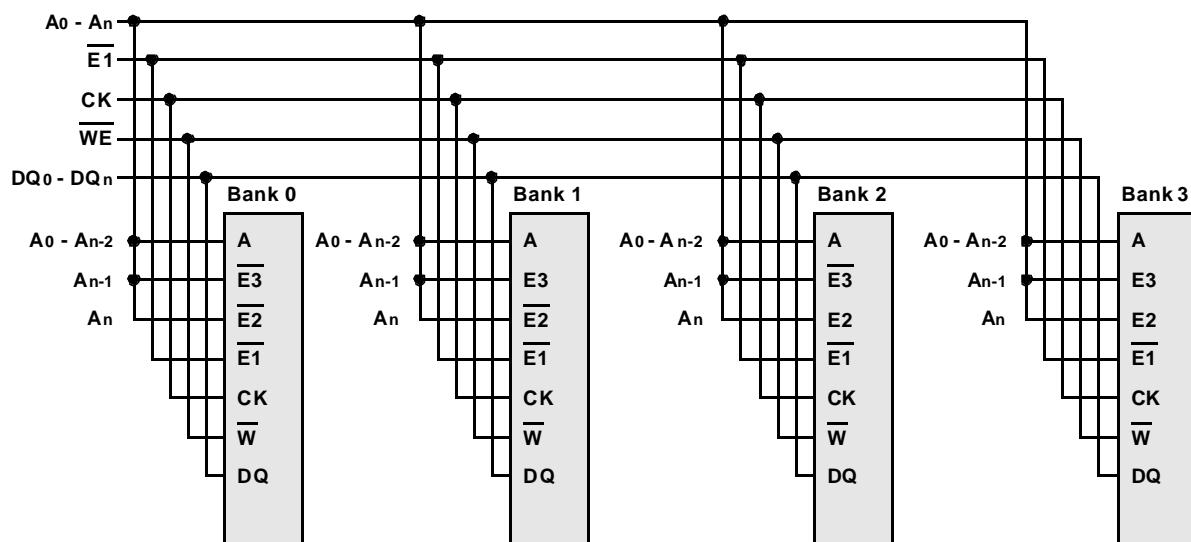
Programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four Double Late Write RAMs in binary sequence(00, 01, 10, 11)and driving the enable inputs with two address inputs. Four Double Late Write RAM can be made to look like one larger RAM to the system.

Deselection of the RAM via $\overline{E1}$ does not deactive the Echo Clocks.

Programmable Impedance Output Driver

The data output and echo clock driver impedance are adjusted by an external resistor, RQ, connected between ZQ pin and VSS, and are equal to RQ/5. For example, 250Ω resistor will give an output impedance of 50Ω. Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with $\overline{G}$ high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time $\overline{G}$ are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.
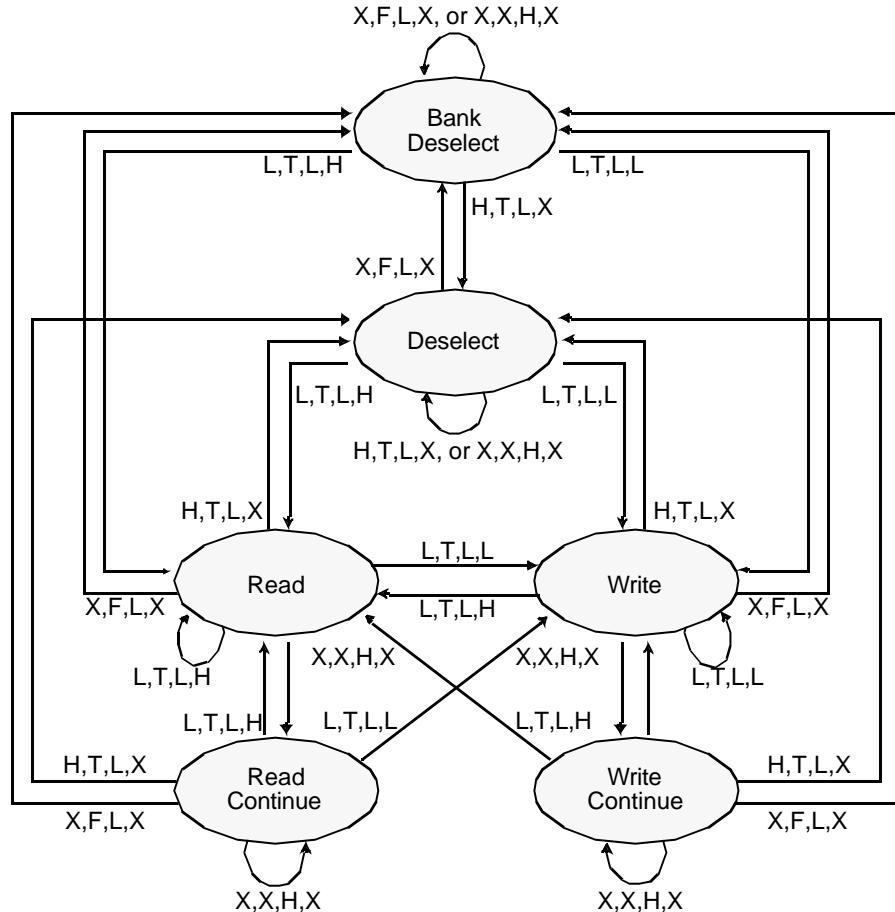
Example Four Bank Depth Expansion Schematic

Bank Enable Truth Table

	EP2	EP3	E2	E3
Bank 0	Vss	Vss	Active Low	Active Low
Bank 1	Vss	VDD	Active Low	Active High
Bank 2	VDD	Vss	Active High	Active Low
Bank 3	VDD	VDD	Active High	Active High

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STATE DIAGRAM FOR Double Late Write RAM

X,F,L,X, or X,X,H,X

Bank Deselect

L,T,L,H   L,T,L,L

H,T,L,X

X,F,L,X

Deselect

L,T,L,H   L,T,L,L

H,T,L,X, or X,X,H,X

H,T,L,X   H,T,L,X

L,T,L,L

Read   **Write**

L,T,L,H

X,F,L,X   X,F,L,X

L,T,L,H   L,T,L,L

X,X,H,X   X,X,H,X

L,T,L,H   L,T,L,L   L,T,L,H

H,T,L,X   **Read Continue**   **Write Continue**   H,T,L,X

X,F,L,X   X,F,L,X

X,X,H,X   X,X,H,X

Notes:
1. The notation "X,X,X,X" controlling the state transitions above indicate the states of inputs $\overline{E1}$,E,ADV, and $\overline{WE}$ respectively.
2. If (E2=EP2 and E3=EP3) then E="T" else E="F".
3. "H"=input "high"; "L"=input"low"; "X"=input"don' t care"; "T"=input "true"; "F"=input "false".

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TRUTH TABLES

Previous Cycle	Input Type	$\overline{E}_1$ (tn)	E (tn)	ADV (tn)	$\overline{WE}$ (tn)	$\overline{BW}$x (tn)	Current Operation	Address	DQ/CQ (tn)	DQ/CQ (tn+1)	Notes
N/A	D	H	T	L	X	X	Deselect Cycle	None	*	Hi-Z/CQ	4
Deselect	C	X	X	H	X	X	Deselect Cycle, Continue	Next	Hi-Z/CQ	Hi-Z/CQ	4
N/A	D	X	F	L	X	X	Bank Deselect Cycle	None	*	Hi-Z	4, 5
Bank Deselect	C	X	X	H	X	X	Bank Deselect Cycle, Continue	Next	Hi-Z	Hi-Z	4 , 5
N/A	R	L	T	L	H	X	Read Cycle, Begin Burst	External	*	Q/CQ	2
Read	C	X	X	H	X	X	Read Cycle, Continue Burst	Next	Q/CQ	Q/CQ	
N/A	W	L	T	L	L	X	Write Cycle, Begin Burst	External	*	D/CQ	2, 3
N/A	W	L	T	L	L	F	Non-Write Cycle, Begin Burst	External	*	*	2, 3
Write	C	X	X	H	X	T	Write Cycle, Continue Burst	Next	D/CQ	D/CQ	3
Write	C	X	X	H	X	F	Non-Write Cycle, Continue Burst	Next	*	D/CQ	3, 4, 5

Note:
1. X=Don' t Care, H=High, L=Low.
2. E=T(True) if E2=active and E3=active; E=F(False) if E2=inactive or E3=inactive .
3. " * " indicates that the DQ input requirement / output <u>state</u> and CQ output state are determined by the previous operation.
4. $\overline{BW}$x= F(False) if all Byte Write Enable pins are high. $\overline{BW}$x=T(True) if any one Byte Write Enable pin is low.
5. DQs are tri-state <u>in</u> response to Bank Deselect, Deselect, and Write commands.
6. Deassertion of $\overline{E}$1 does not deactive the echo clock outputs(CQ1, $\overline{CQ1}$, CQ2, $\overline{CQ2}$).

   Echo clock outputs are tri-stated in response to Bank Deselect Commands only.

WRITE TRUTH TABLE(x36)

$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b	$\overline{BW}$c	$\overline{BW}$d	OPERATION
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don′t Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(⤊).

WRITE TRUTH TABLE(x72)

$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b	$\overline{BW}$c	$\overline{BW}$d	$\overline{BW}$e	$\overline{BW}$f	$\overline{BW}$g	$\overline{BW}$h	OPERATION
H	X	X	X	X	X	X	X	X	READ
L	L	H	H	H	H	H	H	H	WRITE BYTE a
L	H	L	H	H	H	H	H	H	WRITE BYTE b
L	H	H	L	H	H	H	H	H	WRITE BYTE c
L	H	H	H	L	H	H	H	H	WRITE BYTE d
L	H	H	H	H	L	H	H	H	WRITE BYTE e
L	H	H	H	H	H	L	H	H	WRITE BYTE f
L	H	H	H	H	H	H	L	H	WRITE BYTE g
L	H	H	H	H	H	H	H	L	WRITE BYTE h
L	L	L	L	L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don′t Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(⤊).

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K7Z167288B
K7Z163688B
512Kx36 & 256Kx72 DLW(Double Late Write) RAM

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 2.9	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	-0.5 to V_{DD}	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	-0.5 to V_{DD}+0.3	V
Power Dissipation	P_D	1.6	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0°C \leq T_A \leq 70°C$)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	1.7	1.8	1.95	V
	V_{DDQ}	1.4	1.5	1.6	V
Ground	V_{SS}	0	0	0	V

*Note : V_{DD} and V_{DDQ} must be supplied with identical voltage levels.

DC ELECTRICAL CHARACTERISTICS(V_{DD}=1.8V + 150/-100mV, T_A=0°C to +70°C)

PARAMETER	SYM.	TEST CONDITIONS		MIN	MAX	UNIT	NOTE
Input Leakage Current	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	µA	
Operating Current	I_{CC}	V_{DD}=Max , I_{OUT}=0mA Cycle Time $\geq t_{CYC}$ Min -35	x72	-	TBD	mA	1,2
			x36	-	TBD		
Standby Current	I_{SB1}	E2 or E3 False, I_{OUT}=0mA , f=Max All Inputs$\leq V_{IL}$ or $\geq V_{IH}$		-	TBD	mA	
	I_{SB2}	$\overline{E1} \geq V_{IH}$, I_{OUT}=0mA, f=Max, All Inputs$\leq V_{IL}$ or $\geq V_{IH}$		-	TBD	mA	
	I_{SB3}	Device deselected, I_{OUT}=0mA, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	TBD	mA	
Input Low Voltage	V_{IL}			-0.3	V_{ref} * 0.1	V	3,5,6
Input High Voltage	V_{IH}			V_{ref} +0.1	V_{DD}+0.3	V	3,5,7
Output High Voltage(Programmable Impedance)	V_{OH1}			V_{DDQ}/2	V_{DDQ}	V	8
Output Low Voltage(Programmable Impedance)	V_{OL1}			V_{SS}	V_{DDQ}/2	V	9
Output High Voltage(I_{OH}=-0.1mA)	V_{OH2}			V_{DDQ}-0.2	V_{DDQ}	V	10
Output Low Voltage(I_{OL}=0.1mA)	V_{OL2}			V_{SS}	0.2	V	10

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
    2. Data states are all zero.
    3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V
    4. The EP2, EP3 pins must not be changed during operation.
    5. These are DC test criteria. DC design criteria is $V_{REF}\pm$50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
    6. V_{IL} (Min)DC=-0.3V, V_{IL} (Min)AC=-1.5V(pulse width $\leq$ 3ns).
    7. V_{IH} (Max)DC=V_{DDQ}+0.3, V_{IH} (Max)AC=V_{DDQ}+0.85V(pulse width $\leq$ 3ns).
    8. $|I_{OH}|$=(V_{DDQ}/2)/(RQ/5)$\pm$15% @ V_{OH}=V_{DDQ}/2 for 175$\Omega \leq$ RQ $\leq$ 350Ω.
    9. $|I_{OL}|$=(V_{DDQ}/2)/(RQ/5)$\pm$15% @ V_{OL}=V_{DDQ}/2 for 175$\Omega \leq$ RQ $\leq$ 350Ω.
    10. Minimum Impedance Mode when ZQ pin is connected to V_{SS}.
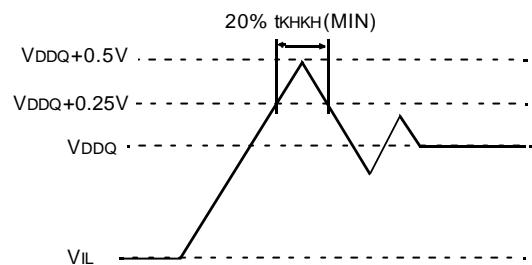
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CAPACITANCE*(T_A=25°C, f=1MHz)
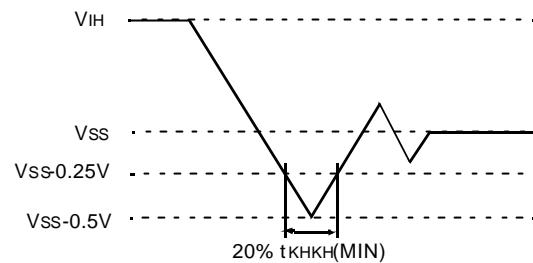
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	TBD	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	TBD	pF

*Note : Sampled not 100% tested.

Overershoot Timing

Undershoot Timing
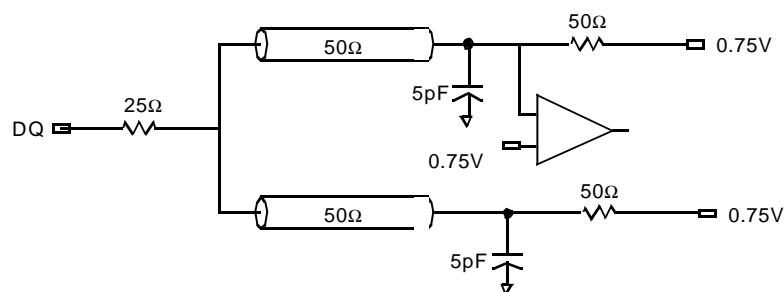
Note: For power-up, $V_H \leq V_{DDQ}$+0.3V and $V_{DD} \leq$ 1.7V and $V_{DDQ} \leq$ 1.4V t $\leq$ 200ms

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V_{DD}	1.7~1.9	V
Output Power Supply Voltage	V_{DDQ}	1.4~1.6	V
Input High/Low Level	V_{IH}/V_{IL}	1.25/0.25	V
Input Reference Level	V_{REF}	0.75	V
Input Rise/Fall Time	T_R/T_F	0.3/0.3	ns
Output Timing Reference Level		V_{DDQ}/2	V

Note: Parameters are tested with RQ=250Ω

AC TEST OUTPUT LOAD

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AC TIMING CHARACTERISTICS (V$_{DD}$=1.8V + 150/-100mV, T$_A$=0 to 70°C)
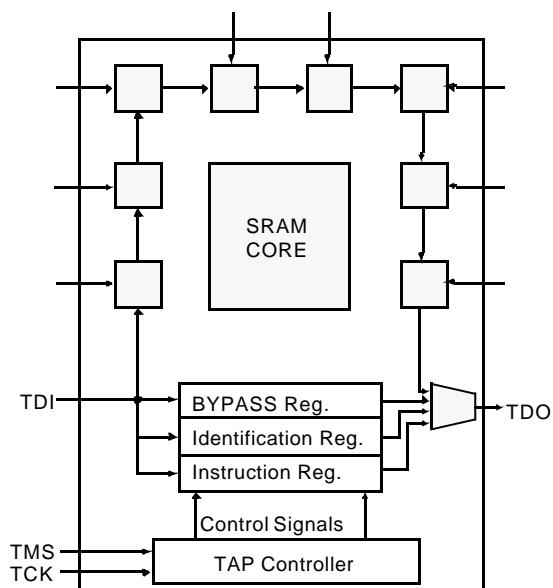
PARAMETER	SYMBOL	-35 $\overline{SD}$=VDD		-35 $\overline{SD}$=VSS		UNIT
		MIN	MAX	MIN	MAX	
Cycle Time	tKHKH	2.85	-	2.85	-	ns
Clock High to Output Valid	tKHQV	-	1.7	-	2.6	ns
Clock High to Output High-Z	tKHQZ	0.5	1.7	1.4	2.6	ns
Output Hold from Clock High	tKHQX	0.5	-	1.4	-	ns
Clock High to Output Low-Z	tKHQX1	0.5	-	1.4	-	ns
Clock High to CQ High	tKHCH	0.5	1.7	1.4	2.6	ns
Clock Low to CQ Low	tKLCL	0.5	1.7	1.4	2.6	ns
Output Hold from CQ High	tCHQX	-0.4	-	-0.4	-	ns
CQ High to Output Low-Z	tCHQX1	-0.4	-	-0.4	-	ns
CQ High to Output Valid	tCHQV	-	0.4	-	0.4	ns
Clock High to CQ Low-Z	tKHCX1	0.5	-	1.4	-	ns
Clock High to CQ High-Z	tKHCZ	0.5	1.5	1.4	2.4	ns
Clock High Pulse Width	tKHKL	1.2	-	1.2	-	ns
Clock Low Pulse Width	tKLKH	1.2	-	1.2	-	ns
Address Setup to Clock High	tAVKH	0.6	-	0.6	-	ns
Chip Enable Setup to Clock High	tEVKH	0.6	-	0.6	-	ns
Write Setup to Clock High($\overline{WE}$, $\overline{BW}$x)	tWVKH	0.6	-	0.6	-	ns
Data Setup to Clock High	tDVKH	0.6	-	0.6	-	ns
Address Advance Setup to Clock High	tadvVKH	0.6	-	0.6	-	ns
Address Hold from Clock High	tKHAX	0.4	-	0.4	-	ns
Chip Enable Hold from Clock High	tKHEX	0.4	-	0.4	-	ns
Write Hold from Clock High($\overline{WE}$, $\overline{BW}$x)	tKHWX	0.4	-	0.4	-	ns
Data Hold from Clock High	tKHDX	0.4	-	0.4	-	ns
Address Advance Hold from Clock High	tKHadvX	0.4		0.4		ns

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{E1}$ is
sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by $\overline{WE}$ low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low,
Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature tKHQX1 is more than tKHQZ.
The specs as shown do not imply bus contention because tKHQX1 is a Min. parameter that is worst case at totally different test conditions
(0°C,1.95V) than tKHQZ, which is a Max. parameter(worst case at 70°C,1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG
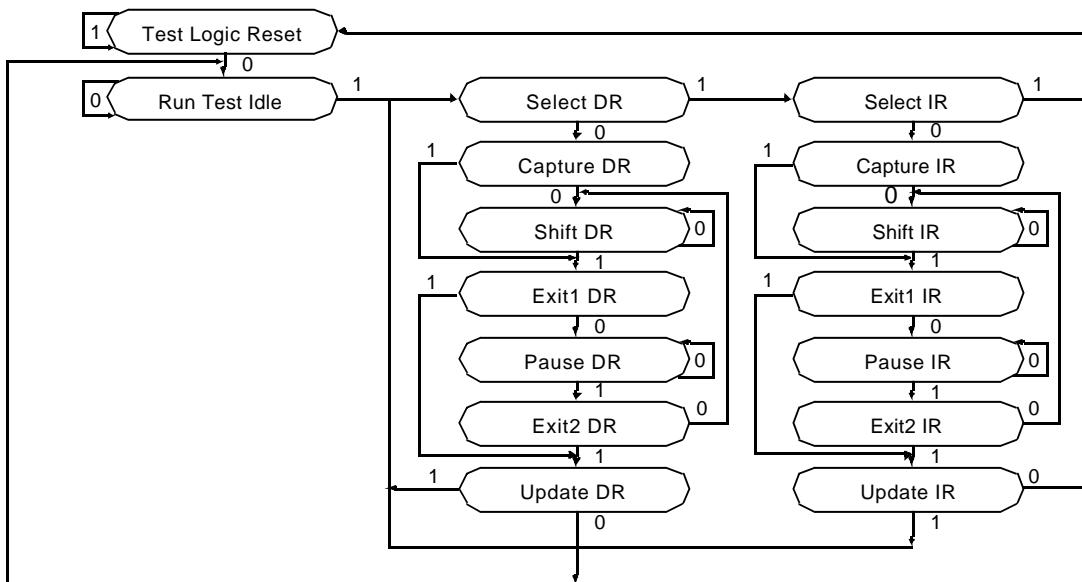
This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram

JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE :
1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
512Kx36	3 bits	1 bits	32 bits	121 bits
256Kx72	3 bits	1 bits	32 bits	121 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
512Kx36	0000	00111 00100	XXXXXX	00001001110	1
256Kx72	0000	00110 00101	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER

Order	Pin ID	Order	Pin ID	Order	Pin ID	Order	Pin ID
1	6W	36	11H	71	4A	106	2R
2	6V	37	10H	72	3C	107	1R
3	6U	38	10G	73	3B	108	1T
4	7V	39	11G	74	3A	109	2T
5	7U	40	11F	75	2A	110	2U
6	7W	41	10F	76	1A	111	1U
7	8U	42	10E	77	1B	112	1V
8	8V	43	11E	78	2B	113	2V
9	9V	44	11D	79	2C	114	2W
10	10W	45	10D	80	1C	115	1W
11	11W	46	10C	81	1D	116	3V
12	11V	47	11C	82	2D	117	4V
13	10V	48	11B	83	1E	118	4U
14	10U	49	10B	84	2E	119	5U
15	11U	50	10A	85	2F	120	5V
16	11T	51	11A	86	1F	121	5W
17	10T	52	9C	87	1G		
18	11R	53	9B	88	2G		
19	10R	54	9A	89	2H		
20	10P	55	8C	90	1H		
21	11P	56	8B	91	1J		
22	11N	57	8A	92	2J		
23	10N	58	7B	93	1K		
24	10M	59	7A	94	6N		
25	11M	60	6H	95	3K		
26	11L	61	6G	96	4K		
27	10L	62	6D	97	2K		
28	11K	63	6C	98	2L		
29	6M	64	6B	99	1L		
30	6L	65	6A	100	1M		
31	6J	66	5C	101	2M		
32	6F	67	5A	102	2N		
33	10K	68	4C	103	1N		
34	10J	69	4B	104	1P		
35	11J	70	5B	105	2P		

NOTE,   NC,MCL and MCH ; Don't Care

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JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
Input High Level	V_{IH}	1.3	-	V_{DD}+0.3	V	1
Input Low Level	V_{IL}	-0.3	-	0.5	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	1.5	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.45	V	

*Note : 1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V
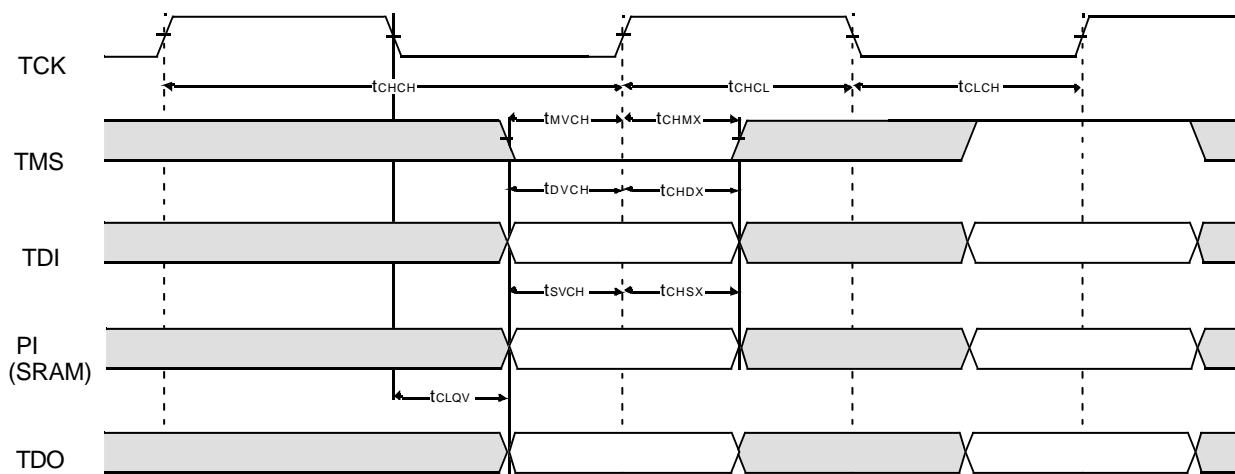
JTAG AC TEST CONDITIONS
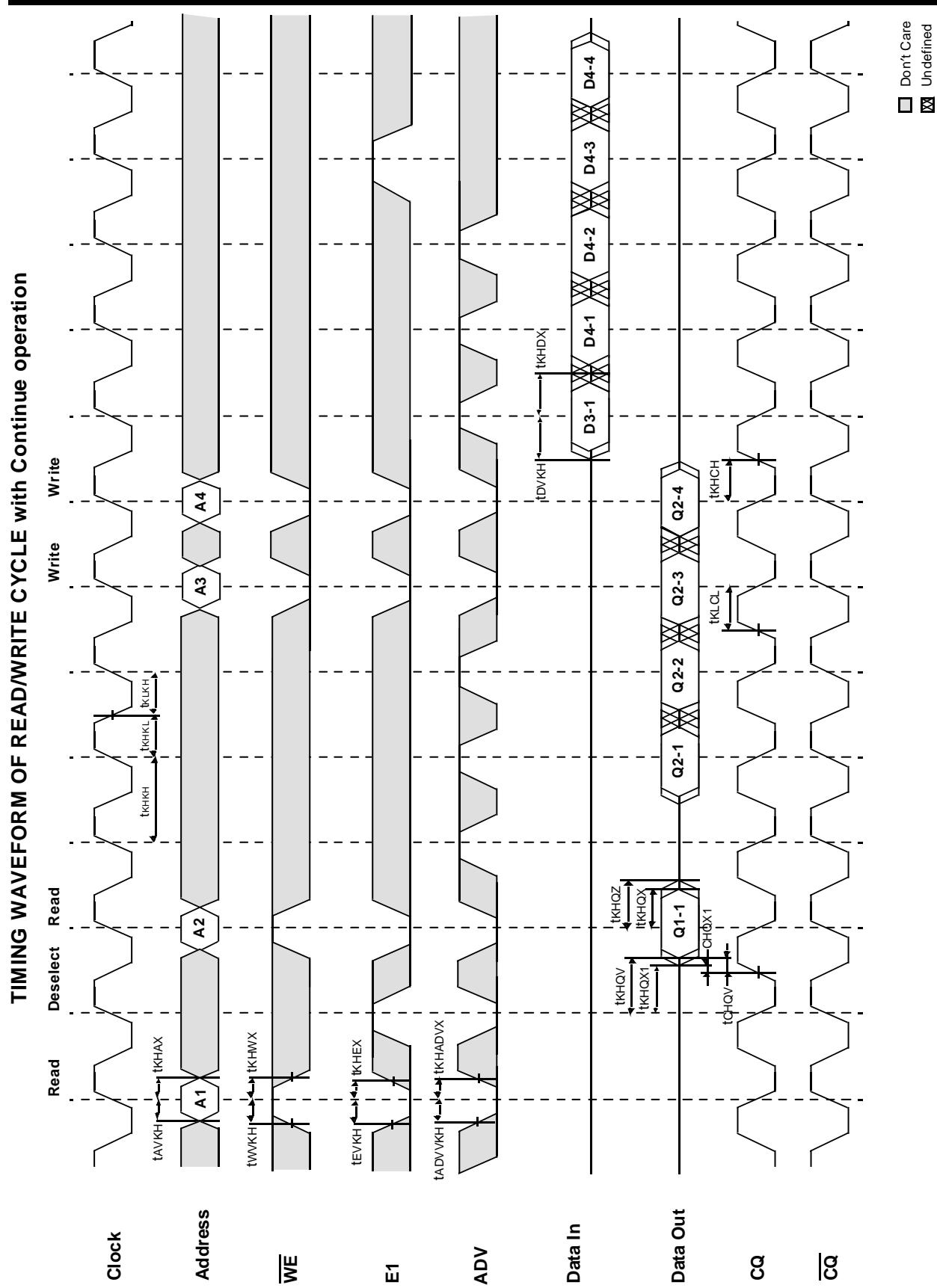
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.3/0.5	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	
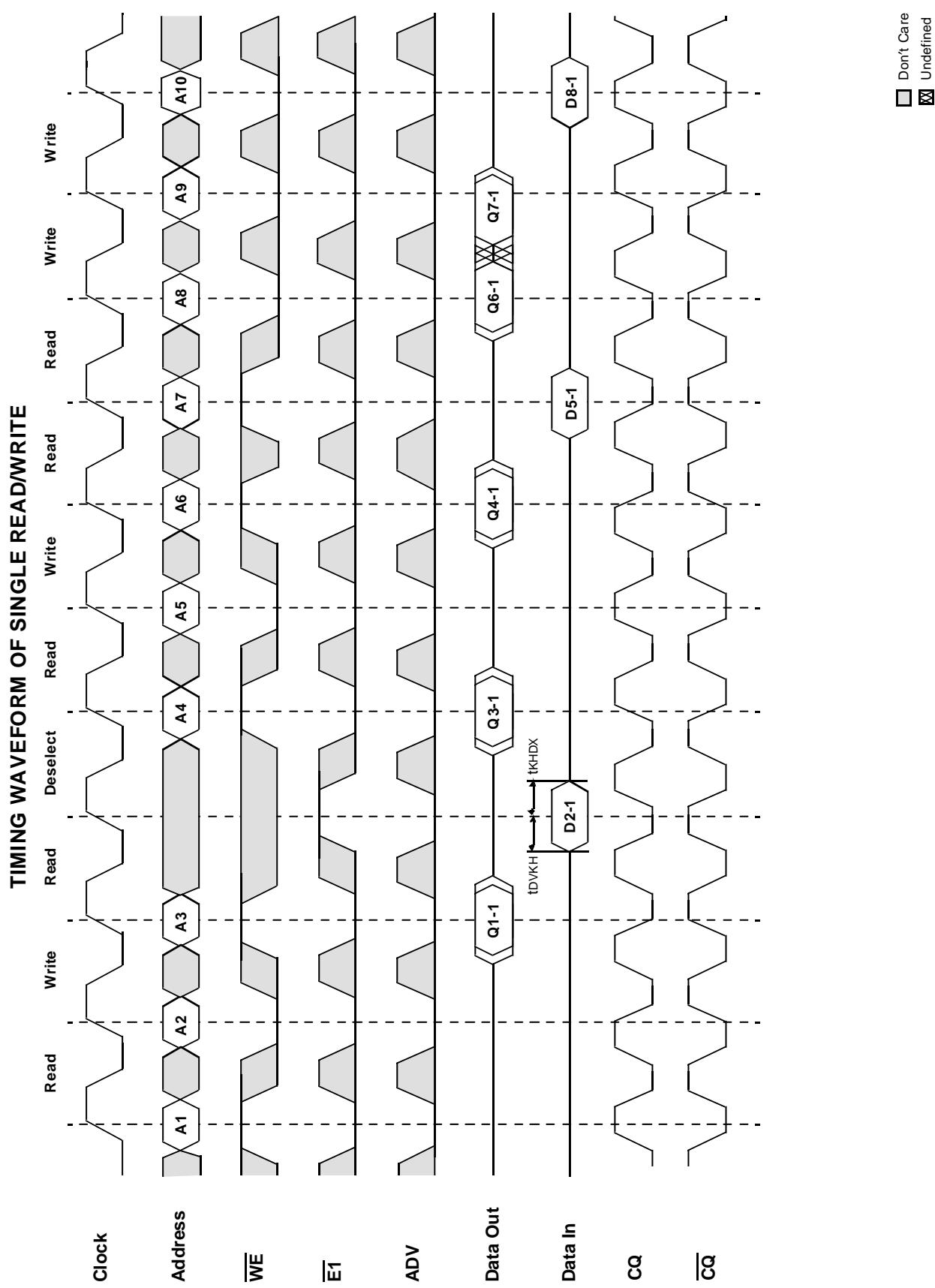
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	20	-	ns	
TCK High Pulse Width	t_{CHCL}	10	-	ns	
TCK Low Pulse Width	t_{CLCH}	10	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM

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TIMING WAVEFORM OF READ/WRITE CYCLE with Continue operation

Read   Deselect   Read   Write   Write

Clock

Address   A1   A2   A3   A4

WE

E1

ADV

Data In   D3-1   D4-1   D4-2   D4-3   D4-4

Data Out   Q1-1   Q2-1   Q2-2   Q2-3   Q2-4

CQ

CQ

tAVKH
tKHAX
tWVKH
tKHWX
tEVKH
tKHEX
tADVVKH
tKHADVX
tKHHKH
tKHHKL
tKLKH
tKHQV
tKHQX1
tKHQZ
tKHQX
tCHQX1
tCHQV
tDVKH
tKHDX
tKLCL
tKHCH

Don't Care
Undefined

TIMING WAVEFORM OF SINGLE READ/WRITE

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ECHO CLOCK CONTROL IN TWO BANKS

NOTE: E1 does not deselect the Echo Clock Outputs. Echo Clock Outputs are de selected by E2 or E3 being sampled false.

BANK SWITCH WITH E1 DESELECT

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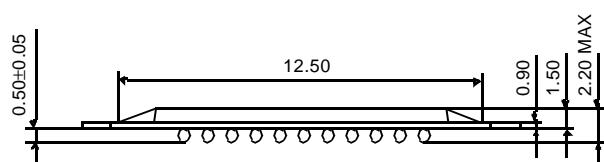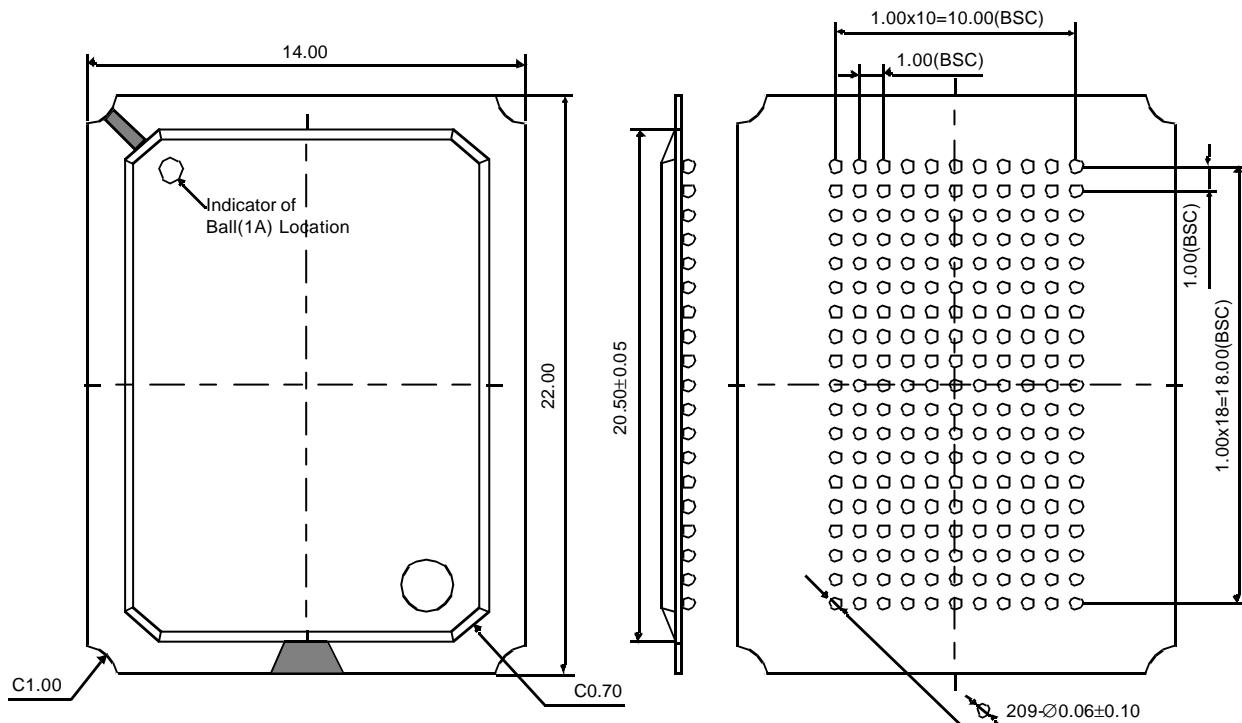
209 Bump BGA PACKAGE DIMENSIONS

14mm x 22mm Body, 1.0mm Bump Pitch, 11x19 Bump Array

NOTE :
1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset: 0.10 MAX.
3. PCB to Cavity Offset: 0.10 MAX.

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