Preliminary User's Manual

NEC

IE-703017-MC-EM1

In-circuit Emulator Option Board

Target device
V850/SA1

[MEMO]

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Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

• Device availability

• Ordering information

• Product release schedule

• Availability of related technical literature

• Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

• Network requirements

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INTRODUCTION

READERS

    This manual is intended for users who design and develop application systems using the V850/SA1.

PURPOSE

    The purpose of this manual is to describe the proper operation of the IE-703017-MC-EM1 and its basic specifications.

ORGANIZATION

    This manual is broadly divided into the following parts.
- Overview
- Name and function of components
- Cautions

HOW TO READ THIS MANUAL

    This manual assumes readers who have general knowledge of electric engineering, logic circuits, and microcomputers.

    The IE-703017-MC-EM1 is used connected to the IE-703002-MC in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703002-MC when it is connected to the IE-703017-MC-EM1. For the names and functions, and the connection of components, refer to the IE-703002-MC User's Manual – Hardware.

    To broadly learn about the basic specifications and operation methods
        → Read this manual in the order listed in **CONTENTS**.

    To learn the operation methods and command functions, etc., of the IE-703002-MC and IE-703017-MC-EM1
        → Read the user's manual of the debugger (optional) that is used.

LEGEND

Note	:	Footnote explaining items marked with ″Note″ in the text
Caution	:	Information requiring special attention.
Remark	:	Supplementary information provided in addition to the text
Numeral representations	:	Binary ⋯ xxxx or xxxxB
		Decimal ⋯ xxxx
		Hexadecimal ⋯ xxxxH

Prefix representing the power of 2 (Address space, Memory capacity):

        K (kilo)   : $2^{10} = 1024$
        M (mega) : $2^{20} = 1024^2$

TERMINOLOGY

The meaning of terms used in this manual is listed below.

Target device	Device that is emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and user-configured hardware.

RELATED DOCUMENTS

Some of the related documents listed below may be preliminary versions, but are not noted as such.

○ **Documents related V850/SA1**

Document	Document Number
V850/SA1 User's Manual-Hardware	U12768E
V850 Family™ User's Manual-Architecture	U10243E
μPD703015 Data Sheet	To be prepared
μPD703015Y Data Sheet	To be prepared
μPD703017 Data Sheet	To be prepared
μPD703017Y Data Sheet	To be prepared

○ **Documents related to development tools (User's Manual)**

Product		Document Number
IE-703002-MC (In-circuit emulator)		U11595E
IE-703017-MC-EM1 (In-circuit emulator option board)		This manual
CA850 (C Compiler package)	Operation UNIX™ based	U12839E
	Operation Windows™ based	U12827E
	C language	U12840E
	Assembly Language	U10543E
	Project manager (Windows-based)	U11991E
RX850 (Real-time OS)	Basics	U12861E
	Technical	U11117E
	Nucleus installation	U11038E
	Debugger Windows-based	U11158E
	Installation (UNIX-based)	U12863E
	Installation (Windows-based)	U12862E
AZ850 (System performance analyzer) − Operation		U11181E
ID850 (C source debugger)	Operation Windows-based	U11196E
	Operation UNIX-based	U12209E
	Installation UNIX-based	U12210E

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[MEMO]

CHAPTER 1 OVERVIEW

The IE-703017-MC-EM1 is an optional board for the IE-703002-MC in-circuit emulator. By connecting the IE-703017-MC-EM1 and IE-703002-MC, hardware and software can be debugged efficiently in system development using the V850/SA1.

In this manual, the basic setup sequences and switch settings of the IE-703002-MC when using IE-703017-MC-EM1 are described. For the names and functions of the parts of the IE-703002-MC, and for the connection of elements, refer to the **IE-703002-MC User's Manual**.

1.1 Hardware Configuration

Optional hardware	
In-circuit emulator (IE-703002-MC)	

Option board (IE-703017-MC-EM1)	IE-703002-MC can be used as in-circuit emulator for V850/SA1 by adding this board.

Optional hardware	
Extension probe (SC-100SD[Note 1])	General-purpose extension probe made by TOKYO ELETECH CORPORATION
PC interface board (IE-70000-xx-IF-B, IE-70000-xx-IF-C)	This board is used to connect the IE-703002-MC to a personal computer. This board is inserted in the expansion slot of the personal computer.
Network module (IE-70000-MC-SV3[Note 2])	The module is used when a workstation controls the IE-703002-MC via ethernet™.
Power adapter (IE-70000-MC-PS-B)	AC adapter dedicated to the IE-703002-MC

Notes 1. Contact: Daimaru Kogyo Co., Ltd.   Tokyo Electronic Components Division (TEL 03-3820-7112)
                                                    Osaka Electronic Components Division (TEL 06-244-6672)

2. Under development

1.2 Features (When connected to IE-703002-MC)

○ Maximum operation frequency: 17 MHz (at 3.3-V operation)

○ Extremely lightweight and compact

○ Higher equivalence with target device can be achieved by omitting buffer between signal cables.

○ Following pins can be masked.
   $\overline{RESET}$, $\overline{NMI}$, $\overline{WAIT}$, $\overline{HLDRQ}$

○ Two methods of connection to target system:

   • Pod tip direct connection (For information on the pod, refer to the **IE-703002-MC User's Manual**)

   • Attach an extension probe (optional) to the pod tip for connection.

○ Dimensions of the IE-703017-MC-EM1 are as follows.

Parameter		Value
Power dissipation (Max. value at 3.3-V supply voltage)		0.35 W (at 17-MHz operation frequency)**Note**
External dimensions (Refer to **APPENDIX DIMENSIONS**)	Height	15 mm
	Length	194 mm
	Width	96 mm
Weight		160 g

Note 10.35 W when IE-703002-MC with IE-703017-MC-EM1

1.3 Function Specifications (When connected to IE-703002-MC)

Parameter			Capacity
Emulation memory capacity	Internal ROM		256 Kbytes
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte
Execution/pass detection coverage memory capacity	Internal ROM		256 Kbytes
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte
Memory access detection coverage memory capacity (external memory)			1 Mbyte
Coverage memory capacity for branching entry number counting	Internal ROM		256 Kbytes
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte

Caution   Some of the functions may not be supported depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703002-MC to IE-703017-MC-EM1 and a personal computer (PC-9800 series or PC/AT™ (or compatibles)) is shown below.

Figure 1-1. System Configuration
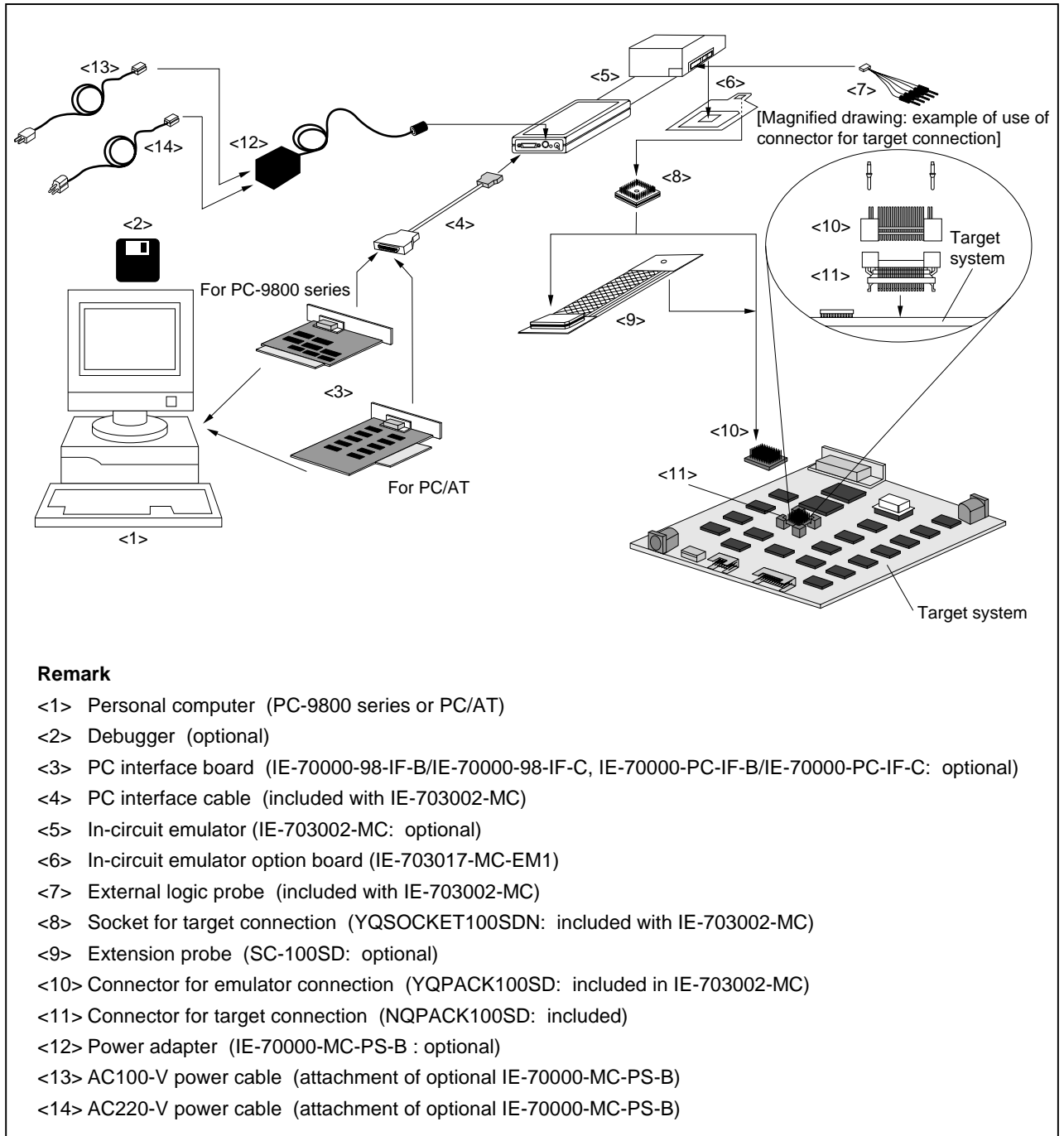
Remark

<1> Personal computer (PC-9800 series or PC/AT)

<2> Debugger (optional)

<3> PC interface board (IE-70000-98-IF-B/IE-70000-98-IF-C, IE-70000-PC-IF-B/IE-70000-PC-IF-C: optional)

<4> PC interface cable (included with IE-703002-MC)

<5> In-circuit emulator (IE-703002-MC: optional)

<6> In-circuit emulator option board (IE-703017-MC-EM1)

<7> External logic probe (included with IE-703002-MC)

<8> Socket for target connection (YQSOCKET100SDN: included with IE-703002-MC)

<9> Extension probe (SC-100SD: optional)

<10> Connector for emulator connection (YQPACK100SD: included in IE-703002-MC)

<11> Connector for target connection (NQPACK100SD: included)

<12> Power adapter (IE-70000-MC-PS-B : optional)

<13> AC100-V power cable (attachment of optional IE-70000-MC-PS-B)

<14> AC220-V power cable (attachment of optional IE-70000-MC-PS-B)

1.5 Contents in Carton

The carton of the IE-703017-MC-EM1 contains a main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and the connector accessories. In case of missing or damaged contents, please contact an NEC sales representative or NEC dealer.
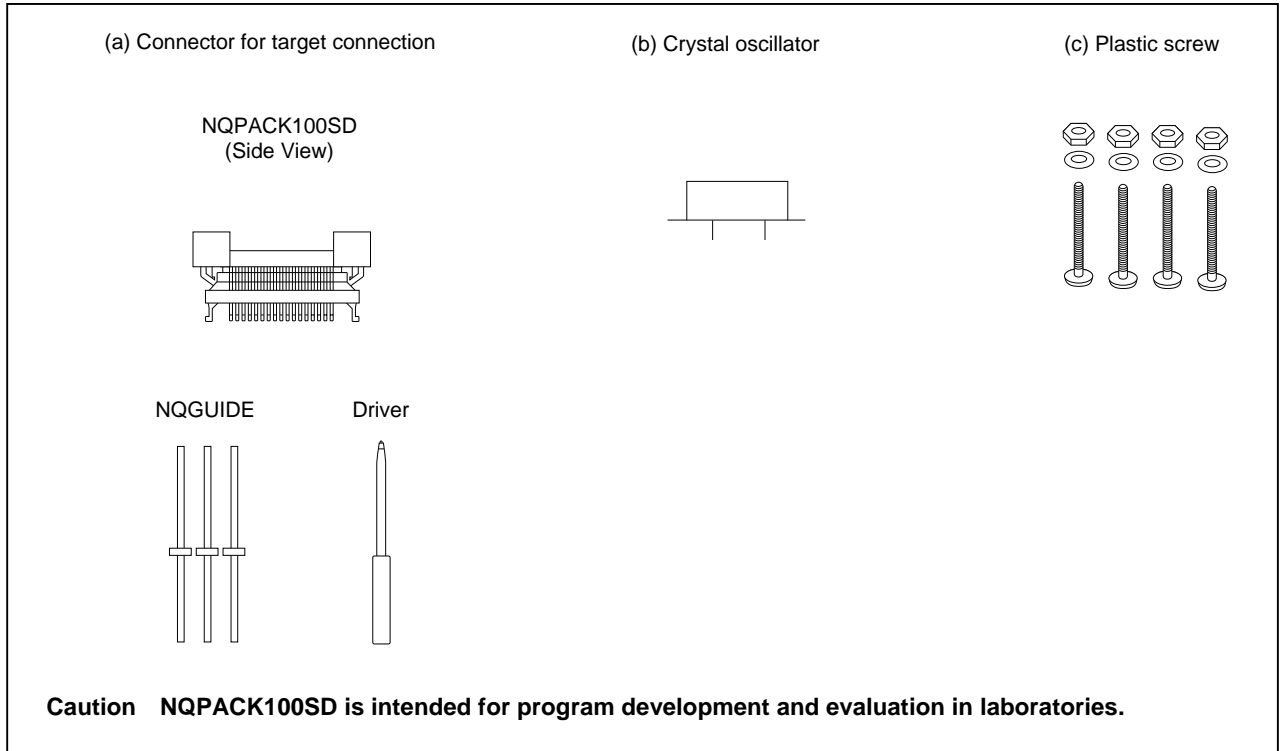
Figure 1-2. Contents in Carton

<1> IE-703017-MC-EM1 × 1 pc.
<2> Accessory bag × 1 pc.
<3> Guarantee card × 1 pc.
<4> Packing list × 1 sheet
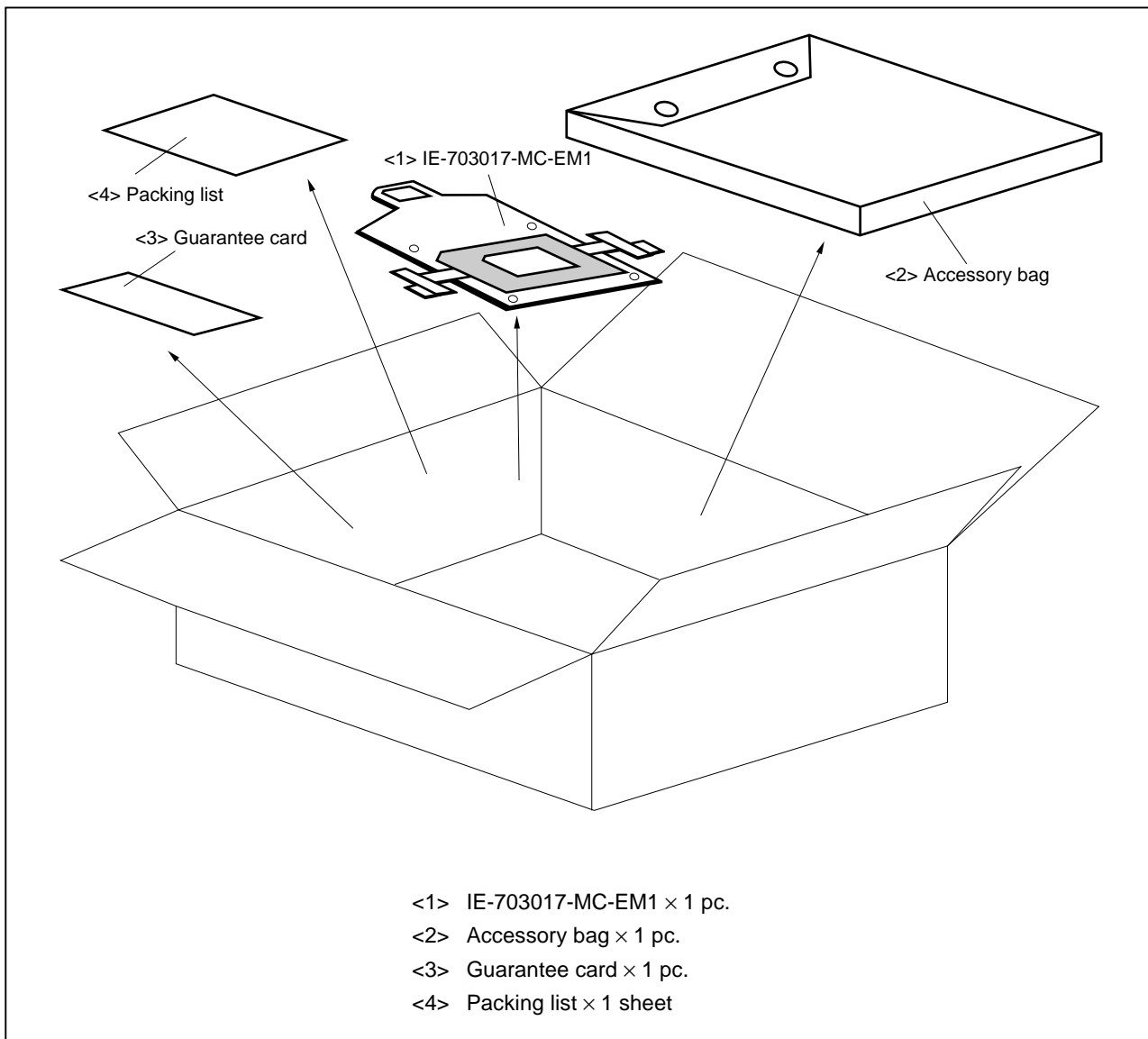
Check that the accessory bag contains this manual, an accessory list, and the following accessories.

(a) Connector for target connection (NQPACK100SD) × 1 set
    (including NQGUIDE 3 pcs., screw driver × 1 pc.)
(b) Crystal oscillator (17 MHz, 8-pin type): 1 pc.
(c) Plastic screws × 4 pcs.
    (including nuts and washer × 4 sets)

Figure 1-3. Accessories

(a) Connector for target connection

NQPACK100SD
(Side View)

NQGUIDE   Driver

(b) Crystal oscillator

(c) Plastic screw

Caution   NQPACK100SD is intended for program development and evaluation in laboratories.

1.6 Connection between IE-703002-MC and IE-703017-MC-EM1

The procedure for connecting the IE-703002-MC and IE-703017-MC-EM1 is described below.

Caution   Connect carefully so as not to break or bend connector pins.

<1> Remove the pod cover (upper and lower) of the IE-703002-MC.

<2> Replace the crystal oscillator mounted in the pod of the IE-703002-MC with the attached crystal oscillator (17 MHz) or user's oscillator (with user's frequency).

<3> Set the PGA socket lever of the IE-703017-MC-EM1 to the OPEN position as shown in Figure 1-4 (b).

<4> Connect the IE-703017-MC-EM1 to the PGA socket at the back of the pod (refer to Figure 1-4 (c)). When connecting, position the IE-703002-MC and IE-703017-MC-EM1 so that they are horizontal.

<5> Set the PGA socket lever of the IE-703017-MC-EM1 to the CLOSE position as shown in Figure 1-4 (b).

<6> Set the jumpers (JP1 to JP4). Open JP1 and JP3 (Remove the jumper contact. Attach the removed jumper contact to one of the jumper pins to avoid losing them.)
Retain the factory settings of JP2 (first and second pins shorted, and the fifth and sixth pins shorted).
Short the second and third pins of JP4.

<7> Fix the IE-703017-MC-EM1 between the pod covers (upper and lower) with the plastic screws (supplied in IE-703002-MC).

<8> Secure the pod cover (upper) end with nylon rivets.

> **Remark**   For JP1 setting, refer to **2.3 Illegal Access Detection ROM Setting**. For JP3 and JP4, refer to **2.4 CPU Operation Voltage Range Switch Setting**.

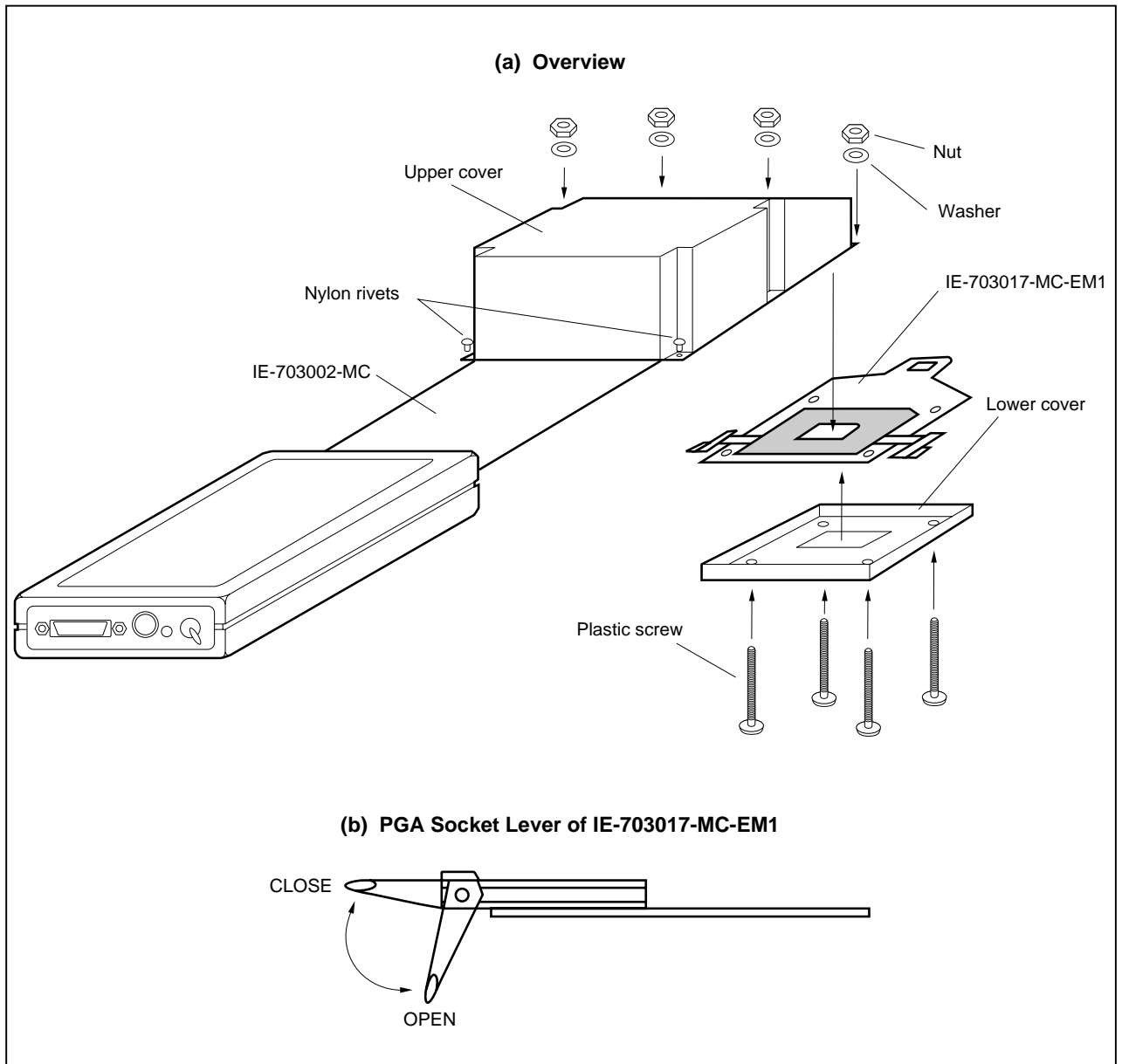**Figure 1-4. Connection between IE-703002-MC and IE-703017-MC-EM1 (1/2)**

(a) Overview

Upper cover

Nut

Washer

Nylon rivets

IE-703017-MC-EM1

IE-703002-MC

Lower cover

Plastic screw

(b) PGA Socket Lever of IE-703017-MC-EM1

CLOSE

OPEN

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Figure 1-4. Connection between IE-703002-MC and IE-703017-MC-EM1 (2/2)

(c) Connecting part (IE-703017-MC-EM1)

Pin A1 location

● : Insertion guide

◯ : IE-703002-MC insertion area
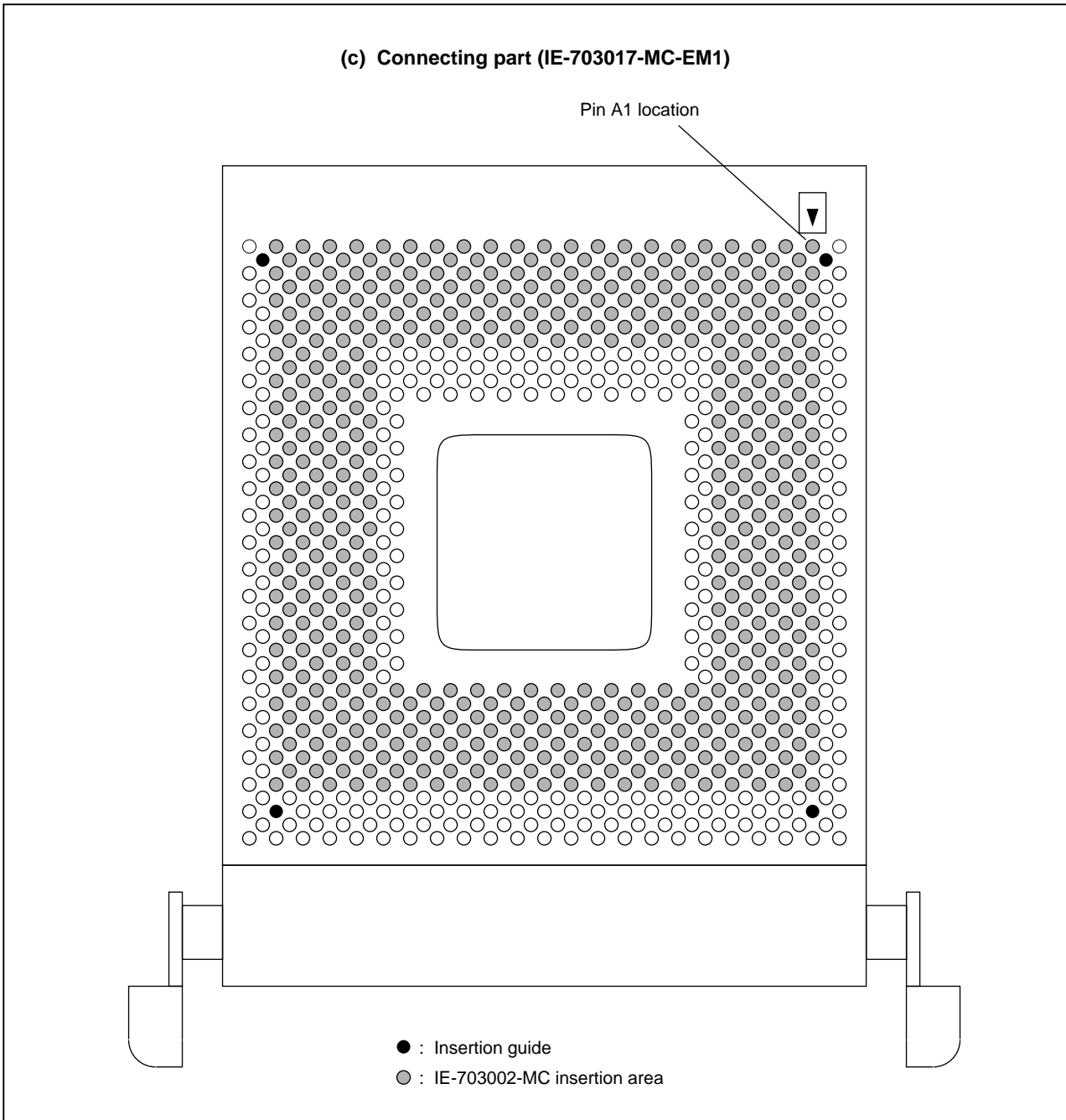
CHAPTER 2   NAME AND FUNCTION OF COMPONENTS

This chapter describes the names, functions, and switch settings of components comprising the IE-703017-MC-EM1. For the details of the pod, jumpers, and switch positions, etc., refer to **IE-703002-MC User's Manual**.

2.1   Component Name and Function of IE-703017-MC-EM1

Figure 2-1. IE-703017-MC-EM1
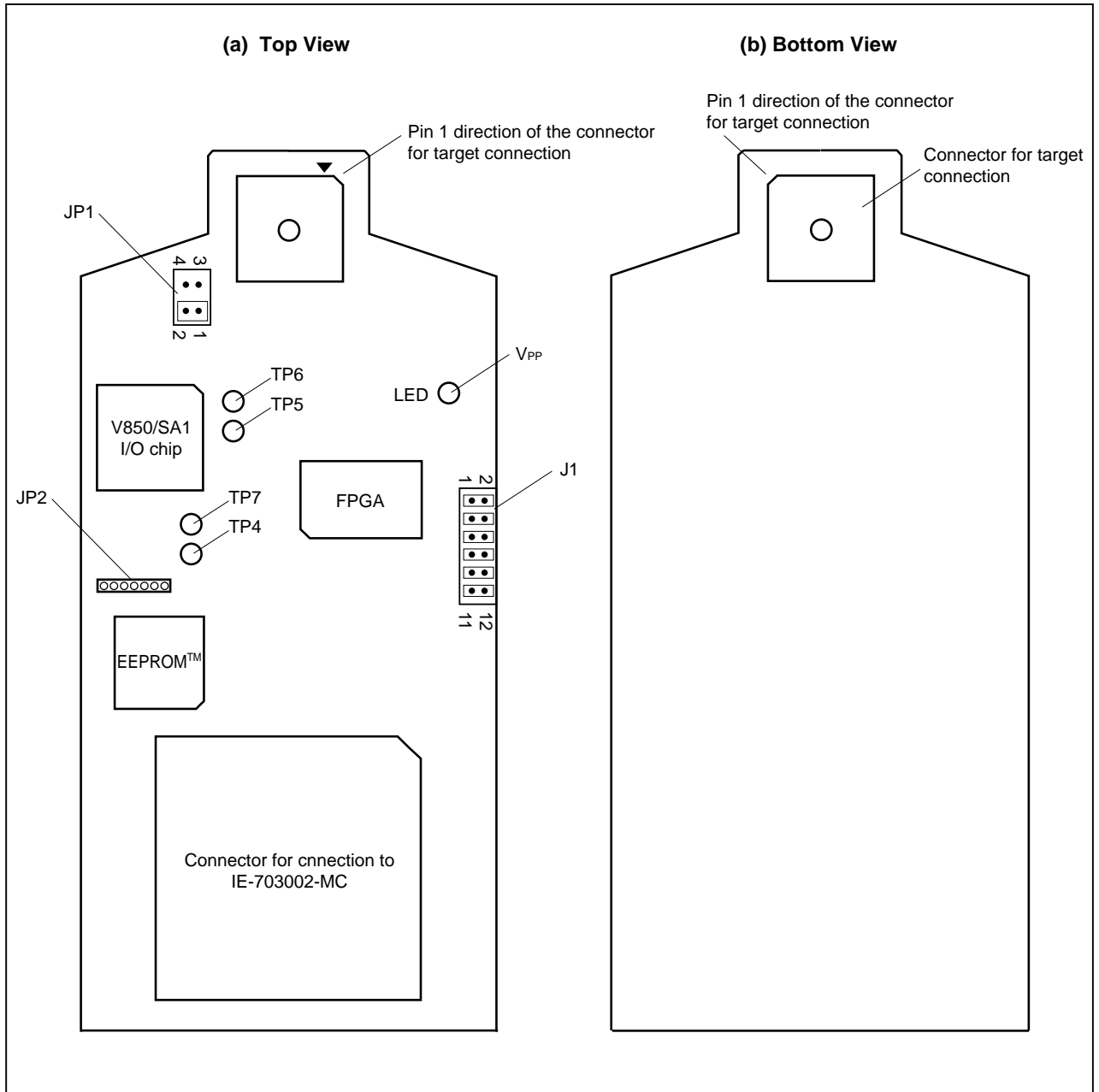
(1) Test pin (TP4-TP7)

These pins are used for testing analog signals for the emulator as a standalone unit.

- TP4: AV_{REF}
- TP5: AV_{SS}
- TP6: AV_{DD}
- TP7: P70 (Analog port)

(2) JP1

This is the switch jumper of the main clock supply source. (For details, refer to **2.2 Clock Settings**)

(3) JP2

This is a pin block for supplying the subclock. (For details, refer to **2.2 Clock Settings**)

(4) LED

LED for V_{PP}

ON: Voltage is applied to V_{PP}

OFF: Voltage is not applied to V_{PP}

(5) Connector for IE-703002-MC connection

This is a connector to connect with the IE-703002-MC.

(6) Connector for target connection

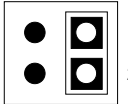This is a connector to connect the target system or the extension probe.
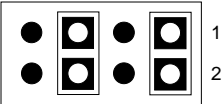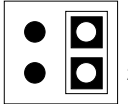
2.2 Clock Settings
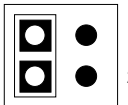
This section describes the clock settings.

For JP1 and JP2 in IE-703017-MC-EM1, refer to Figure 2-1.

For the jumper switch position in the IE-703002-MC, refer to **IE-703002-MC User's Manual**.

2.2.1 Main clock settings

Table 2-1. Main Clock Setting

Emulator use environment	Clock supply method	IE-703017-MC-EM1 setting	IE-703002-MC setting		
		JP1	SW1	SW2	JP2
When using emulator as standalone unit	Internal clock	3 ● □ 1 4 ● □ 2	ON	ON	7 ● □ ● □ 1 8 ● □ ● □ 2
When using emulator with target system	Internal clock	3 ● □ 1 4 ● □ 2			
	Target clock	3 □ ● 1 4 □ ● 2			

2.2.2 Subclock settings

Table 2-2. Subclock Setting

| Emulator use environment	Clock supply method	IE-703017-MC-EM1 setting
		JP2
When using emulator as standalone unit	Internal clock[Note 1]	Oscillator is included (32.768 kHz oscillation circuit is included at factory shipment)[Note 3]
When using emulator with target system	Internal clock[Note 1]	Oscillator is included (32.768 kHz oscillation circuit is included at factory shipment)[Note 3]
	Target clock[Note 2]	Short between XT1 and TG[Note 4]
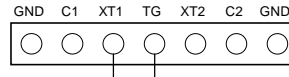
Notes 1. Internal clock does not support the clock input by oscillator.

    2. The target clock supports only an oscillator, and does not support clock input by resonator.

    3. To use the sub-clock frequency of 32.768 kHz, remove the clock module on JP2 and set an oscillation circuit.

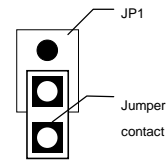   The settings of JP2 are as follows.
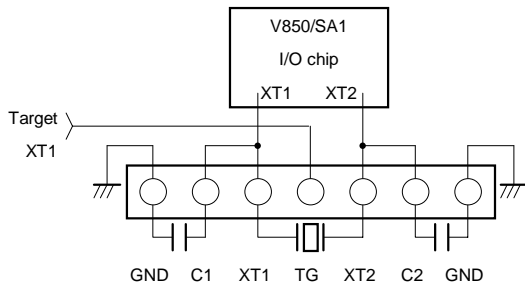
    4. Use a short pin

2.3 Illegal Access Detection ROM Setting

If using the IE-703002-MC for an in-circuit emulator for V850/SA1 by connecting IE-703017-MC-EM1, set JP1 of the IE-703002-MC as follows.

Table 2-3. JP1 setting in IE-703002-MC

JP1		Description
Open**Note**		Illegal Access Detection ROM (mounted on IE-703017-MC-EM1) for V850/SA1 is used.
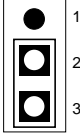
Note When JP1 is set open, keep the removed jumper contact attached to one pin as shown in the drawing at right.

2.4 CPU Operation Voltage Range Switching Setting

If using the IE-703002-MC for an in-circuit emulator for V850/SA1 by connecting IE-703017-MC-EM1, set JP3 and JP4 of the IE-703002-MC as follows.

Table 2-4. JP3 and JP4 Setting in IE-703002-MC

JP3, JP4		Description
JP3	 (Open)	Operating voltage range of IE-703002-MC is from 2 to 3.6 V.
JP4		Operating voltage range of target system is from 2 to 4.5 V. (Since operating voltage of V850/SA1 is from 2 to 3.6 V, this setting is effective)

Caution **With the setting of JP3 and JP4, the IE-703002-MC operates in the same voltage as the target system if the target system power is ON. If the target system power is OFF or the emulator is used as a stand-alone unit, the IE-703002-MC always operates in 3.3 V.**

2.5 Separate Bus Function Setting
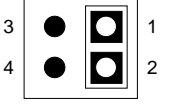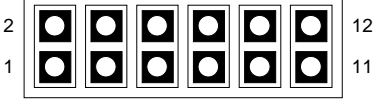
To use the separate bus function, J1 of IE-703017-MC-EM1 must be set. Table 2-5 shows the correspondence between the MAM register and J1 settings.

Table 2-5. MAM Register and J1 Setting Correspondence

MAM2	MAM1	MAM0	Operation of P34-P36, P100-P107, P110-P113		J1 Setting
0	0	0	P34-P36	Port mode	Pins 1-2 to 11-12: all open
			P100-P107	Port mode	
			P110-P113	Port mode	
0	1	0	P34-P36	Port mode	Pins 1, 2 shorted; rest open
			P100-P107	Port mode	
			P110-P113	A1-A4	
0	1	1	P34-P36	Port mode	Pins 1-4 shorted; rest open
			P100-P103	A5-A8	
			P104-P107	Port mode	
			P110-P113	A1-A4	
1	0	0	P34-P36	Port mode	Pins 1-6 shorted; rest open
			P100-P107	A5-A12	
			P110-P113	A1-A4	
1	0	1	P34	A13	Pins 1-8 shorted; rest open
			P35, P36	Port mode	
			P100-P107	A5-A12	
			P110-P113	A1-A4	
1	1	0	P34, P35	A13, A14	Pins 1-10 shorted; 11-12 open
			P36	Port mode	
			P100-P107	A5-A12	
			P110-P113	A1-A4	
1	1	1	P34-P36	A13-A15	Pins 1-12: all shorted
			P100-P107	A5-A12	
			P110-P113	A1-A4	

Pin	Description	Remark
JP1	3 ● ▢ 1 4 ● ▢ 2	Internal main clock setting
JP2	Oscillation circuit is set	32.768-kHz clock is supplied for subclock.
J1	2 ▢ ▢ ▢ ▢ ▢ ▢ 12 1 ▣ ▣ ▣ ▣ ▣ ▣ 11	Set to port mode (P34-P36, P100-P107, P110-P113)

[MEMO]

CHAPTER 4   CAUTIONS

4.1   V$_{DD}$ and BV$_{DD}$ of Target System

(1) BV$_{DD}$ in the target system is not connected to BV$_{DD}$ in the evaluation chip in the IE-703002-MC.
    The IE-703002-MC uses the BV$_{DD}$ of the target system for the following purposes:
    - Power ON/OFF detection of target system
    - BV$_{DD}$ emulation of target system
(2) When the voltage of the target system is 1 V or higher, the evaluation chip in the emulator is supplied V$_{DD}$ to operate by the target system. The power consumption is equivalent to that of the μPD70F3017.
(3) When the voltage of the target system is lower than 1 V, the emulator recognizes the target system power is off and operates at 3.3 V.

Figure 4-1. Schematic Diagram of Power Supply Acquisition
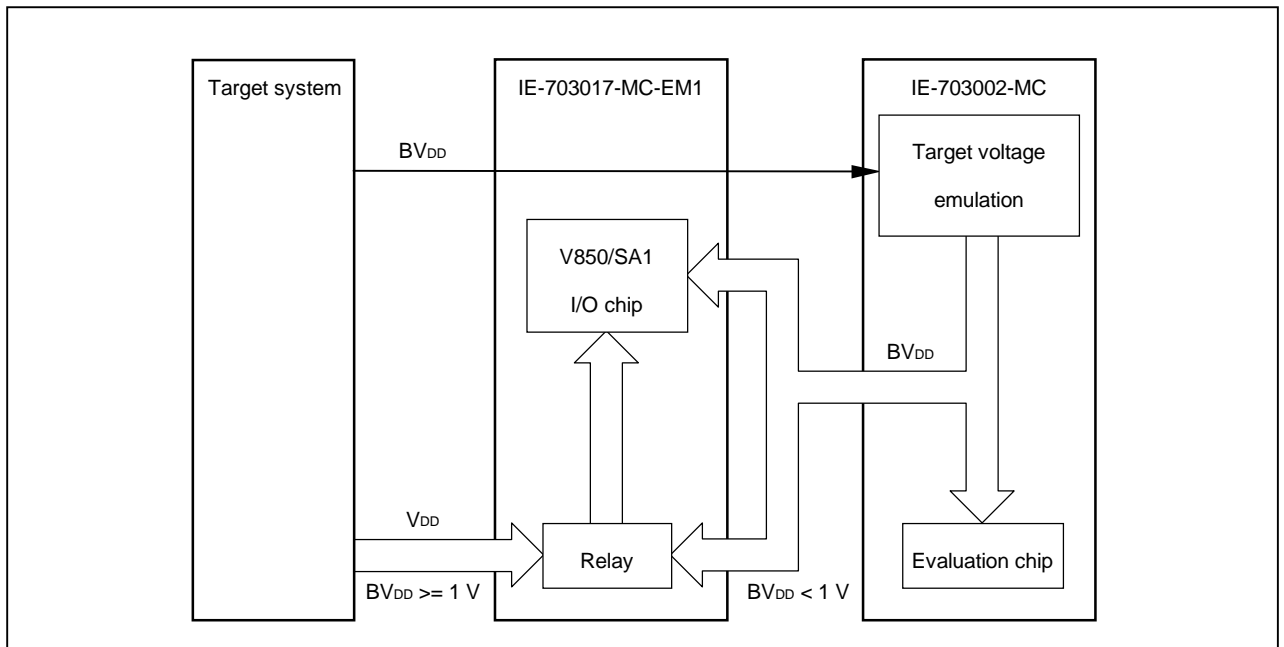
4.2 NMI Signal

The input signal (NMI signal) from the target system is delayed (t_{pD} = 10 ns (MAX.)) because it passes through FPGA before it is input to the I/O chip of the emulator.
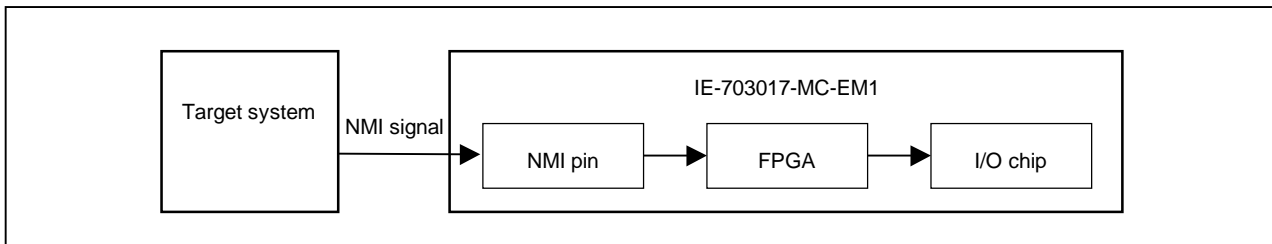
In addition, the DC characteristics change. The input voltage becomes V_{IH} = 2.0 V (MIN.) and V_{IL} = 0.8 V (MAX.). The input current becomes I_{IN} = ±1.0 μA (MAX.).

Figure 4-2. NMI Signal Flow Path

4.3 V~PP~ Signal

The V~PP~ signal from the target system is connected to LED via a 330-Ω resistor in the emulator. It is not connected to the evaluation chip in the emulator.

Figure 4-3. V~PP~ Signal Flow Path
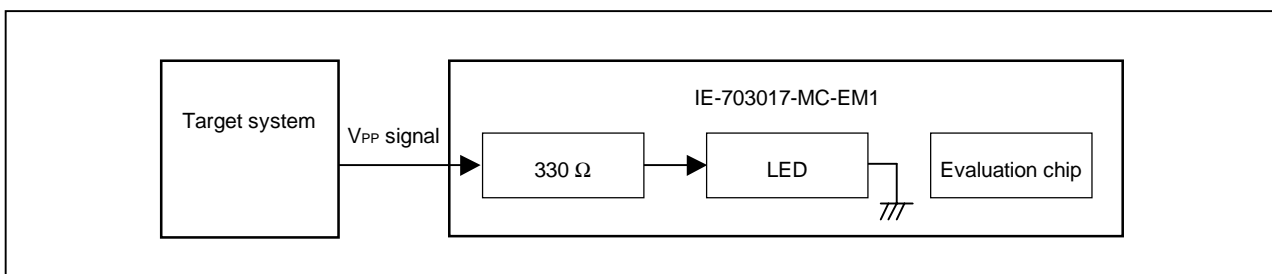
4.4 MAM Register

Debugging of MAM register cannot be performed in the emulator. If debugging MAM register with software, proceed with care.

In the target device, the port can be used as an address bus by setting a value to the MAM register (address: FFFFF068H) that is mapped in the internal peripheral I/O area with the software (Separate bus function). In the emulator, however, switching to the separate bus through MAM register setting by software is impossible.

To use the separate bus function, set the J1 jumper in advance. (refer to **2.5 Separate Bus Function Setting**)

4.5   NMI Signal Mask Function

When using the P00/NMI pin in the port mode, do not mask the NMI signal.

4.6   Bus Interface Pin

The operation of the pin for the bus interface differs between the emulator and the target device as follows.

Table 4-1. Bus Interface Pin Operation List (1/2)
(a) During break

Pin name	Internal memory								External memory			
	Memory used by emulator			Internal ROM	Internal RAM		Internal Peripheral I/O		Emulation RAM		Target System	
	F	R	W	R	R	W	R	W	R	W	R	W
A16-A21	Hold the accessed last								Active		Active	
AD0-AD15	Hi-Z								Active		Active	
ASTB	H								Active		Active	
R/$\overline{\text{W}}$	H								Active		Active	
$\overline{\text{DSTB}}$	H								H		Active	
$\overline{\text{LBEN}}$	H								Active		Active	
$\overline{\text{UBEN}}$	H								Active		Active	
$\overline{\text{WAIT}}$	Invalid								Maskable		Maskable	
$\overline{\text{HLDRQ}}$	Maskable								Maskable		Maskable	
$\overline{\text{HLDAK}}$	H or L								H or L		H or L	
$\overline{\text{WRL}}$	H								H		H	**Note**
$\overline{\text{WRH}}$	H								H		H	**Note**
$\overline{\text{RD}}$	H								H		**Note**	H

Note Active

Remarks 1. F : Fetch
R : Read
W : Write
2. H : High-level output
L : Low-level output
Hi-Z : High-impedance

**Table 4-1. Bus Interface Pin Operation List (2/2)**

(b) During Run

Pin name	Internal memory							External memory					
	Internal ROM		Internal RAM			Internal Peripheral I/O		Emulation RAM			Target System		
	F	R	F	R	W	R	W	F	R	W	F	R	W
A16-A21	Hold the accessed last							Active			Active		
AD0-AD15	Hi-Z							Active			Active		
ASTB	H							Active			Active		
R/$\overline{\text{W}}$	H							Active			Active		
$\overline{\text{DSTB}}$	H							H			Active		
$\overline{\text{LBEN}}$	H							Active			Active		
$\overline{\text{UBEN}}$	H							Active			Active		
$\overline{\text{WAIT}}$	Invalid							Maskable			Maskable		
$\overline{\text{HLDRQ}}$	Maskable							Maskable			Maskable		
$\overline{\text{HLDAK}}$	H or L							H or L			H or L		
$\overline{\text{WRL}}$	H							H			H		**Note**
$\overline{\text{WRH}}$	H							H			H		**Note**
$\overline{\text{RD}}$	H							H			**Note**		H

Note Active

Remarks 1. F : Fetch
R : Read
W : Write
2. H : High-level output
L : Low-level output
Hi-Z : High-impedance

APPENDIX   DIMENSIONS

IE-703002-MC + IE-703017-MC-EM1 (Unit: mm)

Top View

Pin 1 direction

Side View

IE-703002-MC

IE-703017-MC-EM1

Bottom View

Top View
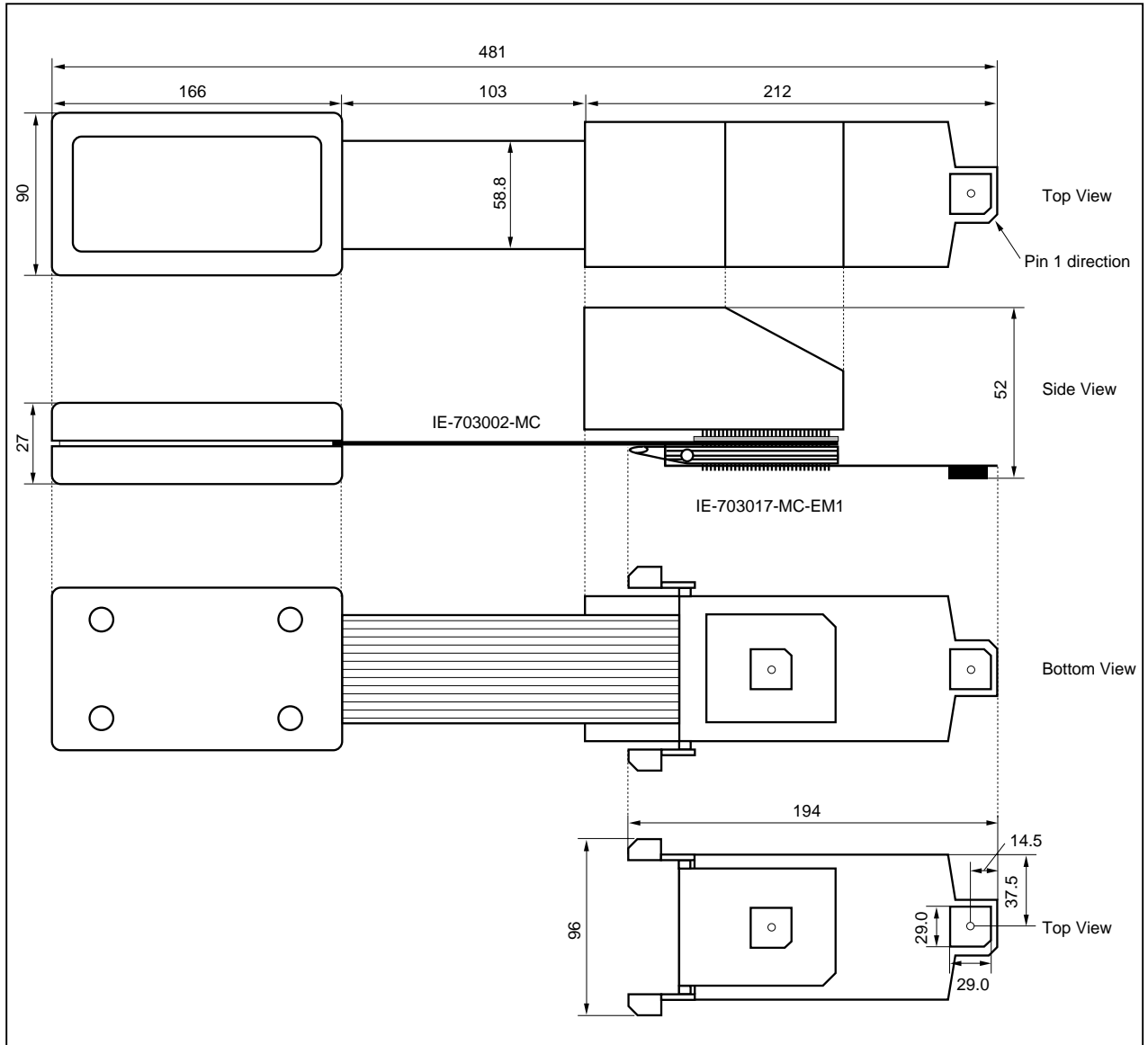
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