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ICL7605/ICL7606
Commutating Auto-Zero (CAZ) Instrumentation Amplifier

GENERAL DESCRIPTION

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace most of today's hybrid or monolithic instrumentation amplifiers, for low frequency applications from DC to 10Hz. This is made possible by the unique construction of this Harris device, which takes an entirely new design approach to low frequency amplifiers.

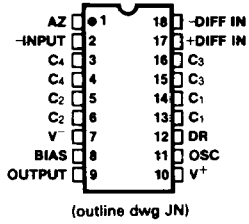
Unlike conventional amplifier designs, which employ three op-amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key features of the CAZ principle involve automatic compensation for long-term drift phenomena and temperature effects, and a flying capacitor input.

The ICL7605/ICL7606 consist of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section senses the differential input and applies it to the CAZ amp section. This section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

FEATURES

- **Exceptionally Low Input Offset Voltage — 2μV**
- **Low Long Term Input Offset Voltage Drift — 0.2μV/Year**
- **Low Input Offset Voltage Temperature Coefficient — 0.05μV/°C**
- **Wide Common Mode Input Voltage Range — 0.3V Above Supply Rail**
- **High Common Mode Rejection Ratio — 100 dB**
- **Operates at Supply Voltages As Low As ±2V**
- **Short Circuit Protection On Outputs for ±5V Operation**
- **Static-Protected Inputs — No Special Handling Required**
- **Compensated (ICL7605) or Uncompensated (ICL7606) Versions**



(outline dwg JN)

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Figure 1: Pin Configuration

ORDERING INFORMATION

Order parts by the following part numbers:

Part Number	Compensation	Temperature Range	Package
ICL7605CJN	INTERNAL	0°C to +70°C	18-PIN CERDIP
ICL7605IJN	INTERNAL	−25°C to +85°C	18-PIN CERDIP
ICL7605MJN	INTERNAL	−55°C to +125°C	18-PIN CERDIP
ICL7606CJN	EXTERNAL	0°C to +70°C	18-PIN CERDIP
ICL7606IJN	EXTERNAL	−25°C to +85°C	18-PIN CERDIP
ICL7606MJN	EXTERNAL	−55°C to +125°C	18-PIN CERDIP

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NOTE: All typical values have been characterized but are not tested.

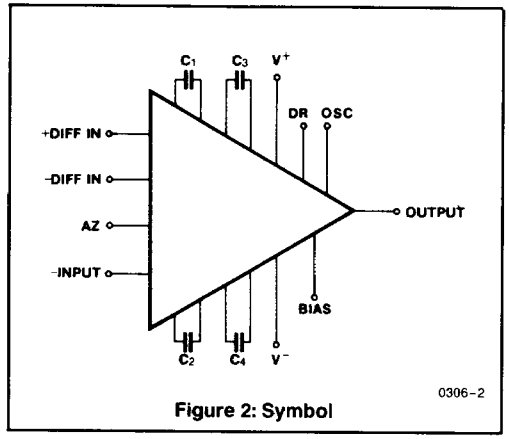


Figure 2: Symbol

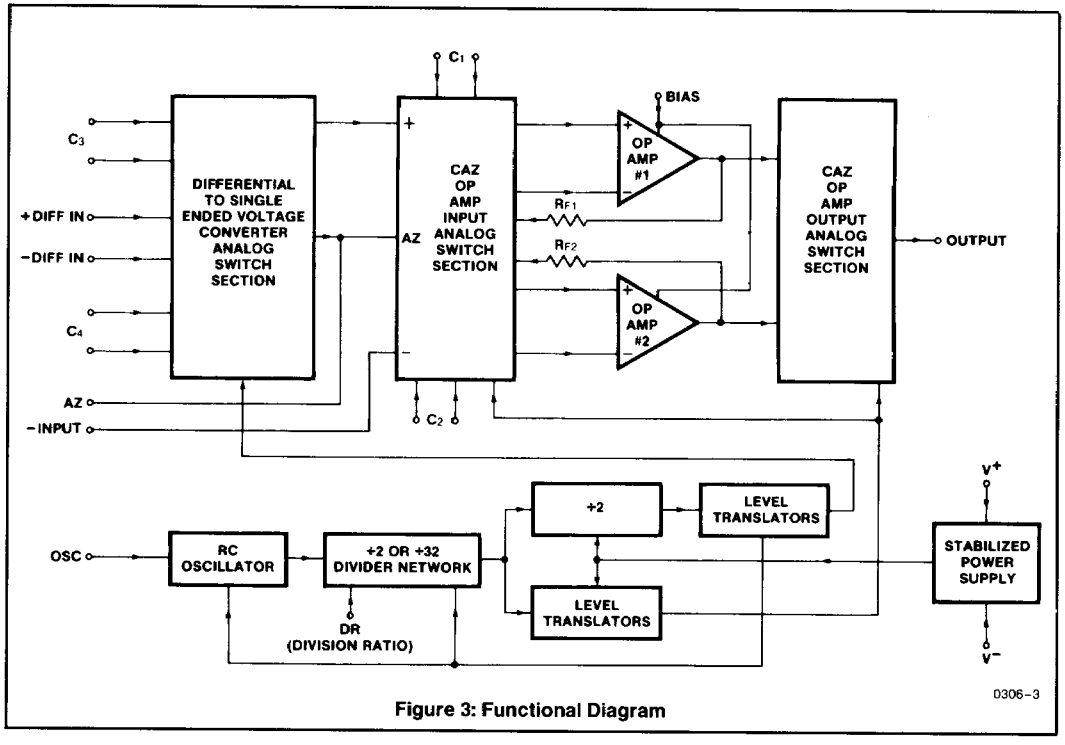


Figure 3: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
DR Input Voltage ..... ($V^+ - 8$) to ($V^+ + 0.3$)V
Input Voltage (C_1, C_2, C_3, C_4 + DIFF IN, − DIFF IN, − INPUT, BIAS, OSC), (Note 1) ..... ($V^- - 0.3$) to ($V^+ + 0.3$)V
Differential Input Voltage (+ DIFF IN to − DIFF IN) (Note 2) ..... ($V^- - 0.3$) to ($V^+ + 0.3$)V
Duration of Output Short Circuit (Note 3) ..... Unlimited
Continuous Total Power Dissipation (Note 4) 500mW
Operating Temperature Range:
ICL7605/ICL7606C ..... 0 to +70°C
ICL7605/ICL7606I ..... −25°C to +85°C
ICL7605/ICL7606M ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Note 1: Due to the SCR structure inherent in all CMOS devices, exceeding these limits may cause destructive latch up. For this reason, it is recommended that no inputs from sources operating on a separate power supply be applied to the 7605/6 before its own power supply is established, and that when using multiple supplies, the supply for the 7605/6 should be turned on first.

Note 2: No restrictions are placed on the differential input voltages on either the + DIFF IN or − DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 3: The outputs may be shorted to ground (GND) or to either supply (V^+ or V^-). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

Note 4: For operation above 25°C ambient temperature, derate 4mW/°C from 500mW above 25°C.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

Symbol	Parameter	Test Conditions		Value Min	Value Typ	Value Max	Units
V_{OS}	Input Offset Voltage	$R_S \leq 1k\Omega$	Low Bias Setting		±2		μV
			Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±30	μV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Temperature Coefficient (Note 5)	Low or Med Bias Settings	$-55°C > T_A > +25°C$		0.01	0.2	μV/°C
			$+25°C > T_A > +85°C$		0.01	0.2	μV/°C
			$+25°C > T_A > +125°C$		0.05	0.2	μV/°C
$\Delta V_{OS}/\Delta t$	Long Term Input Offset Voltage Stability	Low or Med Bias Settings			0.5		μV/Year
CMVR	Common Mode Input Range			−5.3		+5.3	V
CMRR	Common Mode Rejection Ratio	$C_{OSC} = 0$, DR connected to V^+, $C_3 = C_4 = 1\mu F$			94		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 1\mu F$			100		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 10\mu F$			104		dB
PSRR	Power Supply Rejection Ratio				110		dB
$-I_{BIAS}$	−INPUT Bias Current	Any bias setting, $f_c = 160Hz$ (Includes charge injection currents)			0.15	1.5	nA
$\bar{e}_n(p\text{-}p)$	Equivalent Input Noise Voltage peak-to-peak	Band Width 0.1 to 10Hz	Low Bias Mode		4.0		μV
			Med Bias Mode		4.0		μV
			High Bias Mode		5.0		μV

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified. (Continued)

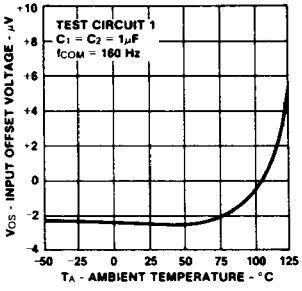
Symbol	Parameter	Test Conditions		Value			Units
				Min	Typ	Max	
$\bar{e}_n$	Equivalent Input Noise voltage	Band Width 0.1 to 1.0Hz	All Bias Modes		1.7		μV
A_{VOL}	Open Loop Voltage Gain	$R_L = 100k\Omega$	Low Bias Setting	90	105		dB
			Med Bias Setting	90	105		dB
			High Bias Setting	80	100		dB
$\pm V_O$	Maximum Output Voltage Swing	$R_L = 1M\Omega$			± 4.9		V
		$R_L = 100k\Omega$			± 4.8		V
		$R_L = 10k\Omega$	Positive Swing	+4.4			V
			Negative Swing			−4.5	V
GBW	Bandwidth of Input Voltage Translator	$C_3 = C_4 = 1\mu F$	All Bias Modes		10		Hz
f_{COM}	Nominal Commutation Frequency	$C_{OSC} = 0$	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
f_{COM1}	Nominal Input Converter Commutation Frequency	$C_{OSC} = 0$	DR Connected to V^+		80		Hz
			DR Connected to GND		1280		Hz
V_{BH}	Bias Voltage required to set Quiescent Current	Low Bias Setting		$V^+ - 0.3$	V^+	$V^+ + 0.3$	V
V_{BM}		Med Bias Setting		$V^- + 1.4$	GND	$V^+ - 1.4$	V
V_{BL}		High Bias Setting		$V^- - 0.3$	V^-	$V^- + 0.3$	V
I_{BIAS}	Bias (Pin 8) Input Current				± 30		pA
I_{DR}	Division Ratio Input Current	$V^+ - 8.0 \leq V_{DR} \leq V^+ + 0.3$ volt			± 30		pA
V_{DRH}	DR Voltage required to set Oscillator division ratio	Internal oscillator division ratio 32		$V^+ - 0.3$		$V^+ + 0.3$	V
V_{DRL}		Internal oscillator division ratio 2		$V^+ - 8$		$V^+ - 1.4$	V
R_{AS}	Effective Impedance of Voltage Translator Analog Switches				30		kΩ
I_{SUPP}	Supply Current	High Bias Setting			7	15	mA
		Med Bias Setting			1.7	5	mA
		Low Bias Setting			0.6	1.5	mA
$V^+ - V^-$	Operating Supply Voltage Range	High Bias Setting		5		10	V
		Med or Low Bias Setting		4		10	V

Note 5: For Design only, not tested.

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



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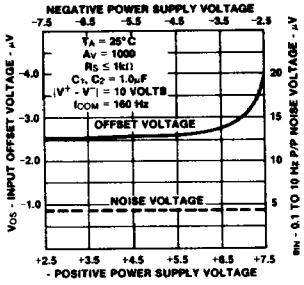
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



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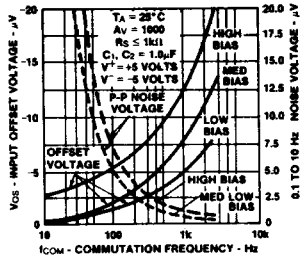
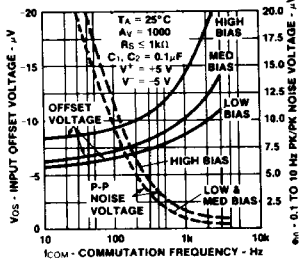
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1µF)



0306-6

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1 µF)



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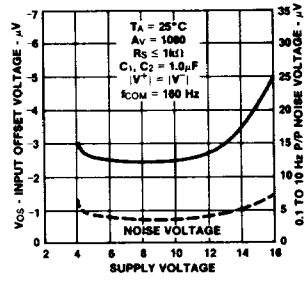
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)



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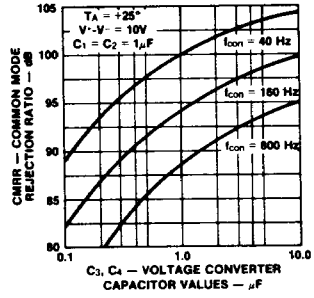
COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS



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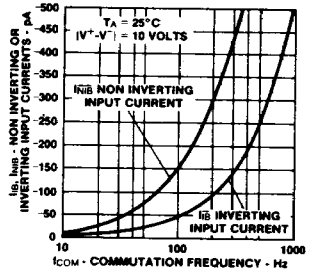
NOTE: All typical values have been characterized but are not tested.

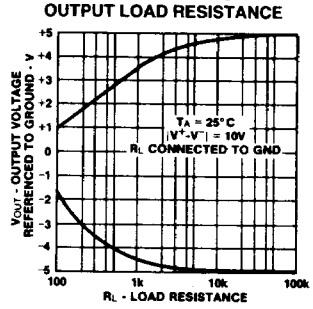
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



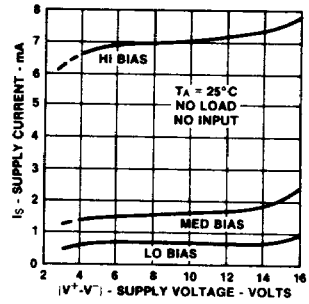
0306-10

MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



0306-11

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



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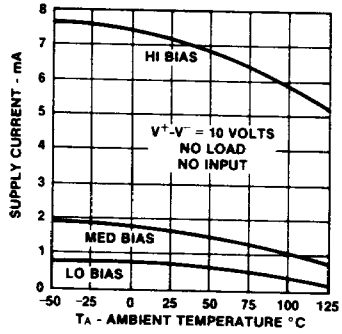
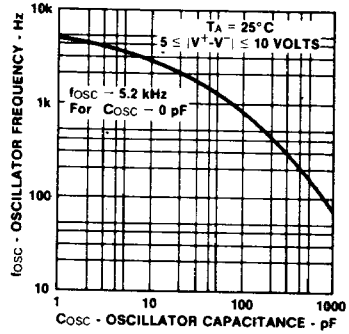
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



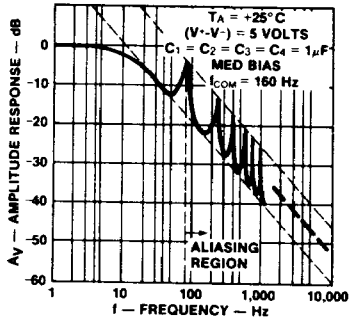
0306-13

OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



0306-14

AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER



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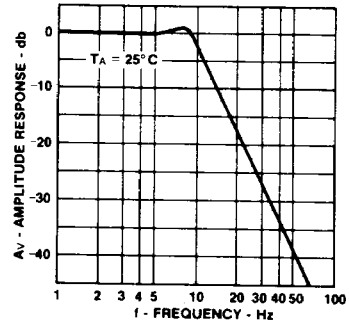
FREQUENCY RESPONSE OF THE 10Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).



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NOTE: All typical values have been characterized but are not tested.

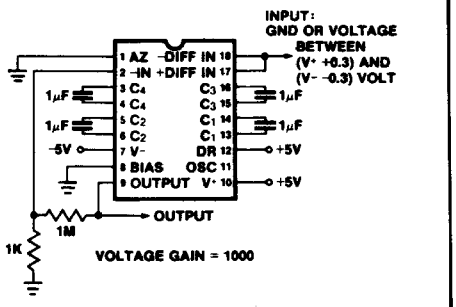


Figure 4: Test Circuit 1

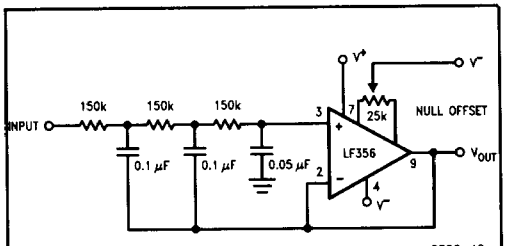


Figure 5: Test Circuit 2
DC to 10Hz Unity Gain Low Pass Filter

DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op-amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation of internal error voltages, whether they are derived from steady-state conditions, such as temperature and supply voltage fluctuations, or are due to long term drift.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 6.

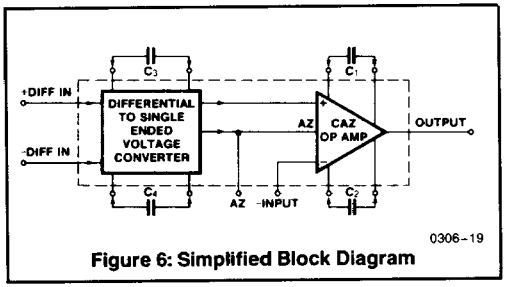


Figure 6: Simplified Block Diagram

The ICL7605/ICL7606 have approximately constant equivalent input noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20Hz maximum). However in many applications bandwidth is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ op-amp section of the ICL7605/ICL7606 is best illustrated by referring to Figure 7. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level at which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected in a unity gain mode through on-chip analog switches. It charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier plus the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, charging a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}), so that at all times one or the other of the on-chip op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

NOTE: All typical values have been charactenzed but are not tested.

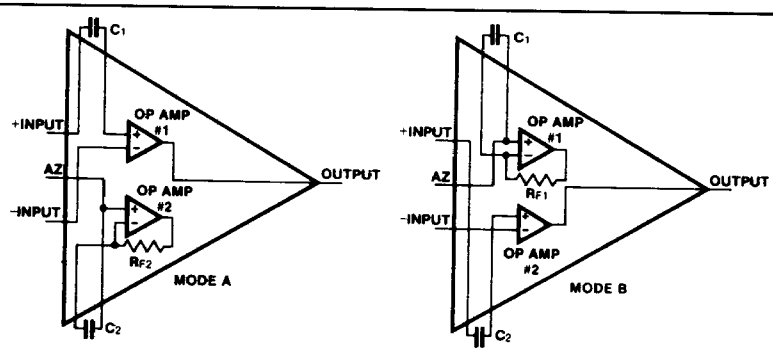


Figure 7: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

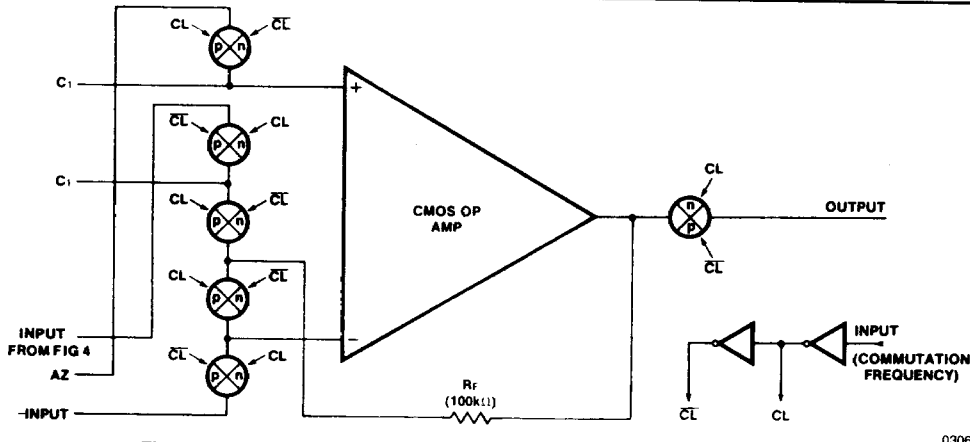


Figure 8: Schematic of analog switches connecting each internal OP AMP to its inputs and output.

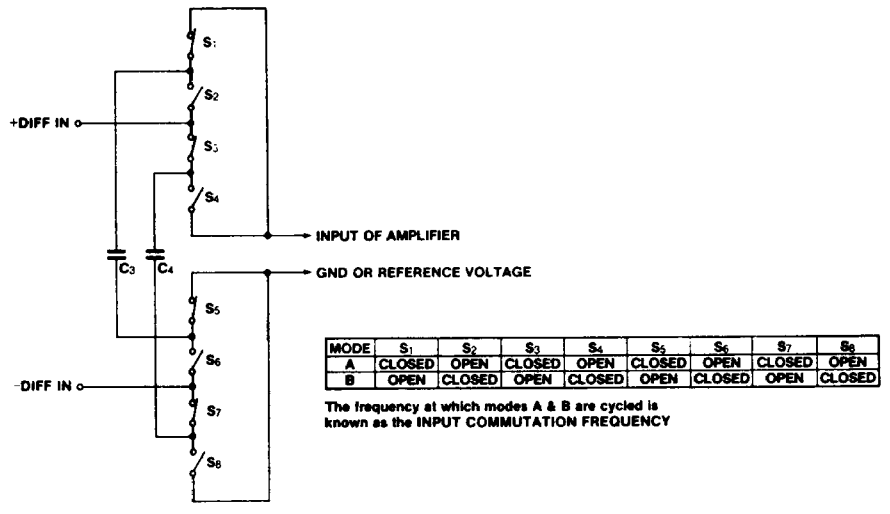
Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. The CMOS structure provides the CAZ op-amp with open-loop gains of greater than 100dB, typical input offset voltages of ±5mV, and ultra-low leakage currents, typically 1pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 8. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

NOTE: All typical values have been characterized but are not tested.



MODE	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
A	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
B	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED

The frequency at which modes A & B are cycled is known as the INPUT COMMUTATION FREQUENCY

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Figure 9: Schematic of the differential to single ended voltage converter

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of the voltage converter block is shown in Figure 9. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input, and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 10, where the voltage steps equal the differential voltage (V_A-V_B) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, including commutation and noise voltages. Sampling theory states that to preserve the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency being sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is translated to a lower frequency. This phenomenon is known as aliasing. Although the output responds to inputs above the commutation frequency, the frequencies of the output responses will be below the commutation frequency.

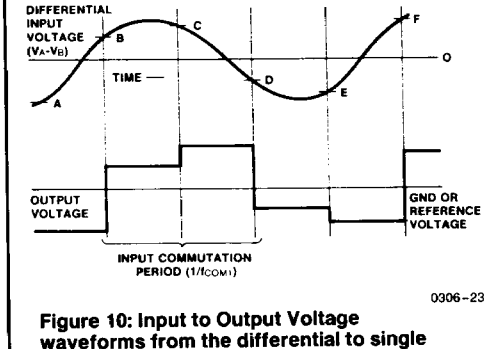

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Figure 10: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph.

3 OPERATIONAL AMPLIFIERS

NOTE: All typical values have been characterized but are not tested.

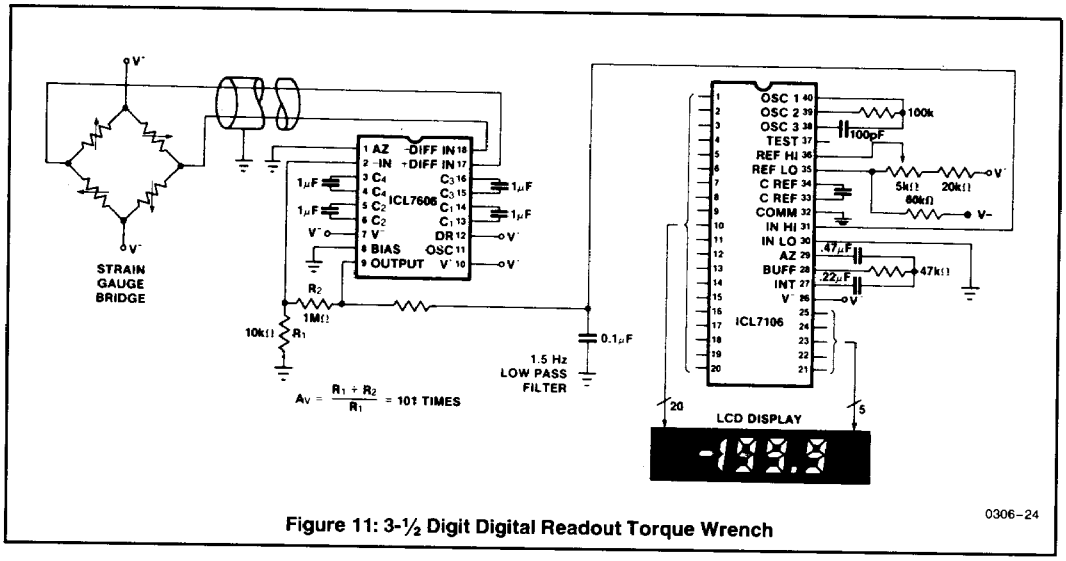

Figure 11: 3-½ Digit Digital Readout Torque Wrench

The voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have a finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C_3 and C_4 must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is down approximately 3dB at 10Hz.

APPLICATIONS

Using the ICL7605/ICL7606 to Build a Digital Readout Torque Wrench

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ instrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting it to a single-ended voltage referenced to ground. The signal is then amplified by the CAZ instrumentation amplifier and applied to the input of a 3-½ digit dual-slope A/D converter which drives the LCD panel meter display. The A/D converter device used in this instance is the Harris ICL7106.

In the digital readout torque wrench circuit, the reference voltage for the ICL7106 is derived from the stimulus applied to the strain gauge, to utilize the ratiometric capabilities of the A/D. In order to set the full-scale reading, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp must be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale, the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2mA. The accuracy is limited only by resistor ratios and the transducer.

SOME HELPFUL HINTS

Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

Figure 4 and 5 (Test Circuits) provide a convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be a high-input impedance RC type — not simply a capacitor across the feedback resistor R_2. Resistor and capacitor values of about 100kΩ and 1.0μF are necessary so that the output load impedance on the CAZ op-amp is greater than 100kΩ.

NOTE: All typical values have been characterized but are not tested.

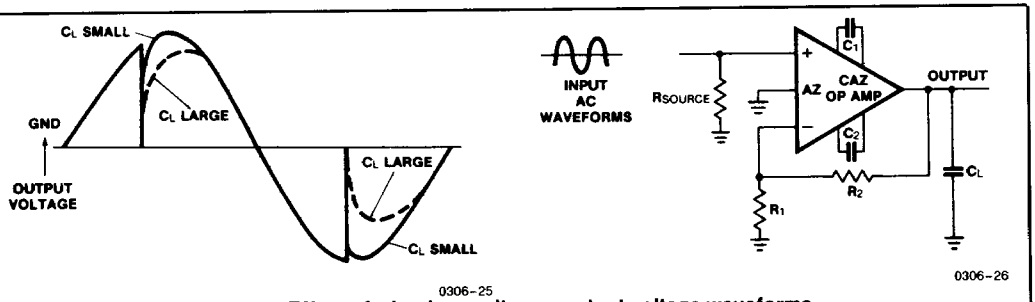

Figure 12: Effect of a load capacitor on output voltage waveforms.

Bias Control

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606. For this reason, the internal op amps have externally programmable bias levels. These levels are set by connecting the BIAS terminal to either V^+, GND, or V^-, for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of quiescent supply current versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the better the recovery from commutation spikes), and offset errors due to "IR" voltage drops and thermoelectric effects (the higher the power dissipation, the higher the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output load of 100kΩ or more is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked. This is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 12. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1MΩ resistor and a 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V^+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 13) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V^+ supply is $+5V$ ($\pm 10\%$) and the logic driver also operates from a similar voltage supply. The reason for this requirement is that the logic section (including the oscillator) operates from an internal $-5V$ supply, referenced to V^+ supply, which is not accessible externally.

NOTE: All typical values have been characterized but are not tested.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects in electrical junctions consisting of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

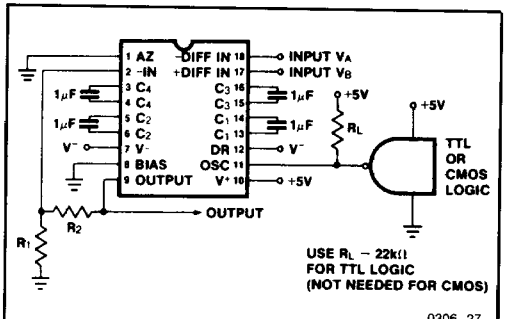

Figure 13: ICL7605 being clocked from external logic into the oscillator terminal.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep the ICL7605/ICL7606 away from equipment which dissipates heat.

Component Selection

The four capacitors (C_1 thru C_4) should each be about 1.0μF. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them change significantly, problems of dielectric absorption, charge bleed-off and the like are as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene types are the best for C_3 and C_4, although Mylar may be adequate for C_1 and C_2.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors are not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op-amps are typically in the 10pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least 10,000×10pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0pA at an ambient temperature of 25°C.

The output waveform in Figure 4 (with no input signal) is shown in Figure 14. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7mV are amplified by a factor of less than 1000.

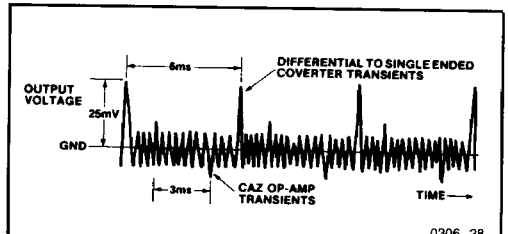

Figure 14: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board particularly the capacitors C_1, C_2, C_3 and C_4, which must all be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

NOTE: All typical values have been characterized but are not tested.