General Purpose Low Pass Filter

GENERAL DESCRIPTION

Each of these devices in the series is a fourth order switched capacitor low pass filter providing 24dB/octave (Butterworth) of roll off outside of the pass band, Within this series, Butterworth, Bessel or Chebyshev (0.5 or 0.1dB of ripple) filter responses can be obtained. Also, each filter response is available in either a 50:1 or 100:1 clock-to-corner ratio device for added flexibility. All devices have the same pin out (8 pin dual-in-line), so one can easily be substituted for the other, depending on the application.

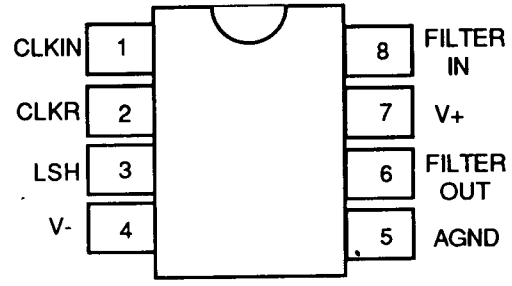
Switched capacitor filters provide the ability to tune the corner frequency of the filter response with the adjustment of the input clock. The XR-1001/1008 can also be used in a stand alone mode, where an external resistor and capacitor will set the input clock frequency. For additional precision, a external crystal can be used to set the corner frequency.

The XR-1001 is pin-for-pin compatible with the MF-4-100 and the XR-1002 in pin-for-pin compatible with the MF- 4-50. The XR-1001/1008 are fabricated in 3 micron dual-polysilicon gate single metal CMOS for additional performance over other processes.

FEATURES

Single 5 Volt Operation
Low Power Consumption
Precise Filter Positioning
Stand Alone Mode with RC or Crystal
Low Noise — Typically –78dBm
Corner Frequency Adjustable to 40kHz

PIN ASSIGNMENT



APPLICATIONS

Mechanical Processes
Telecommunications
Instrumentation
Anti-alias Filters
Reconstruction Filters
Digital Signal Processing
Musical Effects

ABSOLUTE MAXIMUM RATINGS

Power Supply (Single Supply)	14V
Input Signal Level	V^+ –0.7 to V^- +0.7V
Power Dissipation (Package Limitation)	
Ceramic Package	385mW
Derate Above T_A = 25°C	5mW/°C
Plastic Package	300mW
Derate Above T_A = 25°C	6mW/°C
Storage Temperature Range	–65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Response/Ripple	f_{clock}/f_{corner}	Operating Temperature
XR-1001CP/CN/D	Plastic/Ceramic/SO	Butterworth	100:1	0°C to 70°C
XR-1002CP/CN/D	Plastic/Ceramic/SO	Butterworth	50:1	0°C to 70°C
XR-1003CP/CN/D	Plastic/Ceramic/SO	Bessel	100:1	0°C to 70°C
XR-1004CP/CN/D	Plaslic/Ceramic/SO	Bessel	50:1	0°C to 70°C
XR-1005CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.1dB)	100:1	0°C to 70°C
XR-1006CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.1dB)	50:1	0°C to 70°C
XR-1007CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.5dB)	100:1	0°C to 70°C
XR-1008CP/CN/D	Plastic/Ceramic/SO	Chebyshev (0.5dB)	50:1	0°C to 70°C

SYSTEM DESCRIPTION

The XR-1001 and XR-1002 with their Butterworth filter responses are suitable for applications where the pass band must be maximally flat, such as instrumentation. The XR-1003 and XR-1004 with Bessel filter response have a maximally flat group delay response. This is ideal for telecommunication and modem applications where phase distortion would affect the performance. The XR-1005 through XR-1008 provide Chebyshev filter response. With Chebyshev filter response, the roll-off outside of the pass band is steeper and attenuates out-of-band signals greater than the Bessel or Butterworth responses. The ripple in the band is larger to obtain the steeper roll-off. The application will determine the amount of ripple which can be accepted within the pass band of the filter response.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 5$ VDC, $V^- = -5$ VDC, $f_{CLOCK} = 1$MHz, $R_{Load} = 1M\Omega$, $C_{Load} = 40$pF, $T_A = 25°C$, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
GENERAL CHARACTERISTICS						
V_{DD}	Supply Voltage					
	Single Supply	4.5		11.0	VDC	Referenced to V_{SS}(Pin 4)
	Split supply	+2.25		5.5	VDC	Refrenced to AGND (PIn 6)
V_{SS}	Supply Voltage					
	Split supply	−5.5		−2.25	VDC	Referenced to AGND (Pin 6)
I_{DD}	Supply Current					
	Single Supply		2.5	3.5	mA	$V_{DD} = 10.0$ VDC
	Split supply		2.5	3.5	mA	$V_{DD} = 5$ VDC
	Split Supply		1.50	2.25	mA	$V_{DD} = 2.25$ VDC
I_{SS}	Supply Current					
	Split supply	−3.5	−2.5		mA	$V_{DD} = 5.0$ VDC, $V_{SS} = -5.0$ VDC
	Split Supply	−2.25	−1.5		mA	$V_{DD} = +2.25$ VDC, $V_{SS} = -2.25$
FILTER CHARACTERISTICS						
$f_{CLOCKMAX}$	Upper Clocking Freq. Limit	1.0	1.5		MHz	
$f_{CLOCKMIN}$	Lowest Practical Clock		100		Hz	For 1001,1003,1005,1007
			50		Hz	For 1002,1004,1006,1008
	Gain at Corner Frequency	−3.5	−3	−2.5	dB	
A_2f_{corner}	Attenuation at 2 Times	23	24.6	26	dB	For 1001,1002
	The Corner Frequency	11	13	14	dB	For 1003,1004
		30	31	33	dB	For 1005,1006
		33	34	36	dB	For 1007,1008
V_{OUT}	Maximum Output Signal	8			Vpp	Input = ±4.2 VDC
$e_{n\ out}$	Output Noise		0.5		mVrms	From 1Hz to 25kHz
S/N	Signal-to-Noise Ratio		84		dB	
THD	Total Harmonic Distortion		0.1		%	$V_{IN} = 2.4$Vrms, $f_{IN} = 1$kHz
V_{OS}	Output Offset Voltage (DC)	−0.4		+0.4	VDC	$f_{clock} = 1$MHz
	Clock Feedthrough		50		mVpp	
I_{OSS}	Output Short Circuit Current					
	Source	−60	−50		mA	See Note *1
	Sink		30	50	mA	
	Temperature Coefficient of f_{corner}		±35		ppm/°C	From −40°C to +85°C not lested in production
	Passband Gain					
	For 1001,1002	−0.3	0	+0.3	dB	Tested at 3 and 5kHz for
	For 1003,1004	−1.0	−0.1	+0.2	dB	1001,1003,1005,1007
	For 1005,1006	−0.4	−0.1	+0.3	dB	Tested at 6 and 10 kHz for
	For 1007,1008	−0.7	−0.2	+0.3	dB	1002,1004,1006,1008

Note 1: Caution should be used so that the power dissipation does not exceed the package limitation.

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ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: $V^+ = 5$ VDC, $V^- = -5$ VDC, $f_{CLOCK} = 1$MHz, $R_{Load} = 1M\Omega$, $C_{Load} = 40$pF, $T_A = 25°C$, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
FILTER CHARACTERISTICS (Continued)						
	Passband Gain					
	For 1001,1002	–0.7	–0.06	–0.0	dB	Tested at 7.5kHz for
	For 1003,1004	–2.0	–1.5	–1.0	dB	1001,1003,1005,1007
	For 1005,1006	–0.3	–0.1	+0.3	dB	Tested at 15kHz for
	For 1007,1008	–0.7	–0.2	+0.3	dB	1002,1004,1006,1008
FILTER CHARACTERISTICS: $V^+ = +2.25$, $V^- = -2.25$ VDC						
$f_{CLOCKMAX}$	Upper Clocking Freq. Limit	0.25	0.5		MHz	
$f_{CLOCKMIN}$	Lower Practical Clock		100		Hz	For 1001,1003,1005,1007
			50		Hz	For 1002,1004,1006,1008
A_2f_{comer}	Attenuation at 2 Times	23	24.6	26	dB	For 1001,1002
	The Corner Frequency	11	13	14	dB	For 1003,1004
		30	31	33	dB	For 1005,1006
		33	34	36	dB	For 1007,1008
	Maximum Output Signal	3	4		Vpp	$V_{IN} = \pm 2.0$ VDC
S/N	Signal-to-Noise Ratio		76		dB	
V_{OS}	DC Offset voltage	–0.4	±0.05	+0.4	VDC	
LOGIC INPUT & LOGIC OUTPUT TESTS: $V = \pm 2.25$ VDC and $V = \pm 5$ VDC, Pin 3 tied to V_{SS}						
	Schmitt Trigger Input					
V_{T+}	Positive Going Threshold Voltage	0.6	1.3	2.0	V	V = ±5.0 VDC
		0.0	0.55	+1.1	V	V = ±2.25 VDC
V_{T-}	Negative Going Threshold Voltage	–1.4	–0.7	0.0	V	V = ±5.0 VDC
		–0.6	–0.2	+0.4	V	V = ±2.25 VDC
$V_{T+} - V_{T-}$	Hysteresis	0.8	2.1	2.9	V	V = ±5.0 VDC
		0.2	0.75	1.3	V	V = ±2.25 VDC
V_{OH}	Output High Voltage	4.5			V	V = ±5.0 VDC
		2.03			V	V = ±2.25 VDC, $I_O = 400\mu A$
V_{OL}	Output Low Voltage			1	V	V = ±5.0 VDC
				0.5	V	V = ±2.25 VDC, $I_O = -400\mu A$
I_{OS}	Output Sink Current		-5.0	-2.5	mA	V = ±5.0 VDC
			-1.3	-0.65	mA	V = ±2.25 VDC
	Output Source Current	3.0	6.0		mA	V = ±5.0 VDC
		0.75	1.5		mA	V = ±2.25 VDC
TTL CLOCK INPUT: V = ±5.0 VDC, Pin 3 tied to 0 VDC						
V_{IL}	Input Low Voltage		0.8		V	
V_{IH}	Input High Voltage		2.8		V	
STAND ALONE OPERATION: R = 5.0kΩ and C = 120pF for f_O = 985kHz						
f_O	Frequency Accuracy of Oscillator	–15	±4	+15	%	Measured at Pin 2 Error increases at lower f_O (< 500kHz). See Figure 3.

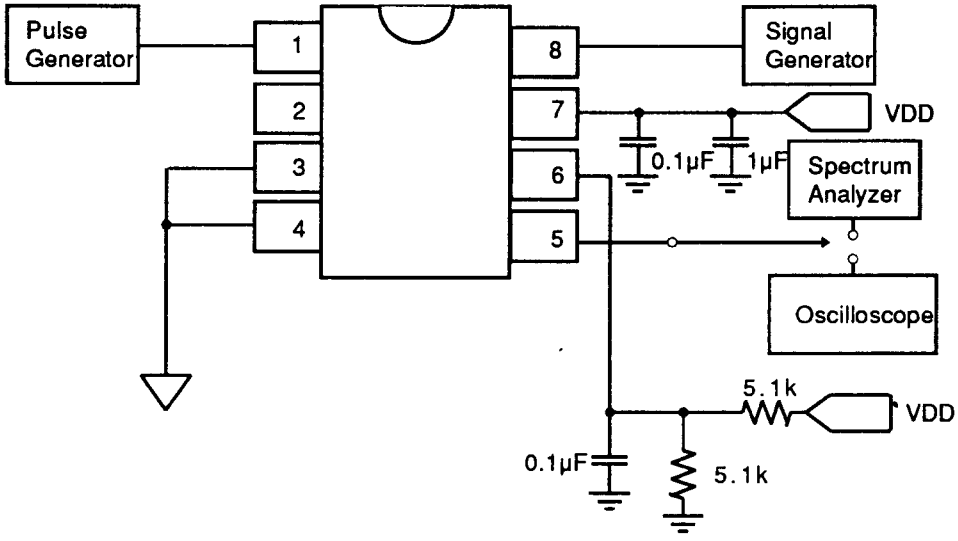


Figure 1. Single Supply Test Circuit

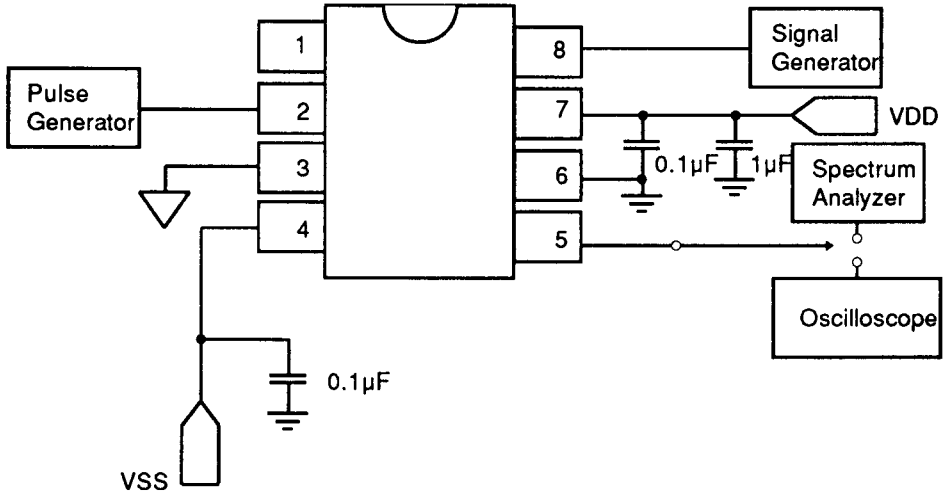


Figure 2. Split Supply Test Circuit

XR-1001/1008 PIN DESCRIPTIONS

Pin#	Symbol	Description
1	CLKIN	*Clock Input:* This input pin is for application of the MOS-level clock used for sampling and switching. For best results, this clock should be approximately 50% duty cycle. A crystal can be used from Pin 1 to Pin 2 to create a self-contained oscillator. A 10MΩ resistor should be hooked up in parallel with the crystal The maximum clock frequency is > 1MHz. For stand alone operation with a resistor and capacitor, the capacitor should be tied from this point to ground.
2	CLKR	*Clock Resistor:* This is an inverted output of signal found on Pin 1. It is used for creating a crystal oscillator or for an RC network. The resistor would be tied back to Pin 1. The frequency of osciillation would be equal to 1/(1.7 x RC). It is also used as the TTL-level clock input. Figure 4 shows the connections for RC mode.
3	LSH	*Level Shift:* This input is used to set the logic zero point of the clock input. For MOS level clocks, it should be tied to V_{SS}. For TTL-level clock. it should be grounded (split supply). For single supply operation, MOS level clock operation is recommended. When a crystal and resistor or a resistor and capacitor are used to create an oscillator, the level shift pin should be tied to V_{SS}.
4	V-	*V_{SS}:* This is the negative supply. It should have substantial decoupling to prevent noise on the output of the filter. A minimum 0.1µF capacitor to ground as close to the device as possible is strongly recommended. The range of operation for dual supplies is from –2.5 VDC to –5 VDC. This device can also be operated from ground positive. In this case, the V_{SS} pin is tied to the analog ground of the circuit. The quality of the ground in this mode of operation is very important. It should have very low series inductance.
5	FILTEROUT	*Filter Ouput:* This is the output of the low pass filter. A 10kΩ load or larger is the smallest load recommended for the output.
6	AGND	*Analog Ground:* This should be tied to the analog ground of the circuit in which the device is being used. The filter output of this device will swing around this potential. For single supply operation, this pin is externally biased at a point one half of the VDD voltage. A 0.1µF capacitor is the minimum capacitance needed for decoupling with single supply operation.
7	V+	*V_{DD}:* The positive supply is tied here. Since this pin is also common with the substrate, a 0.1µF and 1µF capacitor to ground are recommended to decouple any noise on the positive supply. The range of operation is from +5 to +10 VDC for single supply operation. For dual supply operation, +2.5 to +5 VDC can be applied to this pin.
8	FILTERIN	This is the input of the low pass filter. The input signal should be biased to mid-supply before applying to this pin. Also, to prevent alias frequencies from being created, the input frequency should be less than 1/2 of the clock frequency.

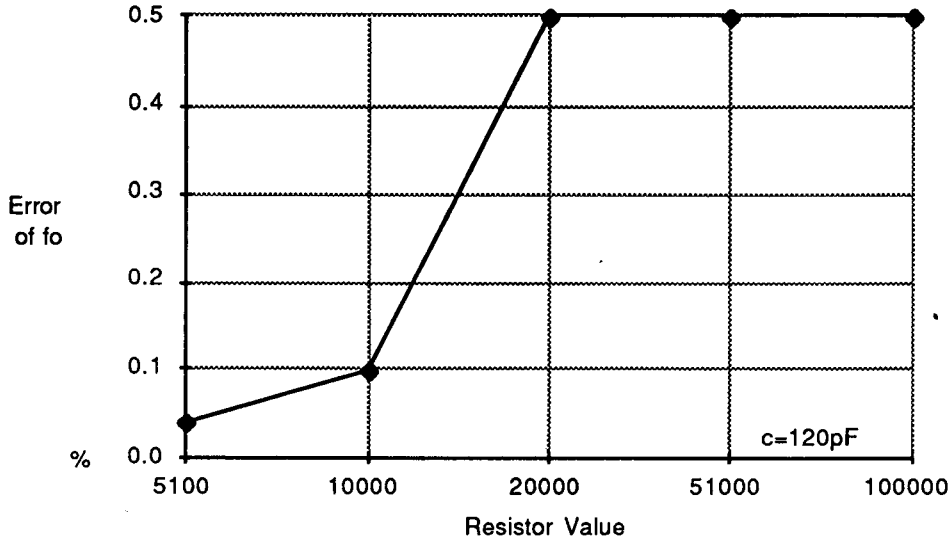


Figure 3. Error vs Timing Resistor

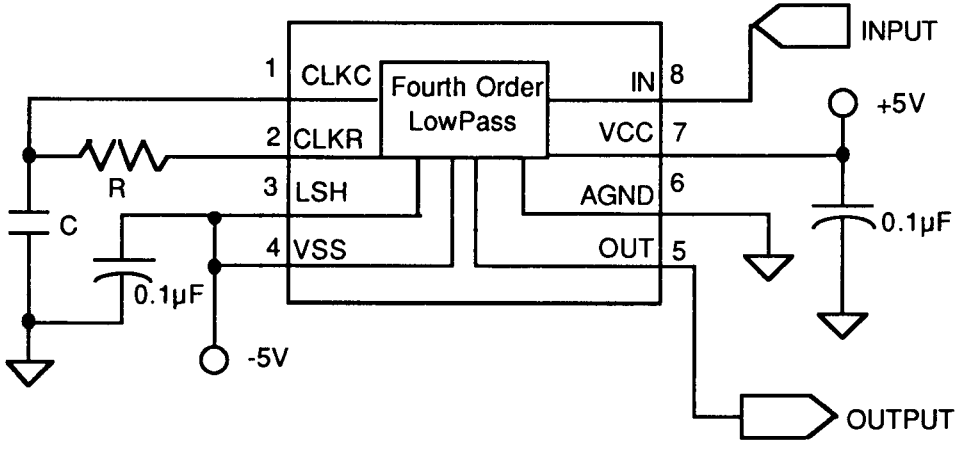
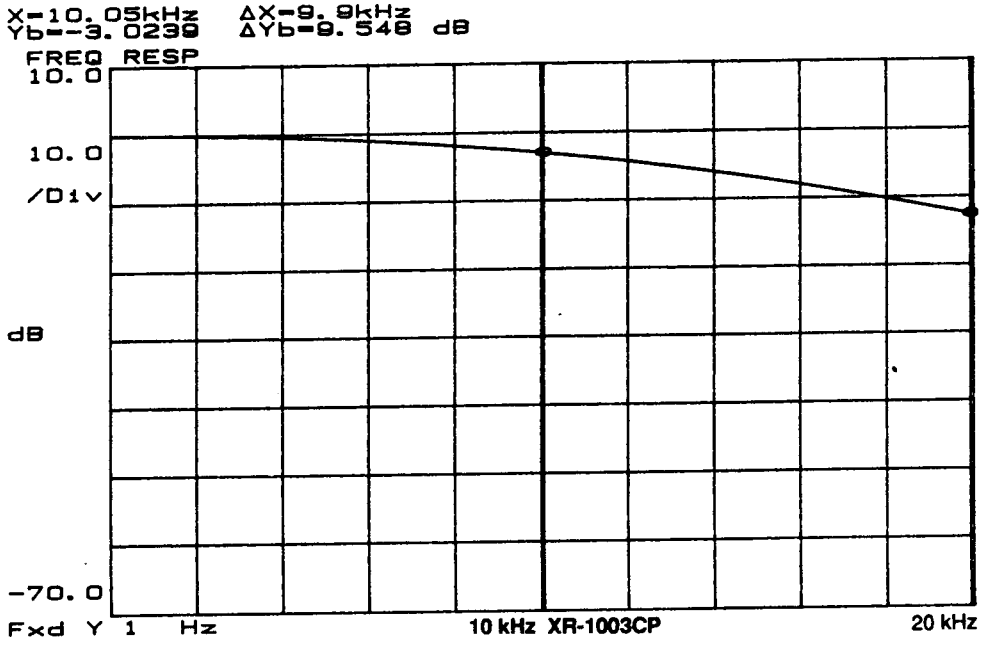
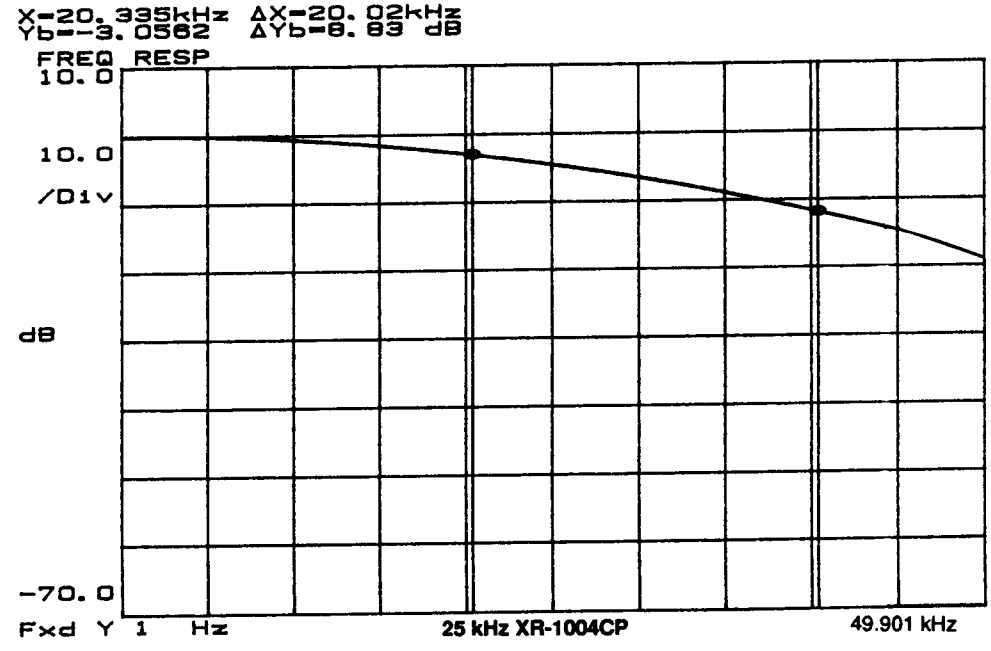
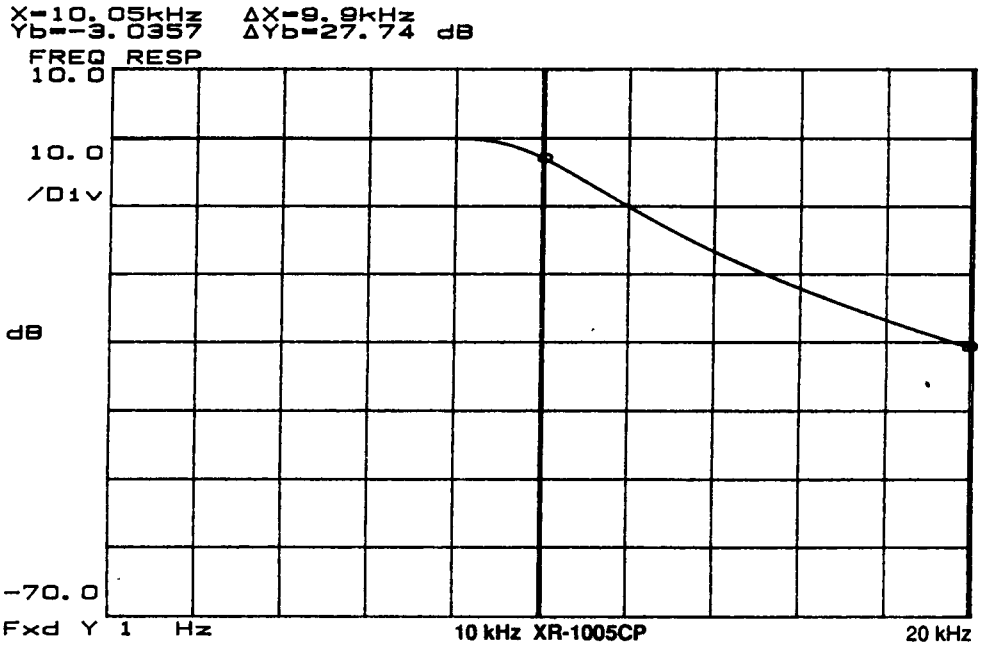
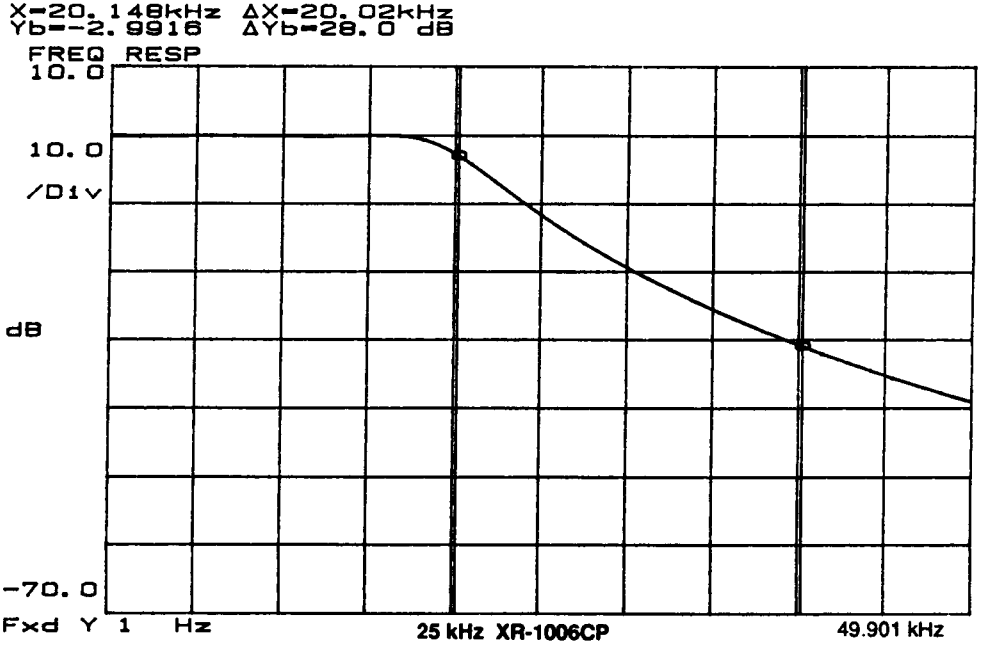


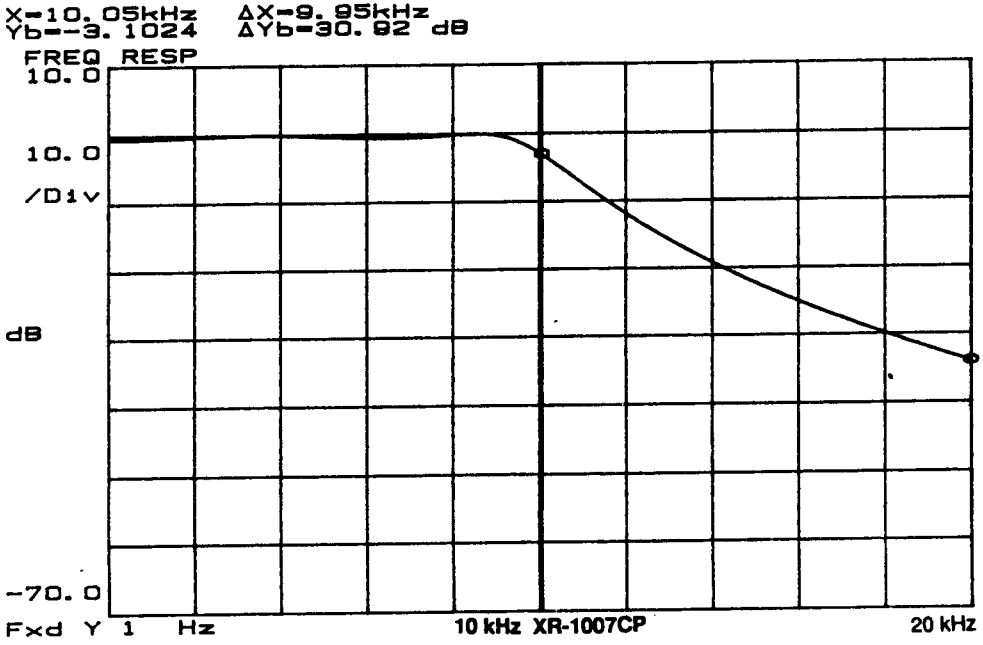
Figure 4. Operation of XR-1001/8 In RC Mode

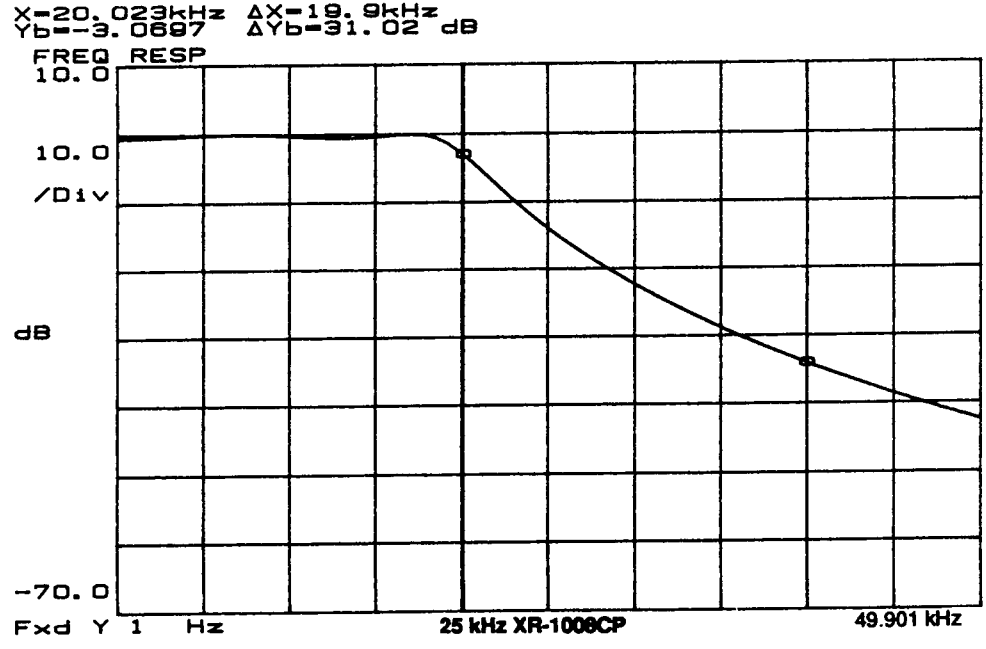

X=10.05kHz ΔX=9.9kHz
Yb=-3.0239 ΔYb=9.548 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1003CP
20 kHz


X=20.335kHz ΔX=20.02kHz
Yb=-3.0562 ΔYb=8.83 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1004CP
49.901 kHz


X=10.05kHz ΔX=9.9kHz
Yb=-3.0357 ΔYb=27.74 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1005CP
20 kHz


X=20.148kHz ΔX=20.02kHz
Yb=-2.9916 ΔYb=28.0 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1006CP
49.901 kHz


X=10.05kHz ΔX=9.95kHz
Yb=-3.1024 ΔYb=30.92 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
10 kHz XR-1007CP
20 kHz


X=20.023kHz ΔX=19.9kHz
Yb=-3.0697 ΔYb=31.02 dB
FREQ RESP
10.0
10.0
/Div
dB
-70.0
Fxd Y 1 Hz
25 kHz XR-1008CP
49.901 kHz