BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1361C

ELECTRONIC CHANNEL SELECTOR

DESCRIPTION

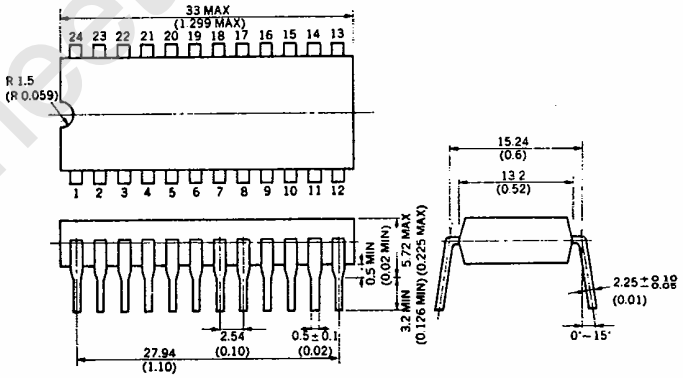
The μPC1361C is an electronic channel selector integrated circuit with 4 bit output. It is capable of selecting up to 12 channels. The output terminals are design to permit the direct driving of LED or neon lamps.

This IC consists of Clock Oscillator circuit, Channel Up and Down circuit, Channel skip circuit, 4 bit Up and Down Counter circuit, 1-12 Decoder circuit, 4 bit Output Buffer circuit and 12 channel Output Buffer circuit, all of which are contained in a 24 pins dual in-line package.

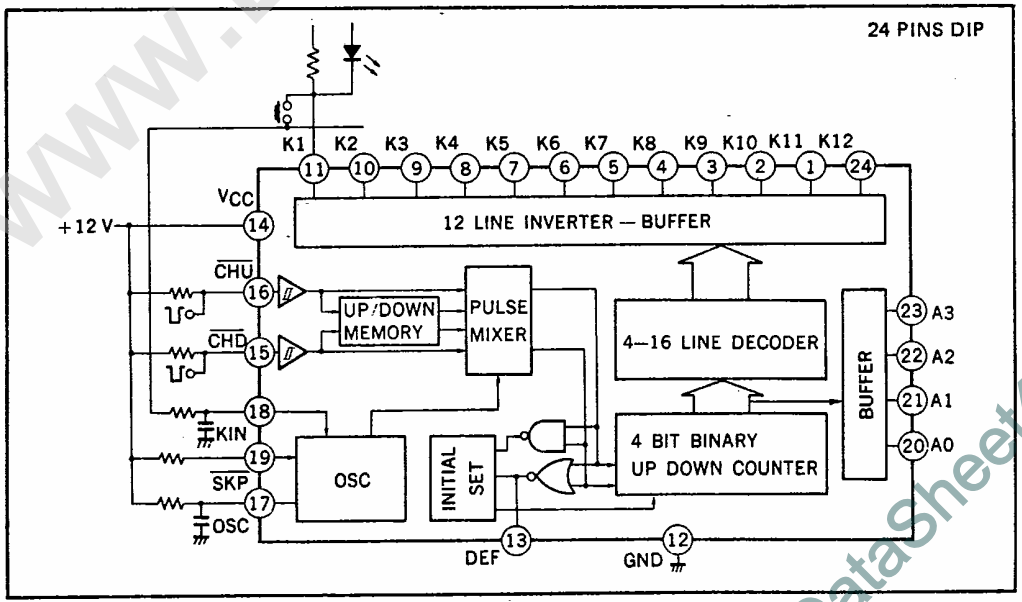
FEATURES

- 4 bit output
- LED, Neon lamps direct drive.
  I_K=5 mA, V_{kSAT} 150 mV MAX.
- Low power consumption.
  V_{CC}=12 V, I_{CC}=9 mA TYP.
- Up to 12 channel selection.
- Internal schmitt trigger circuit. (CHU, CHD INPUT)
- Power ON initial channel set.
- TV, Radio etc. channel selection use.

PACKAGE DIMENSIONS in millimeters (inches)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

Supply Voltage	V_{CC}	15.0	V
Input Current to Channel Selection Circuit	$I_{K1\sim11,\ 24}$	−5 to 30	mA
Input Current to Control Circuit	$I_{A0\sim A3}$	−5 to 10	mA
Input Current to Control Circuit	$I_{C18,\ 19}$	−5 to 10	mA
Input Current to Control Circuit	I_{C13}	−5 to 30	mA
*Output Voltage to Channel Selection Circuit	$V_{K1\sim11,\ 20}$	−0.5 to 45	V
*Output Voltage to Control Circuit	$V_{13},\ V_{A0\sim A3}$	−0.5 to 14.4	V
*Input Voltage to Control Circuit	$V_{15,\ 16,\ 17}$	−0.5 to V_{CC}+0.5	V
Power Dissipation	P_d	300	mW
Operating Temperature Range	T_{opt}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

* At V_{CC}=12 V

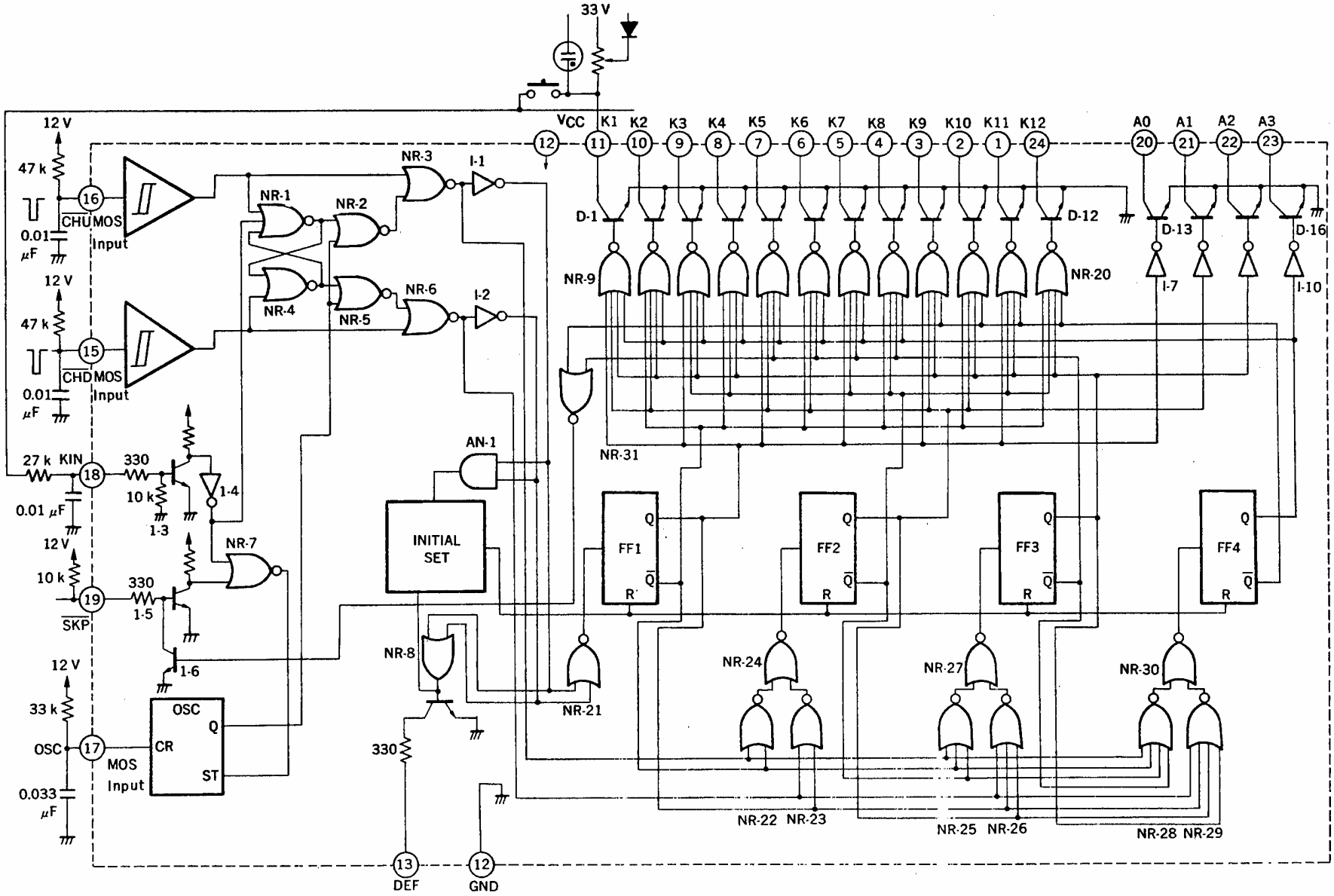
RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	9.6	12.0	14.4	V
Channel Selection Input Current	I_K		5.0		mA
Clock Oscillation Frequency	f_{OSC}		2.0	10.0	kHz

ELECTRICAL CHARACTERISTICS (Ta=25 ±3 °C)

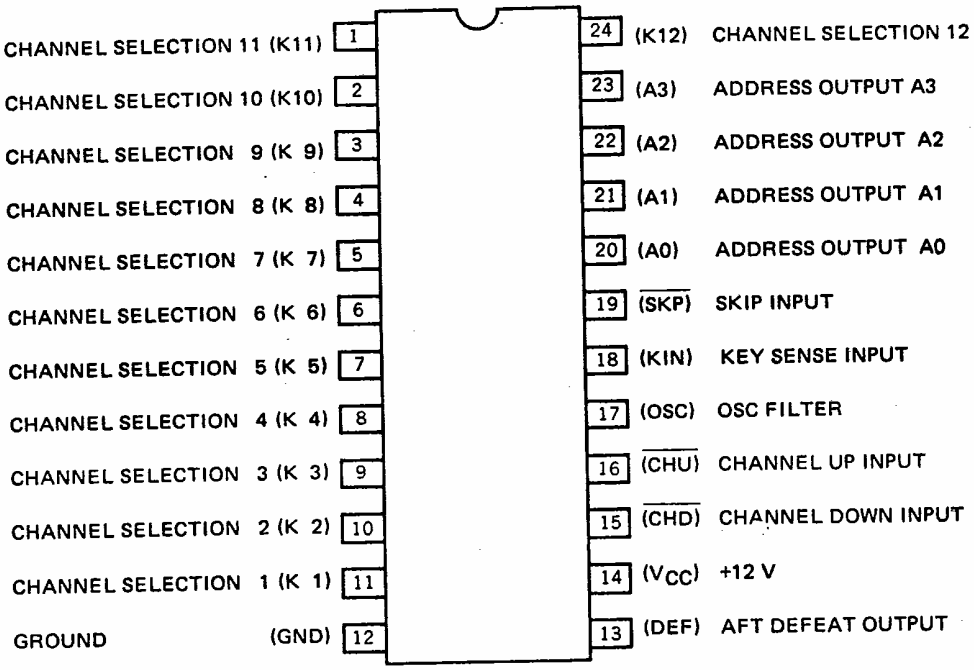
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{DD}	2.0	9.0	13.0	mA	V_{CC}=12 V
Channel Selection Saturation Voltage	$V_{OL(K)}$			150	mV	V_{CC}=9.6 V, I_{OL}=5 mA
Channel Selection Leakage Current	$I_{OH(K)}$			10	μA	V_{CC}=14.4 V, V_{OH}=35 V
Address Output Saturation Voltage	$V_{OL(A)}$			0.5	V	V_{CC}=9.6 V, I_{OL}=2 mA
Address Output Leakage Current	$I_{OH(A)}$			10	μA	V_{CC}=14.4 V, V_{OH}=14.4 V
AFT Defeat Output Voltage	$V_{OL(D)}$			6	V	V_{CC}=9.6 V, I_{OL}=12 mA
AFT Defeat Leakage Current	$I_{OH(D)}$			10	μA	V_{CC}=14.4 V, V_{OH}=14.4 V
Channel Input High Threshold Voltage	$V_{TH(CH)}$	7.2		9.0	V	V_{CC}=12 V
Channel Input Low Threshold Voltage	$V_{TL(CH)}$	5.0		8.0	V	V_{CC}=12 V
Channel Input Leakage Current	$I_{CH(CH)}$	−5			μA	V_{CC}=14.4 V, V_{IL}=0 V
Channel Input Leakage Current	$I_{CH(CH)}$			5	μA	V_{CC}=14.4 V, V_{IH}=14.4 V
Key Input Current	$I_{IH(KI)}$	200			μA	V_{CC}=9.6 V
Key Input Leakage Current	$I_{IL(KI)}$	−10			μA	V_{CC}=14.4 V, V_{IL}=0 V
Skip Input Current	$I_{IH(SK)}$	50			μA	V_{CC}=9.6 V
Skip Input Leakage Current	$I_{IL(SK)}$	−5			μA	V_{CC}=14.4 V, V_{IL}=0 V
Channel Hold Voltage	V_{HOLD}	6.5			V	
OSC Frequency	f_{OSC}	1.0	2.0	3.0	kHz	V_{CC}=12 V, R=33 kΩ, C=0.033 μF

EQUIVALENT CIRCUIT



Logic Blocks consist of PMOS technology
Output and Input consist of Bipolar technology.

CONNECTION DIAGRAM (Top View)



PIN FUNCTION

K1 ~ 12 (#11 ~ 1, #24) CHANNEL SELECTION OUTPUT

These are the output terminals constructed of collector-opened transistors, so they can drive potentiometers and indicators, and key output. They have saturation voltage of 150 mV at I_K=5 mA, so they can drive neon or LED lamps directly.

GND (#12) GROUND

DEF (#13) AFT DEFEAT OUTPUT

This terminal is made of open collector transistor output through a resistor of 330 Ω. It is used for AFT (Automatic Fine Tuning ..... TV use) defeat, sound muting and LED indicate erasing.

V_{CC} (#14) +12 V (9.6 ~ 14.4 V)

CHD (#15) CHANNEL DOWN INPUT

Usually pulled up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K12 to K1.

CHU (#16) CHANNEL UP INPUT

Usually pull up to V_{CC} through a resistor, Channel selector changes at positive going edge of input signal of this terminal and the channel selector works orderly from K1 to K12. If CHU and CHD terminals put down to ground at same time, initial channel is selected. So, it is very useful to remote control operation use. These terminals include schmitt trigger circuit. If these terminals are not used as remote control operation, connect these terminals to V_{CC} directry.

OSC (#17) OSC FILTER

When a Channel key is pushed or skip function is operated, oscillator contained in this IC oscillate with C, R connected to this terminal. Typical oscillation frequency is 2 kHz. (R=33 kΩ, C=0.033 μF)

KIN (#18) KEY INPUT

When channel selection key is pushed, as pushed channel is not selected, "High" level of signal is applied to this terminal through a potentiometer resistor. Then channel selector scans terminals of K1 ~ K12. And when sense up this terminal, it pull down the voltage of this terminal and stop the scanning.

SKP (#19) SKIP INPUT

Usually pull up to V_{CC} through resistor. When only 10 channels are used, connect open channel outputs (K11, K12) to this terminal with CR filter.

A0 ~ A3 (#20 ~ 23) ADDRESS OUTPUT A0 ~ A3

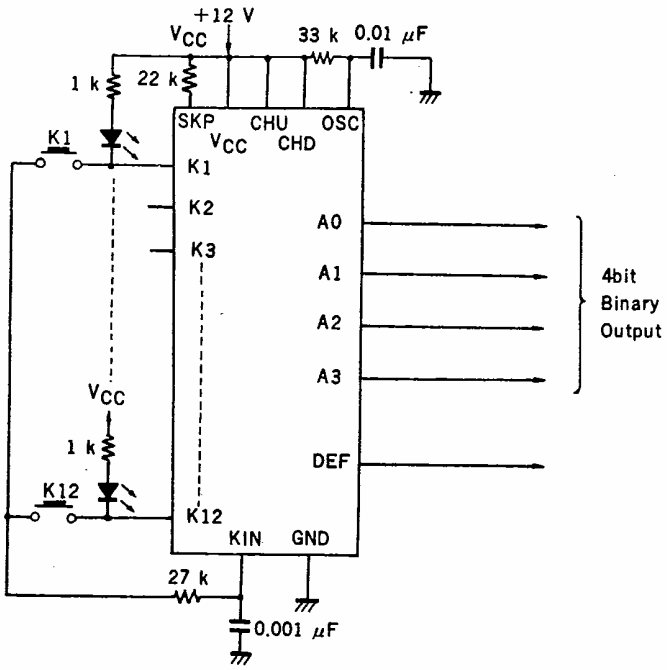
These are internal 4 bit counter output terminals constructed of collector-opened transistors. These output can be used as 7 segment LED display or possition output for MPU reading.

Selectchannel	Address output			
	A0...L	A1...L	A2...L	A3...L
K 1	H	L	L	L
K 2	L	H	L	L
K 3	H	H	L	L
K 4	L	L	H	L
K 5	H	L	H	L
K 6	L	H	H	L
K 7	H	H	H	L
K 8	L	L	L	H
K 9	H	L	L	H
K 10	L	H	L	H
K 11	H	H	L	H
K 12	L	H	L	H

* L...GND
H...OPEN

APPLICATION CIRCUIT

12 Position Display/4 bit Encoder Output



APPLICATION CIRCUIT

Example of TV channel selection circuit with 7 segment LED display