CMOS 4-BIT MICROCONTROLLER

TMP47C623F, TMP47C823F

The 47C623/823 are high speed and high performance 4-bit single chip microcomputers based on the TLCS-470A series with a LCD driver, High Speed Event Counter and Pulse output circuit.

PART No.	ROM	RAM	PACKAGE	OTP version
TMP47C623F	6144 × 8-bit	384 × 4-bit	QFP64-P-1420-1.00A	TMP47P823VF
TMP47C823F	8192 × 8-bit	512 × 4-bit		

FEATURES

◆4-bit single chip microcomputer
◆Instruction execution time :
1.3μs (at 6MHz), 244μs (at 32.8kHz)
◆100 basic instructions
- Table look-up instructions

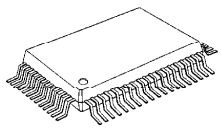
◆Subroutine nesting : 15 levels max.
◆6 interrupt sources (External :2, Internal : 4)
All sources have independent latches each, and multiple interrupt control is available.
◆I/O port (32 to 28 pins)
- Input 2 ports 5 pins
- I/O 7 ports 27 pins

◆Two 12-bit Timer/Counters
Timer, event counter, and pulse width measurement mode
◆16-bit High Speed Event Counter
◆Interval Timer (22 stages)
◆Watchdog Timer
◆Serial Interface with 8-bit buffer
- Simultaneous transmission and reception capability.
- External/internal colck, leading/trailing edge, and 4/8-bit mode

◆LCD driver
- LCD direct drive capability (max. 12-digit display at 1/4 duty LCD)
- 1/4, 1/3 1/2 duties or static drive are programmably selectable.

◆Pulse output
Pulse output frequency select
◆High current outputs
LED direct drive capability (typ.20mA × 4bits)
◆Dual-clock operation
High-speed/Low-power consumption operating mode
◆Hold function
Battery/Capacitor back-up
◆Real Time Emulator : BM47C823F0A

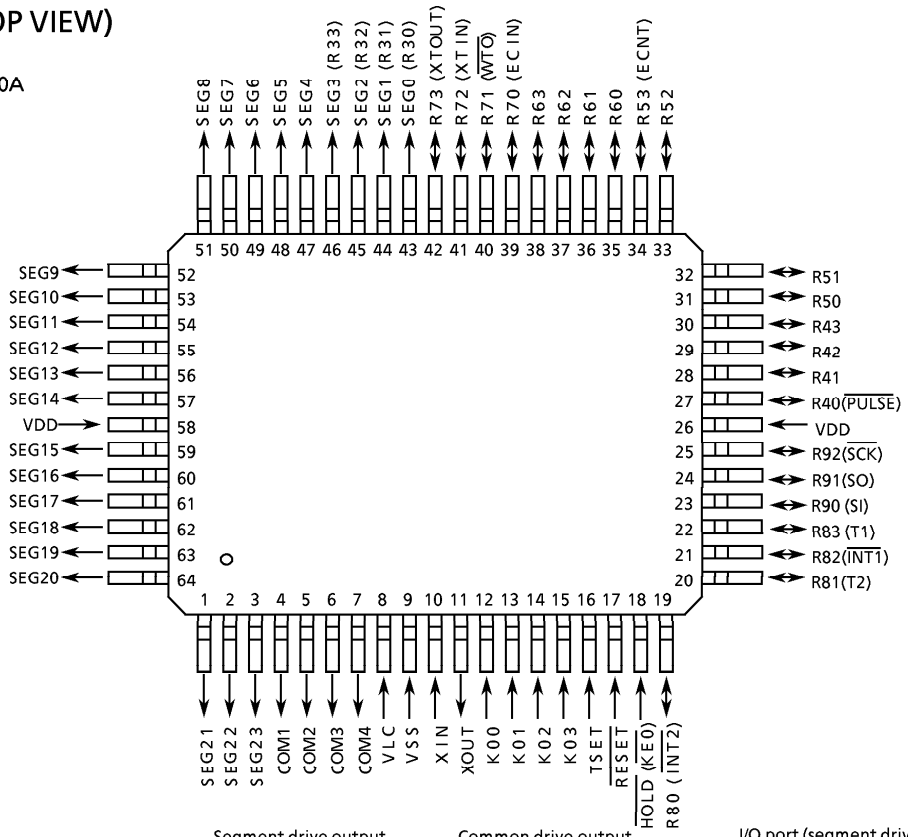
QFP64-P-1420-1.00A



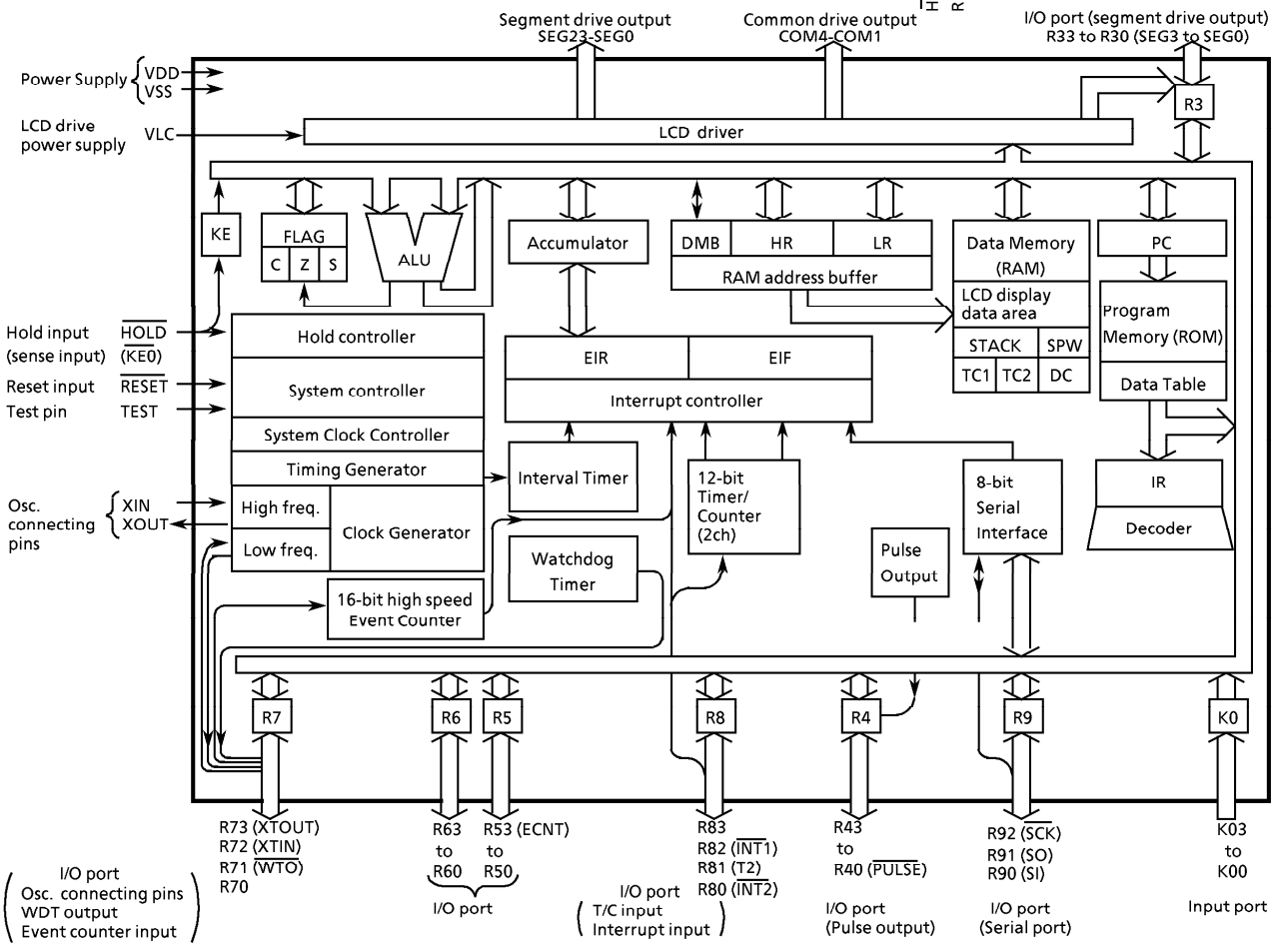
TMP47C623F
TMP47C823F
TMP47P823VF

PIN ASSIGNMENT (TOP VIEW)

QFP64-P-1420-1.00A



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
R33 - R30	I/O	4-bit I/O port with latch. When used as input port the latch must be set to "1".	LCD Segment drive output. When used as segment drive output the port R3 control resister must be set to "1".
R43 - R41	I/O	4-bit I/O port with latch. When used as input port, pulse output, the latch must be set to "1".	
R40 ($\overline{PULSE}$)	I/O (Output)		Pulse output
R53 (ECNT)	I/O	4-bit I/O port with latch. When used as input port, External interrupt input, the latch must be set to "1".	External interrupt input
R52 - R50			
R63 - R60			
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch. When used as input port, watchdog timer output or External pulse input pin, the latch must be set to "1".	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70 (ECIN)	I/O		External pulse input pin
R83 (T1)	I/O	4-bit I/O port with latch. When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)	I/O (Input)		External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port, serial port the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
SEG23 - SEG0	Output	LCD Segment drive output	
COM4 - COM1		LCD Common drive output	
XIN	Input	Resonator connecting pins (high-frequency) .	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/ release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VLC		LCD drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C623/823 the configuration and functions of hardwars are described. As the description has been provided with priority on those parts deffering from the 47C1260/1660 (TLCS-470A), thchnical data sheets for the 47C1260/1660 shall also be referred to.

1. SYSTEM CONFIGURATION

(1) INTERNAL CPU FUNCTION

2.1 Program Counter (PC)

2.2 Program Memory (ROM) , and Data Table Bank Selector (DTB)

2.3 Data Memory (RAM)

The others are the same as those of the 47C1260/0660.

(2) PERIPHERAL HARDWARE FUNCTION

① I/O Port
② Interval Timer
③ Timer/Counter
④ Watchdog Timer
⑤ High Speed Event/Counter
⑥ Pulse output
⑦ LCD Driver
⑧ Serial Interface

The description has been provide with priority on functions (①, ⑤, ⑥ and ⑦) added to and changed from the 47C1260/1660.

2. INTERNAL CPU FUNCTION

2.1 Program Counter (PC)

The program counter is a 13-bit binary counter which indicates the address of the program memory storing the next instruction to be executed.

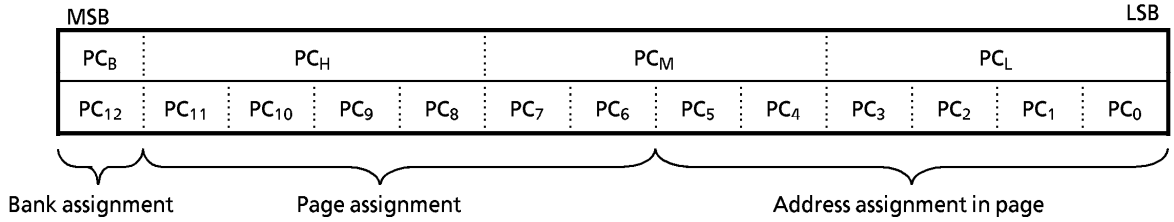


Figure 2-1. Configuration of Program Counter

The PC can directly address an 8192-byte address space.

2.2 Program Memory (ROM), and Data Table Bank Selector (DTB)

The 47C823 contains a program memory (masked ROM) of 8192 × 8 bit (addresses 0000 through $1FFF_H$).
The 47C623 contains a program memory (masked ROM) of 6144 × 8 bits (addresses 0000 through $17FF_H$).
The 47C623/823 don't have a data table bank selector (DTB).
The fixed data is read from the table look-up instructions is located in the program memory (address 1000 through 17FF for the 47C623, 1000 through 1FFF for the 47C823) and the fixed data can specify the data counter of a 12-bit register.

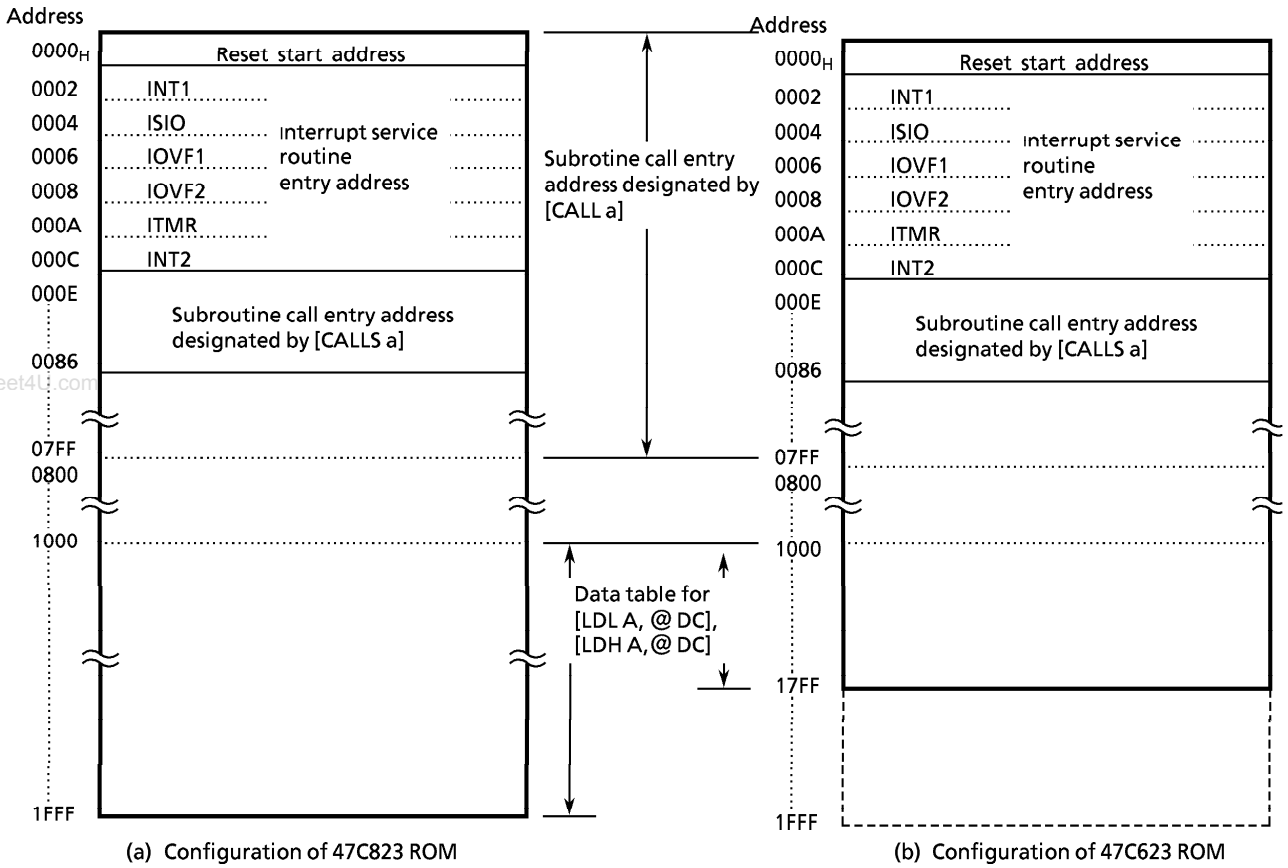


Figure 2-2. Program Memory Map

2.2 Data Memory Capacity

The 47C823 has two data memory banks (banks 0 and 1) of 256 × 4bit.
The 47C623 has a data memory banks 0 of 256 × 4bit and a data memory banks 1 of 128 × 4bit.
A private stack (STK13) and stack pointer word (SPW13) for PC_{13} have not been installed. When power-on is performed, the contents of the data memory become unpredictable, so that they must be initialized by the initialize routine.

Example : To clear RAM

```
        LD      HL, #00H
SCLR1 : CLR     DMB
SCLR2 : ST      #0, @HL+
        B       SCLR2
        SET     DMB
SCLR3 : ST      #0, @HL+
        B       SCLR3
        ADD     H, #1
        B       SCLR1
```

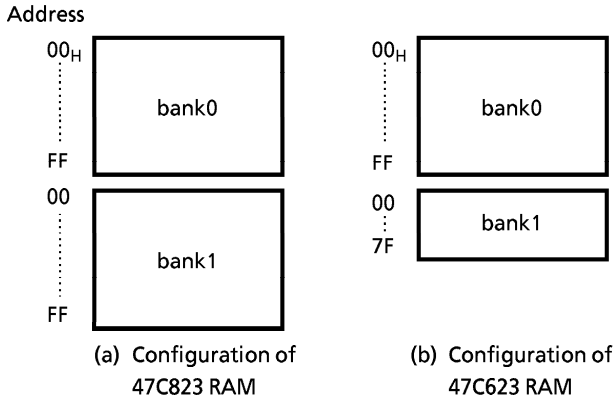


Figure 2-3. Data Memory (RAM)

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Port

The 47C623/823 have 9 I/O port (32pins) each as follows.

① K0 ; 4-bit input
② R3 ; 4-bit input/output (shared with segment output)
③ R4 ; 4-bit input/output (R40 pin is shared with pulse output)
④ R5 ; 4-bit input/output (R53 pin is shared with external interruput input)
⑤ R6 ; 4-bit input/output
⑥ R7 ; 4-bit input/output (shared with the Low-frequency reasonator connecting pin and the Watchdog timer output and high speed event counter input)
⑦ R8 ; 4-bit input/output (shared with external interrupt and timer/counter input)
⑧ R9 ; 3-bit input/output (shared with serial port)
⑨ KE ; 1-bit sense input (shared with hold request/release signal input)

The description has been provided with priority on ports (②③④⑥ and ⑧) changed from 47C1660. Futher, 47C623/823 have not P1, P2 port, Therefore, the instruction [OUTB @ HL] and 5bit to 8bit data conversion table cannot be used.

Table 2-1 lists the port address assignments and the I/O instruction that can access the ports.

(1) port R3 (R33-R30)

Port R3 is a 4-bit I/O port with latch shared by the segment output pin of LCD Driver. The port R3 control register (OP0E) determine whether this port is used for I/O port or segment output. The port R3 control register is initialized to "0" during reset and the Port R3 is I/O port. When used as an input port, the latch showld be set to "1". The output latch of port R3 is initialized to "1" during reset.

Port R3 (port address OP03 / IP03)

3	2	1	0
R33 (SEG3)	R32 (SEG2)	R31 (SEG1)	R30 (SEG0)

Control of port R3/Segment output
(port address : OP0E) (Initial value : 0000)

3	2	1	0
R3CR3	R3CR2	R3CR1	R3CR0

R3CR	Selection of port R3/segment output

0 : Port R3
1 : Segment output

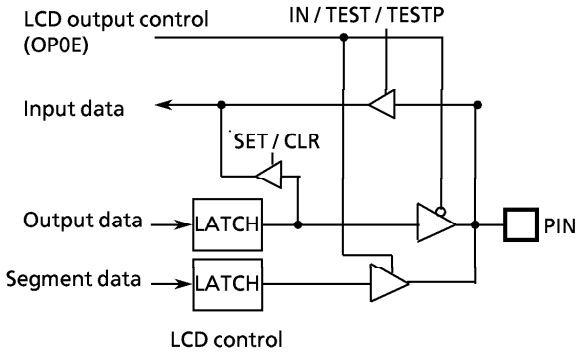


Figure 3-1. port R3

Port Address (**)	Port		Input / output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	R3 input port	R3 output port (LCD OUTPUT)	○	○	○	–	○	○	○
04	R4 input port	R4 output port (PULSE OUTPUT)	○	○	○	–	○	○	○
05	R5 input port (Interrupt input)	R5 output port	○	○	○	–	○	○	○
06	R6 input port (HEC input)	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	HEC Status (Note 2)	HEC1 Ta Setting register	–	○	○	–	–	–	–
0B	——	HEC2 Tb Setting resister	–	○	○	–	–	–	–
0C	HEC Low data input	——	○	–	–	–	–	–	–
0D	HEC High data input	Window gate pulse control	○	○	○	–	–	–	–
0E	Status input (Note 3)	R3 output control	○	○	○	–	–	–	–
0F	Serial receive buffer	Serial tansmit buffer	○	○	○	–	–	–	–
10_H	HOLD pin status	Hold operating mode control	○	○	–	–	–	–	–
11	HOLD pin status	——	–	–	–	–	–	–	–
12	HOLD pin status	——	–	–	–	–	–	–	–
13	HOLD pin status	——	–	–	–	–	–	–	–
14	HOLD pin status	——	–	–	–	–	–	–	–
15	HOLD pin status	Watchdog timer control	–	○	–	–	–	–	–
16	HOLD pin status	System clock control	–	○	–	–	–	–	–
17	HOLD pin status	HEC Control	–	○	–	–	–	–	–
18	HOLD pin status	Pulse output control	–	○	–	–	–	–	–
19	HOLD pin status	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	HOLD pin status	LCD driver control 1	–	○	–	–	–	–	–
1B	HOLD pin status	LCD driver control 2	–	○	–	–	–	–	–
1C	HOLD pin status	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	HOLD pin status	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	HOLD pin status	Serial Interface control 1	–	○	–	–	–	–	–
1F	HOLD pin status	Serial Interface control 2	–	○	–	–	–	–	–

Note 1. "——" means the reserved state. Unavailable for the user programs.

Note 2. To detect the overflow and status input of the high speed event counter (HEC).

Note 3. The status input of serial interface, clock generator, and $\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$) pin.

Table 3-1. Port Address Assigments and Available I/O Insruction

(2) Port R4 (R43-R40), R5 (R53-R50), R7 (R73-R70)

The 4-bit I/O ports with a latch. When used as an input port, the latch showld be set to "1". The latch is initialized to "1" during reset. R40 pin is shared by pulse output pin. To use this pin for the functional pin, the latch must be set to "1".

R53 pin is shared by pulse input pin. To use this pin for the functional pin, the latch must be set to "1". R70 pin is shared by high speed event counter pin. To use this pin for the functional pin, the latch must be set to "1".

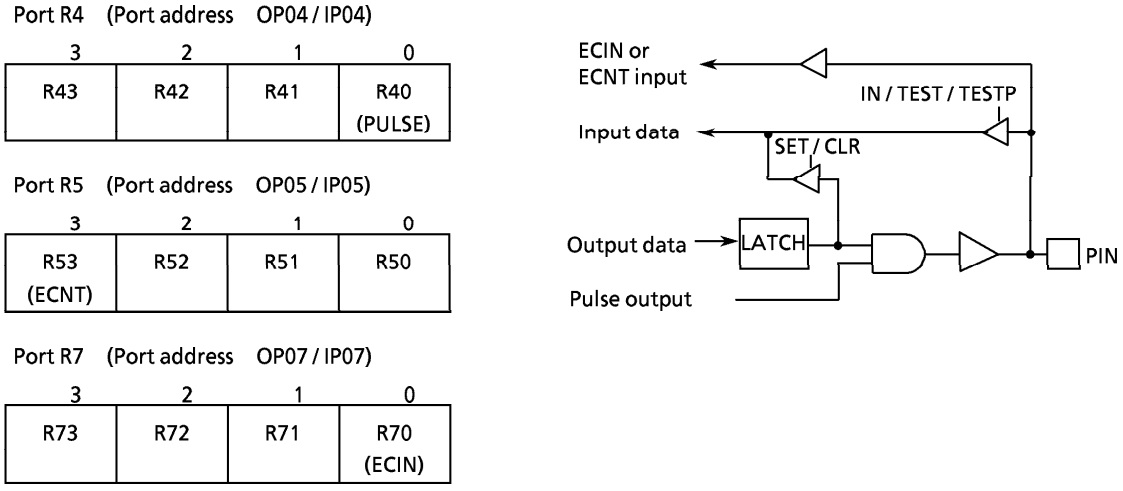


Figure 3-2. Port R4, R5, R7

3.2 High Speed Event/Counter (HEC)

The 47C623/823 have a 16-bit high-speed event counter (HEC) which can be used for ECIN pin input frequency measurement. HEC counts the edge (falling edge, falling edge/rising edge) of input pulses while the window gate pulse is at "H" level and interrupt requests (ECNT) are generated when the window gate pulse edge (falling edge, falling edge/rising edge).

The window gate pulse cycle is set by command.

The ECIN pin is also used as the R70 pin. When used as the ECIN pin, the R70 output latch is set to "1".

3.2.1 Configuration of HEC circuit

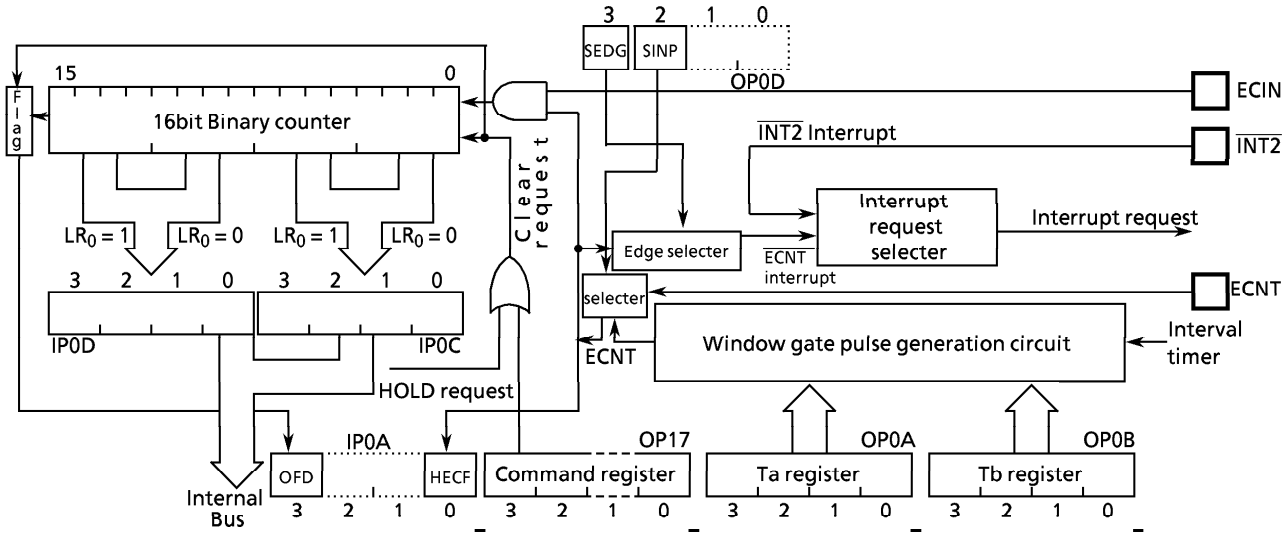


Figure 3-3. Configuration of High Speed Event/Counter

3.2.2 Control of HEC

HEC is controlled by the command register (OP17). External interrupt 2 is used as the interrupt source. The INT2 interrupt request is selected during reset, so ECNT interrupt is requested by command. Interrupt priority is the same as for external interrupt 2.

HEC control command reguster
(port address OP17)

3	2	1	0	
EHEC	CHEC		SINT	(Initial value 00*0)

EHEC	High Speed Event/Counter Function
0 :	Disable
1 :	Enable (Enable window gate pulse generation)

CHEC	Clear of High Speed Event/counter
0 :	Clear requset (After Clear, CHEC is set to "1" autmatticary)

SINT	Select of Interrupt request
0 :	$\overline{INT2}$ Interrupt request
1 :	$\overline{ECNT}$ Interrupt request (folling edge of window gate pulse)

*Note. * ; don't care*

Figure 3-4. HEC Control Command Resister

3.2.3 HEC Operation

HEC counts input frequency only during the intervals that the window gate pulse is at "H" level when EHEC (command register bit3) is"1". The window gate pulse can be set to 256 different cyclse using port addresses OP0A and OP0B.

(1) Select of window gate pulse input
The window gate pulse (ECNT) input can be set to the window gate pulse generation circuit or ECNT input (R53) using SINP (bit2) of command register (OP0D).
The window gate pulse is selected the window gate pulse generation circuit during initial.

Window gate pulse control command register
(port address OP0D)

3	2	1	0	
SEDG	SINP			(Initial value 00**)

SEDG	Select of edge
0 :	falling edge
1 :	falling edge/rising edge

SINP	Select of window gate pulse
0 :	Window gate pulse generation circuit input
1 :	ECNT input

Figure 3-5. Window gate pulse control command register

(2) Window gate pulse setting

The window gate pulse (ECNT) consists of a count time (Ta) and non-count time (Tb), each of which can be set independently using OP0A and OP0B. Thus, one cycle is Ta + Tb. The Ta and Tb setting times are as follows.

$$(16 - n) \times 2^{13} / fc \ [s] \qquad (n = 0 \text{ to } 15)$$

Table 3-2 shows the setting times when fc = 4.194304MHz ECNT can be generated at the next rise edge of interval timer output (fc/2^{13} [Hz] by setting EHEC = 1.)

HEC operation status register
(port address IP0A)

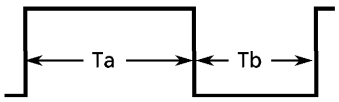
3	2	1	0	
(OFD)			HECF	(Initial value 0110)

HECF	Operation status
0 :	Stop (Tb) or Disable
1 :	Counting (Ta)

Figure 3-6. HEC operation status register

Example : Generating ECNT with a cycle of approximately 29ms and a duty ratio of 3:2.

```
OUT     #07H, %OP0A  ;   Set Ta to 17.58ms
OUT     #0AH, %OP0B  ;   Set Tb to 11.72msC
LD      A, #0FH
OUT     A, % OP17    ;   Enables ECNT generation
```



Setting value	Setting time	Setting value	Setting time
0	31.25 ms	8	15.63 ms
1	29.30 ms	9	13.67 ms
2	27.34 ms	A	11.72 ms
3	25.39 ms	B	9.77 ms
4	23.44 ms	C	7.81 ms
5	21.48 ms	D	5.86 ms
6	19.53 ms	E	3.91 ms
7	17.58 ms	F	1.95 ms

Table 3-2. Setting of Ta, Tb

(3) Count operation

Counting is enabled by setting EHEC to "1". Counting is stopped by clearing EHEC to "0" but the binary count values are held.

An INT2 interrupt is issued at the fall edge of the window gate pulse when SINT(command register bit 0) is set to"1". Normally, binary counter date are read, the counter cleared and the next count operation started by the interrupt service routine.

Select of window gate pulse edge can be set to edge (falling edge, falling edge/rising edge) using SEDG of command register (OP0D).

The binary counter is cleared with CHEC (command register bit2). EHEC and the binary counter are cleared during hold operation.

The window gate pulse (ECNT) status can be monitored using the status register. "1" is read out at "H" level (during counting). Figure 3-7 shows the HEC operation timing.
The detection of overflow (binary counter) can be monitored using the OFD (bit3) of command register (IP0A). The flag of OFD is held till the CHEC is cleaved to "0".

Detection of overflow command register
(port address IP0A)

3	2	1	0	
(OFD)			(HECF)	(Initial value 0110)

OFD	Detection of overflow
0 :	Not overflow
1 :	Overflow

Figure 3-8. Detection of overflow command register

(4) Reading of count data
Binary counter data are read out by port addresses IP0C and IP0D. At that time, a total of 16 bits of data is read out by reading 4 bits at a time in accordance with the LR0 (L register bit 0) value. Table 3-3 shows the relationship between port address LR0 and count data.

Port address	LR_0	Reading bit of HEC
IP0C	0	HEC3 to HEC0
	1	HEC7 to HEC4
IP0D	0	HEC11 to HEC8
	1	HEC15 to HEC12

Table 3-3. The relation ship between port address LR0 or count data

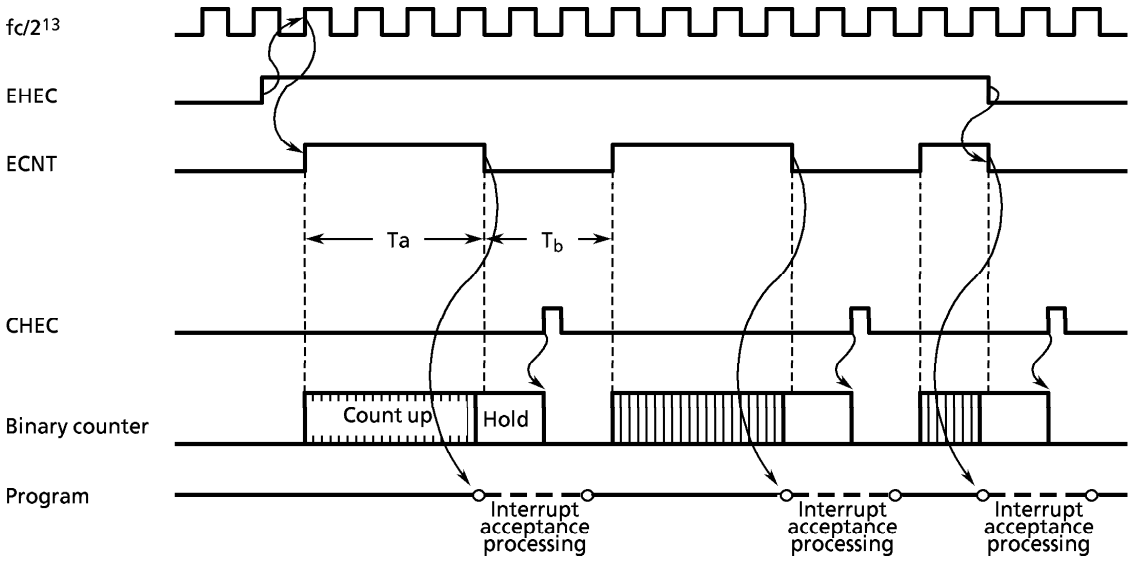


Figure 3-7. HEC Operation Timing

3.3 Pulse output circuit

The 47C623/823 has a built-in one-channel pulse output to use in driving, for example, a buzzer. Eight different pulse output frequencies can be selected by command. Pulses are output from the PULSE pin. The PULSE pin is also used as the R40 pin. When used as the PULSE pin, the R40 output latch is set to "1".

3.3.1 Control of pulse output circuit

The pulse output circuit is controlled by the command register (OP18). Pulses are output by setting EPULS to "1". Pulse output is disabled (by clearing OP18 to"0") during hold operation.

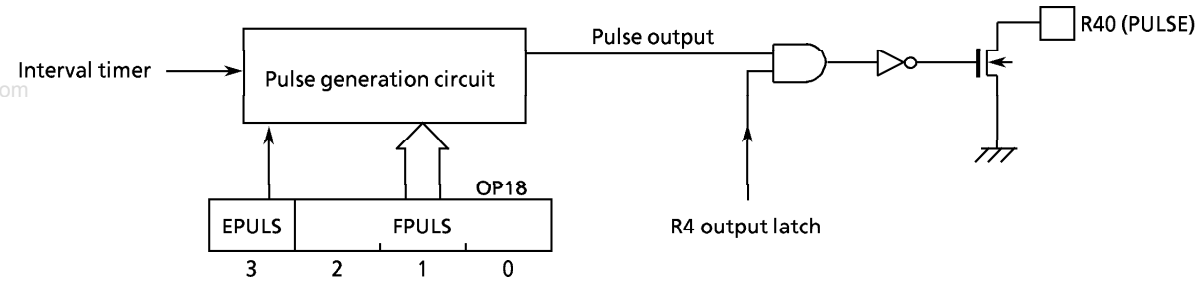


Figure 3-9. Pulse output circuit

Pulse output control command resister
(Port address OP18)

3	2	1	0
EPULS	FPULS		

EPULS	Pulse output control

0 : Disable
1 : Enable

FPULS	Pulse output frequency select

Example: At fc = 4.19MHz

000:	fc / (2^9 × 8) [Hz]	1.024 [kHz]
001:	fc / (2^9 × 7)	1.170
010:	fc / (2^9 × 6)	1.365
011:	fc / (2^9 × 5)	1.638
100:	fc / (2^9 × 4)	2.048
101:	fc / (2^9 × 3)	2.731
110:	fc / (2^9 × 2)	4.096
111:	fc / (2^9 × 1)	8.192

Note. fc : High-frequency clock

Figure 3-10. Pulse output command resister

3.4 LCD Driver

The 47C623/823 have the circuit that directly drives the liquid crystal display (LCD) and its control circuit.

The 47C623/823 have the following connecting pins with LCD.

① Segment output port 24 pins (SEG23-SEG4)
② Segment output port (R3 I/O port) 4 pins (SEG3 to SEG0)
③ Common output port 4 pins (COM4-COM1)

In addition, VLC pin is provided as the drive power pin.

The devices that can be directly driven is selectable from LCD of the following drive methods.

① 1 / 4 Duty (1 / 3 Bias) LCD ····· Max. 96 Segment (12 digits × 8 segments)
② 1 / 3 Duty (1 / 3 Bias) LCD ····· Max. 72 Segment (9 digits × 8 segments)
③ 1 / 3 Duty (1 / 2 Bias) LCD ····· Max. 72 Segment (9 digits × 8 segments)
④ 1 / 2Duty (1 / 2 Bias) LCD ····· Max. 48 Segment (6 digits × 8 segments)
⑤ Static LCD ····· Max. 24 Segment (3 digits × 8 segments)

3.4.1 Configuration of LCD driver

Figure 2-8 shows the configuration of the LCD driver.

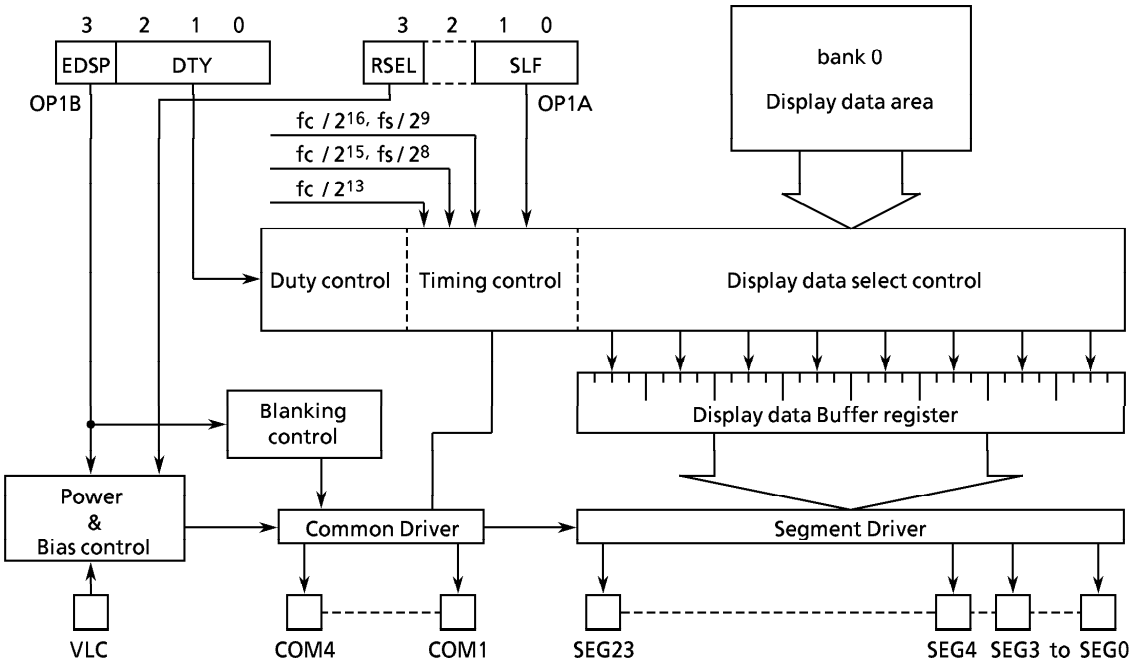


Figure 3-11. LCD Driver

3.4.2 Control of LCD driver circuit

The LCD driver is controlled by the command register 1,2 (OP1A, OP1B). Further, when the command register 1 is accessed, the most significant bit of the command register 2 must be set to "0" (Blanking).

LCD Driver control command register 1
(Port address OP1A)

3	2	1	0
RSEL		SLF	

(Initial value 0000)

RSEL	Selection of LCD output resistance

(Ros1, Roc1/Ros2, Roc2)

0: Output resistance 1 (20/200kΩ)
1: Output resistance 2 (10/70kΩ)

SLF	Selection of LCD drive frequency

	Single Clock Mode	Dual Clock Mode
00:	$fc / 2^{13}$ [Hz]	Unused
01:	$fc / 2^{15}$	$fs / 2^{8}$ [Hz]
10:	$fc / 2^{16}$	$fs / 2^{9}$
11:	Reserved	Reserved

LCD Driver control command register 2
(Port address OP1B)

3	2	1	0
EDSP		DTY	

(Initial value 0000)

EDSP	LCD Display Control

0: Blanking
1: Enables LCD display (Blanking is released)

DTY	Selection of driving methods

000:	1 / 4 Duty	(1 / 3 Bias)
001:	1 / 3 Duty	(1 / 3 Bias)
010:	1 / 3 Duty	(1 / 2 Bias)
011:	1 / 2 Duty	(1 / 2 Bias)
100:	Static	
101:	Reserved	
11*:	Reserved	

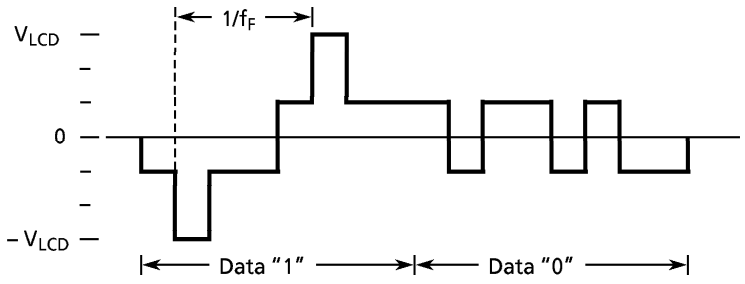
Note. *fc ; High-frequency clock [Hz]*
fs ; Low-frequency clock [Hz]
** ; don't care*

Figure 3-12. LCD Driver control Command Register

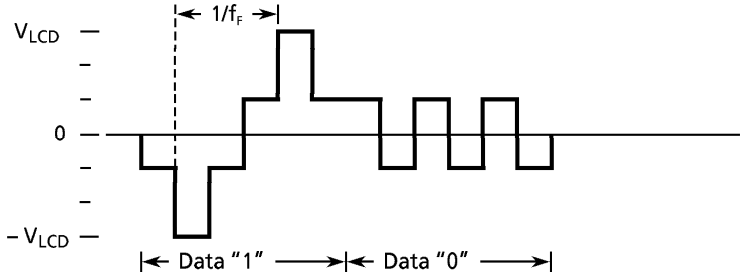
(1) Driving methods of LCD driver

Driving methods of LCD is selected 5 kind of DTY (bit 2-0 of command register 2). The drive method is initialized according to LCD used in the initial program.
Example of LCD and their drive waveform are shown in Figure 3-13.

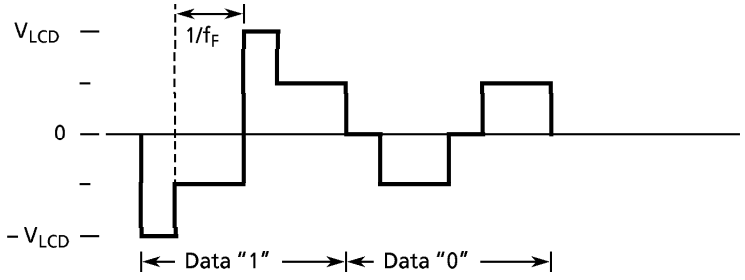
① 1 / 4 Duty (1 / 3 Bias)



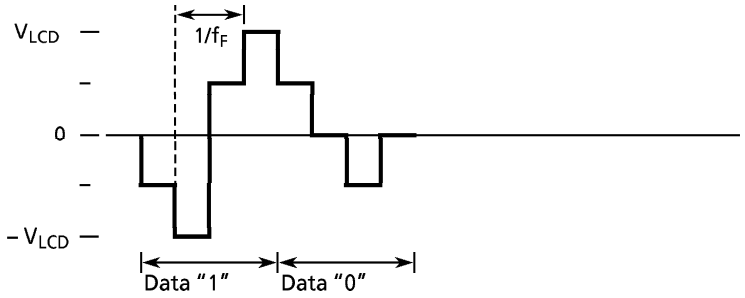
② 1 / 3 Duty (1 / 3 Bias)



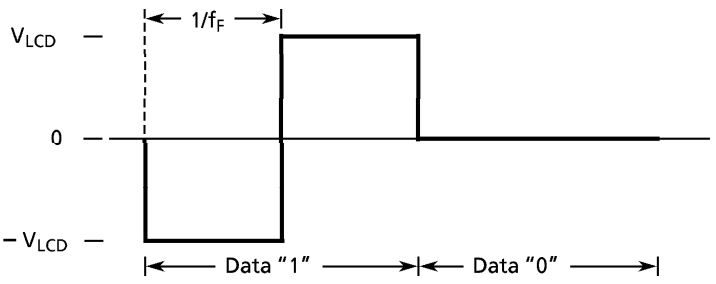
③ 1 / 3 Duty (1 / 2 Bias)



④ 1 / 2 Duty (1 / 2 Bias)



⑤ Static



Note f_F ; *FRAME FREQUENCY*
V_{LCD} ; *LCD drive voltage* ($= V_{DD} - V_{LC}$)

Figure 3-13. LCD drive waveform (COM-SEG pins)

(2) Frame frequency

Frame frequency (f_F) is set according to the drive method and base frequency as shown in the following table 3-4.

The base frequency is selected by SLF (the lower 2 bits of the command register) according to the reference clock frequency and fs.

a. At the single clock mode

SLF	BASE FREQUENCY [Hz]	FRAME FREQUENCY [Hz]			
		1 / 4 DUTY	1 / 3 DUTY	1 / 2 DUTY	STATIC
10	$\frac{fc}{2^{16}}$	$\frac{fc}{2^{16}}$	$\frac{4}{3} \cdot \frac{fc}{2^{16}}$	$\frac{4}{2} \cdot \frac{fc}{2^{16}}$	$\frac{fc}{2^{16}}$
	fc = 4MHz	61	81	122	61
01	$\frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$	$\frac{4}{3} \cdot \frac{fc}{2^{15}}$	$\frac{4}{2} \cdot \frac{fc}{2^{15}}$	$\frac{fc}{2^{15}}$
	fc = 4MHz	122	163	244	122
00	$\frac{fc}{2^{13}}$	$\frac{fc}{2^{13}}$	$\frac{4}{3} \cdot \frac{fc}{2^{13}}$	$\frac{4}{2} \cdot \frac{fc}{2^{13}}$	$\frac{fc}{2^{13}}$
	fc = 1MHz	122	163	244	122

Note . fc ; High-frequency clock [Hz]

b. At the dual clock mode

SLF	BASE FREQUENCY [Hz]	FRAME FREQUENCY [Hz]			
		1 / 4 DUTY	1 / 3 DUTY	1 / 2 DUTY	STATIC
10	$\frac{fs}{2^{9}}$	$\frac{fs}{2^{9}}$	$\frac{4}{3} \cdot \frac{fs}{2^{9}}$	$\frac{4}{2} \cdot \frac{fs}{2^{9}}$	$\frac{fs}{2^{9}}$
	fs = 32kHz	61	83	125	61
01	$\frac{fs}{2^{8}}$	$\frac{fs}{2^{8}}$	$\frac{4}{3} \cdot \frac{fs}{2^{8}}$	$\frac{4}{2} \cdot \frac{fs}{2^{8}}$	$\frac{fs}{2^{8}}$
	fs = 32kHz	125	167	250	125

Note . fs ; Low-frequency clock [Hz]

Table 3-4. Setting of LCD Frame Frequency

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is given by the difference in potential (V_{DD}-V_{LC}) between pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCDs light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage.

Both the segment output and common output become V_{DD} level at this time and the LCDs turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bit 3 of the command register 2) to "1". After that, the power switch will not turn off even during blanking (setting EDSP to "0") and the VLC voltage continues to flow.

The power switch is turned off during hold operation low power consumption by turning off the LCD. When hold operation is released the status in effect immediately before the hold operation is reinstated.

(4) LDC output resistance

Selection of LCD output resistance can be selected by command register (OP1A).
The LDC output resistance is selected by RSEL (MSB of command register) according to LCD used.
The LDC output resistance is selected 20/200kΩ (RSEL) during initial.

RSEL	Output low resistance		Output high resistance	
	Segment R_{OS1}	Common R_{OC1}	Segment R_{OS2}	Common R_{OC2}
0	20kΩ		200kΩ	
1	10kΩ		70kΩ	

Note. The output resistance shows Typ. values (Topr = 25°C, VDD = 5V)

Figure 3-5. Selection of LCD output resistance

3.4.3 LCD display operation

(1) Display data setting

Display data are stored to the display data area (Max 32 words) in the data memory (bank0).
The display data stored to the display data area (address 20-3F_H) are read automatically and sent to the LCD driver by the hardware.
The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display data area with a program. The table look up instruction is mainly used for this overwriting.
Figure 3-14 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".
The number of segment which can be driven differs depending on the LCD drive method therefore, the number of display data area bits used to store the data also differs. Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.

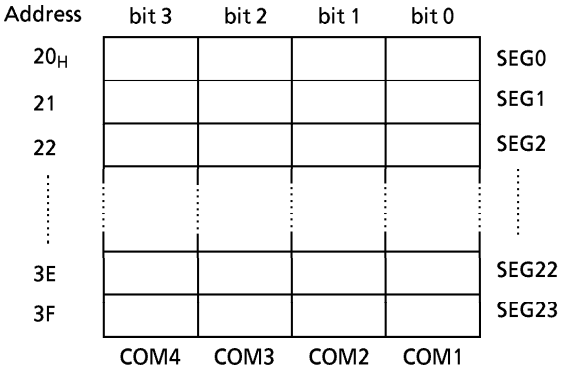


Figure 3-14. LCD Display Data Area (Bank 0)

Driving methods	bit 3	bit 2	bit 1	bit 0
1 / 4 Duty	COM4	COM3	COM2	COM1
1 / 3 Duty	–	COM3	COM2	COM1
1 / 2 Duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. – ; This bit is not used for display data.

Table 3-6. Drivinig Method and Bit for Display Data

(2) Blanking

Blanking is applied by setting EDSP to "0" and turns off the LCD by outputting the non light operation level to the COM pin.

The SEG pin continuously outputs the signal level in accordance with the display data and drive method.

With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

3.4.4 Control method of LCD driver

(1) Initial Setting

Flow chart of intial setting are as shown in Figure 3-15.

Example : When operating the 47C623/823 with 1/4 duty LCD using a from frequency of fc/2^{16} [HZ] .

```
LD      A, #0000B  ;  Sets the 1/4 duty drive
OUT     A, %OP1B
LD      A, #0010B  ;  Setting of base frequency
OUT     A, %OP1A
  ⋮                ;  Setting of clear or intial value of
  ⋮                   display area in the data memory
LD      A, #1000B  ;  Display enable
OUT     A, %OP1B
  ⋮
```

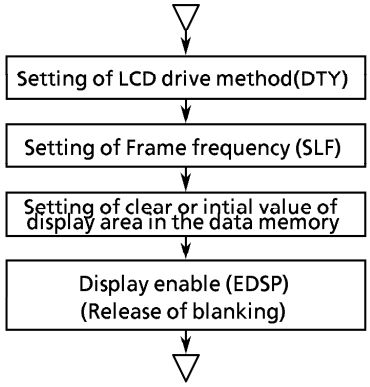


Figure 3-15. Intial setting of LCD driver

(2) Store of display data

Normally, display data are kept permanently in the program memory and are then stored to the display data area by the table look-up instruction.

This can be explained using numerical display with 1/4 duty LCD as an example. The COM and SEG connections to the LCD are the same as those shown in Figure 3-16 and the display data are as shown in Table 3-7. Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below.

```
        LD        HL,  #0FCH      ; To set the DC
        LD        A,   10H
        ST        A,   @HL+
        ST        #DTBL / 16,@HL+
        ST        #DTBL / 256,@HL+
        LD        HL,  #20H       ; Store of display data
        LDL       A,   @DC
        ST        A,   @HL+
        LDH       A.   @DC+
        ST        A,   @HL+
         ⋮
DTBL  :DATA       11011111B,   00000110B,
                  11100011B,   10100111B,
                  00110110B,   10110101B,
                  11110101B,   00010111B,
                  11110111B,   10110111B
```

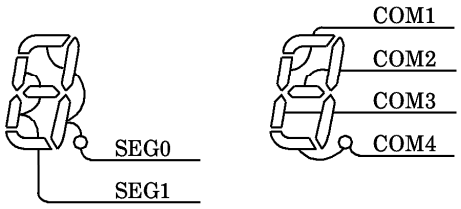


Figure 3-16. Example of COM and SEG connections

Numeral	Display	Display data		Numeral	Display	Display data	
		Upper	Lower			Upper	Lower
0		1101	1111	5		1011	0101
1		0000	0110	6		1111	0101
2		1110	0011	7		0001	0111
3		1010	0111	8		1111	0111
4		0011	0110	9		1011	0111

Table 3-7. Example of display data (1 / 4 Duty LCD)

Table 3-8 shows the same numerical display used in Table 3-7, but using 1/2 duty LCD. The connections of the COM and SEG pins to the LCD are the same as those shown in Figure 3-17.

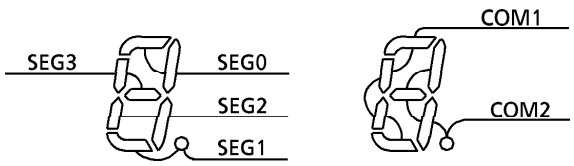


Figure 2-17 Example of COM and SEG Connections

Numeral	Display data				Numeral	Display data			
	Upper		Lower			Upper		Lower	
0	**01	**11	**01	**11	5	**11	**10	**01	**01
1	**00	**10	**00	**10	6	**11	**11	**01	**01
2	**10	**01	**01	**11	7	**01	**10	**00	**11
3	**10	**10	**01	**11	8	**11	**11	**01	**11
4	**11	**10	**00	**10	9	**11	**10	**01	**11

Note. ** ; don't care*

Table 3-8. Example of display data (1 / 2 Duty LCD)

(3) Example of drive output

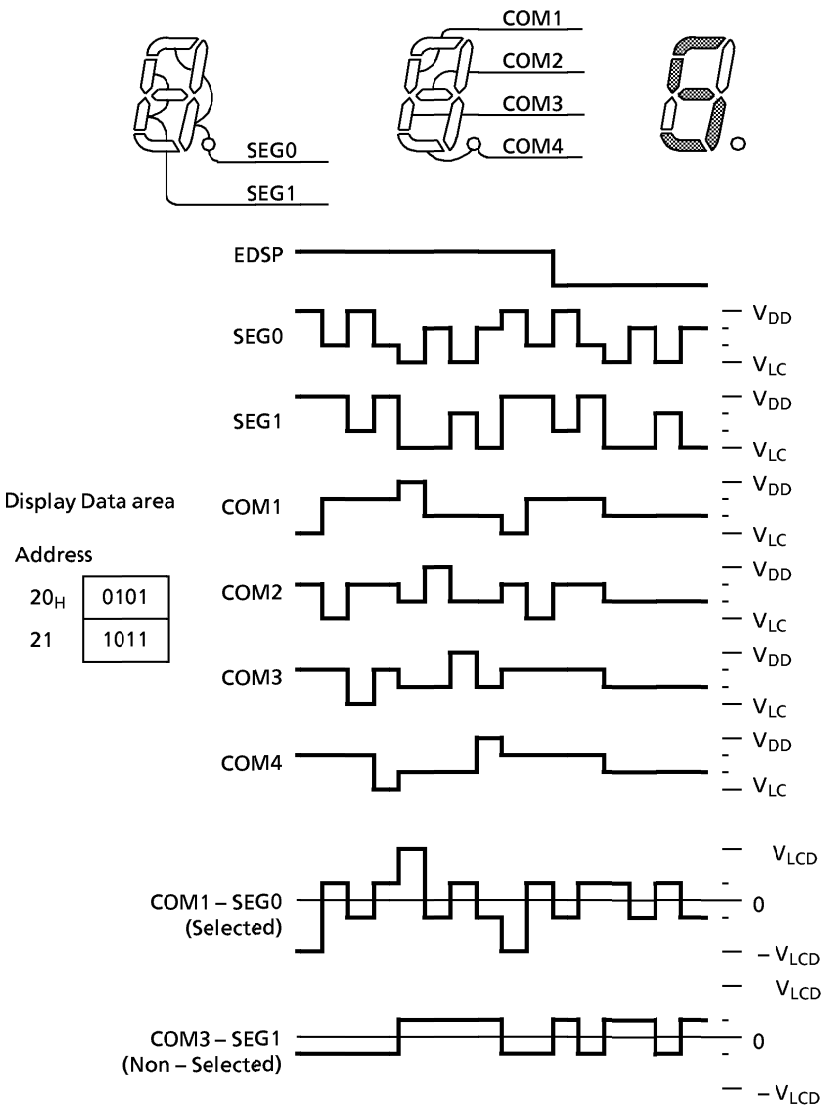


Figure 3-18. 1/4 Duty (1/3 Bias) Drive

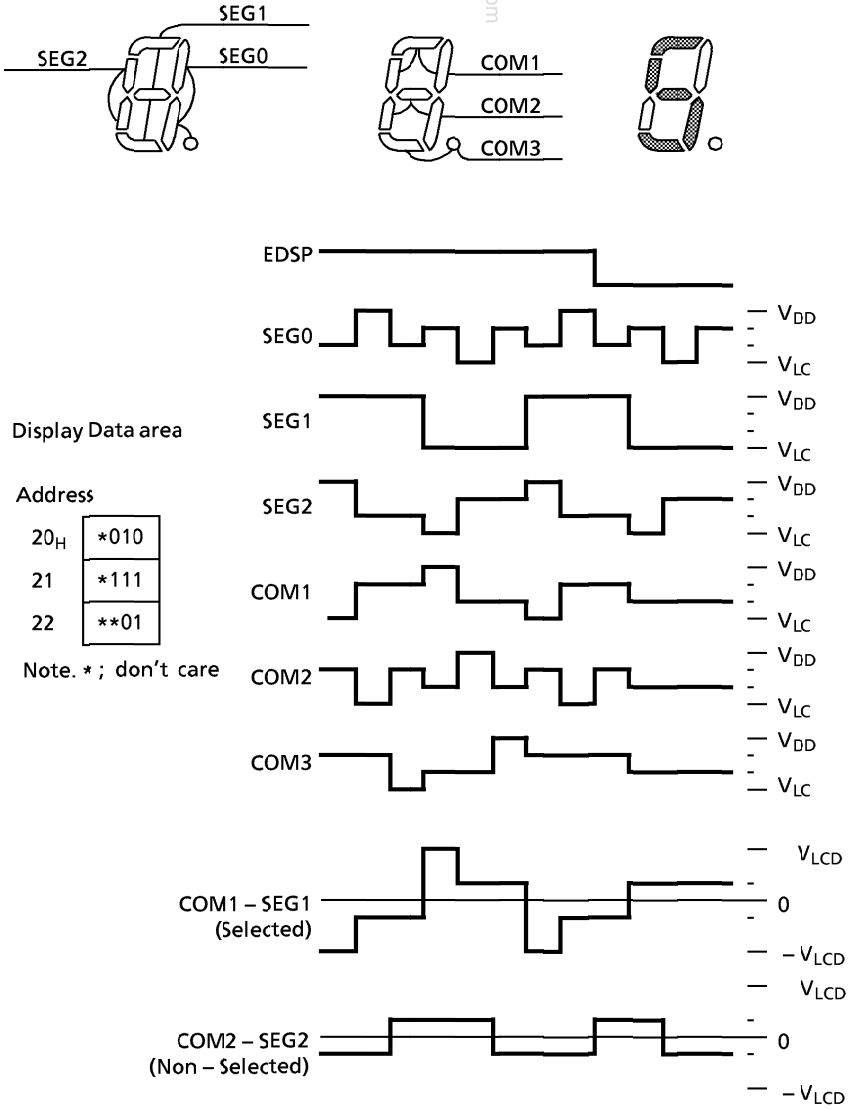


Figure 3-19. 1/3 Duty (1/3 Bias) Drive

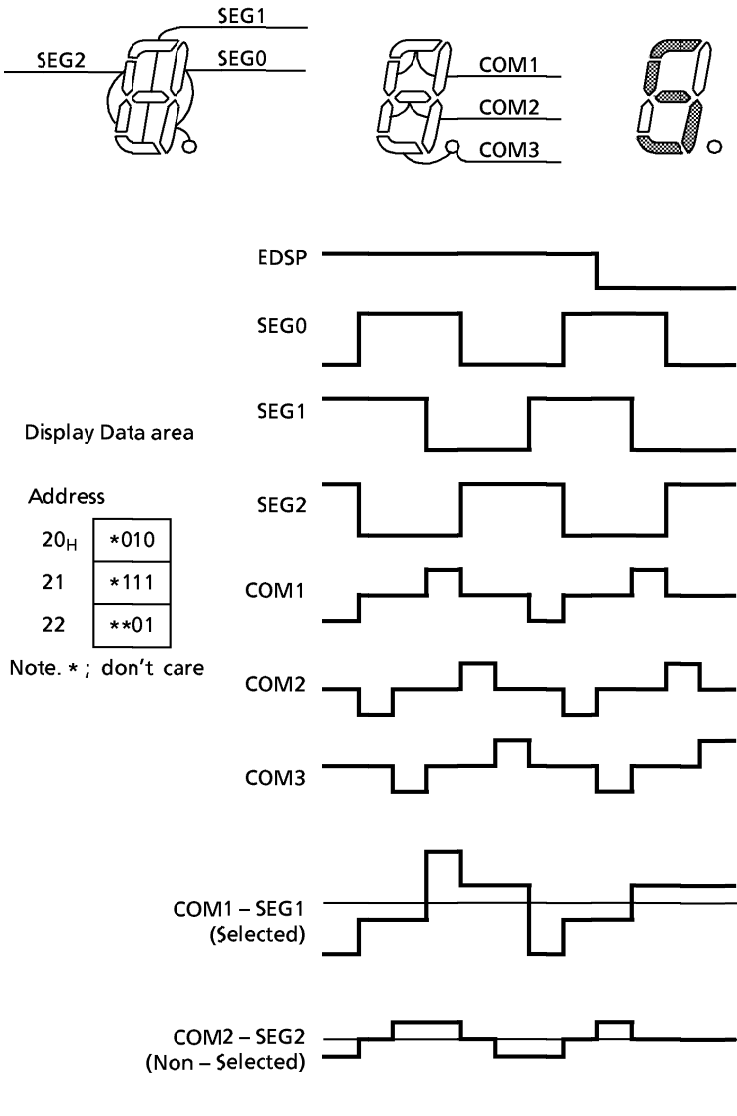


Figure 3-20. 1/3 Duty (1/2 Bias) Drive

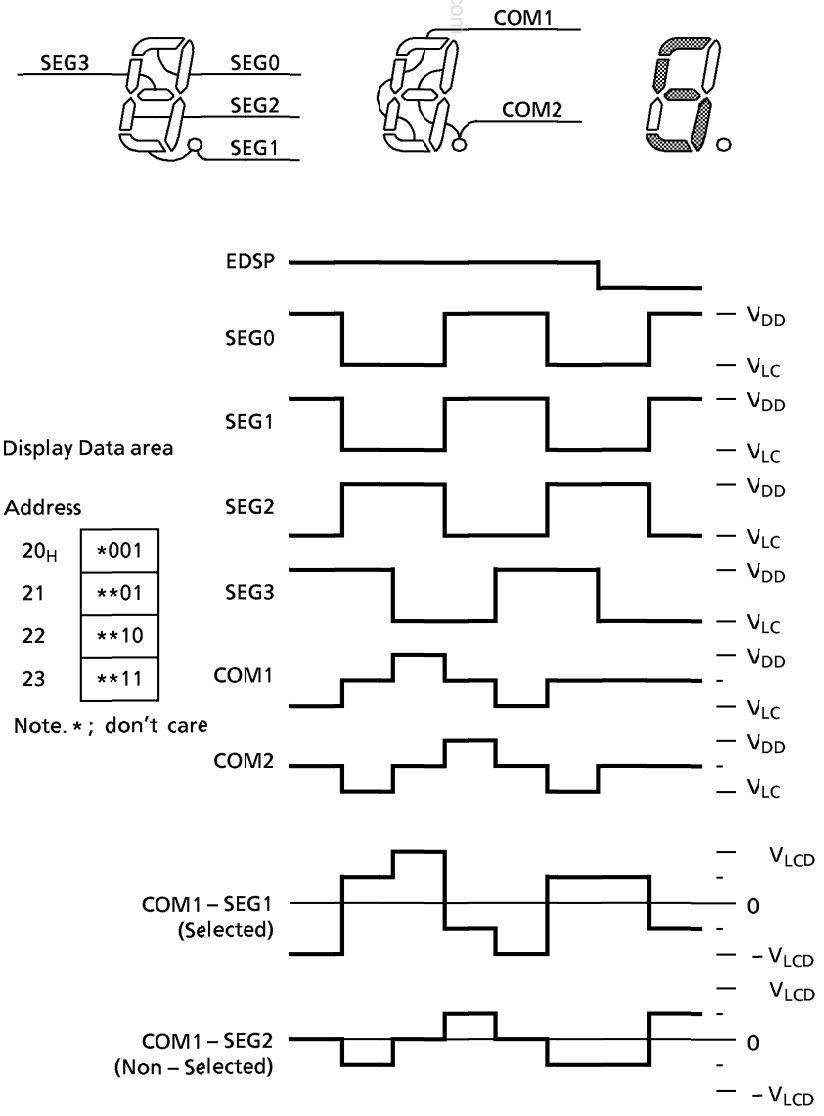
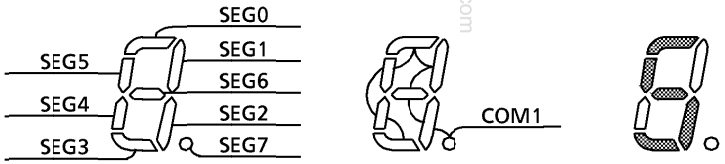


Figure 3-21. 1/2 Duty (1/2 Bias) Drive



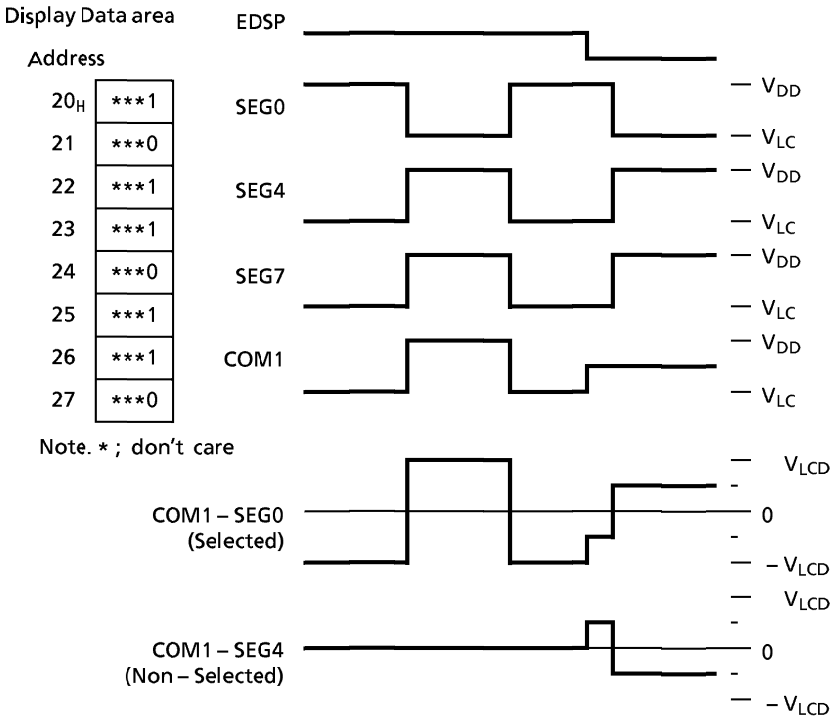


Figure 2-11. Static Drive

INPUT/OUTPUT CIRCUITRY

(1) Control pins
The input/output circuitries of the 47C623/823 control pins are similar to those of the 47C1260/1660.

(2) I/O Ports
The input/output circuitries of the 47C623/823 I/O ports are shown as belows, any one of the circuitries can be chosen by a code (GA to GF) as a mask option.

PORT	I/O	IINPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	GA, GD: R GB, GE: VDD, R_{IN}, R GC, GF: R, R_{IN}	Pull-up/pull-down resister R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)
R4	I/O	R	Sink open drain output Initial "Hi-Z" High current I_{OL} = 20mA (typ.) R = 1kΩ (typ.)
R5 R6	I/O	GA, GB, GC: Initial "Hi-Z", R GD, GE, GF: Initial "High", VDD, R	Sink open darin output or push-pull output R = 1kΩ (typ.)
R7	I/O	R	Sink open drain output Initial "Hi-Z" R = 1kΩ (typ.)
R8 R9	I/O	R	Sink open drain output Initial "Hi-Z" Hysteresis input R = 1kΩ (typ.)
R3	I/O	Segment output, disable, R	Sink open drain output or Segment output R = 1kΩ (typ.)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Supply Voltage (LCD drive)	V_{LC}		– 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include ports R7, R3	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin, but include ports R7, R3	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Except port R4	3.2	mA
	I_{OUT2}	Port R4	30	
Output Current (Total)	ΣI_{OUT1}	Port R4	60	mA
Power Dissipation [T_{opr} = 50°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode (fc = 4.2MHz)	2.7	6.0	V
			In the Normal mode (fc = 5.0MHz) Note2	2.9		
			In the Normal mode (fc = 6.0MHz)	4.5		
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT	High freq. $V_{DD} \geqq 2.7V$	0.4	4.2	MHz
			High freq. $V_{DD} \geqq 2.9V$ Note2		5.0	
			High freq. $V_{DD} \geqq 4.5V$		6.0	
	fs	XTIN, XTOUT	Low freq.	30.0	34.0	kHz

Note1. Input Voltage V_{IH3}, V_{IL3} : in the SLOW and HOLD mode.
Note2. Operating Temperature – 30 to 50°C

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Open drain R port					
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Registance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain port R	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Output Low Current	I_{OL}	Ports R4	V_{DD} = 4.5V, V_{OL} = 1.0V	15	20	—	mA
Segment Output Low Registance	R_{OS1}	SEG pin	V_{DD} = 5V, V_{DD} – V_{LC} = 3V	—	10/20	—	kΩ
Common Output Low Registance	R_{OC1}	COM pin					
Segment Output High Resistance	R_{OS2}	SEG pin		—	70 /200	—	kΩ
Common Output High Resistance	R_{OC2}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, V_{LC} = V_{SS} fc = 4MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, V_{LC} = V_{SS} fs = 32.768kHz	—	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. $V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.

Note 6. $V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 7. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.
Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).

Note 8. When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.

Note 9. Times for SEG / COM output resistance switching on :
R_{OS1}, R_{OC1} : 2/fs (s)
R_{OS2}, R_{OC2} : 1/(n · f_F) (1/n : duty, f_F : frame frequency)

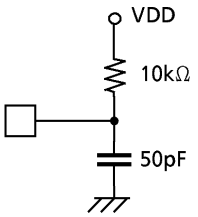
A.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = – 40 to 70°C)

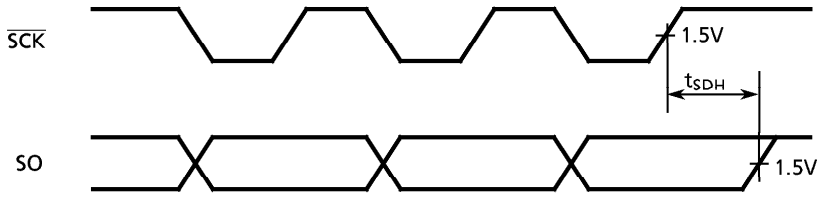
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.3	–	20	μs
		in the SLOW mode	235	–	267	μs
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns
High Speed Timer/Counter input frequency	f_{HT}	ECIN input	–	–	fc	MHz

Note. Shift data Hold time :

External circuit for $\overline{SCK}$ pin and SO pin



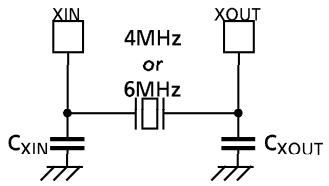
Serial port (completion of transmission)



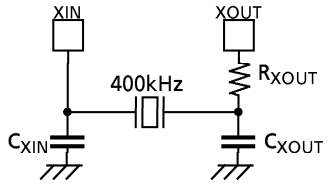
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, T_{opr} = – 40 to 70°C)

(1) 6MHz
Ceramic Resonator
CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF

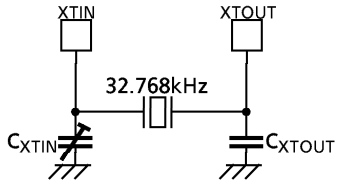


(2) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
FCR-4.0M5 (TDK) $C_{XIN} = C_{XOUT}$ = 33pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF



(3) 400kHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8kΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10kΩ

(4) 32.768kHz (V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 70°C)
Crystal Oscillator C_{XTIN}, C_{XTOUT} ; 10 to 33pF



Note : In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

TYPICAL CHARACTERISTICS