Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF80N20 Series

80 AMP , 200 Volts, 25 mΩ Avalanche Rated N-channel MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information [1/]

SFF80N20

Screening [2/]
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

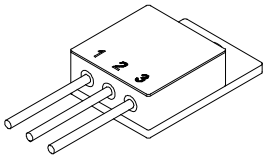
Lead Option [3/]
__ = Straight Leads
DB = Down Bend
UB = Up Bend

Package [3/ 4/]
M = TO-254
Z = TO-254Z
N = TO-258
P = TO-259

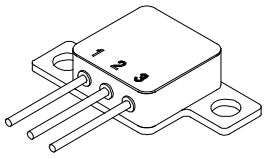
Features:
- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings [5/]		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	200	V
Gate – Source Voltage	continuous transient	V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited)	@ T_C = 25ºC	I_{D1}	55	A
Max. Instantaneous Drain Current (Tj limited)	@ T_C = 25ºC @ T_C = 175ºC	I_{D2} I_{D3}	80 48	A
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	60	A
Single and Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS} E_{AR}	1500 50	mJ
Total Power Dissipation	@ T_C = 25ºC	P_D	150	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +175	ºC
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	1.0 (typ.0.75)	ºC/W

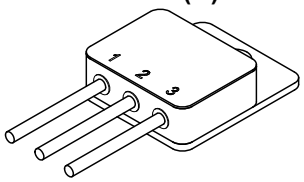
TO-254 (M)



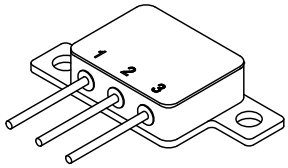
TO-254Z (Z)



TO-258 (N)



TO-259 (P)



NOTES:
*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ For lead bending options / pinout configurations - contact factory.
4/ Maximum current limited by package configuration
5/ Unless otherwise specified, all electrical characteristics @25°C.

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Electrical Characteristics[5/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	BV_{DSS}	200	220	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 48A, Tj= 25°C	$R_{DS(on)}$	—	25	30	mΩ
	V_{GS} = 10V, I_D = 48A, Tj=125°C		—	50	65	
	V_{GS} = 10V, I_D = 48A, Tj= 175°C		—	65	—	
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 4.0mA, Tj= 25°C	$V_{GS(th)}$	2.5	4.5	5.0	V
	V_{DS} = V_{GS}, I_D = 4.0mA, Tj= 125°C		1.5	3.6	—	
	V_{DS} = V_{GS}, I_D = 4.0mA, Tj= -55°C		—	5	6	
Gate to Source Leakage	V_{GS} = ±20V, Tj= 25°C	I_{GSS}	—	10	±100	nA
	V_{GS} = ±20V, Tj= 125°C		—	30	—	
Zero Gate Voltage Drain Current	V_{DS} = 200V, V_{GS} = 0V, T_j = 25°C	I_{DSS}	—	0.01	25	µA
	V_{DS} = 200V, V_{GS} = 0V, T_j = 125°C		—	2.5	150	µA
	V_{DS} = 200V, V_{GS} = 0V, T_j = 150°C		—	25	—	µA
Forward Transconductance	V_{DS} = 10V, I_D = 48A, T_j = 25°C	g_{fs}	25	50	—	Mho
Total Gate Charge	V_{GS} = 10V	Q_g	—	150	250	nC
Gate to Source Charge	V_{DS} = 100V	Q_{gs}	—	45	65	
Gate to Drain Charge	I_D = 48A	Q_{gd}	—	75	120	
Turn on Delay Time	V_{GS} = 10V	$t_{d(on)}$	—	50	75	nsec
Rise Time	V_{DS} = 100V	t_r	—	50	75	
Turn off Delay Time	I_D = 48A	$t_{d(off)}$	—	110	135	
Fall Time	R_G = 4.0Ω, pw= 3us	t_f	—	50	75	
Diode Forward Voltage	I_F = 48A, V_{GS} = 0V	V_{SD}	—	0.90	1.5	V
Diode Reverse Recovery Time	I_F = 10A, di/dt = 100A/usec	t_{rr1}	—	190	250	nsec
	I_F = 10A, di/dt = 100A/usec	I_{rm1}	—	11	—	A
	I_F = 10A, di/dt = 100A/usec	Q_{rr1}	—	1	—	µC
Reverse Recovery Charge	I_F = 25A, di/dt = 100A/usec	t_{rr2}	—	310	—	nsec
	I_F = 25A, di/dt = 100A/usec	I_{rm2}	—	17	—	A
	I_F = 25A, di/dt = 100A/usec	Q_{rr2}	—	2.5	—	µC
Input Capacitance	V_{GS} = 0V	C_{iss}	—	5300	—	pF
Output Capacitance	V_{DS} = 25V	C_{oss}	—	1050	—	
Reverse Transfer Capacitance	f = 1 MHz	C_{rss}	—	175	—	

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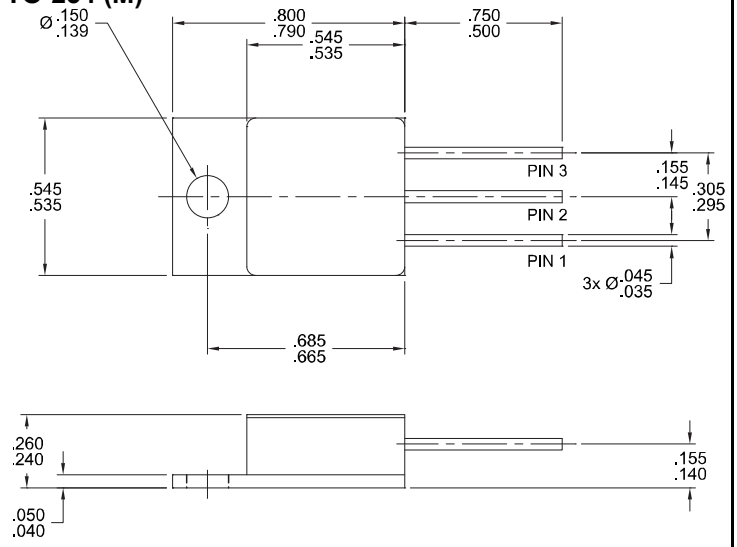
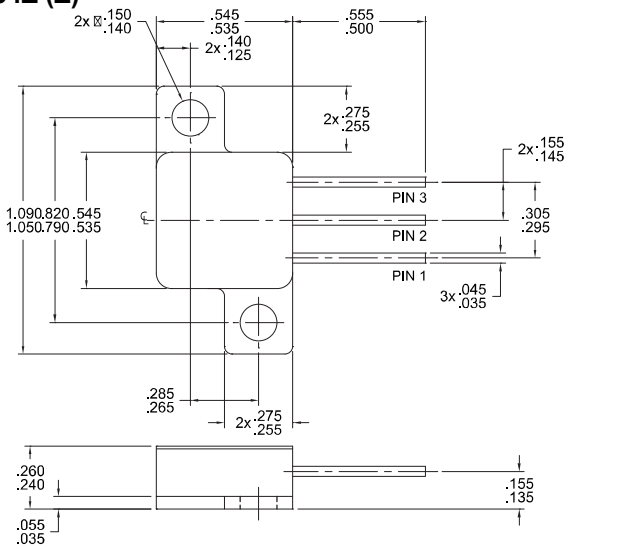
TO-254 (M)



TO-254Z (Z)



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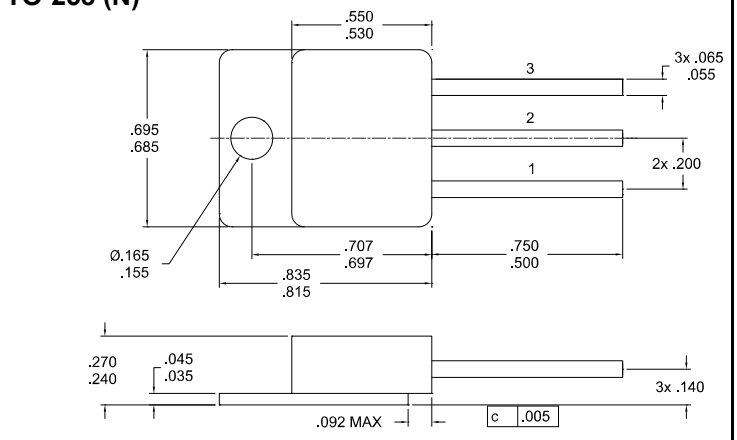
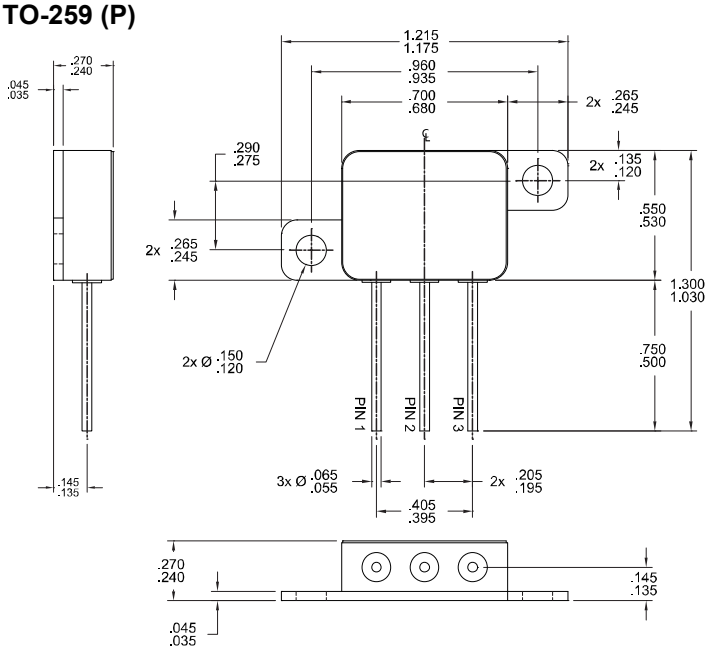


TOLERANCES ARE ±.005 UNLESS OTHERWISE SPECIFIED

TO-259 (P)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3
TO-258 (N)	Pin 1	Pin 2	Pin 3
TO-259 (P)	Pin 1	Pin 2	Pin 3