

## 8M-Bit (1Mx8) CMOS MASK ROM

### FEATURES

- 1,048,576 x 8 bit organization
- Fast access time
  - 3.3V Operation : 100ns(max.)
  - 3.0V Operation : 120ns(max.)
- Supply voltage : 2.7V to 3.6V
- Current consumption
  - Operating : 30/25mA(max.)
  - Standby : 30 $\mu$ A(max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
  - KM23V8000D : 32-DIP-600
  - KM23V8000DG : 32-SOP-525

### GENERAL DESCRIPTION

The KM23V8000D(G) is a fully static mask programmable ROM organized 1,048,576 x 8 bit. It is fabricated using silicon gate CMOS process technology.

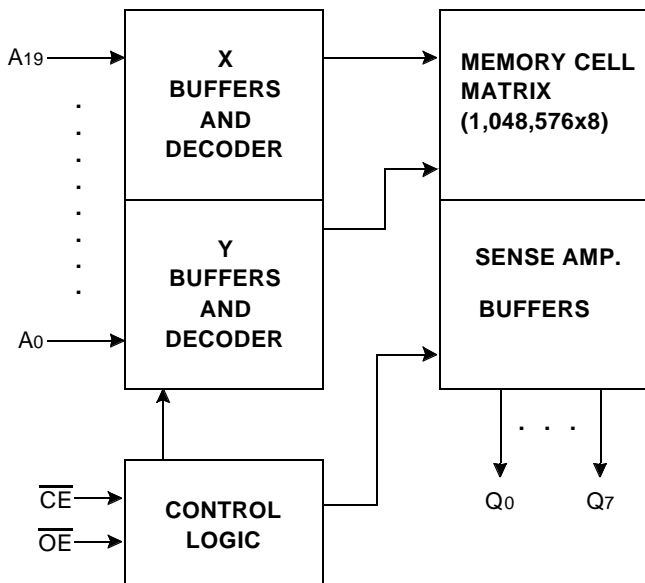
This device operates with 2.7V to 3.6V power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

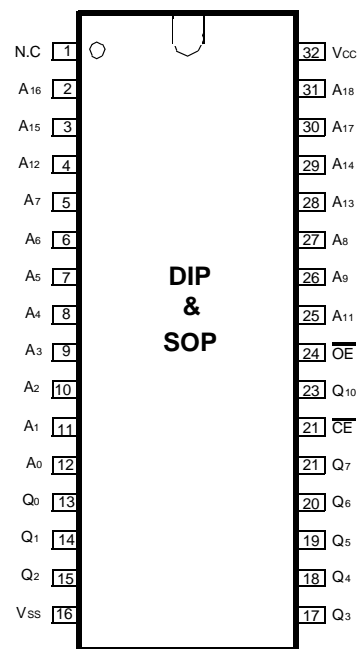
It is suitable for use in program memory of microprocessor, and data memory, character generator.

The KM23V8000D is packaged in a 32-DIP and the KM23V8000DG in a 32-SOP.

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION



KM23V8000D(G)

| Pin Name        | Pin Function   |
|-----------------|----------------|
| A0 - A19        | Address Inputs |
| Q0 - Q7         | Data Outputs   |
| $\overline{CE}$ | Chip Enable    |
| $\overline{OE}$ | Output Enable  |
| Vcc             | Power          |
| Vss             | Ground         |
| N.C             | No Connection  |

**ABSOLUTE MAXIMUM RATINGS**

| Item   | Symbol            | Rating       | Unit |
|--|-------------------|--------------|------|
| Voltage on Any Pin Relative to V <sub>SS</sub> | V <sub>IN</sub>   | -0.3 to +4.5 | V    |
| Temperature Under Bias                         | T <sub>BIAS</sub> | -10 to +85   | °C   |
| Storage Temperature                            | T <sub>Stg</sub>  | -55 to +150  | °C   |

**NOTE** : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage reference to V<sub>SS</sub>, T<sub>A</sub> = 0 to 70°C)

| Item           | Symbol          | Min     | Typ     | Max     | Unit |
|----------------|-----------------|---------|---------|---------|------|
| Supply Voltage | V <sub>CC</sub> | 2.7/3.0 | 3.0/3.3 | 3.3/3.6 | V    |
| Supply Voltage | V <sub>SS</sub> | 0       | 0       | 0       | V    |

**DC CHARACTERISTICS**

| Parameter                      | Symbol           | Test Conditions  | Min                         | Max                  | Unit |    |
|--------------------------------|------------------|--|-----------------------------|----------------------|------|----|
| Operating Current              | I <sub>CC</sub>  | $\overline{CE}=\overline{OE}=V_{IL}$<br>all outputs open | V <sub>CC</sub> =3.3V ±0.3V | -                    | 30   | mA |
|                                |                  |  | V <sub>CC</sub> =3.0V ±0.3V | -                    | 25   | mA |
| Standby Current(TTL)           | I <sub>SB1</sub> | $\overline{CE}=V_{IH}$ , all outputs open                | -                           | 500                  | µA   |    |
| Standby Current(CMOS)          | I <sub>SB2</sub> | $\overline{CE}=V_{CC}$ , all outputs open                | -                           | 30                   | µA   |    |
| Input Leakage Current          | I <sub>LI</sub>  | V <sub>IN</sub> =0 to V <sub>CC</sub>                    | -                           | 10                   | µA   |    |
| Output Leakage Current         | I <sub>LO</sub>  | V <sub>OUT</sub> =0 to V <sub>CC</sub>                   | -                           | 10                   | µA   |    |
| Input High Voltage, All Inputs | V <sub>IH</sub>  |  | 2.0                         | V <sub>CC</sub> +0.3 | V    |    |
| Input Low Voltage, All Inputs  | V <sub>IL</sub>  |  | -0.3                        | 0.6                  | V    |    |
| Output High Voltage Level      | V <sub>OH</sub>  | I <sub>OH</sub> = -400µA                                 | 2.4                         | -                    | V    |    |
| Output Low Voltage Level       | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1mA                                  | -                           | 0.4                  | V    |    |

**NOTE** : Minimum DC Voltage(V<sub>IL</sub>) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input pins(V<sub>IH</sub>) is V<sub>CC</sub>+0.3V which, during transitions, may overshoot to V<sub>CC</sub>+2.0V for periods <20ns.

**MODE SELECTION**

| $\overline{CE}$ | $\overline{OE}$ | Mode      | Data   | Power   |
|-----------------|-----------------|-----------|--------|---------|
| H               | X               | Standby   | High-Z | Standby |
| L               | H               | Operating | High-Z | Active  |
|                 | L               | Operating | Dout   | Active  |

**CAPACITANCE** ( T<sub>A</sub> =25°C, f=1.0MHz)

| Item               | Symbol           | Test Conditions      | MIN | Max | Unit |
|--------------------|------------------|----------------------|-----|-----|------|
| Output Capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> =0V | -   | 12  | pF   |
| Input Capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> =0V  | -   | 12  | pF   |

**NOTE** : Capacitance is periodically sampled and not 100% tested.

## AC CHARACTERISTICS (TA = 0°C to +70°C, VCC = 3.3V/3.0V ± 0.3V, unless otherwise noted.)

### TEST CONDITIONS

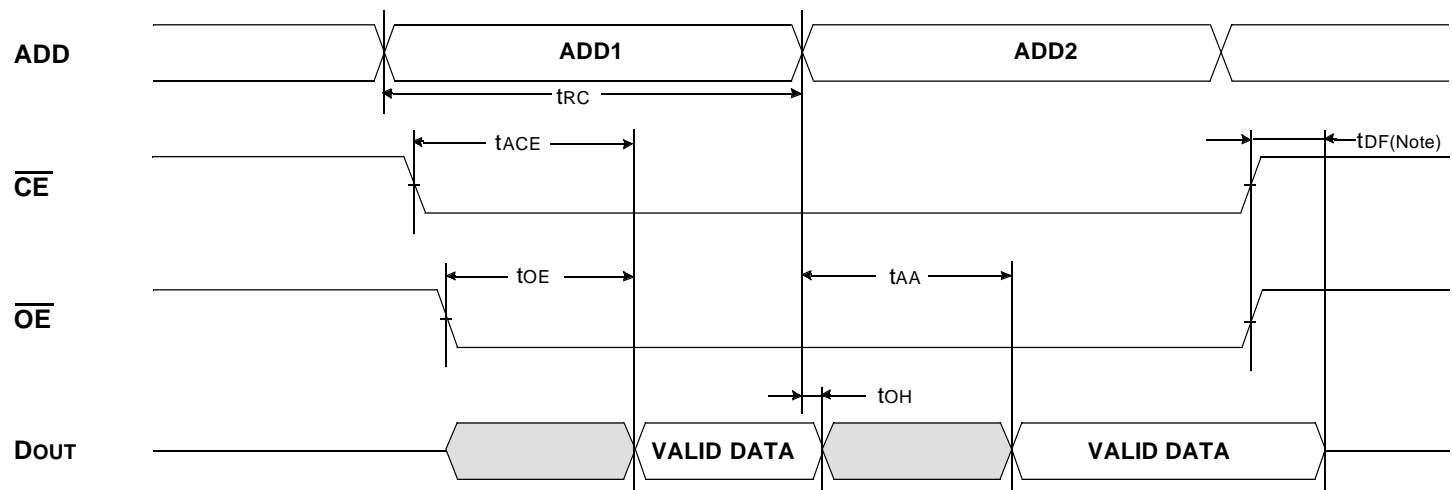
| Item                           | Value                   |
|--------------------------------|-------------------------|
| Input Pulse Levels             | 0.45V to 2.4V           |
| Input Rise and Fall Times      | 10ns                    |
| Input and Output timing Levels | 1.5V                    |
| Output Loads                   | 1 TTL Gate and CL=100pF |

### READ CYCLE

| Item                                    | Symbol | VCC=3.3V ± 0.3V |     | VCC=3.0V ± 0.3V |     | Unit |
|---|--------|-----------------|-----|-----------------|-----|------|
|   |        | Min             | Max | Min             | Max |      |
| Read Cycle Time                         | tRC    | 100             |     | 120             |     | ns   |
| Chip Enable Access Time                 | tACE   |                 | 100 |                 | 120 | ns   |
| Address Access Time                     | tAA    |                 | 100 |                 | 120 | ns   |
| Output Enable Access Time               | tOE    |                 | 50  |                 | 60  | ns   |
| Output or Chip Disable to Output High-Z | tDF    |                 | 20  |                 | 20  | ns   |
| Output Hold from Address Change         | tOH    | 0               |     | 0               |     | ns   |

### TIMING DIAGRAM

#### READ



**NOTE :** tDF is defined as the time at which the outputs achieve the open circuit condition and is not referenced to VOH or VOL level.