CLRC663

Contactless reader IC

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Preliminary data sheet
PUBLIC

1. Introduction

Remark: The information contained in this data sheet is to provide a preview of the contactless reader IC and must be regarded as a provisional advance specification. The complete overview will soon be available in a new revision.

This document describes the functionality and electrical specifications of the contactless reader/writer IC CLRC663.

2. General description

The CLRC663 is a highly integrated transceiver IC for contactless communication at 13.56 MHz. This transceiver IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

The CLRC663 transceiver ICs support the following operating modes

- read/write mode supporting ISO/IEC 14443A/MIFARE
- read/write mode supporting ISO/IEC 14443B
- read/write mode supporting JIS X 6319-4 (comparable with FeliCa[1] (see Section 30.5) scheme)
- passive initiator mode according to ISO/IEC 18092
- read/write mode supporting ISO/IEC 15693
- read/write mode supporting ICODE EPC UID/ EPC OTP
- read/write mode supporting ISO/IEC 18000-3 Mode 3

The CLRC663's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO 14443A/MIFARE compatible cards and transponders. The digital module manages the complete ISO 14443A framing and error detection functionality (parity and CRC).

The CLRC663 supports MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE Ultralight C, MIFARE PLUS and MIFARE DESFire products. The CLRC663 supports contactless communication and uses the MIFARE higher transfer speeds of up to 848 kbit/s in both directions.

1. In the following the word FeliCa is used for JIS X 6319-4

The CLRC663 supports all layers of the ISO/IEC 14443B reader/writer communication scheme provided that:

- additional components, such as oscillators, power supplies and coils etc. are correctly implemented
- standard protocols are used, such as ISO/IEC 14443-4 and/or ISO/IEC 14443B anticollision

The use of this NXP IC according to ISO/IEC 14443B could infringe upon third party patent rights. Consequently, a purchaser must ensure that the appropriate third party patent licenses are obtained.

When the CLRC663 transceiver IC is enabled in the read/write mode for FeliCa, it supports the FeliCa communication scheme. The receiver part provides the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection such as CRC. The CLRC663 supports contactless communication using FeliCa higher transfer speeds of up to 424 kbit/s in both directions.

The CLRC663 accommodates future development by supporting the P2P passive initiator mode in accordance with ISO/IEC 18092.

The CLRC663 supports vicinity protocol according ISO/IEC15693, EPC UID and ISO/IEC 18000-3 mode 3. The complete vicinity product family of NXP is supported and enable a readability for mid-ranger reader applications

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependent on pin voltage supply)
- I^2C-bus interface (two version are implemented: I2C and I2CL)

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE, ISO/IEC 14443 B and FeliCa, P2P passive initiator mode in accordance with ISO/IEC 18092
- Supports ISO/IEC15693, ICODE EPC UID and ISO/IEC 18000-3 Mode 3
- Typical operating distance in read/write mode for communication to a ISO/IEC 14443A/MIFARE up to 12 cm depending on the antenna size and tuning
- Supports MIFARE Classic encryption in read/write mode
- Supports higher transfer speed communication up to 848 kbit/s
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - Two I^2C-bus interfaces up to 400 kBd in Fast mode, up to 1000 kBd in Fast mode plus
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependent on pin voltage supply
- FiFo buffer handles 512 byte send and receive

- Flexible interrupt modes
- Hard Power Down
- Standby mode
- Programmable and cascadable timers
- Oscillator circuit for connection to 27.12 MHz quartz crystal
- 3.3 V to 5 V power supply with Integrated voltage regulators for 1.8 V Analog and Digital Core Supplies
- Free programmable I/O pins (GPIO0/SIGIN; SIGOUT)
- IntegerN PLL providing clock for standard microcontroller used frequencies
- Low power card detection
- Boundary Scan Interface
- Integrated Free-Running Low Power Oscillator
- True Random Number Generator

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			3	5	5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage		[1]	3	5	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage			3	5	5.5	V
I_{pd}	power-down current	PDOWN pin pulled HIGH	[2]		8	40	nA
I_{VDD}	supply current				17	20	mA
$I_{DD(TVDD)}$	TVDD supply current		[3][4][5]		100	200	mA
T_{amb}	ambient temperature			−25		+85	°C

[1] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DD}.

[2] I_{pd} are the total currents over all supplies.

[3] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuitry connected to TX1 and TX2.

[4] During typical circuit operation, the overall current is below 100 mA.

[5] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
CLRC66301HN1/TRAYB[1]	HVQFN33	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
CLRC66301HN1/TRAYBM[2]			

[1] Delivered in one tray.

[2] Delivered in five trays.

6. Block diagram

The analog interface handles the modulation and demodulation of the antenna signals for the contactless interface.

The contactless UART manages the protocol dependency of the contactless interface settings managed by the host. The FiFo buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

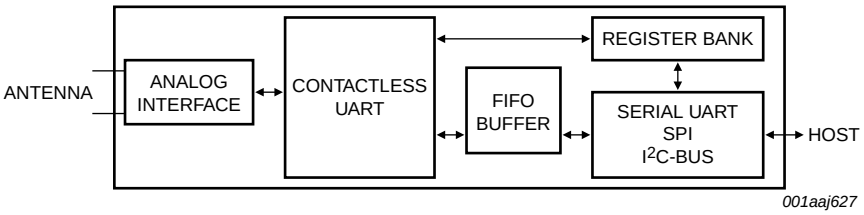


Fig 1. Simplified block diagram of the CLRC663

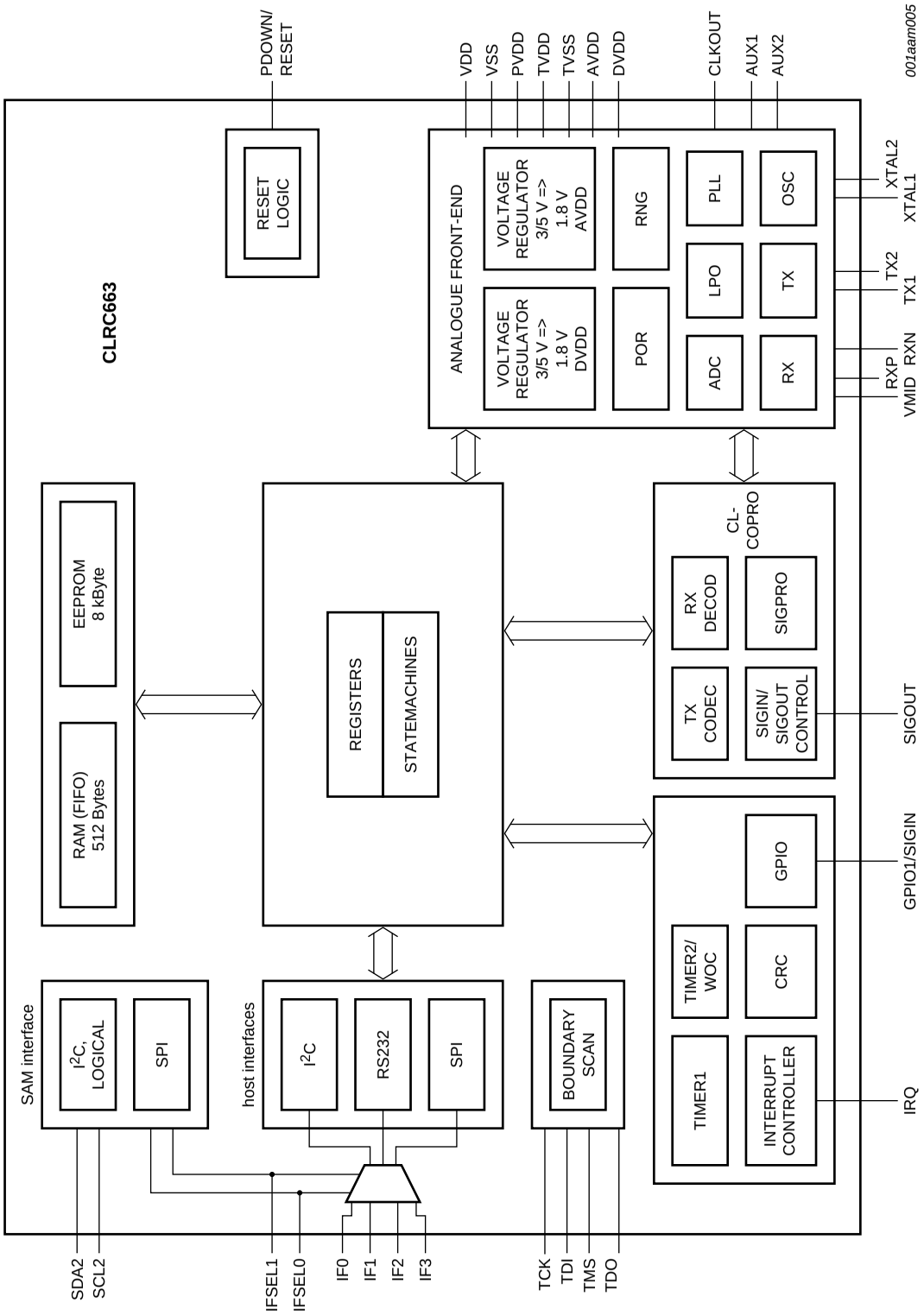


Fig 2. Detailed block diagram of the CLRC663

7. Pinning information

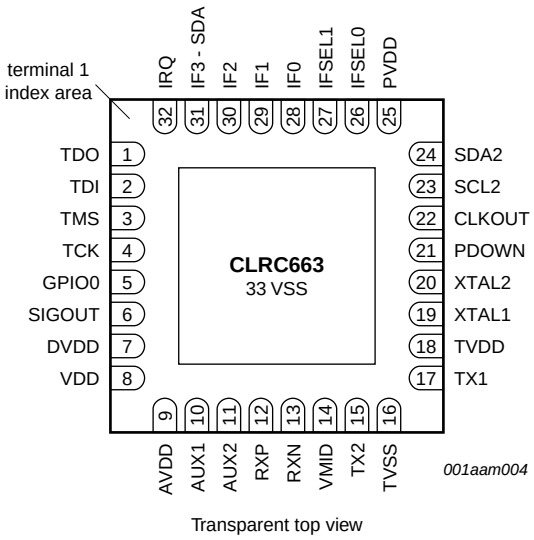


Fig 3. Pinning configuration HVQFN33 (SOT617-1) V_{SS} on heatsink

7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type	Description
1	TDO	O	test data output for boundary scan interface
2	TDI	I	test data input boundary scan interface
3	TMS	I/O	test mode select boundary scan interface
4	TCK	I	test clock boundary scan interface
5	GPIO0/SIGIN	I/O	general purpose I/O
6	SIGOUT	O	analog signal output
7	DVDD	O	digital power supply buffer
8	VDD	PWR	power supply
9	AVDD	O	analog power supply buffer
10	AUX1	O	auxiliary outputs: Pin is used for analog test signal
11	AUX2	O	auxiliary outputs: Pin is used for analog test signal
12	RXP	I	receiver input pin for the received RF signal.
13	RXN	I	receiver Input pin for the received RF signal.
14	VMID	I/O	internal receiver reference voltage
15	TX2	O	transmitter 1: delivers the modulated 13.56 MHz carrier
16	TVSS	PWR	transmitter Ground
17	TX1	O	transmitter 2: delivers the modulated 13.56 MHz carrier
18	TVDD	PWR	transmitter voltage supply
19	XTAL1	I	oscillator input
20	XTAL2	I	oscillator input

Table 3. Pin description *...continued*

Pin	Symbol	Type	Description
21	PDOWN/RESET	I	Reset and power-down: When HIGH, internal voltage regulator is switched off, the oscillator is stopped, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts. Refer to Table 1 “Quick reference data”
22	CLKOUT	O	clock output.
23	SCL2	O	Serial Clock line[1]
24	SDA2	I	Serial Data Line[1]
25	PVDD	I/O	pad power supply
26	IFSEL0	I/O	interface selection 0
27	IFSEL1	I/O	interface selection 1
28	IF0	I/O	interface pin[1]
29	IF1	I/O	interface pin[1]
30	IF2	I/O	interface pin[1]
31	IF3 - SDA	I/O	interface pin[1]
32	IRQ	O	interrupt request: output to signal an interrupt event
33	Vss	PWR	ground and heatsink connection

[1] The pin functionality for the interfaces is explained in Section 10 “DIGITAL interfaces”.

8. Functional description

The CLRC663 has the following read/write operating modes that support:

- ISO/IEC14443A/MIFARE
- ISO/IEC14443B
- FeliCA
- ISO/IEC15693/ICODE
- ICODE EPC UID
- ISO/IEC18000-3 Mode 3

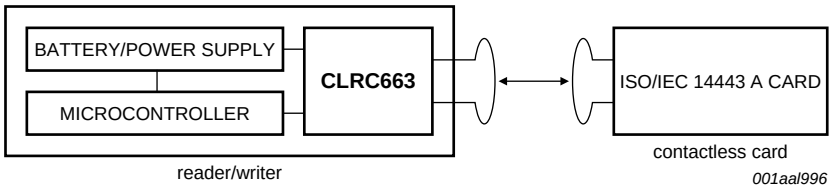
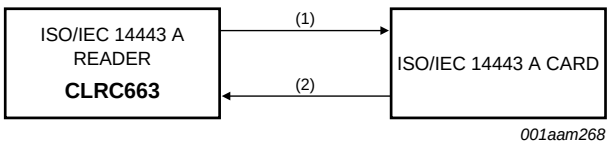


Fig 4. read/write mode

In the read/write mode the CLRC663 enables the communication to a contactless ISO 14443 A/MIFARE, ISO 14443B or FeliCa card. When using this NXP IC according to ISO/IEC 14443B no additional license fees will come up.

8.1 ISO/IEC14443A/MIFARE read/write functionality

The physical level communication is shown in Figure 5.



(1) Reader to Card 100 % ASK, Miller Coded, Transfer speed 106 kbit/s to 848 kbit/s

(2) Card to Reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Fig 5. ISO/IEC 14443 A/MIFARE read/write mode communication diagram

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Reader to card (send data from the CLRC663 to a card) fc = 13.56 MHz	reader side modulation	100 % ASK	ASK	ASK	ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit rate [kbit/s]	fc/128	fc/64	fc/32	fc/16
Card to reader (CLRC663 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	baseband load modulation
	subcarrier frequency	fc / 16	fc / 16	fc / 16	fc / 16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The CLRC663's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. Figure 6 shows the data coding and framing according to ISO/IEC 14443A /MIFARE.

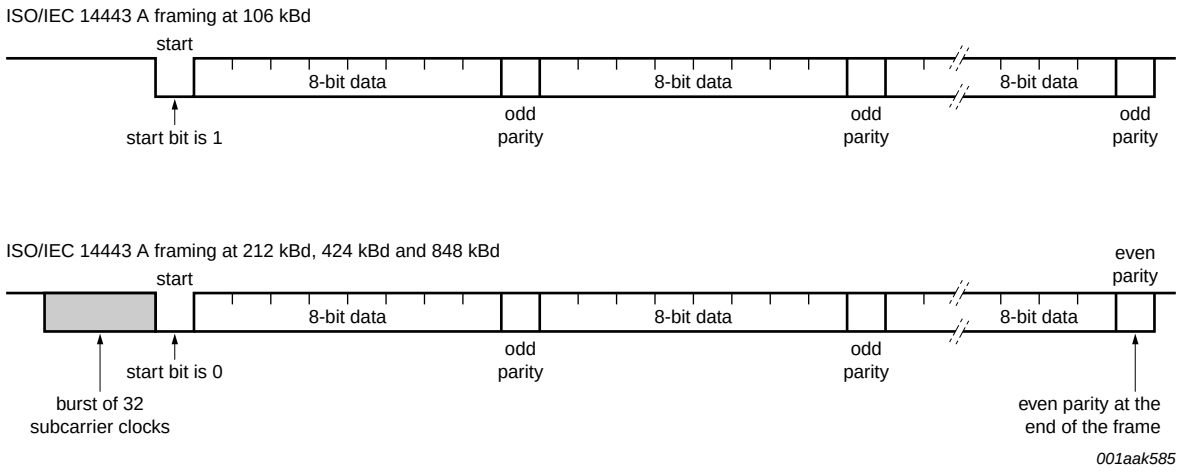
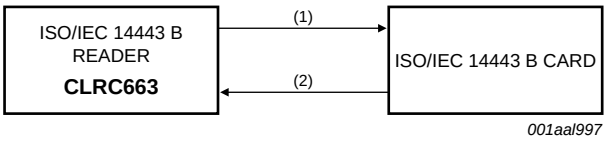


Fig 6. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the TxBitMode register -TxParityEn bit.

8.2 ISO/IEC14443B read/write functionality

The physical level communication is shown in Figure 7.



(1) Reader to Card NRZ, Miller coded, transfer speed 106 kbit/s to 848 kbit/s

(2) Card to reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Fig 7. ISO/IEC 14443 A/MIFARE read/write mode communication diagram

The physical parameters are described in Table 5.

Table 5. Communication overview for ISO/IEC 14443 B reader/writer

Communication direction	Signal type	Transfer speed			
		106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Reader to card (send data from the CLRC663 to a card) fc = 13.56 MHz	reader side modulation	10 % ASK	10 % ASK	10 % ASK	10 % ASK
	bit encoding	NRZ	NRZ	NRZ	NRZ
	bit rate [kbit/s]	128 / fc	64 / fc	32 / fc	16 / fc
Card to reader (CLRC663 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	fc / 16	fc / 16	fc / 16	fc / 16
	bit encoding	BPSK	BPSK	BPSK	BPSK

The contactless UART of CLRC663 and a dedicated external host are required to handle the complete ISO/IEC 14443B protocol. The following Figure 8 “Data coding and framing according to ISO/IEC 14443 B” shows the Data Coding and framing according to ISO/IEC 14443B SOF and EOF.

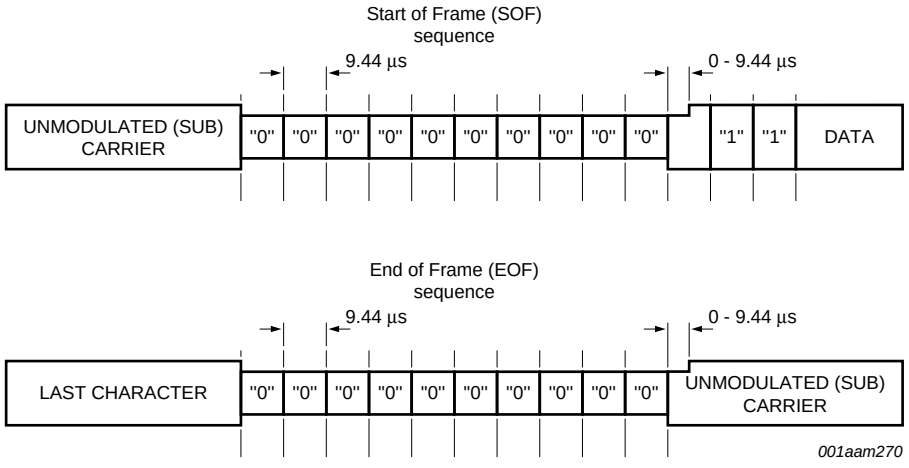


Fig 8. Data coding and framing according to ISO/IEC 14443 B

8.3 Felica read/write functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The communication on a physical level is shown in Figure 9.

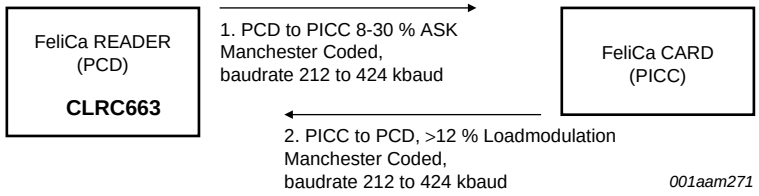


Fig 9. FeliCa read/write communication diagram

The physical parameters are described in Table 6.

Table 6. Communication overview for FeliCa reader/writer

Communication direction	Signal type	Transfer speed FeliCa	FeliCa higher transfer speeds
		212 kbit/s	424 kbit/s
Reader to card (send data from the CLRC663 to a card) fc = 13.56 MHz	reader side modulation	8 to 30 % ASK	8 to 30 % ASK
	bit encoding	Manchester encoding	Manchester encoding
	bit rate	fc/64	fc/31
Card to reader (CLRC663 receives data from a card)	card side load modulation	30/H^1.2 (H = field strength [A/m])	30/H^1.2 (H = field strength [A/m])
	bit encoding	Manchester encoding	Manchester encoding

The contactless UART of CLRC663 and a dedicated external host controller are required to handle the complete FeliCa protocol.

8.3.1 FeliCa framing and coding

Table 7. FeliCa framing and coding

Preamble						Sync		Len	n-Data				CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh							

To enable the FeliCa communication a 6 byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2 bytes Sync bytes (B2h, 4Dh) are sent to synchronize the receiver.

The following Len byte indicates the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the host controller has to send the Len- and data-bytes to the CLRC663's FiFo-buffer. The preamble and the sync bytes are generated by the CLRC663 automatically and must not be written to the FiFo by the host controller. The CLRC663 performs internally the CRC calculation and adds the result to the data frame.

Example for FeliCa CRC calculation:

Table 8. Start value for the CRC Polynomial: (00h), (00h)

Preamble						Sync		Len	2 Data Bytes		CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh	03h	ABh	CDh	90h	35h

8.4 ISO/IEC15693 read/write functionality

The physical parameters are described in Table 9.

Table 9. Communication overview for ISO/IEC 15693 reader/writer reader to label

Communication direction	Signal type	Transfer speed	
		fc/8192 kbit/s	fc/512 kbit/s
Reader to label (send data from the CLRC663 to a card)	reader side modulation	10 to 30 % ASK or 100 % ASK	10 to 30 % ASK 90 % to 100 % ASK
	bit encoding	1/256	1/4
	bit length	4.833 ms	302.08 µs

Table 10. Communication overview for ISO/IEC 15693 reader/writer label to reader

Communication direction	Signal type	Transfer speed			
		6.62 (6.67) kbit/s	13.24 kbit/s[1]	26.48 (26.69) kbit/s	52.96 kbit/s
Label to reader (CLRC663 receives data from a card) fc = 13.56 MHz	card side modulation	single (dual) subcarrier load modulation ASK	single subcarrier load modulation ASK	single (dual) subcarrier load modulation ASK	single subcarrier load modulation ASK
	bit length µs	151.06 (149.84)	75.52	37.76 (3.746)	18.88
	bit encoding	Manchester coding	Manchester coding	Manchester coding	Manchester coding
	subcarrier frequency [MHz]	fc/32 (fc/28)	fc/32 (fc/28)	fc/32 (fc/28)	fc/32 (fc/28)

[1] Fast inventory (page) read command only (ICODE proprietary command).

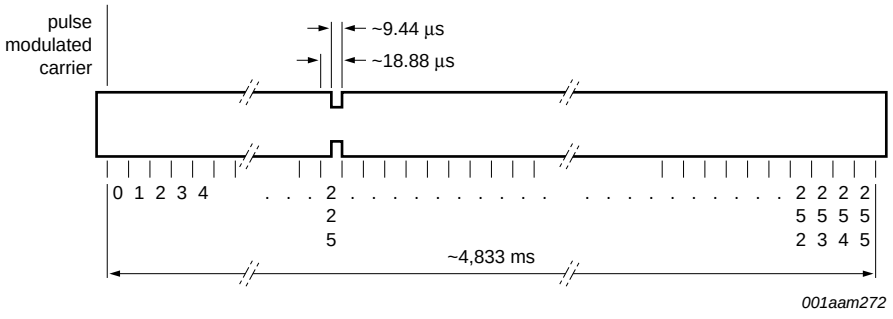


Fig 10. Data Coding and framing according to ISO/IEC 15693. standard mode reader to label

8.5 EPC-UID/UID-OTP read/write functionality

The physical parameters are described in Table 11.

Table 11. Communication overview for EPC/UID

Communication direction	Signal type	Transfer speed	
		26.48 kbit/s	52.96 kbit/s
Reader to card (send data from the CLRC663 to a card)	reader side modulation	10 % to 30 % ASK	
	bit encoding	RTZ	
	bit length	37.76 µs	
Card to reader (CLRC663 receives data from a card)	card side modulation		single subcarrier load modulation
	bit length		18.88 µs
	bit encoding		Manchester coding

Data coding and framing according EPC global 13.56 MHz ISM Band Class 1 Radio Frequency Identification Tag Interface Specification (Candidate Recommendation, Version 1.0.0).

8.6 ISO/IEC18000-3 Mode 3 read/write functionality

This section intentionally left blank.

8.7 ISO/IEC 18092 mode

The ISO/IEC 18092 communication for Passive Communication mode.

- Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: generates RF field at 13.56 MHz and starts the ISO/IEC 18092 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

The CLRC663 supports Passive Initiator Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the ISO/IEC 18092 standard.

8.7.1 Passive communication mode

Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active meaning generating the RF field.

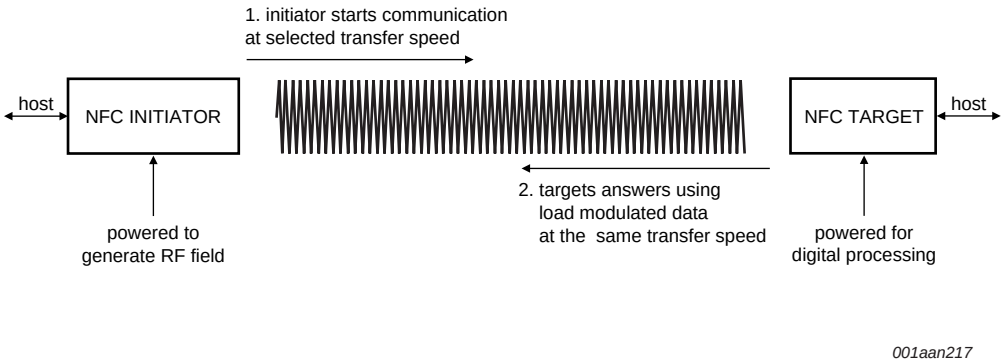


Fig 11. Passive communication mode

Table 12. Communication overview for Passive communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s	1.69 Mbit/s, 3.39 Mbit/s
Initiator → Target	According to ISO/IEC 14443A 100 % ASK, Modified Miller Coded	According to FeliCa, 8 % to 30 % ASK Manchester Coded		digital capability to handle this communication	
Target → Initiator	According to ISO/IEC 14443A subcarrier load modulation, Manchester Coded	According to FeliCa, > 12 % ASK Manchester Coded			

The contactless UART of CLRC663 and a dedicated host controller are required to handle the ISO/IEC 18092 passive initiator protocol.

Note: Transfer speeds above 424 kbit/s are not defined in the ISO/IEC 18092 standard. The CLRC663 supports these transfer speeds only with dedicated external circuits.

8.7.2 ISO/IEC 18092 framing and coding

The ISO/IEC 18092 framing and coding in Passive Communication mode is defined in the ISO/IEC 18092 standard.

Table 13. Framing and coding overview

Transfer speed	Framing and Coding
106 kbit/s	According to the ISO/IEC 14443A/MIFARE scheme
212 kbit/s	According to the FeliCa scheme
424 kbit/s	According to the FeliCa scheme

8.7.3 ISO/IEC 18092 protocol support

The ISO/IEC 18092 protocol is not completely described in this document. For a detailed explanation of the protocol, refer to the ISO/IEC 18092 standard. However the data link layer is in accordance with the following policy:

- Speed shall not be changed while continuum data exchange in a transaction.
- Transaction includes initialization and anti-collision methods and data exchange (in continuous way, meaning no interruption by another transaction).

9. CLRC663 registers

9.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle, bits with same behavior are grouped in common registers. The access conditions are described in Table 14.

Table 14. Behavior of register bits and their designation

Abbreviation	Behavior	Description
r/w	read and write	These bits can be written and read via the host interface. Since they are used only for control purposes, the content is not influenced by the state machines but can be read by internal state machines.
dy	dynamic	These bits can be written and read via the host interface. They can also be written automatically by internal state machines, for example Command_Reg register changes its value automatically after the execution of the command.
r	read only	These register bits indicates hold values which are determined by internal states only.
w	write only	Reading these register bits always returns zero.
RFU	-	These registers are reserved for future use and must not be changed. In case of a write access, it is recommended to write the value “0”.

Table 15. CLRC663 registers overview

Address	Register name	Function
00h	Command_Reg	starts and stops command execution
01h	HostCtrl_Reg	host control register
02h	FiFoControl_Reg	control register of the FiFo
03h	WaterLevel_Reg	defines the level of the FiFo underflow and overflow warning
04h	FiFoLength_Reg	defines the length of the FiFo
05h	FiFoData_Reg	data IN/Out exchange register of FIFO buffer
06h	IRQ0_Reg	interrupt register 0
07h	IRQ1_Reg	interrupt register 1
08h	IRQ0En_Reg	interrupt enable register 0
09h	IRQ1En_Reg	interrupt enable register 1
0Ah	Error_Reg	Error bits showing the error status of the last command execution
0Bh	Status_Reg	Contains status of the communication
0Ch	RxBitCtrl_Reg	Control register for anticollision adjustments for bit oriented protocols
0Dh	RxColl_Reg	Collision position register
0Eh	TControl_Reg	Control of timer the timer section
0Fh	T0Control_Reg	Control of timer0
10h	T0ReloadHi_Reg	High byte of the reload value of timer0
11h	T0ReloadLo_Reg	Low byte of the reload value of timer0
12h	T0CounterValHi_Reg	Counter value high byte of timer0
13h	T0CounterValLo_Reg	Counter value low byte of timer0

Table 15. CLRC663 registers overview *…continued*

Address	Register name	Function
14h	T1Control_Reg	Control of timer1
15h	T1ReloadHi_Reg	High byte of the reload value of timer1
16h	T1ReloadLo_Reg	Low byte of the reload value of timer1
17h	T1CounterValHi_Reg	Counter value high byte of timer1
18h	T1CounterValLo_Reg	Counter value low byte of timer1
19h	T2Control_Reg	Control of timer2
1Ah	T2ReloadHi_Reg	High byte of the reload value of timer2
1Bh	T2ReloadLo_Reg	Low byte of the reload value of timer2
1Ch	T2CounterValHi_Reg	Counter value high byte of timer2
1Dh	T2CounterValLo_Reg	Counter value low byte of timer2
1Eh	T3Control_Reg	Control of timer3
1Fh	T3ReloadHi_Reg	High byte of the reload value of timer3
20h	T3ReloadLo_Reg	Low byte of the reload value of timer3
21h	T3CounterValHi_Reg	Counter value high byte of timer3
22h	T3CounterValLo_Reg	Counter value low byte of timer3
23h	T4Control_Reg	Control of timer4
24h	T4ReloadHi_Reg	High byte of the reload value of timer4
25h	T4ReloadLo_Reg	Low byte of the reload value of timer4
26h	T4CounterValHi_Reg	Counter value high byte of timer4
27h	T4CounterValLo_Reg	Counter value low byte of timer4
28h	DrvMod_Reg	Driver mode register
29h	TxAmp_Reg	Transmitter amplifier register
2Ah	DrvCon_Reg	Driver configuration register
2Bh	Txl_Reg	Transmitter register
2Ch	TxCrcCon_Reg	Transmitter CRC control register
2Dh	RxCrcCon_Reg	Receiver CRC control register
2Eh	TxDataNum_Reg	Transmitter data number register
2Fh	TxModWidth_Reg	Transmitter modulation width register
30h	TxSym10BurstLen_Reg	Transmitter symbol 1 + symbol 0 burst length register
31h	TXWaitCtrl_Reg	Transmitter wait control
32h	TxWaitLo_Reg	Transmitter wait low
33h	FrameCon_Reg	Transmitter frame control
34h	RxSofD_Reg	Receiver start of frame detection
35h	RxCtrl_Reg	Receiver control
36h	RxWait_Reg	Receiver wait register
37h	RxThreshold_Reg	Receiver threshold
38h	Rcv_Reg	Receiver register
39h	RxAna_Reg	Receiver analog register
3Ah	RFU	-
3Bh	SerialSpeed_Reg	Serial speed register

Table 15. CLRC663 registers overview *…continued*

Address	Register name	Function
3Ch	LPO_Trimm_Reg	Low power oscillator trimming register for Low Power Card Detection register
3Dh	PLL_Ctrl_Reg	IntegerN PLL control register, for uC clock output adjustment
3Eh	PLL_DivOut_Reg	IntegerN PLL control register, for uC clock output adjustment
3Fh	LPCD_QMin_Reg	Low power card detection Q channel minimum threshold
40h	LPCD_QMax_Reg	Low power card detection Q channel maximum threshold
41h	LPCD_IMin_Reg	Low power card detection I channel minimum threshold
42h	LPCD_I_Result_Reg	Low power card detection I channel result register
43h	LPCD_Q_Result_Reg	Low power card detection Q channel result register
44h	PadEn_Reg	GPIO0 pin enable register
45h	PadOut_Reg	GPIO0 pin out register
46h	PadIn_Reg	GPIO0 pin in register
47h	SigOut_Reg	Enables and controls the SigOut Pin
48h	TxBitMod_Reg	Transmitter bit modus register
49h	RFU	-
4Ah	TxDataCon_Reg	Transmitter data configuration register
4Bh	TxDataMod_Reg	Transmitter data modulation register
4Ch	TxSymFreq_Reg	Transmitter symbol frequency
4Dh	TxSym0H_Reg	Transmitter symbol 0 high register
4Eh	TxSym0L_Reg	Transmitter symbol 0 low register
4Fh	TxSym1H_Reg	Transmitter symbol 1 high register
50h	TxSym1L_Reg	Transmitter symbol 1 low register
51h	TxSym2_Reg	Transmitter symbol 2 register
52h	TxSym3_Reg	Transmitter symbol 3 register
53h	TxSym10Len_Reg	Transmitter symbol 1 + symbol 0 length register
54h	TxSym32Len_Reg	Transmitter symbol 3 + symbol 2 length register
55h	TxSym10BurstCtrl_Reg	Transmitter symbol 1 + symbol 0 burst control register
56h	TxSym10Mod_Reg	Transmitter symbol 1 + symbol 0 modulation register
57h	TxSym32Mod_Reg	Transmitter symbol 3 + symbol 2 modulation register
58h	RxBitMod_Reg	Receiver bit modulation register
59h	RxEofSym_Reg	Receiver end of frame symbol register
5Ah	RxSyncValH_Reg	Receiver synchronisation value high register
5Bh	RxSyncValL_Reg	Receiver synchronisation value low register
5Ch	RxSyncMod_Reg	Receiver synchronisation mode register
5Dh	RxMod_Reg	Receiver modulation register
5Eh	RxCorr_Reg	Receiver correlation register
5Fh	FabCal_Reg	Fab calibration register of the receiver
7Fh	Version_Reg	Version and subversion register

9.2 Description/Command register

9.2.1 Command_Reg

Starts and stops command execution.

Table 16: Command_Reg register (address 00h); reset value: 40h

Bit	7	6	5	4	3	2	1	0
Symbol	Standby	Mode Off	-	Command				
Access rights	dy	r/w	RFU	dy				

Table 17: Description of Command_Reg bits

Bit	Symbol	Description
7	Standby	Set to 1, the IC is entering power-down mode.
6	ModemOff	Set to logic 1, the receiver and the transmitter circuit is powering down.
5	0	RFU
4 to 0	Command	Defines the actual command for the CLRC663.

Table 18: Command overview

Command	Nr.	Nr.	Short description
Idle	0.0000	00h	no action, cancels current command execution
LPCD	0.0001	01h	Low power card detection and/or auto trimming
LoadKey	0.0010	02h	Reads a key from FiFo buffer and puts it into key buffer
MFAuthent	0.0011	03h	Performs the MIFARE standard authentication in MIFARE read/write mode only
AckReq	0.0100	04h	Performs a query, a Ack and a Req-Rn for ISO/IEC 18000-3 mode 3
Receive	0.0101	05h	Enables data receive
Transmit	0.0110	06h	Transmits data from the FiFo buffer
Transceive	0.0111	07h	Transmits data from the FiFo buffer and automatically activates the receiver after transmission finished
WriteE2	0.1000	08h	Gets one byte from FiFo buffer and writes it to the internal EEProm
WriteE2Pages	0.1001	09h	Gets up to 64 bytes from FiFo buffer and writes it to the internal EEPROM
ReadE2	0.1010	0Ah	Reads data from the EEPROM and puts it into the FiFo buffer
LoadReg	0.1100	0Bh	Reads data from the internal EEPROM and initializes the CLRC663 registers
LoadProtocol	0.1101	0Ch	Reads data from the internal EEPROM and initializes the CLRC663 registers needed for a protocol change
LoadKeyE2	0.1110	0Eh	Copies a MIFARE key of the EEPROM into the key buffer
StoreKeyE2	0.1111	0Fh	Stores a MIFARE key into the EEPROM
Soft Reset	1.1111	1Fh	Resets the CLRC663 to EEPROM configuration

9.3 Register Description/SAM register

9.3.1 HostCtrl_Reg

Via the HostCtrl_Register the Interface access right can be controlled

Table 19. HostCtrl_Reg register (address 01h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	RegEn	Bus Host	BusSam	-	Sam Interface	SAM Interface	-	-
Access rights	r/w	r/w	r/w	RFU	r/w	r/w	RFU	RFU

Table 20: Description of HostCtrl_Reg bits

Bit	Symbol	Description
7	RegEn	If this bit is set to logic 1, the register can be changed at the next register access. The next write access clears this bit automatically.
6	BusHost	Set to logic 1, the buscontrol enables the host interface. This bit can not be set together with BusSam. This bit can only be set if the bit RegEn was previously set.
5	BusSam	Set to logic 1, the buscontrol enables the SAM interface. This bit can not be set together with BusHost. This bit can only be set if the bit RegEn is previously set.
4	-	RFU
3 to 2	Sam Interface	00:Off (default) 01:SPI 10:I2CL 11:I2C standard I/O pad
1 to 0	-	RFU

9.4 Register Description/FiFo register

9.4.1 FiFoControl_Reg

FiFoControl_Reg register controls the behavior of the FiFo

Table 21. FiFoControl_Reg register (address 02h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	FiFo Size	HiAlert	LoAlert	FiFo Flash	-	Water Level	FiFo Length	
Access rights	r/w	r	r	w	RFU	r/w	r	

Table 22: Description of FiFoControl_Reg bits

Bit	Symbol	Description
7	FiFoSize	Set to logic 1, FiFo size 255 bytes; Set to logic 0, FiFo size is 512 bytes. The size can only be changed, when at the same write command a FiFo Flash is executed
6	HiAlert	Set to logic 1, when the number of bytes stored in the FiFo buffer fulfils the following equation: HiAlert = (FiFoSize - FiFoLength) <= WaterLevel
5	LoAlert	Set to logic 1, when the number of bytes stored in the FiFo buffer fulfils the following conditions: LoAlert =1 if FiFoLength <= WaterLevel
4	FiFoFlash	Set to logic 1 empties the FiFo buffer. Reading this bit will always return 0
3	-	RFU
2	WaterLevel	Defines the higher bit for the waterlevel. This bit is only needed in the 512 bit FiFo mode
1 to 0	FiFoLength	Defines the two higher bit for the FiFo length. These two bits are only needed in the 512 bit FiFo mode

9.4.2 WaterLevel_Reg

Defines the level for FiFo under- and overflow warning.

Table 23: WaterLevel_Reg register (address 03h); reset value: 05h

Bit	7	6	5	4	3	2	1	0
Symbol	WaterLevel							
Access rights	r/w							

Table 24: Description of WaterLevel_Reg bits

Bit	Symbol	Description
7 to 0	WaterLevel	This register defines a warning level to indicate a FiFo-buffer overflow or underflow: The bit HiAlert bit in FiFo Control is set to logic 1, if the remaining number of bytes in the FIFO-buffer space is equal or less than the defined number of WaterLevel bytes. The bit LoAlert bit in FiFo control is set to logic 1, if equal or less than WaterLevel bytes are in the FiFo. Note: For the calculation of HiAlert and LoAlert see register description of these bits. Note: In the 512 byte mode also the higher bit of FiFoLength in the FiFoControl Register have to be taken into account

9.4.3 FiFoLength_Reg

Number of bytes in the FiFo buffer.

Table 25: FiFoLength_Reg register (address 04h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	FiFoLength							
Access rights	r/w							

Table 26: Description of FiFoLength_Reg bits

Bit	Symbol	Description
7 to 0	FiFoLength	Indicates the number of bytes in the FiFo buffer. writing to the FiFoData_Reg register increments, reading decrements the FiFo level. Note: In the 512 byte mode also the higher bits of FiFoLength bit in the FiFoControl_Reg register have to be taken into account.

9.4.4 FiFoData_Reg

In- and output of FiFo buffer.

Table 27: FiFoData_Reg register (address 09h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	FiFoData							
Access rights	dy							

Table 28: Description of FiFoData_Reg bits

Bit	Symbol	Description
7 to 0	FiFoData	Data input and output port for the internal FiFo buffer. Refer to Section 13 “FiFo Buffer”

9.5 Register Description/interrupt register

9.5.1 IRQ0_Reg register

interrupt register 0.

Table 29: IRQ0_Reg register (address 06h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Set	Hi AlertIrq	Lo AlertIrq	IdleIrq	TxIrq	RxIrq	ErrIrq	RxSOF Irq
Access rights	w	r/w/dy	r/w/dy	r/w/dy	r/w/dy	r/w/dy	r/w/dy	r/w/dy

Table 30: Description of IRQ0_Reg bits

Bit	Symbol	Description
7	Set	Set to logic 1, set defined bits in IRQ0_Reg Set to logic 0, clears marked bits in the IRQ0_Reg.
6	HiAlerIrq	Set to logic 1, when bit HiAlert in register Status1Reg is set. In opposition to HiAlert, HiAlertIrq stores this event and can only be reset as indicated by bit Set.
5	LoAlertIrq	Set to logic 1, when bit LoAlert in register Status1_Reg is set. In opposition to LoAlert, LoAlertIrq stores this event and can only be reset as indicated by bit Set1
4	IdleIIrq	Set to logic 1, when a command terminates by itself e.g. when the Command_Reg changes its value from any command to the Idle command. If an unknown command is started, the Command_Reg changes its content to the idle state and the bit IdleIRq is set. Starting the Idle command by the Controller does not set bit IdleIRq.
3	TxIrq	Set to 1, when data transmission is completed, which is immediately after the last bit is send.
2	RxIrq	Set to 1, when the receiver detects the end of a data stream. Note: This flag is no indication that the received data stream is correct. The error flags have to be evaluated to get the status of the reception.
1	ErrIrq	Set to 1, when the one of the following errors is set: FifoWrErr, FiFoOvl, ProtErr, NoDataErr, IntegErr
0	RxSOFIrq	Set to 1 when a SOF or a subcarrier is detected

9.5.2 IRQ1_Reg register

interrupt register 1.

Table 31: IRQ1_Reg register (address 07h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Set	Global Irq	LPCD_ Irq	Timer4 Irq	Timer3 Irq	Timer2 Irq	Timer1 Irq	Timer0 Irq
Access rights	w	r/w/dy	r/w/dy	r/w/dy	r/w/dy	r/w/dy	r/w/dy	r/w/dy

Table 32: Description of IRQ1_Reg bits

Bit	Symbol	Description
7	Set	Set to logic 1, set defined bits in IRQ1_Reg Set to logic 0, clears marked bits in the IRQ1_Reg.
6	GlobalIrq	Set, if an enabled Irq occurs.
5	LPCD_Irq	Set if a card is detected in Low power card detection sequence.
4	Timer4Irq	Set to logic 1 when Timer4 has an underflow.
3	Timer3Irq	Set to logic 1 when Timer3 has an underflow.
2	Timer2Irq	Set to logic 1 when Timer2 has an underflow.
1	Timer1Irq	Set to logic 1 when Timer1 has an underflow.
0	Timer0Irq	Set to logic 1 when Timer0 has an underflow.

9.5.3 IRQ0En_Reg register

interrupt Enable register for IRQ0_Reg.

Table 33: IRQ0En_Reg register (address 08h); reset value: 10h

Bit	7	6	5	4	3	2	1	0
Symbol	Irq_Inv	Hi AlertIrq En	Lo AlertIrq En	IdleIrq En	TxIrqEn	RxIrqEn	ErrIrqEn	RxSOF Irq En
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 34: Description of IRQ0En_Reg bits

Bit	Symbol	Description
7	Irq_Inv	Set to one the signal of the IRQ pin is inverted
6	Hi AlerIrqEn	Set to logic 1, it allows the transmitter interrupt request (indicated by the bit HiAlertIrq) to be propagated to the GlobalIrq
5	Lo AlertIrqEn	Set to logic 1, it allows the transmitter interrupt request (indicated by the bit LoAlertIrq) to be propagated to the GlobalIrq
4	IdleIIrqEn	Set to logic 1, it allows the transmitter interrupt request (indicated by the bit IdleIrq) to be propagated to the GlobalIrq
3	TxIRqEn	Set to logic 1, it allows the transmitter interrupt request (indicated by the bit TxtIrq) to be propagated to the GlobalIrq
2	RxIRqEn	Set to logic 1, it allows the receiver interrupt request (indicated by the bit RxIrq) to be propagated to the GlobalIrq
1	ErrIRqEn	Set to logic 1, it allows the Error interrupt request (indicated by the bit ErrorIrq) to be propagated to the GlobalIrq
0	RxSOF IrqEn	Set to logic 1, it allows the RxSOF interrupt request (indicated by the bit RxSOFIrq) to be propagated to the GlobalIrq

9.5.4 IRQ1En_Reg register

interrupt Enable register for IRQ1_Reg.

Table 35: IRQ1EN_Reg register (address 09h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Irq PushPull	IrqPin En	LPCD_ IrqEn	Timer4 IRqEn	Timer3 IrqEn	Timer2 IrqEn	Timer1 IrqEn	Timer0 IrqEn
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 36: Description of IRQ1EN_Reg bits

Bit	Symbol	Description
7	IrqPushPull	Set to 1 the IRQ-pin acts as PushPull pin, otherwise it acts as OpenDrain pin
6	IrqPinEN	Set to logic 1, it allows the global interrupt request (indicated by the bit GlobalIrq) to be propagated to the interrupt pin
5	LPCD_IrqEN	Set to logic 1, it allows the LPCDinterrupt request (indicated by the bit LPCDIrq) to be propagated to the GlobalIrq
4	Timer4IRqEn	Set to logic 1, it allows the timer4 interrupt request (indicated by the bit timer4Irq) to be propagated to the GlobalIrq

Table 36: Description of IRQ1EN_Reg bits …continued

Bit	Symbol	Description
3	Timer3IrqEn	Set to logic 1, it allows the timer3 interrupt request (indicated by the bit Timer3tIrq) to be propagated to the GlobalIrq
2	Timer2IrqEn	Set to logic 1, it allows the timer2 interrupt request (indicated by the bit timer2Irq) to be propagated to the GlobalIrq
1	Timer1IrqEn	Set to logic 1, it allows the timer1 interrupt request (indicated by the bit timer1Irq) to be propagated to the GlobalIrq
0	Timer0IrqEn	Set to logic 1, it allows the timer0 interrupt request (indicated by the bit timer0Irq) to be propagated to the GlobalIrq

9.6 Register Description/CL register

9.6.1 Error_Reg register

Error register.

Table 37: Error_Reg register (address 0Ah); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	EE_Err	FiFo WrErr	FiFoOvl	minFra meErr	NoData Err	CollDet	ProtErr	IntegErr
Access rights	d/w/r	d/w/r	d/w/r	d/w/r	d/w/r	d/w/r	d/w/r	d/w/r

Table 38: Description of Error_Reg bits

Bit	Symbol	Description
7	EE_Err	If this flag is set, an error appeared during the last EEPROM command. For details see the descriptions of the EEPROM commands
6	FiFoWrErr	If this Flag is set, data was written into the FIFO, during a transmission of a possible CRC, during "RxWait", "Wait for data" or "Receiving" state, or during an authentication command. The Flag is cleared when a new CL command is started. If RxMultiple is active, the flag is cleared after the error flags have been written to the FiFo.
5	FiFoOvl	This flag is set to 1 if data is written into the FIFO when it is already full. The data that is already in the FiFo will remain untouched. All data that is written to the FiFo after this Flag is set to 1 will be ignored.
4	min FrameErr	This flag is set to 1, if a valid SOF was received, but afterwards less then 4 bits of data were received. Note: Frames with less than 4 bits of data are automatically discarded and the RxDecoder stays enabled. Furthermore no RxIrq is set. The same is valid for less than 3 Bytes if the EMD suppression is activated Note: MinFrameErr is automatically cleared at the start of a receive or transceive command. In case of a transceive command, it is cleared at the start of the receiving phase ("Wait for data" state)
3	NoDataErr	This flag is set if data should be sent, but no data is in FiFo

Table 38: Description of Error_Reg bits

Bit	Symbol	Description
2	CollDet	This flag is set to 1, if a collision has occurred. The position of the first collision is shown in the register RxColl_Reg. Note: CollDet is automatically cleared at the start of a receive or transceive command. In case of a transceive command, it is cleared at the start of the receiving phase (“Wait for data” state). Note: If a collision is part of the defined EOF symbol, CollDet is not set to 1.
1	ProtErr	This flag is set to 1, if a protocol error has occurred. A protocol error can be a wrong stop bit, a missing or wrong ISO/IEC14443B EOF or SOF or a wrong number of received data bytes. When a protocol error is detected, data reception is stopped. Note: ProtErr is automatically cleared at start of a receive or transceive command. In case of a transceive command, it is cleared at the start of the receiving phase (“Wait for data” state). Note: When a protocol error occurs the last received data byte is not written into the FIFO.
0	IntegErr	This flag is set to 1, if a data integrity error has been detected. Possible cause can be a wrong parity or a wrong CRC. In case of a data integrity error the reception is continued. Note: IntegErr is automatically cleared at start of a Receive or Transceive command. In case of a Transceive command, it is cleared at the start of the receiving phase (“Wait for data” state). Note: If a reversed parity bit is a stop criteria, IntegErr is not set to 1. Note: If the NoColl bit is set, also a collision is setting the IntegErr.

9.6.2 Status_Reg

Status register.

Table 39: Status_Reg register (address 0Bh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	Crypto1 On	-	-	ComState		
Access rights	RFU	RFU	r/w	RFU	RFU	r		

Table 40: Description of Status_Reg bits

Bit	Symbol	Description
7, 6	-	RFU
5	Crypto1On	Indicates if the MIFARE Crypto is on. Clearing this bit is switching the MIFARE Crypto off. The bit can only be set by the MFAuthent command.
4 to 3	-	RFU
2 to 0	ComState	ComState shows the status of the transmitter and receiver state machine 000...Idle 001...TxWait 011...Transmitting 101...RxWait 110...Wait for data 111...Receiving 100...not used

9.6.3 RxBitCtrl_Reg

Receiver control register.

Table 41: RxBitCtrl_Reg register (address 0Ch); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Values After Coll	RxAlign			NoColl	RxLastBits		
Access rights	r/w	r/w			r/w	r/w		

Table 42: Description of RxBitCtrl_Reg bits

Bit	Symbol	Description
7	Values After Coll	If cleared, every received bit after a collision is replaced by a zero. This function is needed for type A anticollision
6 to 4	RxAlign	Used for reception of bit oriented frames: RxAlign defines the bit position length for the first bit received to be stored. Further received bits are stored at the following bit positions. Example: RxAlign = 0h - the LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1. RxAlign = 1h - the LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2. RxAlign = 7h - the LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at position 0. Note: If RxAlign = 0, data is received byte-oriented, otherwise bit-oriented. The hardware does not cross-check this settings in any way
3	NoColl	If this bit is set, a collision will result in an IntegErr
2 to 0	RxLastBits	Defines the number of valid bits of the last data byte received in bit-oriented communications. If zero the whole byte is valid. Note: These bits are set by the RxDecoder in a bit-oriented communication at the end of the communication. They are reset at start of reception.

9.6.4 RxColl_Reg

Receiver collision register.

Table 43: RxColl_Reg register (address 0Dh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	CollPos Valid	CollPos						
Access rights	r/w/dy	r/w/dy						

Table 44: Description of RxColl_Reg bits

Bit	Symbol	Description
7	CollPos Valid	If set to 1, the value for position of the collision is valid. Otherwise no collision is detected or the position of the collision is out of the range of bits CollPos. This bit shall only be interpreted in passive communication mode at 106 kbit/s or ISO14443A/MIFARE reader/writer mode.
6 to 0	CollPos	These bits show the bit position of the first detected collision in a received frame (only data bits are interpreted). CollPos can only be displayed for the first 8 bytes of a data stream. Example: 00h indicates a bit collision in the 1st bit 01h indicates a bit collision in the 2nd bit 08h indicates a bit collision in the 9th bit (1st bit of 2nd byte) 3Fh indicates a bit collision in the 64th bit (8th bit of the 8th byte) These bits shall only be interpreted in passive communication mode at 106 kbit/s or ISO/IEC 14443A/MIFARE reader /writer or ISO/IEC 15693/I-CODE SLI read/write mode if bit *CollPosValid* is set to 1. Note: If *RxBitCtrl.RxAlign* is set to a value different to 0, this value is included in the *CollPos*. Example: RxAlign = 4h, a collision occurs in the 4th received bit (which is the last bit of that UID byte). The CollPos = 7h in this case. .

9.7 Register Description/Timer register

9.7.1 TControl_Reg

Control register of the timer section.

Table 45: TControl_Reg register (address 0Eh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T3 Running	T2 Running	T1 Running	T0 Running	T3Start StopNow	T2Start StopNow	T1Start StopNow	T0Start StopNow
Access rights	dy/r/w	dy/r/w	dy/r/w	dy/r/w	r/w	r/w	r/w	r/w

Table 46: Description of TControl_Reg bits

Bit	Symbol	Description
7	T*3*Running	Shows if the timer n is running. if the T3startStopNow is set, this bit and the timer can be controlled
6	T*2*Running	Shows if the timer n is running. if the T2startStopNow is set, this bit and the timer can be controlled
5	T*1*Running	Shows if the timer n is running. if the T1startStopNow is set, this bit and the timer can be controlled
4	T*0*Running	Shows if the timer n is running. if the T0startStopNow is set, this bit and the timer can be controlled
3	T*3*StartStop Now	Set to logic 1 the bit T3Running can be set.
2	T*2*StartStop Now	Set to logic 1 the bit T2Running can be set.
1	T*1*StartStop Now	Set to logic 1 the bit T1Running can be set.
0	T*0*StartStop Now	Set to logic 1 the bit T0Running can be set.

9.8 T0Control_Reg

Control register of the Timer0.

Table 47: T0Control_Reg register (address 0Fh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T0Stop Rx	-	T0Start		T0Auto Restarted	-	T0Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 48: Description of T0Control_Reg bits

Bit	Symbol	Description
7	T0StopRx	If set to one, the timer stops immediately after receiving the first data. Set to logic 0, indicates that the timer is not stopped automatically. Note: If LFO Trimming is selected by T0Start, this bit has no effect
6	-	RFU
5 to 4	T0Start	00b: The timer is not started automatically 01b: The timer starts automatically at the end of the transmission 10b: Timer is used for LFO trimming without underflow (Start/Stop on PosEdge) 11b: Timer is used for LFO trimming with underflow (Start/Stop on PosEdge)
3	T0AutoRestart	Set to logic 1, the timer automatically restarts its count-down from T0ReloadValue, after the counter value has reached the value zero. Set to logic 0 the timer decrements to zero and stops. The bit Timer1Irq is set to logic 1 when the timer reaches zero.
2	-	RFU
1 to 0	T0Clk	00b: The timer input clock is 13.56 MHz. 01b: The timer input clock is 212 kHz. 10b: The timer input clock is an underflow of Timer 2. 11b: The timer input clock is an underflow of Timer 1.

9.8.1 T0ReloadHi_Reg

High byte reload value of the timer 0.

Table 49: T0ReloadHi_Reg register (address 10h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T0Reload Hi							
Access rights	r/w							

Table 50: Description of T0ReloadHi_Reg bits

Bit	Symbol	Description
7 to 0	T0ReloadHi	Defines the high byte of the reload value of the timer. With the start event the timer loads the value of the T0ReloadVal. Changing this register affects the timer only at the next start event.

9.8.2 T0ReloadLo_Reg

Low byte reload value of the timer 0.

Table 51: T0ReloadLo_Reg register (address 11h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	T0ReloadLo							
Access rights	r/w							

Table 52: Description of T0ReloadLo_Reg bits

Bit	Symbol	Description
7..0	T0ReloadLo	Defines the low byte of the reload value of the timer. With the start event the timer loads the value of the T0ReloadVal. Changing this register affects the timer only at the next start event.

9.8.3 T0CounterValHi_Reg

High byte of the counter value of timer0.

Table 53: T0CounterValHi_Reg register (address 12h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T0CounterHi							
Access rights	r/w							

Table 54: Description of T0CounterValHi_Reg bits

Bit	Symbol	Description
7..0	T0Counter ValHi	Current high byte value of the counter 0. This value shall not be read out during reception.

9.8.4 T0CounterValLo_Reg

Low byte of the counter value of timer0.

Table 55: T0CounterValLo_Reg register (address 13h); reset value:00h

Bit	7	6	5	4	3	2	1	0
Symbol	T0CounterValLo							
Access rights	r/w							

Table 56: Description of T0CounterValLo_Reg bits

Bit	Symbol	Description
7 to 0	T0CounterValLo	Current Value of the counter n. This value shall not be read out during reception.

9.8.5 T1Control_Reg

Control register of the Timer1.

Table 57: T1Control_Reg register (address 14h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T1Stop Rx	-	T1Start		T1Auto Restart	-	T1Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 58: Description of T1Control_Reg bits

Bit	Symbol	Description
7	T1StopRx	If set to one, the timer stops immediately after receiving the first data. Set to logic 0, indicates that the timer is not stopped automatically. Note: If LFO trimming is selected by T1start, this bit has no effect
6	-	RFU
5 to 4	T1Start	00b: The timer is not started automatically 01b: The timer starts automatically at the end of the transmission 10b: Timer is used for LFO trimming without underflow (Start/Stop on PosEdge) 11b: Timer is used for LFO trimming with underflow (Start/Stop on PosEdge)
3	T1AutoRestart	Set to logic 1, the timer automatically restarts its countdown from TnReloadValue, after the counter value has reached the value zero. Set to logic 0 the timer decrements to zero and stops. The bit Timer1IRq is set to logic 1 when the timer reaches zero
2	-	RFU
1 to 0	T1Clk	00b: The timer input clock is 13.56 MHz 01b: The timer input clock is 212 kHz. 10b: The timer input clock is an underflow of timer 0 11b: The timer input clock is an underflow of timer 2

9.8.6 T1ReloadHi_Reg

High byte reload value of the Timer1.

Table 59: T0ReloadHi_Reg register (address 15h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T1ReloadHi							
Access rights	r/w							

Table 60: Description of T1ReloadHi_Reg bits

Bit	Symbol	Description
7 to 0	T1ReloadHi	Defines the high byte reload value of the timer1. With the start event the timer loads the value of the T1ReloadValHi_Reg and T1ReloadValLo_Reg. Changing this register affects the Timer only at the next start event.

9.8.7 T1ReloadLo_Reg

Low byte reload value of the timer 1.

Table 61: T1ReloadLo_Reg register (address 16h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	T1ReloadLo							
Access rights	r/w							

Table 62: Description of T1ReloadValLo_Reg bits

Bit	Symbol	Description
7 to 0	T1ReloadLo	Defines the low byte of the reload value of the timer1.With the start event the timer load the value of the T1ReloadValHi_Reg and T1ReloadValLo_Reg. Changing this register affects the timer only at the next start event.

9.8.8 T1CounterValHi_Reg

High byte of the counter value of byte Timer1.

Table 63: T1CounterValHi_Reg register (address 17h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T1CounterValHi							
Access rights	r/w							

Table 64: Description of TnCounterValHi_Reg bits

Bit	Symbol	Description
7 to 0	T1Counter ValHi	High byte of the current value of the timer1. This value shall not be read out during receive.

9.8.9 T1CounterValLo_Reg

Low byte of the counter value of byte Timer1.

Table 65: T1CounterValLo_Reg register (address 18h); reset value:00h

Bit	7	6	5	4	3	2	1	0
Symbol	T1CounterValLo							
Access rights	r/w							

Table 66: Description of T1CounterValLo_Reg bits

Bit	Symbol	Description
7 to 0	T1Counter ValLo	Low byte of the current value of the counter 1. This value shall not be read out during receive.

9.8.10 T2Control_Reg

Control register of the Timer2.

Table 67: T2Control_Reg register (address 19h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T2Stop Rx	-	T2Start		T2Auto Restart	-	T2Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 68: Description of T2Control_Reg bits

Bit	Symbol	Description
7	T2StopRx	If set to 1 the timer stops immediately after receiving the first data. Set to logic 0, indicates, that the timer is not stopped automatically. Note: If LFO Trimming is selected by T2Start, this bit has no effect
6	-	RFU
5 to 4	T2Start	00b: The timer is not started automatically. 01b: The timer starts automatically at the end of the transmission. 10b: Timer is used for LFO trimming without underflow (Start/Stop on PosEdge). 11b: Timer is used for LFO trimming with underflow (Start/Stop on PosEdge).
3	T2AutoRestart	Set to logic 1, the timer automatically restarts its countdown from TnReloadValue, after the counter value has reached the value zero. Set to logic 0 the timer decrements to zero and stops. The bit Timer2IRq is set to logic 1 when the timer reaches zero
2	-	RFU
1 to 0	T2Clk	00b: The timer input clock is 13.56 MHz. 01b: The timer input clock is 212 kHz. 10b: The timer input clock is an underflow of timer 0 11b: The timer input clock is an underflow of timer 1

9.8.11 T2ReloadHi_Reg

High byte of the reload value of Timer2.

Table 69: T2ReloadHi_Reg register (address 1Ah); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T2ReloadHi							
Access rights	r/w							

Table 70: Description of TnReload_Reg bits

Bit	Symbol	Description
7 to 0	T2ReloadHi	Defines the high byte of the reload value of the timer 2. With the start event the timer load the value of the T2ReloadValHi_Reg and T2ReloadValLo_Reg. Changing this register affects the timer only at the next start event.

9.8.12 T2ReloadLo_Reg

Low byte of the reload value of Timer2.

Table 71: T2ReloadLo_Reg register (address 1Bh); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	T2ReloadLo							
Access rights	r/w							

Table 72: Description of T2ReloadLo_Reg bits

Bit	Symbol	Description
7 to 0	T2ReloadLo	Defines the low byte of the reload value of the timer 2. With the start event the timer load the value of the T2ReloadValHi_Reg and T2RelaodVaLo_Reg. Changing this register affects the timer only at the next start event.

9.8.13 T2CounterValHi_Reg

High byte of the counter register of timer 2.

Table 73: T2CounterValHi_Reg register (address 1Ch); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T2CounterHi							
Access rights	r/w							

Table 74: Description of T2CounterValHi_Reg bits

Bit	Symbol	Description
7 to 0	T2Counter ValHi	High byte current counter value of timer 2. This value shall not be read out during receive.

9.8.14 T2CounterValLoReg

Low byte of the current value of Timer 2.

Table 75: T2CounterValLo_Reg register (address 1Dh); reset value:00h

Bit	7	6	5	4	3	2	1	0
Symbol	T2CounterValLo							
Access rights	r/w							

Table 76: Description of T2CounterValLo_Reg bits

Bit	Symbol	Description
7..0	T2Counter ValLo	Low byte of the current counter value of timer 2. This value shall not be read out during receive.

9.8.15 T3Control_Reg

Control register of the Timer 3.

Table 77: T3Control_Reg register (address 1Eh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T3Stop Rx	-	T3Start		T3Auto Restart	-	T3Clk	
Access rights	r/w	RFU	r/w		r/w	RFU	r/w	

Table 78: Description of T3Control_Reg bits

Bit	Symbol	Description
7	T3StopRx	If set to one, the timer stops immediately after receiving the first data. Set to logic 0, indicates that the timer is not stopped automatically. Note: If LFO Trimming is selected by T3Start, this bit has no effect
6	-	RFU
5 to 4	T3Start	00b - timer is not started automatically 01b - timer starts automatically at the end of the transmission 10b - timer is used for LFO trimming without underflow (Start/Stop on PosEdge) 11b - timer is used for LFO trimming with underflow (Start/Stop on PosEdge)
3	T3AutoRestart	Set to logic 1, the timer automatically restarts its countdown from TnReloadValue, after the counter value has reached the value zero. Set to logic 0 the timer decrements to zero and stops. The bit Timer1IRq is set to logic 1 when the timer reaches zero
2	-	RFU
1 to 0	T3Clk	00b - the timer input clock is 13.56 MHz. 01b - the timer input clock is 212 kHz. 10b - the timer input clock is an underflow of timer 0 11b - the timer input clock is an underflow of timer 1

9.8.16 T3ReloadHi_Reg

High byte of the reload value of Timer3.

Table 79: T3ReloadHi_Reg register (address 1Fh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T3ReloadHi							
Access rights	r/w							

Table 80: Description of T3ReloadHi_Reg bits

Bit	Symbol	Description
7 to 0	T3ReloadHi	Defines the high byte of the reload value of the timer 3. With the start event the timer load the value of the T3ReloadValHi_Reg and T3ReloadValLo_Reg. Changing this register affects the timer only at the next start event.

9.8.17 T3ReloadLo_Reg

Low byte of the reload value of timer 3.

Table 81: T3ReloadLo_Reg register (address 20h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	T3ReloadLo							
Access rights	r/w							

Table 82: Description of T3ReloadLo_Reg bits

Bit	Symbol	Description
7 to 0	T3ReloadLo	Defines the low byte of the reload value of timer 3. With the start event the timer load the value of the T3ReloadValHi_Reg and T3RelaodValLo_Reg. Changing this register affects the timer only at the next start event.

9.8.18 T3CounterValHi_Reg

High byte of the current counter value the 16 bit timer 3.

Table 83: T3CounterValHi_Reg register (address 21h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T3CounterHi							
Access rights	r/w							

Table 84: Description of T3CounterValHi_Reg bits

Bit	Symbol	Description
7 to 0	T3Counter ValHi	High byte of the current counter value of timer 3. This value shall not be read out during receive.

9.8.19 T3CounterValLo_Reg

Low byte of the current counter value the 16 bit Timer3.

Table 85: T3CounterValLo_Reg register (address 22h); reset value:00h

Bit	7	6	5	4	3	2	1	0
Symbol	T3CounterValLo							
Access rights	r/w							

Table 86: Description of T3CounterValLo_Reg bits

Bit	Symbol	Description
7 to 0	T3Counter ValLo	Low byte current counter value of timer 3. This value shall not be read out during receive.

9.8.20 T4Control_Reg

The wake-up timer T4 activates the system after a given time. It can start a low power card detection

Table 87. T4Control_Reg register (address 23h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T4 Running	T4Start StopNow	T4Auto Trimm	T4Auto LPCD	T4Auto Restart	T4Auto WakeUp	T4Clk	
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	

Table 88: Description of T4Control_Reg bits

Bit	Symbol	Description
7	T4Running	Shows if the timer 4 is running. If the bit T4StartStopNow is set, this bit and the timer can be controlled.
6	T4Start StopNow	Set to logic 1, the bit T4Running can be written
5	T4AutoTrimm	If set to one, the timer activates an LPO trimming procedure when it underflows. For the T4AutoTrimm function, at least one timer (T0…T3) has to be configured properly for trimming (T3 is not allowed if T4AutoLPCD is set in parallel).
4	T4AutoLPCD	If set to one, the timer activates a low power card detection sequence. If a card is detected an irq is raised and the system remains active if enabled. If no card is detected the CLRC663 enters the power down state if enabled. The timer is automatically restarted (no gap). Timer 3 is used to specify the time where the RF field is enabled to check if a card is present. Therefor you may not use Timer 3 for T4AutoTrimm in parallel.
3	T4AutoRestart	Set to logic 1, the timer automatically restarts its countdown from T4ReloadValue, after the counter value has reached the value zero. Set to logic 0 the timer decrements to zero and stops. The bit Timer4Irq is set to logic 1 when the timer reaches zero
2	T4Auto WakeUp	If set, the CLRC663 wakes up automatically, when the timer T4 has an underflow. This bit has to be set if the IC should enter the power down state after T4AutoTrimm and/or T4AutoLPCD is finished and no card has been detected. If the IC should stay active after one of these procedure this bit has to be set to 0.
1 to 0	T4Clk	00b - the timer input clock is the LFO clock 01b - the timer input clock is the LFO clock/8 10b - the timer input clock is the LFO clock/16 11b - the timer input clock is the LFO clock/32

9.8.21 T4ReloadHi_Reg

High byte of the reload value of the 16 bit timer 4.

Table 89: T4ReloadHi_Reg register (address 24h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T4ReloadHi							
Access rights	r/w							

Table 90: Description of T4ReloadHi_Reg bits

Bit	Symbol	Description
7 to 0	T4ReloadHi	Defines high byte of the for the reload value of timer 4. With the start event the timer 4 loads the T4ReloadVal. Changing this register affects the timer only at the next start event

9.8.22 T4ReloadLo_Reg

Low byte of the reload value of the 16 bit timer 4.

Table 91: T4ReloadLo_Reg register (address 25h); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	T4ReloadLo							
Access rights	r/w							

Table 92: Description of T4ReloadLo_Reg bits

Bit	Symbol	Description
7 to 0	T4ReloadLo	Defines the low byte of the reload value of the timer 4. With the start event the timer loads the value of the TnReloadVal. Changing this register affects the timer only at the next start event.

9.8.23 T4CounterValHi_Reg

High byte of the counter value of the 16 bit timer 4.

Table 93: T4CounterValHi_Reg register (address 26h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	T4ReloadHi							
Access rights	r/w							

Table 94: Description of T4CounterValHi_Reg bits

Bit	Symbol	Description
7 to 0	T4Counter ValHi	High byte of the current counter value of timer 4.

9.8.24 T4CounterValLo_Reg

Low byte of the counter value of the 16 bit timer 4.

Table 95: T4CounterValLo_Reg register (address 27h); reset value:00h

Bit	7	6	5	4	3	2	1	0
Symbol	T4CounterValLo							
Access rights	r/w							

Table 96: Description of T4CounterValLo_Reg bits

Bit	Symbol	Description
7 to 0	T4Counter ValLo	Low byte of the current counter value of the timer 4.

9.9 Description/Transmitter register

9.9.1 TxMode_Reg

Table 97. DrvMode_Reg register (address 28h); reset value: 86h

Bit	7	6	5	4	3	2	1	0
Symbol	Tx2Inv	Tx1Inv	-	-	TxEn	TxClk Mode		
Access rights	r/w	r/w	RFU	RFU	r/w	r/w		

Table 98: Description of DrvMode_Reg bits

Bit	Symbol	Description
7	Tx2Inv	Inverts transmitter Tx2 at TX2 pin
6	Tx1Inv	Inverts transmitter Tx1 at TX1 pin
5	-	RFU
4	-	RFU
3	TxEn	If set to 1 both transmitter pins are enabled
2 to 0	TxClkMode	Transmitter clock settings: refer to Table 220 “Settings for TX1/2”

9.9.2 TxAmp_Reg

Table 99. TxAmp_ Reg register (address 29h); reset value: 15h

Bit	7	6	5	4	3	2	1	0
Symbol	set_cw_amplitude		-	set_residual_carrier				
Access rights	r/w		RFU	r/w				

Table 100. Description of TxAmp_Reg bits

Bit	Symbol	Description
7 to 6	set_cw_amplitude	0: tvdd - 100 mV 1: tvdd - 250 mV 2: tvdd - 500 mV 3: tvdd - 1 V Note: if Cwmax is set to 1, set_cw_amplitude has no influence onto the continuous amplitude
5	-	RFU
4 to 0	set_residual_ carrier	Set the residual carrier percentage. refer to Section 11.2

9.9.3 TxCon_Reg

Table 101. TxCon_Reg register (address 2Ah); reset value: 11h

Bit	7	6	5	4	3	2	1	0
Symbol	OvershootT2				Cw max	Tx Inv	TxSel	
Access rights	r/w				r/w	r/w	r/w	

Table 102: Description of DrvCon_Reg bits

Bit	Symbol	Description
7 to 4	OvershootT2	Specifies the length (number of carrier clocks) of the additional modulation for overshoot prevention. Refer to Section 11.2.1 "Overshoot protection"
3	Cwmax	Set amplitude of continuous wave carrier to the maximum. If set to1, set_cw_amplitude has no influence on the continuous amplitude.
2	TxInv	If set to 1, the resulting modulation signal (which is defined by TxSel is inverted
1 to 0	TxSel	Defines which signal is used as source for modulation 00b...Low 01b...TxEnvelope 10b...SigIn 11b...RFU

9.9.4 TxI_Reg

Table 103. TxI_Reg register (address 2Bh); reset value: 06h

Bit	7	6	5	4	3	2	1	0
Symbol	OvershootT1				tx_set_iiLoad			
Access rights	r/w				r/w			

Table 104: Description of TxI Reg bits

Bit	Symbol	Description
7 to 4	OvershootT1	Overshoot value for timer 1. Refer to Section 11.2.1 "Overshoot protection"
3 to 0	tx_set_iLoad	Settings for set_iload and corresponding assumed Tx-load current. Default setting: Ah **Remark:** 0h is not allowed;

9.10 Description/CRC register

9.10.1 TxCrcCon_Reg

Table 105. TXCrcOn_Reg register (address 2Ch); reset value: 18h

Bit	7	6	5	4	3	2	1	0
Symbol	-	TXPresetVal			TxCRCtype		TxCRC Invert	TxCRC En
Access rights	RFU	r/w			r/w		r/w	r/w

Table 106: Description of TcCrcOn_Reg bits

Bit	Symbol	Description
7	-	RFU
6 to 4	TXPresetVal	Specifies the CRC preset value (hex) for transmission. | CRC16 CRC8 CRC5 ---------- 000b | 0000……..00……..00 001b | 6363……..12……..12 010b | A671……..BF……..RFU 011b | FFFE……FD……..RFU 100b | RFU…….. RFU……...RFU 101b | RFU…… RFU……...RFU 110b | User Def. …….User Def. ….User Def. 111b | FFFF……FF……...1F
3 to 2	TxCRCtype	Defines which type of CRC (CRC8/CRC16/CRC5) is calculated: 00b:…… CRC5 is calculated 01b:…… CRC8 is calculated 10b:…… CRC16 is calculated 11b:…… RFU
1	TxCRCInvert	if set to 1, the resulting CRC is inverted and attached to the data frame (ISO/IEC 3309)
0	TxCRCEn	if set to 1, a CRC is appended to the data stream

9.10.2 RxCrcCon_Reg

Table 107. RxCrcCon_Reg register (address 2Dh); reset value: 18h

Bit	7	6	5	4	3	2	1	0
Symbol	RxForce CRCWrite	RXPresetVal			RXPresetVal		RxCRCInvert	RxCRCEn
Access rights	r/w	r/w			r/w		r/w	r/w

Table 108: Description of RxCrcCon_Reg bits

Bit	Symbol	Description
7	RxForceCrc Write	Set to 1, the received CRC byte(s) are written to FiFo. (if this bit is set to 0) CRC Bytes are only checked, but not written to FiFo. This bit has to be always set in case of a not byte aligned CRC (e.g. ISO/IEC 18000-3 Mode3)
6 to 4	RXPresetVal	Specifies the CRC preset value (hex) for transmission. | CRC16 CRC8 CRC5 ---------- 000b | 0000……..00……...00 001b | 6363……..12……...12 010b | A671……..BF……..RFU 011b | FFFE……..FD……..RFU 100b | RFU…….. RFU……...RFU 101b | RFU…… RFU……...RFU 110b | User Def. …….User Def. ….User Def. 111b | FFFF……..FF……...1F
3 to 2	RxCRCtype	Defines which type of CRC (CRC8/CRC16/CRC5) is calculated: 00b:…… CRC5 is calculated 01b:…… CRC8 is calculated 10b:…… CRC16 is calculated 11b:…… RFU
1	RxCrcInvert	If set to 1, the CRC check is done for the inverted CRC.
0	RxCrcEn	If set to 1, the CRC is checked and in case of a wrong CRC an error flag is set. Otherwise the CRC is calculated but the error flag is not modified.

9.11 Description/Transmitter register

9.11.1 TxDataNum_Reg

Table 109: TxDataNum_Reg register (address 2Eh); reset value: 0Fh

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	KeepBit Grid	DataEn	TxLastBits		
Access rights	RFU	RFU	RFU	r/w	r/w	r/w		

Table 110: Description of TxDataNum_Reg bits

Bit	Symbol	Description
7-5	RFU	-
4	KeepBitGrid	If set, the time between consecutive transmissions starts is a multiple of the ETU. Depending on the DCodeType settings one ETU is defined as follows: 4h - 7h - 37.76 μs (26 kHz)(EPC/UID) 8h - 37.76 μs (26 kHz)(1 out of 4) 9h - Bh - 604.16 μs (1.6 kHz)(1 out of 256) Ch (DBFreq = 106 kHz) - 18.88 μs (53 kHz)(EPCv2) Ch (DBFreq = 212 kHz) - 9.44 μs (106 kHz)(EPCv2) Others - 1/DBFreq
3	DataEn	If set to 0 - it is possible to send only a symbol pattern If set to 1 - also data is sent (be aware - that it is not possible to send only two symbols)
2 to 0	TxLastBits	Defines how many bits of the last data byte to be sent. If set to 000b all bits of the last data byte are sent. Note - bits are skipped at the end of the byte. Example - Data byte B2h (sent LSB first). TxLastBits = 011b (0x3) => 010b (LSB first) is sent TxLastBits = 110b (0x6) => 010011b (LSB first) is sent

9.11.2 TxDATAModWidth_Reg

Transmitter mode width register

Table 111: TxDataModWidth_Reg register (address 2Fh); reset value: 27h

Bit	7	6	5	4	3	2	1	0
Symbol	DModWidth							
Access rights	r/w							

Table 112: Description of TxDataModWidth_Reg bits

Bit	Symbol	Description
7 to 0	DModWidth	Specifies the length of a pulse for sending data with enabled pulse modulation. The length is given by the number of carrier clocks + 1. A pulse can never be longer than from the start of the pulse to the end of the bit. The starting position of a pulse is given by the setting of TxDataMod.DPulseType. Note: This register is only used if Miller modulation (ISO/IEC 14443A PCD) is used. The settings are also used for the ModWidth of start and/or stop symbols.

9.11.3 TxSym10BurstLen_Reg

Table 113. TxSym10BurstLen_Reg register (address 30h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	Sym1Burst Len			-	Sym0Burst Len		
Access rights	RFU	r/w			RFU	r/w		

Table 114: Description of TxSym10BurstLen_Reg bits

Bit	Symbol	Description
6 to 4	Sym1Burst Len	Specifies the number of bits issued for symbol 1 burst. The 3 bits encodes a range from 8 to 256 bit
2 to 0	Sym0Burst Len	Specifies the number of valid bits of the symbol definition of symbol0. The range is from 1 bit (value 0000b) to 16 bit (value 1111b)

9.11.4 TxWaitCtrl_Reg

Table 115. TxWaitCtrl_Reg register (address 31h); reset value: C0h

Bit	7	6	5	4	3	2	1	0
Symbol	TxWait Start	TxWait Etu	TxWait High.10	TxWait High.9	TxWait High.8	TxStopBitLength		
Access rights	r/w	r/w	r/w	r/w	r/w	r/w		

Table 116: Description of TXWaitCtrl_Reg bits

Bit	Symbol	Description
7	TxWait Start	If set to 0, the TxWait time is starting at the End of the send data (TX) If set to 1, the TxWait time is starting at the End of the received data (RX)
6	TxWaitEtu	If set to 0, the TxWait time is TxWait × 16/13.56 MHz If set to 1, the TxWait time is TxWait × (0.5/DBFreq)
5 to 3	TxWait High	Higher 3 bits of TxWait.
2 to 0	TxStopBit Length	Defines number of stop-bits (= stop-bit + EGT) to be send 000b: no stop-bit, no EGT 001b: stop-bit, no EGT 010b: stop-bit + 1 EGT 011b: stop-bit + 2 EGT 100b: stop-bit + 3 EGT 101b:stop-bit + 4 EGT 110b: stop-bit + 5 EGT 111b: stop-bit + 6 EGT Note: This is only valid for ISO/IEC14443 Type B

9.11.5 TxWaitLo_Reg

Table 117. TxWaitLo_Reg register (address 32h); reset value: 12h

Bit	7	6	5	4	3	2	1	0
Symbol	TxWaitLo							
Access rights	r/w							

Table 118: Description of TxWaitLo_Reg bits

Bit	Symbol	Description
7 to 0	TxWaitLo	Defines the minimum time between receive and send or between two send data streams Note: TxWait is a 11bit register (additional 3 bits are in the TxWaitCtrl register)! See also TxWaitEtu and TxWaitStart.

9.11.6 FrameCon_Reg

Table 119. FrameCon_Reg register (address 33h); reset value: CFh

Bit	7	6	5	4	3	2	1	0
Symbol	TxParityEn	RxParityEn	-	-	StopSym		StartSym	
Access rights	r/w	r/w	RFU	RFU	r/w		r/w	

Table 120: Description of FrameCon_Reg bits

Bit	Symbol	Description
7	TxParityEn	If HIGH, a parity bit is calculated and appended to each byte transmitted
6	RxParityEn	Defines which type of parity-bit is calculated. 0b: even parity 1b: odd parity
5 to 4	-	-
3 to 2	StopSym	Defines which symbol should be sent as stop-symbol 00b: No Symbol is sent 01b: Symbol1 is sent 10b: Symbol2 is sent 11b: Symbol3 is sent
1 to 0	StartSym	Defines which symbol should be sent as start-symbol 00b: No symbol is sent 01b: Symbol0 is sent 10b: Symbol1 is sent 11b: Symbol2 is sent

9.12 Description/Receiver register

9.12.1 RxSofD_Reg

Table 121. RxSofD_Reg register (address 34h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	SOF_En	SOF Detected	-	SubC_ En	SubC_ Detected	SubC_ Present
Access rights	RFU	RFU	r/w	r/w	RFU	r/w	r/w	r/w

Table 122: Description of RxSofD_Reg bits

Bit	Symbol	Description
7 to 6	-	RFU
5	SOF_En	If set and a SOF is detected an RxSOFIrq is raised
4	SOF_Detected	Shows that a SOF is or was detected. Can be cleared by SW
3	-	RFU
2	SubC_En	If set and a subcarrier is detected an RxSOFIrq is raised.
1	SubC_Detected	Shows that a subcarrier is or was detected. Can be cleared by SW
0	SubC_Present	Shows that a subcarrier is currently detected.

9.12.2 RxCtrl_Reg

Table 123. RxCtrl_Reg register (address 35h); reset value: 04h

Bit	7	6	5	4	3	2	1	0
Symbol	RxAllow Bits	Rx Multiple	RxEOF Type	EGT_ Check	EMD_ Sup	Baud rate		
Access rights	r/w	r/w	r/w	r/w	r/w	r/w		

Table 124: Description of RxCtrl_Reg bits

Bit	Symbol	Description
7	RxAllowBits	If set to 1, data is written into FiFo even if CRC is enabled, and no complete byte has been received. This causes a data integrity error, because the CRC is not correct
6	RxMultiple	If set to 1, RxMultiple is activated and the receiver will not terminate automatically (refer Section 18.3.1.6 “Receive command”)
5	RxEOFType	If set to 0, an EOF as defined in the RxEOFSymbolReg is expected. If set to 1, an ISO/IEC14443B EOF is expected. Note: Setting this bit to 0 and additionally setting the 2 LSB in the RxEOFSymbolReg to 0, disables the EOF check

Table 124: Description of RxCtrl_Reg bits

Bit	Symbol	Description
4	EGT_Check	If set to 1, the EGT is checked and if it is too long a protocol error is set. (This is only valid for ISO/IEC14443 Type B)
3	EMD_Sup	Enables the EMD suppression according ISO/IEC14443. If an error occurs within the first three bytes, this frame is seen as EMD and ignored. If RxForceCRCWrite is set, the FIFO should not be read out before three bytes are written into. The FIFO is cleared automatically in case of an EMD error. A collision is treated as error.
2 to 0	Baudrate	Defines the baud rate of the receiving signal. 000b: RFU 001b: RFU 010b: 26 kBd 011b: 52 kBd 100b: 106 kBd 101b: 212 kBd 110b: 424 kBd 111b: 847 kBd

9.12.3 RxWait_Reg

Selects internal receiver settings.

Table 125. RxWait_Reg register (address 36h); reset value: 90h

Bit	7	6	5	4	3	2	1	0
Symbol	RxWaitEtu	RxWait						
Access rights	r/w	r/w						

Table 126: Description of RxWait_Reg bits

Bit	Symbol	Description
7	RXWaitEtu	If set to 0, the RxWait time is RxWait × 16/13.56 MHz If set to 1, the RxWait time is RxWait × (0.5/DBFreq)
6 to 0	RxWait	Defines the time after sending, where every input is ignored.

9.12.4 RxThreshold_Reg

Selects minimum threshold level for the bit decoder.

Table 127: RxThreshold_Reg register (address 37h); reset value: 3Fh

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel				MinLevelP			
Access rights	r/w				r/w			

Table 128: Description of RxThreshold_Reg bits

Bit	Symbol	Description
7 to 4	MinLevel	Defines the MinLevel of the reception. Note: The MinLevel should be higher than the noise level in the system
3 to 0	MinLevelP	Defines the MinLevel of the phase shift detector unit

9.12.5 Rcv_Reg

Table 129. Rcv_Reg register (address 38h); reset value: 12h

Bit	7	6	5	4	3	2	1	0
Symbol	Rcv_Rx_single	-	sigpro_in_sel		-		CollLevel	
Access rights	r/w	RFU	r/w		RFU		r/w	

Table 130: Description of Rcv_Reg bits

Bit	Symbol	Description
7	Rcv_Rx_single	Single rx Input Pin Mode; 0 -> Fully Differential; 1 -> Quasi-Differential
6	-	RFU
5 to 4	sigpro_in_sel	Defines input for the signal processing unit 00b - idle 01b - internal analogue block (RX) 10b - signal in over envelope 11b - signal in over s3c-generic
3 to 2	-	RFU
1 to 0	CollLevel	Defines how strong a signal must be to be interpreted as a collision. 00b - Collision has at least 1/8 of signal strength 01b - Collision has at least 1/4 of signal strength 10b - Collision has at least 1/2 of signal strength 11b - Collision detection is switched off.

9.12.6 RxAna_Reg

Table 131. RxAna_Reg register (address 39h); reset value: 0Ah

Bit	7	6	5	4	3	2	1	0
Symbol	VMid_r_sel		-	-	rcv_hpcf		rcv_gain	
Access rights	r/w		RFU	RFU	r/w		r/w	

Table 132: Description of RxAna_Reg bits

Bit	Symbol	Description
7, 6	VMid_r_setl	Selection of resistance between VDD and VSS: 00h->1.4 kΩ (recommended); 01h->2.8 kΩ; 10h->5.7 kΩ; 11h->11 kΩ
5, 4	-	RFU
3, 2	rcv_hpcf	The rcv_hpcf [1:0] signals allow 4 different settings of the base band amplifier lower cut-off frequency from ~40 kHz to ~300 kHz.
1 to 0	rcv_gain	With rcv_gain[1:0] four different gain settings from 30 dB and 60 dB can be configured (differential output voltage/differential input voltage)

9.13 Description/Clock register

9.13.1 SerialSpeed_Reg

Table 133. SerialSpeed_Reg register (address3Bh); reset value: 7Ah

Bit	7	6	5	4	3	2	1	0
Symbol	BR_T0			BR_T1				
Access rights	r/w			r/w				

Table 134: SerialSpeed_Reg bits

Bit	Symbol	Description
7 to 5	BR_T0	if BR_T0 = 0: transfer speed = 27.12 MHz / (BR_T1 + 1) if BR_T0 > 0: transfer speed = 27.12 MHz / (BR_T1 + 33) / 2^(BR_T0 – 1) Refer to Section 10.3.1
4 to 0	BR_T1	if BR_T0 > 0: transfer speed = 27.12 MHz / (BR_T1 + 33) / 2^(BR_T0 – 1) refer to digital interfaces UARD Refer to Section 10.3.1

9.13.2 LPO_Trimm_Reg

Table 135. LPO_Trim_Reg register (address 3Ch); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	lpo_trimm							
Access rights	r/w							

Table 136: LPO_Trim_Reg bits

Bit	Symbol	Description
7 to 0	lpo_trimm	Trimm value. Refer to Section 16.3 “Low Power Oscillator (LPO)” Note: If the trimm value is increased, the frequency of the oscillator decreases

9.13.3 PLL_Ctrl_Reg Register

Control register for the IntegerN PLL.

Table 137. PLL_Ctrl_Reg register (address3Dh); reset value: 04h

Bit	7	6	5	4	3	2	1	0
Symbol	CLKOutSel				ClkOut_En	PLL_PD	PLL_DivFB	
Access rights	r/w				r/w	r/w	r/w	

Table 138: Description of PLL_Ctrl_Reg register bits

Bit	Symbol	Description
7 to 4	CLKout	0000h.0001h... The Pin ClkOut is not used as Clock Output. It is used as IO 0010b - pin ClkOut is hold on 0 0011b - pin ClkOut is hold on 1 0011b - pin ClkOut shows the output of the analog PLL 0100b - pin ClkOut shows 27.12 MHz from the crystal 0101b - pin ClkOut shows 13.56 MHz derived from the crystal 0110b - pin ClkOut shows 6.78 MHz derived from the crystal 0111b - pin ClkOut shows 3.39 MHz derived from the crystal 1000b - pin ClkOut is toggled by the timer 0 overflow 1001b - pin ClkOut is toggled by the timer 1 overflow 1010b - pin ClkOut is toggled by the timer 2 overflow 1011b - pin ClkOut is toggled by the timer 3 overflow 1100b-1111b RFU
3	ClkOut_En	Enables the clock at Pin ClkOut
2	PLL_PD	PLL power down
1-0	PLL_DivFD	PLL feedback divider

9.13.4 PLL_Div_Out_Reg

Table 139. PLL_Div_Out_Reg register (address 3Eh); reset value: 20h

Bit	7	6	5	4	3	2	1	0
Symbol	PLLDiv_Out							
Access rights	r/w							

Table 140: PLLDiv_Out_Reg bits

Bit	Symbol	Description
7-0	PLLDiv_Out	PLL output divider factor; Refer to Section 16.2

9.14 Description/LPCD register

9.14.1 LPCD_Qmin_Reg

Table 141. LPCD_QMin_Reg register (address 3Fh); reset value: 48h

Bit	7	6	5	4	3	2	1	0
Symbol	LPCD_IMax.5	LPCD_IMax.4	LPCD_QMin					
Access rights	dy/r/w	r/w	r/w					

Table 142: LPCD_QMin_Reg bits

Bit	Symbol	Description
7, 6	LPCD_IMax	Defines the highest two bits of the higher border for the LPCD. If the measurement value of the I channel is higher than LPCD IMax, a LPCD IRQ is raised
5 to 0	LPCD_QMin	Defines the lower border for the LPCD. If the measurement value of the Q channel is higher than LPCD QMin, a LPCD IRQ is raised

9.14.2 LPCD_QMax_Reg

Table 143. LPCD_QMax_Reg register (address 40h); reset value: 12h

Bit	7	6	5	4	3	2	1	0
Symbol	LPCD_IMax.3	LPCD_IMax.2	LPCD_QMax					
Access rights	dy/r/w	r/w	r/w					

Table 144: LPCD_QMax_Reg bits

Bit	Symbol	Description
7 to 6	LPCD_IMax.3-.2	Defines the mid two bits of the higher border for the LPCD. If the measurement value of the I channel is higher than LPCD IMax, a LPCD IRQ is raised
5 to 0	LPCD_QMax	Defines the higher border for the LPCD. If the measurement value of the Q channel is higher than LPCD QMax, a LPCD IRQ is raised

9.14.3 LPCD_IMin_Reg

Table 145. LPCD_IMin_Reg register (address 41h); reset value: 88h

Bit	7	6	5	4	3	2	1	0
Symbol	LPCD_IMax.1	LPCD_IMax.0	LPCD_IMin					
Access rights	dy/r/w	r/w	r/w					

Table 146: LPCD_IMin_Reg bits

Bit	Symbol	Description
7 to 6	LPCD_IMax	Defines lowest two bits of the higher border for the LPCD. If the measurement value of the I channel is higher than LPCD IMax, a LPCD IRQ is raised.
5 to 0	LPCD_IMin	Defines the lower border for the LPCD. If the measurement value of the I channel is lower than LPCD IMin, a LPCD IRQ is raised.

9.14.4 LPCD_I_Result_Reg

Table 147. LPCD_I_Result_Reg register (address 42h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	LPCD_I_Result					
Access rights	RFU	RFU	r					

Table 148: LPCD_I_Result_Reg bits

Bit	Symbol	Description
7 to 6	-	RFU
5 to 0	LPCD_I_Result	Shows the result of the last LPCD (I-Channel)

9.14.5 LPCD_Result_Q_Reg

Table 149. LPCD_Result_Q_Reg register (address 43h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	LPCD_Irq_Clr	LPCD_Reslult_Q					
Access rights	RFU	dy/r/w	r					

Table 150: LPCD_Q_Result_Reg bits

Bit	Symbol	Description
7	-	RFU
6	LPCD_Irq_Clr	If set no LPCD IRQ is raised any more until the next LPCD procedure. Can be used by software to clear the interrupt source
5 to 0	LPCD_Q_Result	Shows the result of the last LPCD (Q-Channel)

9.15 Description/PAD register

9.15.1 PadEn_Reg

Table 151. PadEn_Reg register (address 44h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	GPIO0_En	CLKOUT_En	IFSEL1_En	IFSEL0_En	TCK_En	TDI_En	TDO_En	TMS_En
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 152: PadEn_Reg bits

Bit	Symbol	Description
7	GPIO0_En	Enables the output functionality of the GPIO0 pin
6	CLKOUT_En	Enables the output functionality of the CLKOUT pin
5	IFSEL1_EN	Enables the output functionality of the IFSEL1 pin
4	IFSEL0_EN	Enables the output functionality of the IFSEL0 pin
3	TCK_En	Enables the output functionality of the TCK of the boundary scan interface
2	TMI_En	Enables the output functionality of the TMI of the boundary scan interface
1	TDO_En	Enables the output functionality of the TDO of the boundary scan interface
0	TMS_EN	Enables the output functionality of the TMS of the boundary scan interface

9.15.2 PadOut_Reg

Table 153. PadOut_Reg register (address 45h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	GPIO0_Out	CLKOUT_Out	IFSEL1_Out	IFSEL0_Out	TCK_Out	TMI_Out	TDO_Out	TMS_Out
Access rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Table 154: PadOut_Reg bits

Bit	Symbol	Description
7	GPIO0_OUT	Output buffer of the GPIO0/SIGIN pin
6	CLKOUT_OUT	Output buffer of the CLKOUT pin
5	IFSEL1_OUT	Output buffer of the IFSEL1 pin
4	IFSEL0_OUT	Output buffer of the IFSEL0 pin
3	TCK_OUT	Output buffer of the TCK pin
2	TDI_OUT	Output buffer of the TDI pin
1	TDO_OUT	Output buffer of the TDO pin
0	TMS_OUT	Output buffer of the TMS pin

9.15.3 PadIn_Reg

Table 155. PadIn_Reg register (address 46h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	GPIO0_In	CLKOUT_In	IFSEL1_In	IFSEL0_In	TCK_In	TDI_In	TDO_In	TMS_In
Access rights	r	r	r	r	r	r	r	r

Table 156: PadIn_Reg bits

Bit	Symbol	Description
7	GPIO0_In	Input buffer of the GPIO0/SIGIN pin
6	CLKOUT_In	Input buffer of the CLKOUT pin
5	IFSEL1_In	Input buffer of the IFSEL1 pin
4	IFSEL0_In	Input buffer of the IFSEL0 pin
3	TCK_In	Input buffer of the TCK pin
2	TDI_In	Input buffer of the TDI pin
1	TDO_In	Input buffer of the TDO pin
0	TMS_In	Input buffer of the TMS pin

9.15.4 SigOut_Reg

Table 157. SigOut_Reg register (address 47h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Pad Speed	-	-	-	SigOutSel			
Access rights	r/w	RFU	RFU	RFU	r/w			

Table 158: SigOut_Reg bits

Bit	Symbol	Description
7	PadSpeed	If set, the pads are operating faster. The edges are faster, but it can be a problem if a lot of pads are switching at the same time.
6 to 4	-	RFU
3 to 0	SIGOutSel	0000b, 0001b The pin SIGOUT is tristate 0010b The pin SIGOUT is 0 0011b The pin SIGOUT is 1 0100b The pin SIGOUT shows the TX-envelope 0101b The pin SIGOUT shows the TX-active signal 0110b The pin SIGOUT shows the S3C (generic) signal 0111b The pin SIGOUT shows the RX-envelope (only valid for ISO/IEC 14443A, 106 kBd) 1000b The pin SIGOUT shows the RX-active signal 1001b The pin SIGOUT shows the RX-bit signal

9.16 Description/Transmitter symbol register

9.16.1 TxBitMod_Reg

Table 159. TxBitMod_Reg register (address 48h); reset value: 20h

Bit	7	6	5	4	3	2	1	0
Symbol	TxMSB First	-	TxParity Type	-	TxStopBit Type	-	TxStart BitType	TxStart BitEn
Access rights	r/w	RFU	r/w	RFU	r/w	RFU	r/w	r/w

Table 160: Description of TxBitMod_Reg bits

Bit	Symbol	Description
7	TxMSBFirst	If set to 1, data bytes are interpreted MSB first for data transmission, which means data is converted. If this bit is set to 0, data is interpreted LSB first.
6	-	RFU
5	TxParityType	Defines the type of the parity bit. If set to 1, odd parity is calculated, otherwise even parity is calculated
4	-	RFU
3	TxStopBitType	Defines the type of the stop-bit (0b: logic zero / 1b: logic one)

Table 160: Description of TxBitMod_Reg bits *...continued*

Bit	Symbol	Description
2	-	RFU
1	TxStartBitType	Defines the type of the start-bit (0b: logic zero / 1b: logic one)
0	TxStartBitEn	If set to 1, a start-bit will be sent

9.16.2 TxDataCon_Reg

Table 161. TxDataCon_Reg (address 4Ah); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	DCodeType				DSCFreq	DSCFreq		
Access rights	r/w				r/w	r/w		

Table 162: Description of TxDataCon_Reg bits

Bit	Symbol	Description
7 to 4	DCodeType	specifies the type of encoding of data to be used 0000b - no special coding 0001b - collider datastream is decoded 0010b - RFU 0011b - RFU 0100b - return to zero code - pulse at first position 0101b - return to zero code - pulse at 2nd position 0110b - return to zero code - pulse at 3rd position 0111b - return to zero code - pulse at 4th position 1000b - 1 out of 4 coding 1001b - 1 out of 256 code (range 0 - 255) [I-CODE SLI] 1010b - 1 out of 256 code (range 0 - 255; 0x00 is encoded with no modulation, value 256 not used) [I-CODE 1] 1011b - 1 out of 256 code (range 0 - 255; 0x00 is encoded with a pulse on last position) [I Code quite value] 1100b - Pulse internal encoded (PIE) [ISO(IEC18000-3 Mode 3] 1101b - RFU 1110b - RFU 1111b - RFU
3	DSCFreq	Specifies the subcarrier frequency of the used envelope. 0b 424 kHz 1b 848 kHz Note: This setting is only relevant if an envelope is used which involves a subcarrier, e.g. Manchester with subcarrier coding.
2 to 0	DBFreq	Specifies the frequency of the bit stream 000b - RFU 001b - RFU 010b - 26 kHz 011b - 53 kHz 100b - 106 kHz 101b - 212 kHz 110b - 424 kHz 111b - 848 kHz

9.16.3 TxDataMOD_Reg

Table 163. TxDataMod_Reg register (address 4Bh); reset value:04h

Bit	7	6	5	4	3	2	1	0
Symbol	Frame step	DMillerEn	DPulseType		DInvert	DEnvType		
Access rights	r/w	r/w	r/w		r/w	r/w		

Table 164: Description of TxDataMod_Reg bits

Bit	Symbol	Description
7	Framestep	If set to 1, at every start of transmission, each byte of data is sent in a separate frame. SOF and EOF is appended to the data byte according to the framing settings. After one byte is transmitted, the TxEncoder waits for a new start trigger to continue with the next byte (trigger is generated automatically). If set to 0, transmission is done in the used way, where after a start trigger all data bytes are sent and the framing is done for the complete data stream only once.
6	DMillerEn	If set to 1, pulse modulation is applied according to modified miller code. Note: This bit shall only be set if DPulseType is set to 01(bin)
5 to 4	DPulseType	Specifies which type of pulse modulation is selected. 00b: no pulse modulation 01b: pulse starts at beginning of bit 10b: pulse starts at beginning of second bit half 11b: pulse starts at beginning of third bit quarter Note: If DMillerEn is set to 1, DPulseType must be set to 01b
3	DInvert	If set to 1, the output envelope is inverted.
2 to 0	DEnvType	Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b: Direct output 001b: Manchester code 010b: Manchester code with subcarrier 011b: BPSK 100b: RZ (pulse of half bit length at beginning of second half of bit) 101b: RZ (pulse of half bit length at beginning of bit) 110b: RFU 111b: RFU

9.16.4 TxSymFreq_Reg

Table 165. TxSymFreq_Reg (address 4Ch); reset value: 50h

Bit	7	6	5	4	3	2	1	0
Symbol	S32SC Freq	S32BFreq			S10SC Freq	S10B Freq		
Access rights	r/w	r/w			r/w	r/w		

Table 166: Description of TxSymFreq_Reg bits

Bit	Symbol	Description
7	S32SCFreq	Specifies the frequency of the subcarrier of symbol2 and symbol3 0b...424 kHz 1b...848 kHz
6 to 4	S32BFreq	Specifies the frequency of the bit stream of symbol2 and symbole3 000b...RFU 001b...RFU 010b...26 kHz 011b...53 kHz 100b...106 kHz 101b...212 kHz 110b...424 kHz 111b...848 kHz
3	S10SCFreq	Specifies the frequency of the subcarrier of symbol0 and symbol1 0b...424 kHz 1b...848 kHz
2 to 0	S10BFreq	Specifies the frequency of the bit stream of symbol0 and symbol1 000b...RFU 001b...RFU 010b...26 kHz 011b...53 kHz 100b...106 kHz 101b...212 kHz 110b...424 kHz 111b...848 kHz

9.16.5 TxSym0H_Reg

Table 167. TxSym0H_Reg (address 4Dh); reset value: 40h

Bit	7	6	5	4	3	2	1	0
Symbol	Symbol0_H							
Access rights	r/w							

Table 168: Description of TxSYM0H_Reg bits

Bit	Symbol	Description
7 to 0	Symbol0H	Higher 8 bits of symbol definition for Symbol0

9.16.6 TxSym0L_Reg

Table 169. TxSym0L_Reg (address 4Eh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Symbol0_L							
Access rights	r/w							

Table 170: Description of TxSYM0L_Reg bits

Bit	Symbol	Description
7 to 0	Symbol0	Lower 8 bits of symbol definition for Symbol0

9.16.7 TxSym1H_Reg

Table 171. TxSym1H_Reg (address 4Fh); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Symbol1_H							
Access rights	r/w							

Table 172: Description of TxSym1H_Reg bits

Bit	Symbol	Description
7 to 0	Symbol1_H	Higher 8 bits of symbol definition for Symbol1

9.16.8 TxSym1L_Reg

Table 173. TxSym1L_Reg (address 50h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Symbol1_L							
Access rights	r/w							

Table 174: Description of TxSym1L_Reg bits

Bit	Symbol	Description
7 to 0	Symbol1_L	Lower 8 bits of symbol definition for Symbol1

9.16.9 TxSym2_Reg

Table 175. TxSYM2_Reg (address 51h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Symbol2							
Access rights	r/w							

Table 176: Description of TxSym2_Reg bits

Bit	Symbol	Description
7 to 0	Symbol2	Symbol definition for Symbol2

9.16.10 TxSym3_Reg

Table 177. TxSym3_Reg (address 52h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Symbol3							
Access rights	r/w							

Table 178: Description of TxSym3_Reg bits

Bit	Symbol	Description
7 to 0	Symbol3	Symbol definition for Symbol3

9.16.11 TxSym10Len_Reg

Table 179. TxSym10Len_Reg (address 53h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	Sym1Len				Sym0Len			
Access rights	r/w				r/w			

Table 180: Description of TxSym10Len_Reg bits

Bit	Symbol	Description
7 to 4	Sym1Len	Specifies the number of valid bits of the symbol definition of Symbol1. The range is from 1 bit (value 0000b) to 16 bits (value 1111b)
3 to 0	Sym0Len	Specifies the number of valid bits of the symbol definition of Symbol0. The range is from 1 bit (value 0000b) to 16 bits (value 1111b)

9.16.12 TxSym32Len_Reg

Table 181. TxSym32Len_Reg (address 54h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	SYM3Len			-	SYM2Len		
Access rights	RFU	r/w	r/w	r/w	RFU	r/w	r/w	r/w

Table 182: Description of TxSym32Len_Reg bits

Bit	Symbol	Description
7	-	RFU
6 to 4	Sym3Len	Specifies the number of valid bits of the symbol definition of Symbol3. The range is from 1bit (000b) to 8 bits (111b)
3	-	RFU
2 to 0	Sym2Len	Specifies the number of valid bits of the symbol definition of Symbol2. The range is from 1bit (000b) to 8 bits (111b)

9.16.13 TxSym10BurstCtrl_Reg

Table 183. TxSym10BurstCtrl_Reg register (address 55h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	Sym1 Burst Type	Sym1Burst Len Only	Sym1 BurstEn	-	Sym0 Burst Type	Sym0B urst Only	Sym0Bu rstEn
Access rights	RFU	r/w	r/w	r/w	RFU	r/w	r/w	r/w

Table 184: Description of TxSym10BurstCtrl_Reg bits

Bit	Symbol	Description
7	-	RFU
6	Sym1Burst Type	Specifies the type of the burst of Symbol1 (logical zero / logical one)
5	Sym1Burst Only	If set to 1 Symbol1 consists only of a burst and no symbol pattern

Table 184: Description of TxSym10BurstCtrl_Reg bits ...continued

Bit	Symbol	Description
4	Sym1BurstEn	Enables the burst of symbol 1 of the length defined in TxSym10BurstLen_Reg
3	-	RFU
2	Sym0Burst Type	Specifies the type of the burst of symbol 0 (logical zero / logical one)
1	Sym0Burst Only	If set to 1, symbol 0 consists only of a burst and no symbol pattern
0	Sym0BurstEn	Enables the burst of symbol 0 of the length defined in TxSym10BurstLen_Reg

9.16.14 TxSym10Mod Reg

Table 185. TxSym10Mod_Reg register (address 56h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	-	S10 MillerEn	S10PulseType		S10Invert	S10EnvType		
Access rights	RFU	r/w	r/w		r/w	r/w		

Table 186: Description of TxSym10Mod_Reg bits

Bit	Symbol	Description
7	-	RFU
6	S10MillerEn	If set to 1, pulse modulation is applied according to modified miller code. Note: This bit shall be set only if S10PulseType is set to 01
5 to 4	S10PulseType	Specifies which type of pulse modulation is selected. 00b: no pulse modulation 01b: pulse starts at beginning of bit 10b: pulse starts at beginning of second bit half 11b: pulse starts at beginning of third bit quarter
3	S10Inv	If set to 1, the output envelope is inverted.
2 to 0	S10EnvType	Specifies the type of envelope used for transmission of symbol 0 and symbol 1. The pseudo bit stream is logically combined with the selected envelope type. 000b: Direct output 001b: Manchester code 010b: Manchester code with subcarrier 011b: BPSK 100b: RZ (pulse of half bit length at beginning of second half of bit) 101b: RZ (pulse of half bit length at beginning of bit) 110b - 111b: RFU

9.16.15 TxSym32Mod_Reg

Table 187. TxSym32Mod_Reg register (address 57h); reset value: 50h

Bit	7	6	5	4	3	2	1	0
Symbol	-	S32 MillerEn	S32PulseType		S32Invert	S32EnvType		
Access rights	RFU	r/w	r/w		r/w	r/w		

Table 188: Description of TxSym32Mod_Reg bits

Bit	Symbol	Description
7	-	RFU
6	S32MillerEn	If set to 1, pulse modulation is applied according to modified miller code. Note: This bit shall be set only if S32PulseType is set to 01
5 to 4	S32PulseType	Specifies which type of pulse modulation is selected. 00b: no pulse modulation 01b: pulse starts at beginning of bit 10b: pulse starts at beginning of second bit half 11b: pulse starts at beginning of third bit quarter
3	S32Inv	If set to 1, the output envelope is inverted
2 to 0	S32EnvType	Specifies the type of envelope used for transmission of symbol 0 and symbol 1. The pseudo bit stream is logically combined with the selected envelope type. 000b: Direct output 001b: Manchester code 010b: Manchester code with subcarrier 011b: BPSK 100b: RZ (pulse of half bit length at beginning of second half of bit) 101b: RZ pulse of half bit length at beginning of bit) 110b - 111b: RFU

9.17 Description/Receiver symbol register

9.17.1 RxBitMod_Reg

Table 189: RxBitMod_Reg (address 58h); reset value: 02h

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	RxStop OnInvPar	RxStop OnLength	RxMSB First	RxStop BitEn	RxParity Type	-
Access rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	RFU

Table 190: Description of RxBitMod_Reg bits

Bit	Symbol	Description
7 to 6	-	RFU
5	RxStopOn InvPar	If set to 1, inverse parity bit is a stop condition
4	RxStop OnLength	If set to 1, data reception stops when the number of received bytes reach the defined frame length. The value for the frame length is taken from the first data-byte received.
3	RxMSBFirst	If set to 1, data bytes are interpreted MSB first for data reception, which means data is converted at the CLCoPro interface. If this bit is set to 0, data is interpreted LSB first
2	RxStopBitEn	Set to 1, a stop-bit is expected and will be checked and extracted from data stream. Additionally on detection of a stop-bit a reset signal for the demodulator is generator to enable a re-synchronization of the demodulator. If the expected stop-bit is incorrect, a frame error flag is set and the reception is aborted. Note: A stop bit is always considered to be a logic 1
1	RxParityType	Defines which type of the parity-bit is calculated. 0b:……..Even parity 1b:……..Odd parity
0	-	RFU

9.17.2 RxEofSym_Reg

Table 191. RxEofSym_Reg (address 59h); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	RxEOFSymbol							
Access rights	r/w							

Table 192: Description of RxEOFSym_Reg bits

Bit	Symbol	Description
7 to 0	RxEOF Symbol	This value defines the pattern of the EOF symbol with a maximum length of 4 bit. Every tuple of 2 bits of the RxEOFSymbol encodes one bit of the EOF symbol. A 00 tuple closes the symbol. In this way symbols with less than 4 bits can be defined, starting with the bit0 and bit1. The leftmost active symbol pattern is processed first, which means the pattern is expected first. If the bit0 and bit1 are both zero, the EOF symbol is disabled. The following mapping is defined: 00b - no symbol bit 01b - zero value 10b - one value 11b - collision Example: 00011101b (1Dh): Zero-Collision-Zero 11101000b (E8h): No symbol because two LSBits are 0

9.17.3 RxSyncValH_Reg

Table 193. RxSyncValH_Reg register (address5Ah); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	RxSyncValH							
Access rights	r/w							

Table 194: Description of RxSyncValH_Reg bits

Bit	Symbol	Description
15 to 0	RxSyncValH	Defines the high byte of the Sync Pattern, which must be in front of the receiving data.

9.17.4 RxSyncValL_Reg

Table 195. RxSyncValL_Reg register (address 5Bh); reset value: 01h

Bit	7	6	5	4	3	2	1	0
Symbol	RxSyncValL							
Access rights	r/w							

Table 196: Description of RxSyncValL_Reg bits

Bit	Symbol	Description
7 to 0	RxSyncValL	Defines the low byte of the Sync Pattern, which must be in front of the receiving data.

9.17.5 RxSyncMod_Reg

Table 197. RxSyncMode register (address 5Ch); reset value: 00h

Bit	7	6	5	4	3	2	1	0
Symbol	SyncLen				SyncNegEdge	LastSyncHalf	SyncType	
Access rights	r/w				r/w	r/w	r/w	

Table 198: Description of RxSyncMod_Reg bits

Bit	Symbol	Description
7 to 4	SyncLen	Defines how many Bits of SyncLen are valid.
3	SyncNegEdge	Is used for SOF with no correlation peak. The first negative edge of the correlation is used for defining the bid grid
2	LastSyncHalf	The last Bit of the Sync mode has only half of the length compared to all other bits. (ISO/IEC18000-3 Mode 3)
1 to 0	SyncType	Set to 0 all 16 bits of SyncVal are interpreted as burst. Set to 1 a nibble of bits is interpreted as one bit in following way: {data, coll} data = zero or one; coll = 1 means a collision on this bit. Note: if Coll = 1 the value of data is ignored. Set to 2 the synchronisation is done at every start bit of each byte (type B)

9.17.6 RxMod_Reg

Table 199: RxMod_Reg register (address 5Dh); reset value: 08h

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	PreFilter	RectFilter	Sync High	Corr Inv	FSK	BPSK
Access rights	RFU	RFU	r/w	r/w	r/w	r/w	r/w	r/w

Table 200: Description of RxMod_Reg bits

Bit	Symbol	Description
7 to 6	-	RFU
5	PreFilter	If set to one 4 samples are combined to one data. (average)
4	RectFilter	If set to one, the ADC-values are changed to a more rectangular wave shape
3	SyncHigh	Defines if the bit grid is fixed at maximum (1) or at minimum (0) value of the correlation.
2	CorrInv	Defines a logical one: 0: subcarrier / no subcarrier
1	FSK	If set to 1, the demodulation scheme is set to FSK
0	BPSK	If set to 1, the modulation scheme is BPSK

9.17.7 RxCorr_Reg

Table 201: RxCorr_Reg register (address 5Eh); reset value: 80h

Bit	7	6	5	4	3	2	1	0
Symbol	CorrFreq		CorrSpeed		CorrLen	-	-	-
Access rights	r/w	r/w	r/w	r/w	r/w	RFU	RFU	RFU

Table 202: Description of RxCorr_Reg bits

Bit	Symbol	Description
7, 6	CorrFreq	00b: 212 kHz 01b: 424 kHz 10b: 848 kHz 11b: 848 kHz
5, 4	CorrSpeed	Defines the number of clocks used for one correlation. 00b: ISO/IEC 14443 01b: ICODE 53 kBd, FeliCa 424 kBd 10b: ICODE 26 kBd, FeliCa212 kBd 11b: RFU
3	CorrLen	Defines the length of the Correlation data. (64 or 32 values) Set to one the lengths is 32 values. (ISO/IEC18000-3 Mode3, 2 Pulse Manchester 848 kHz subcarrier)
2 to 0	-	RFU

9.17.8 FabCali_Reg

Table 203: FabCali_Reg register (address 5Fh); reset value: B2h

Bit	7	6	5	4	3	2	1	0
Symbol	FabCali							
Access rights	r/w							

Table 204: Description of FabCali_Reg bits

Bit	Symbol	Description
7 to 0	FabCali	Fab calibration of the receiver NOTE: do not change boot value

9.18 Description/Version register

9.18.1 Version_Reg

Table 205. Version_Reg register (address 7Fh); reset value: 10h

Bit	7	6	5	4	3	2	1	0
Symbol	Version				SubVersion			
Access rights	r				r			

Table 206: Version_Reg bits

Bit	Symbol	Description
7 to 4	Version	Includes the version of the CLRC663
3 to 0	SubVersion	Includes the subversion of the CLRC663

10. DIGITAL interfaces

10.1 Microcontroller interface type

The CLRC663 supports direct interfacing of various hosts as the SPI, I^2C, I^2CL and serial UART interface type. The CLRC663 resets its interface and checks the current host interface type automatically having performed a Power-On or Hard Reset. The CLRC663 identifies the host interface by the means of the logic levels on the control pins after the Reset Phase. This is done by a combination of fixed pin connections.The following table shows the different configurations:

Table 207: Connection Scheme for detecting the different Interface Types

		UART	SPI	I^2C	I^2C-L
IF0	I/O	Rx	MOSI	ADR1	ADR1
IF1(SCL)	I/O	-	SCK	SCL	SCL
IF2	I/O	TX	MISO	ADR2	SDA
IF3(SDA)	I/O	Trigger	NSS	SDA	ADR2
IF1SEL0	I	0	0	1	1
IF1SEL1	I	0	1	0	1

10.2 SPI Compatible interface

A serial peripheral interface (SPI compatible) is supported to enable high speed communication to the host. The SPI Interface can handle data speed of up to 10 Mbit/s. In the communication with a host CLRC663 acts as a slave receiving data from the external host for register settings and to send and receive data relevant for the communication on the RF interface.

10.2.1 General

An interface compatible to an SPI interface enables a high-speed serial communication between the CLRC663 and a µ-Controller for the communication. The implemented SPI compatible interface is according to a standard SPI interface.

For timing specification refer to Table 242 “SPI timing characteristics”.

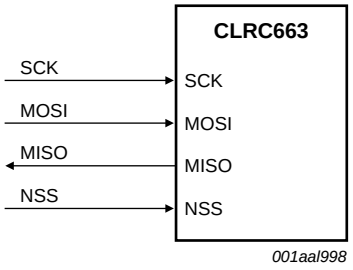


Fig 12. Connection to host with SPI

The CLRC663 acts as a slave during the SPI communication. The SPI clock SCK has to be generated by the master. Data communication from the master to the slave uses the Line MOSI. Line MISO is used to send data back from the CLRC663 to the master.

On both lines (MOSI, MISO) each data byte is sent by MSB first. Data on MOSI line should be stable on rising edge of the clock line and can change on falling edge. The same is valid for the MISO line. Data is provided by the CLRC663 on falling edge and is stable during rising edge.

Remark: Clock polarity: idle LOW

10.2.2 Read data

To read out data using the SPI compatible interface the following byte order has to be used. It is possible to read out up to n-data bytes.

The first sent byte defines both, the mode itself and the address byte.

Table 208: Byte Order for MOSI and MISO

	byte 0	byte 1	byte 2	to	byte n	byte n + 1
MOSI	address 0	address 1	address 2	……..	address n	00
MISO	X	data 0	data 1	……..	data n – 1	data n

Remark: The most significant bit (MSB) has to be send first.

10.2.3 Write data

To write data to the CLRC663 using the SPI interface the following byte order has to be used. It is possible to write out up to n-data bytes by only sending one's address byte.

The first send byte defines both, the mode itself and the address byte.

Table 209: Byte Order for MOSI and MISO

	byte 0	byte 1	byte 2	to	byte n	byte n + 1
MOSI	address 0	data 0	data 1	……..	data n – 1	data n
MISO	X	X	X	……..	X	X

Remark: The most significant bit (MSB) has to be send first.

10.2.4 Address byte

The address byte has to fulfil the following format:

The LSB bit of the first byte defines the used mode. To read data from the CLRC663 the LSB bit is set to logic 1. To write data to the CLRC663 the MSB bit has to be set to logic 0. The bits 6 to 0 define the address byte.

NOTE: When writing the sequence [address byte][data1][data2][data3]..., [data1] is written to address [address byte], [data2] is written to address [address byte + 1] and [data3] is written to [address byte + 2].

Exception: This auto increment of the address byte is not valid for writing data to the FiFo

Table 210. Address byte 0 register; address MOSI

7	6	5	4	3	2	1	0
address 6	address 5	address 4	address 3	address 2	address 1	address 0	1 (read) 0 (write)
MSB							LSB

10.2.5 Timing Specification SPI

The timing conditions for SPI interface is as follow:

Table 211. Timing conditions SPI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	50	-	-	ns
t_{SCKH}	SCK HIGH time	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	50			ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI; $V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	25			ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK; $V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	25			ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	-		25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time		0			ns
t_{NSSH}	NSS HIGH time	before communication	50	-	-	ns

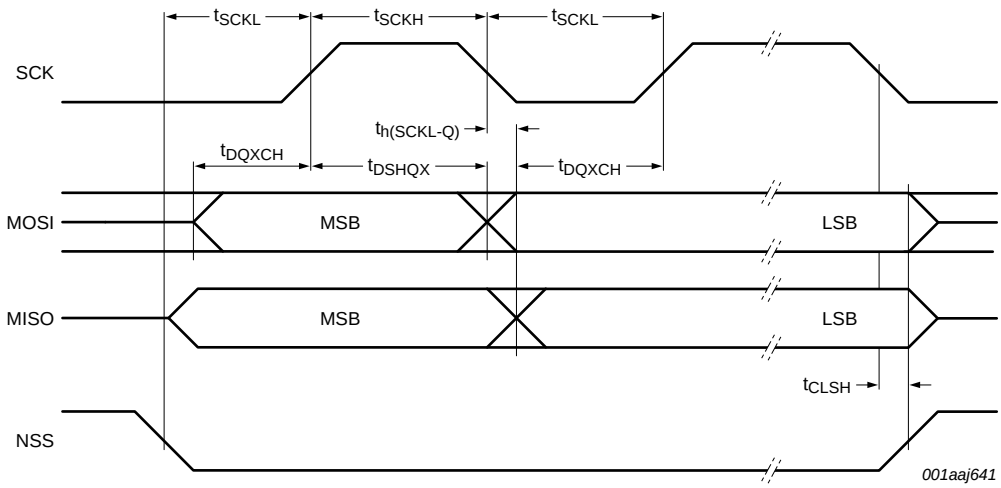


Fig 13. Connection to host with SPI

Remark: To send more bytes in one data stream the NSS signal must be LOW during the send process. To send more than one data stream the NSS signal must be HIGH between each data stream.

10.3 UART Interface

10.3.1 Selection of the transfer speeds

The internal UART interface is compatible to a RS232 serial interface.

Table 213 “Selectable transfer speeds” describes examples for different transfer speeds and relevant register settings. The resulting transfer speed error is less than 1.5 % for all described transfer speeds. The default transfer speed is 115.2 kbit/s.

To change the transfer speed, the host controller has to write a value for the new transfer speed to the register *SerialSpeedReg*. The bits *BR_T0* and *BR_T1* define factors to set the transfer speed in the *SerialSpeedReg*.

Table 212 “Settings of BR_T0 and BR_T1” describes the settings of *BR_T0* and *BR_T1*.

Table 212. Settings of BR_T0 and BR_T1

BR_T0	0	1	2	3	4	5	6	7
factor BR_T0	1	1	2	4	8	16	32	64
range BR_T1	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 213: Selectable transfer speeds

Transfer speed (kbit/s)	Serial SpeedReg		Transfer speed accuracy (%)
	decimal	hexadecimal	
7.2	250	FAh	–0.25
9.6	235	EBh	0.32
14.4	218	DAh	–0.25
19.2	203	CBh	0.32

Table 213: Selectable transfer speeds

Transfer speed (kbit/s)	Serial SpeedReg		Transfer speed accuracy (%)
	decimal	hexadecimal	
38.4 k	171	ABh	0.32
57.6 k	154	9Ah	–0.25
115.2 k	122	7Ah	–0.25
128 k	116	74h	–0.06
230.4 k	90	5Ah	–0.25
460.8 k	58	3Ah	–0.25
921.6 k	28	1Ch	1.45
1228.8 k	21	15h	0.32

The selectable transfer speeds as shown in Table 213 “Selectable transfer speeds” are calculated according to the following formulas:

if *BR_T0* = 0: transfer speed = 27.12 MHz/(*BR_T1* + 1)

if *BR_T0* > 0: transfer speed = 27.12 MHz/(*BR_T1* + 33)/$2^{(BR\_T0 - 1)}$

Remark: Transfer speeds above 1228.8 k are not supported.

10.3.2 Framing

Table 214: UART Framing

	Length	Value
Start bit	1 bit	0
Data bits	8 bit	Data
Stop bit	1 bit	1

Remark: For data and address bytes the LSB bit has to be sent first. No parity bit is used during transmission.

Read data: To read out data using the UART interface the flow described below has to be used. The first send byte defines both the mode itself and the address.

Remark: Note: The Trigger on IF3 pin has to be set, otherwise no “read data” is possible

Table 215: Byte Order to Read Data

	byte 0	byte 1
RX	address	
TX		data 0

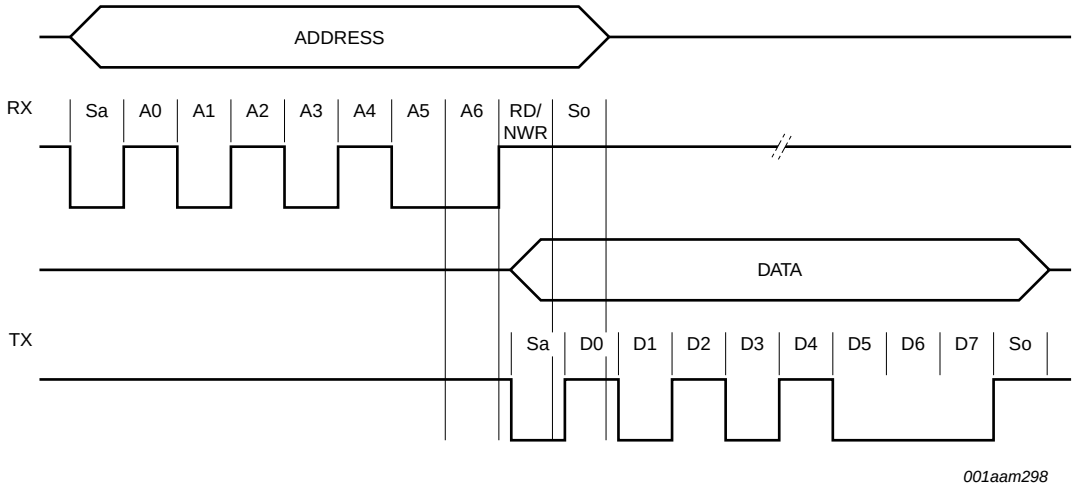


Fig 14. Schematic Diagram to Read Data

Write data:

To write data to the CLRC663 using the UART interface the following structure has to be used.

Remark: Note: The Trigger on IF3 pin has to be set, otherwise no “write data” is possible

The first send byte defines both, the mode itself and the address.

Table 216: Byte Order to Write Data

	byte 0	byte 1
RX	address 0	data 0
TX		address 0

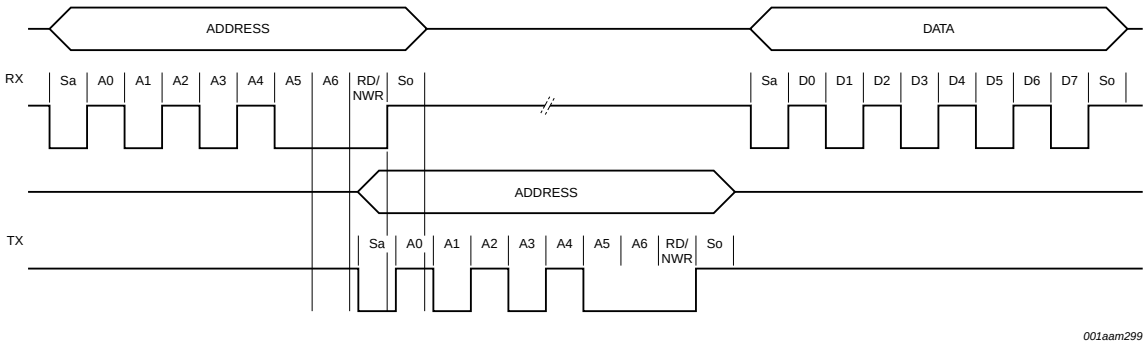


Fig 15. Schematic diagram to write data

10.4 I²C-bus Interface

An Inter IC (I²C) bus interface is supported to enable a low cost, low pin count serial bus interface to the host. The implemented I²C interface is implemented according the NXP Semiconductors I²C interface specification, rev. 3.0, June 2007. The implemented

interface can only act in Slave mode. Therefore no clock generation and access arbitration is implemented in the CLRC663. High speed mode is not supported by the CLRC663

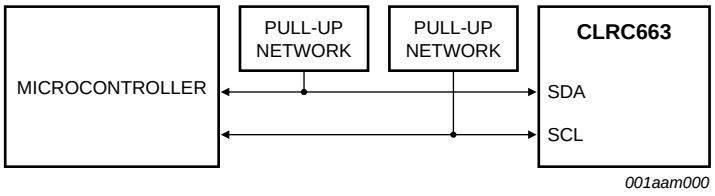


Fig 16. I²C-bus interface

10.4.1 General

The implemented interface is compatible to the "I²C-bus specification version 3.0, June 2007". The CLRC663 can act as a slave receiver or slave transmitter in Standard mode, Fast mode and Fast Mode Plus.

SDA is a bidirectional line, connected to a positive supply voltage via a pull-up resistor. Both lines SDA and SCL are set to HIGH level if no data is transmitted. The CLRC663 has a tri-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 400 kbit/s in Fast mode, up to 1 Mbit/s in the Fast Mode Plus.

If the I²C interface is selected, a spike suppression according to the I²C interface specification on SCL and SDA is activated.

For timing requirements refer to Table 243 "I²C-bus timing in Fast mode and Fast mode Plus"

10.4.2 Data validity

Data on the SDA line shall be stable during the HIGH period of the clock. The HIGH or LOW state of the data line shall only change when the clock signal on SCL is LOW.

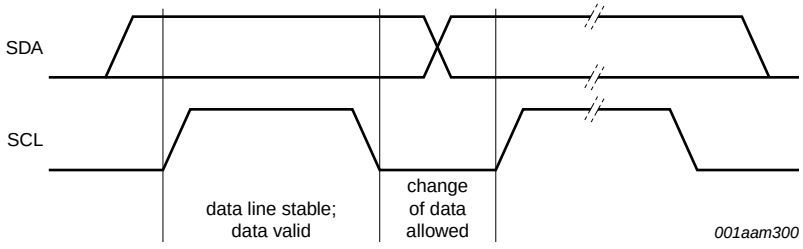


Fig 17. Bit transfer on the I²C-bus.

10.4.3 START and STOP conditions

To handle the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.

A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The master always generates the START and STOP conditions. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In this respect, the START (S) and repeated START (Sr) conditions are functionally identical. Therefore, the S symbol will be used as a generic term to represent both the START and repeated START (Sr) conditions.

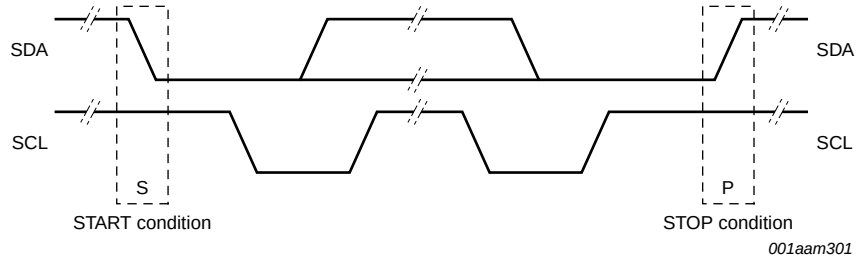


Fig 18. START and STOP conditions

10.4.4 Byte format

Each byte has to be followed by an acknowledge bit. Data is transferred with the MSB first, see Figure 21 “First byte following the START procedure”. The number of transmitted bytes during one data transfer is unrestricted but shall fulfil the read/write cycle format.

10.4.5 Acknowledge

An acknowledge at the end of one data byte is mandatory. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver shall pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer, or a repeated START (Sr) condition to start a new transfer.

A master-receiver shall indicate the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter shall release the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

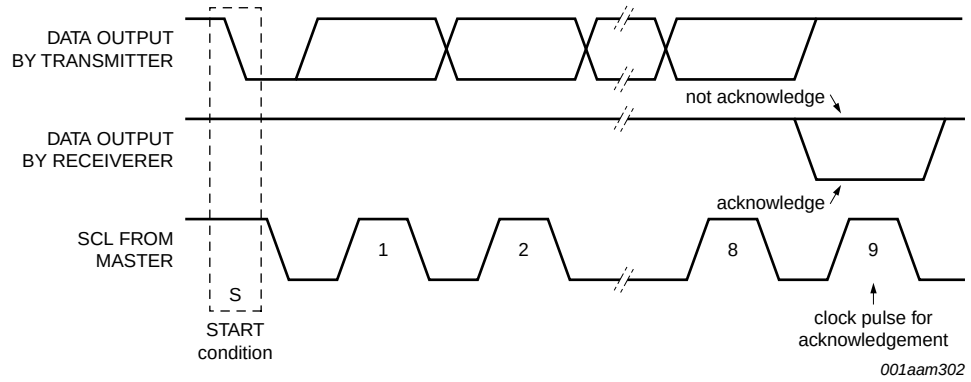


Fig 19. Acknowledge on the I²C- bus

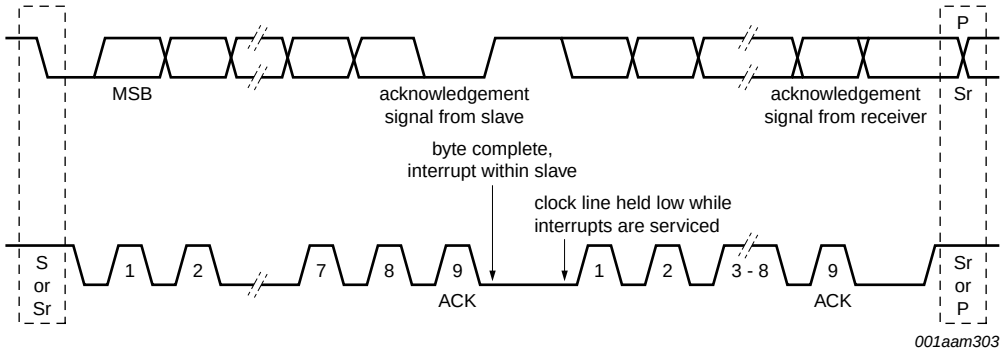


Fig 20. Data transfer on the I²C- bus

10.4.6 7-BIT ADDRESSING

During the I²C-bus addressing procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

As an exception several address numbers are reserved. During device configuration, the designer has to ensure, that no collision with these reserved addresses is possible. Check the corresponding I²C specification for a complete list of reserved addresses.

For all CLRC663 devices the upper 5 bits of the device bus address are reserved by NXP and set to 01010(bin). The remaining 2 bits (ADR_2, ADR_1) of the slave address can freely configured by the customer in order to prevent collisions with other I²C devices by using the interface pins (refer to Table 207) or the value of the I²C address EEPROM register. (Refer to Table 227).

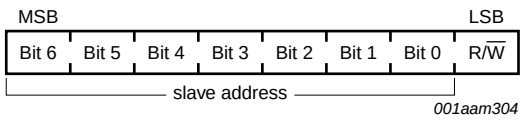


Fig 21. First byte following the START procedure

10.4.7 Register Write Access

To write data from the host controller via I^2C to a specific register of the CLRC663 the following frame format shall be used.

The first byte of a frame indicates the device address according to the I^2C rules. The second byte indicates the register address followed by up to n-data bytes. In one frame all n-data bytes are written to the same register address. This enables for example a fast FiFo access.

The read/write bit shall be set to logic 0.

10.4.8 Register Read Access

To read out data from a specific register address of the CLRC663 the host controller shall use the procedure:

First a write access to the specific register address has to be performed as indicated in the following frame.

The first byte of a frame indicates the device address according to the I^2C rules. The second byte indicates the register address. No data bytes are added.

The read/write bit shall be logic 0.

Having performed this write access, the read access can start. The host has to send the device address of the CLRC663. As an answer to this the CLRC663 responds with the content of this register. In one frame all n-data bytes could be read from the same register address. This enables for example a fast FiFo access or register polling.

NOTE: When writing the sequence [address byte][data1][data2][data3]..., [data1] is written to address [address byte], [data2] is written to address [address byte + 1] and [data3] is written to [address byte + 2].

Exception: This auto increment of the address byte is not valid for writing data to the FiFo

The read/write bit shall be set to logic 1.

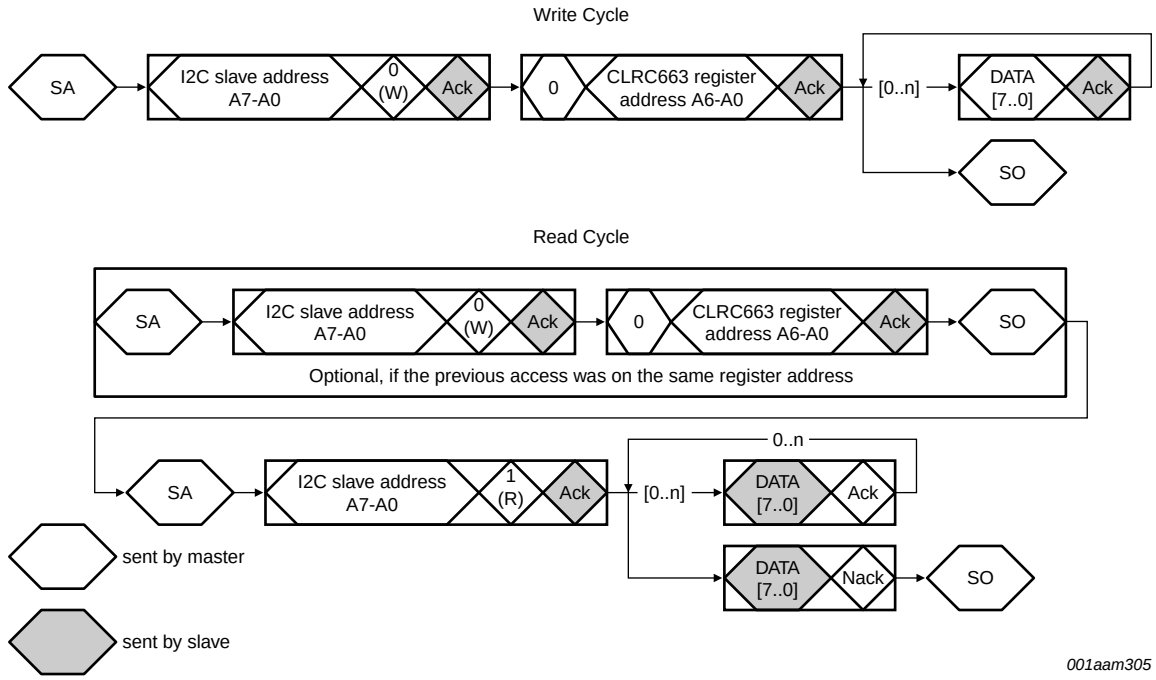


Fig 22. Register read and write access

10.4.9 I²CL Bus Interface

The CLRC663 provides an additional interface according of a logical handling of an I²C interface. This logical interface fulfills in general the I²C specification, but all timing related factor will not be according the standard. Standard I/O pad are used for communication and the communication speed is limited to 5 Mbaud. The protocol itself is equivalent to the FAST mode protocol of I²C. The Interphase address is 01010xxb, where the last two bit of the address can be defined by the application. To define this two bit there are basically two possibilities. Defining it with a pin, where the higher bit is fixed to 0 or the configuration is fixed via EEPROM. Refer to the EEPROM configuration in Section 12.

The output of this interface port is an asynchronous parallel port with two control lines, read (rd) and write (wr). The Write access is synchronized in the host interface module.

Table 217. Timing parameter I²CL

Parameter	Min	Max	Unit
f_{SCL}	0	5	MHz
$t_{HD;STA}$	80	-	ns
t_{LOW}	100	-	ns
t_{HIGH}	100	-	ns
$t_{SU;SDA}$	80	-	ns
$t_{HD;DAT}$	0	50	ns
$t_{SU;DAT}$	0	20	ns
$t_{SU;STO}$	80	-	ns
t_{BUF}	200	-	ns

10.4.10 I²CLSAM Bus Interface

The CLRC663 provides an additional I2C interface. This logical interface fulfills in general the I²C specification, but all timing related factors will not be according the standard. Refer to I²CL. To use this interface the configuration has to be defined via EEPROM. (Refer to Section 12)

One major difference between I²C and I²CL is the missing pull-up resistor. The driver of the pad must push the line to the desired logic voltage. To avoid that two drivers are pushing the line at the same time following regulations must be fulfilled:

SCL: As there is no clock stretching allowed the SCL is always under control of the Master. A buskeeper structure is not required.

SDA: The SDA line is shared between master and slave. Therefore the master and the slave must have the control over the own driver enable line of the SDA pad. Following rules must be followed:

- In the IDLE phase the SDA line is driven HIGH by the MASTER
- In the time between START and STOP condition the SDA line is driven by MASTER or SLAVE when SCL is LOW. If SCL is HIGH the SDA line is not driven by any device
- To keep the value on the SDA line a buskeeper structure is needed for the line

10.5 Boundary Scan

The CLRC663 provides a boundary scan interface according the IEEE 1149.1. This interface provides a possibilities to test interconnections without using physical test probes. This is done by “test cells”, connected to each pin, which overrides the functionality of this pin.

To be able to program the “test cells” the following commands are supported:

Table 218. Boundary Scan command

Value	Command	Parameter in	Parameter out
0h	bypass	-	-
7h			
1h	preload	data (Pin)	-
1h	sample	-	data (Pin)
2h	ID code (default)	-	data (32)
3h	USER code	-	data (32)
4h	clamp	-	-
5h	HIGH Z	-	-
7h	extest	data (pin)	data (pin)
8h	interface on/off	interface (8)	-
9h	register access read	address (7)	data
Ah	register access write	address (7) - data (8)	-

The Standard IEEE 1149.1 describes the four basic blocks necessary to use this interface: Test Access Port (TAP); TAP controller; - Instruction register, - Data register;

10.5.1 Test Access Port (TAP)

The access port is the interface between the Chip and the environment. There are three Inputs: Test Clock (TCK); Test mode Select (TMS); Test Data Input (TDI) and one Output: Test Data Output.TCK and TMS are broadcast signals, TDI to TDO generate a serial line called Scan path.

Advantage of this technique is that independent of the numbers of boundary scan devices the complete path can be handled with four signal lines.

The signals TCK, TMS are directly connected with the TAP controller. Because these signals are responsible for the mode of the chip, all boundary scan devises in one scan path will be in the same TAP mode.

10.5.2 Test Clock (TCK)

The TCK pin is the clock for the JTAG module. This clock is provided so the test logic can operate independently of any other system clocks. In addition, it ensures that multiple JTAG TAP controllers that are daisy-chained together can synchronously communicate serial test data between components. During normal operation, TCK is driven by a free-running clock with a nominal 50 % duty cycle. When necessary, TCK can be stopped at 0 or 1 for extended periods of time. While TCK is stopped at 0 or 1, the state of the TAP controller does not change and data in the JTAG Instruction and Data Registers is not lost.

By default, the internal pull-up resistor on the TCK pin is enabled after reset. This assures that no clocking occurs if the pin is not driven from an external source. The internal pull-up and pull-down resistors can be turned off to save internal power as long as the TCK pin is constantly being driven by an external source.

10.5.3 Test Mode Select (TMS)

The TMS pin selects the next state of the JTAG TAP controller. TMS is sampled on the rising edge of TCK. Depending on the current TAP state and the sampled value of TMS, the next state is entered. Because the TMS pin is sampled on the rising edge of TCK, the IEEE Standard 1149.1 expects the value on TMS to change on the falling edge of TCK. Holding TMS high for five consecutive TCK cycles drives the TAP controller state machine to the Test-Logic-Reset state. When the TAP controller enters the Test-Logic-Reset state, the JTAG Instruction Register (IR) resets to the default instruction, IDCODE. Therefore, this sequence can be used as a reset mechanism, similar to asserting TRST.

By default, the internal pull-up resistor on the TMS pin is enabled after reset. Changes to the pull-up resistor settings on GPIO Port C should ensure that the internal pull-up resistor remains enabled on PC1/TMS; otherwise JTAG communication could be lost an path.

10.5.4 Test Data Input (TDI)

The TDI pin provides a stream of serial information to the IR chain and the DR chains. TDI is sampled on the rising edge of TCK and, depending on the current TAP state and the current instruction, presents this data to the proper shift register chain. Because the TDI pin is sampled on the rising edge of TCK, the IEEE Standard 1149.1 expects the value on TDI to change on the falling edge of TCK.

By default, the internal pull-up resistor on the TDI pin is enabled after reset. Changes to the pull-up resistor settings on GPIO Port C should ensure that the internal pull-up resistor remains enabled on PC2/TDI; otherwise JTAG communication could be lost

10.5.5 Test Data Output (TDO)

The TDO pin provides an output stream of serial information from the IR chain or the DR chains. The value of TDO depends on the current TAP state, the current instruction, and the data in the chain being accessed. In order to save power when the JTAG port is not being used, the TDO pin is placed in an inactive drive state when not actively shifting out data. Because TDO can be connected to the TDI of another controller in a daisy-chain configuration, the IEEE Standard 1149.1 expects the value on TDO to change on the falling edge of TCK.
By default, the internal pull-up resistor on the TDO pin is enabled after reset. This assures that the pin remains at a constant logic level when the JTAG port is not being used. The internal pull-up and pull-down resistors can be turned off to save internal power if a High-Z output value is acceptable during certain TAP controller states

10.5.6 Instruction register

The instruction register handles the working mode of the boundary scan cell. basically there are three modes. BYPASS, SAMPLE/PRELOAD and EXTEST. According to the standard also the definition of further commands are allowed. The CLRC663 Boundary scan interface has Clamp and HighZ as additional instructions.

10.5.7 Data register

According to the IEEE1149.1 standard there are two types of data register defined: bypass, boundary scan

The bypass register enable the possibility to bypass a devise when part of the scan path. The boundary scan register is the chain of the boundary cells. The size of this register can differ per device, in the CLRC663 it has the size of 8 bits.

10.5.8 Boundary scan cell

The boundary scan cell opens the possibility to control a hardware pin independent of its normal usecase. Basically the cell can only do one of the following: control, output and Input.

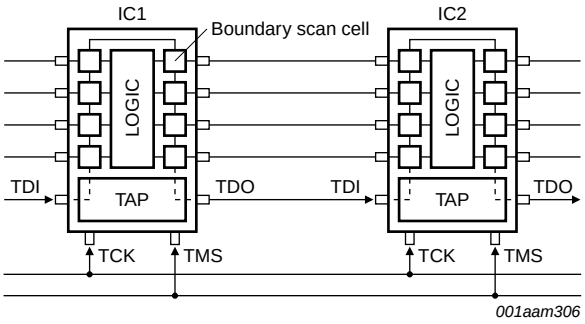


Fig 23. Boundary scan cell path structure

10.5.9 Boundary scan path

This chapter shows the boundary scan path of the CLRC663.

Table 219. Boundary scan path of the CLRC663

Number	Cell	Port	Function
23	BC_1	-	Control
22	BC_8	CLKOUT	Bidir
21	BC_1	-	Control
20	BC_8	SCL2	Bidir
19	BC_1		Control
18	BC_8	SDA2	Bidir
17	BC_1		Control
16	BC_8	IFSEL0	Bidir
15	BC_1		Control
14	BC_8	IFSEL1	Bidir
13	BC_1		Control
12	BC_8	IF0	Bidir
11	BC_1	-	Control
10	BC_8	IF1	Bidir
9	BC_1	-	Control
8	BC_8	IF2	Bidir
7	BC_1	IF2	Output2
6	BC_4	IF3	Bidir
5	BC_1	-	Control
4	BC_8	IRQ	Bidir
3	BC_1	-	Control
2	BC_8	SIGIN	Bidir
1	BC_1	-	Control
0	BC_8	SIGOUT	Bidir

Refer to the CLRC663 BSDL file.

10.5.10 Boundary Scan Description Language (BSDL)

All of the boundary scan devices have a unique boundary structure where it is necessary to know this for working with the device. Important parts of this language are:

- available test bus signal
- compliance pins
- command register
- data register
- boundary scan structure (number and types of the cells, their function and the connection to the pins.)

The CLRC663 is using the cell BC_8 for the IO-Lines. The I^2C Pin is using a BC_4 cell. For all pad enable lines the cell BC5 is used.

The manufacturer's identification is 02Bh.

- attribute IDCODE_REGISTER of CLRC663: entity is "0001" and -- version

- "0011110010000010b" and -- part number (3C82h)
- "00000010101b" and -- manufacturer (02Bh)
- "1b"; -- mandatory
- Instruction_capture = 1001b

The user code data is coded as followed:

- product ID (2 bytes)
- feature lock
- version

These four bytes are stored as the first four bytes in the EEPROM.

10.5.11 NON IEEE1149.1 commands

10.5.11.1 Interface on/off

With this command the host/sam interface can be deactivated and the Read and Write command of the boundary scan interface is activated. (Data = 1). With Update-DR the value is taken over.

10.5.11.2 Register Access Read

At Capture-DR the actual address is read and stored in the DR. Shifting the DR is shifting in a new address. With Update-DR this address is taken over into the actual address.

10.5.11.3 Register Access Writer

With this command the host/sam interface can be deactivated and the Read and Write command of the boundary scan interface is activated. (Data = 1). With Update-DR the value is taken over.

11. Analog Interface and Contactless UART

11.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kbit/s. An external circuit can be connected to the communication interface pins GPIO0/SIGIN and SIGOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication schemes in co-operation with the host. The protocol handling itself generates bit- and byte-oriented framing and handles error detection like Parity and CRC according to the different contactless communication schemes.

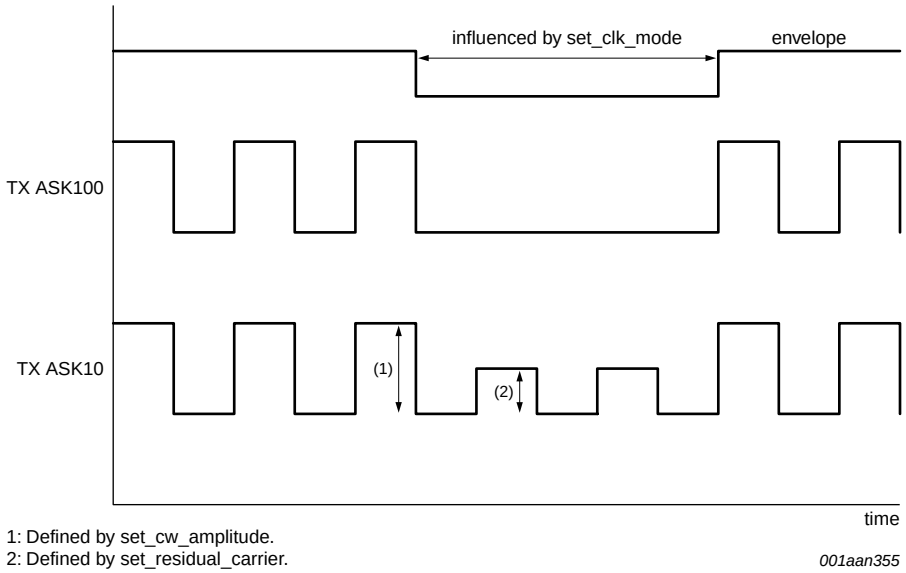
Remark: The size and the tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

11.2 TX Transmitter

The signal delivered on pin TX1 and pin TX2 is the 13.56 MHz carrier modulated by an envelope signal for energy and data transmission. It can be used to drive an antenna directly, using a few passive components for matching and filtering, see Section 23 “Application information”. The signal on TX1 and TX2 can be configured by the register *DrvMode*, see Section 9.9.1 “TxMode_Reg”.

The modulation index can be set by the TxAmp_Reg.

Following figure shows the general relations during modulation



1: Defined by set_cw_amplitude.
2: Defined by set_residual_carrier.

001aan355

Fig 24. General dependences of modulation

Note: When changing the continuous wave, the residual carrier also changes, while the modulation index remains the same.

The registers Section 9.9 and Section 9.11 control the data rate, the framing during transmission and the setting of the antenna driver to support the requirements at the different specified modes and transfer speeds.

Table 220: Settings for TX1/2

Envelope	set_clk_mode	invtx1/2	Tx1/2	Remarks
1	X	0	RF	RF clock depending on invtx
1	X	1	RF_n	RF clock depending on invtx
0	0b000	X	Z	high impedance
0	0b001	X	0	output pulled to 0 in any case
0	0b010	X	1	output pulled to 1 in any case
0	0b110	0	RF_hs	open drain, only high side (push) MOS supplied with clock, clock parity defined by invtx; low side MOS is off
0	0b110	1	RF_hs_n	open drain, only high side (push) MOS supplied with clock, clock polarity defined by invtx; low side MOS is off
0	0b101	0	RF_ls	open drain, only low side (pull) MOS supplied with clock, clock parity defined by invtx; high side MOS is off
0	0b101	1	RF_ls_n	open drain, only low side (pull) MOS supplied with clock, clock parity defined by invtx; high side MOS is off
0	0b111	0	RF	push/pull Operation, clock polarity defined by invtx; setting for 10 % modulation
0	0b111	1	RF_n	push/pull Operation, clock polarity defined by invtx; setting for 10 % modulation

The following abbreviations are used:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz divided by 2
- RF_n: inverted 13.56 MHz clock
- RF_hs: RF high side push
- RF_hs_n: RF high side push negative
- RF_ls: RF low side pull
- RF_ls_n: RF low side pull negative
- Z: High impedance

To adjust the modulation index following parameter has to be considered:

Table 221. Settings for set_residual_carrier and corresponding residual carrier

set_residual_carrier	Residual carrier [%]	Modulation index [%]
0	99	0.5
1	98	1.0
2	96	2.0
3	94	3.1
4	91	4.7
5	89	5.8

Table 221. Settings for set_residual_carrier and corresponding residual carrier *...continued*

set_residual_carrier	Residual carrier [%]	Modulation index [%]
6	87	7.0
7	86	7.5
8	85	8.1
9	84	8.7
10	83	9.3
11	82	9.9
12	81	10.5
13	80	11.1
14	79	11.7
15	78	12.4
16	77	13.0
17	76	13.6
18	75	14.3
19	74	14.9
20	72	16.3
21	70	17.6
22	68	19.0
23	65	21.2
24	60	25.0
25	55	29.0
26	50	33.3
27	45	37.9
28	40	42.9
29	35	48.1
30	30	53.8
31	25	60.0

Note: When VDD(TVDD) < 5 V it is not recommended to use a residual carrier < 50 %

11.2.1 Overshoot protection

The CLRC663 provides an overshoot protection to avoid overshoots during a PCD communication. Therefore two timer overshoot_t1 and overshoot_t2 can be used.

During the timer overshoot_t1 runs an amplitude defined by set_cw_amplitude bits is provided to the output driver. Followed by an amplitude denoted by set_residual_carrier bits with the duration of overshoot_t2.

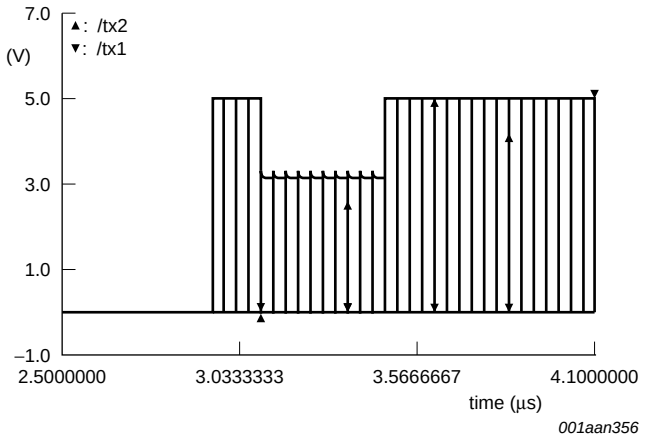


Fig 25. Example 1: overshoot_t1 = 2d; overhoot_t2 = 5d.

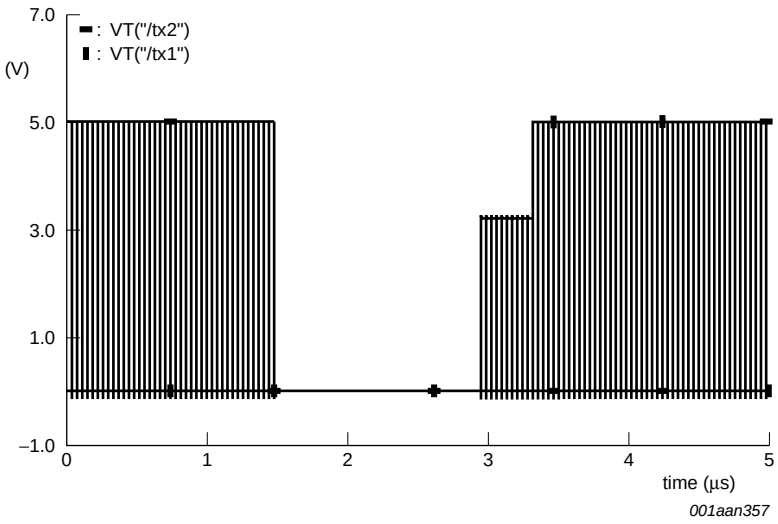


Fig 26. Example 2: overshoot_t1 = 0d; overhoot_t2 = 5d

11.3 Receiver circuitry

11.3.1 General

The CLRC663 features a versatile quadrature receiver architecture with fully differential signal input at RXP and RXN. It can be configured to achieve optimum performance for reception of various 13.56 MHz based protocols.

For all processing units various adjustments can be made to obtain optimum performance.

11.3.2 Block diagram

Figure 27 shows the block diagram of the receiver circuitry. The receiving process includes several steps. First the quadrature demodulation of the carrier signal of 13.56 MHz is done. Several tuning steps in this circuit are possible.

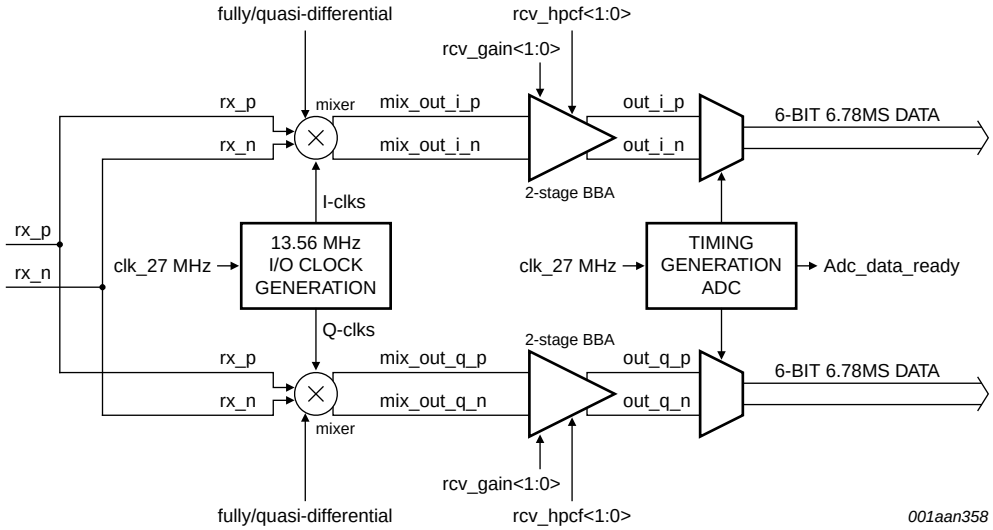


Fig 27. Block diagram of receiver circuitry

The receiver can also be used as single ended solution. In this case only one side has to be assembled and the Rcv_RX_single has to be set. In the single ended use case two receiver pins have to be connected.

Remark: When using the receiver single ended the reading distance will be influenced because of decreased sensitivity as well as the noise immunity.

Table 222. Usage of single or differential receiver

Mode	rcv_rx_single	pins rx_p and rx_n
Fully differential	0	provide differential signal from differential antenna by separate rx-coupling branches
Quasi differential	1	connect RXP and RXN together and provide single ended signal from antenna by a single rx-coupling branch

The quadrature-demodulator uses two different clocks, Q-clock and I-clock, with a phase shift of 90° between them. Both resulting baseband signals are amplified, filtered and forwarded to a correlation circuitry.

11.4 S3C interface / (GPIO0)SigIn-SigOut

Two main blocks are implemented in the CLRC663. A digital circuitry, comprising state machines, coder and decoder logic and an analog circuitry with the modulator and antenna drivers, receiver and amplification circuitry. For example, the interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins (GPIO0)SigIn and SigOut. The most important use of this topology is the active

antenna concept where the digital and the analog part are ideologically separated. This opens the possibility to connect e.g. an additional digital part of another device with the one analog antenna front-end.

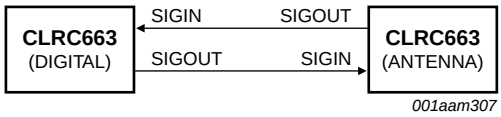


Fig 28. Block diagram of the active Antenna concept

The Table 223 and Table 224 shows the necessary register configuration for the use case active antenna concept.

Table 223. Register configuration of CLRC663 active antenna concept (DIGITAL)

Register	Value	Description
SigOut.SigOutSel	0100h	TxEnvelope
Rcv.sigpro_in_sel	10 11	Receive over SigIn (ISO/IEC14443A) Receive over SigIn (Generic Code)
DrvCon.TxSel	00	Low (idle)

Table 224. Register configuration of CLRC663 active antenna concept (Antenna)

Register	Value	Description
SigOut.SigOutSel	0110h 0111h	Generic Code (Manchester) Manchester with Subcarrier (ISO/IEC14443A)
Rcv.sigpro_in_sel	01	Internal
DrvCon.TxSel	10	External (SigIn)
RxCtrl.RxMultiple	1	RxMultiple on

The interface between these two blocks can be configured in the way, that the interfacing signals may be routed to the pins SIGIN and SIGOUT (see Figure 29 “Overview (GPIO0)SIGIN/SIGOUT Signal Routing”). The configuration is done by bits MFOutSel, TxSel and UARTSel of registers TxSelReg and RxSelReg.

This topology supports, that some parts of the analog part of the CLRC663 may be connected to the digital part of another device.

The switch *MFOutSel* in register *TxSelReg* can be used to measure MIFARE and ISO/IEC14443 related signals. This is especially important during the design In phase or for test purposes to check the transmitted and received data.

However, the most important use of MFIN/MFOUT pins is the active antenna concept. An external active antenna circuit can be connected to the digital circuit of the CLRC663. *MFOutSel* has to be configured in that way that the signal of the internal Miller Coder is send to MFOUT pin (*MFOutSel* = 4). *UARTSel* has to be configured to receive Manchester signal with sub-carrier from MFIN pin (*UARTSel* = 1).

It is possible, to connect a 'passive antenna' to pins TX1, TX2 and RX (via the appropriate filter and matching circuit) and at the same time an Active Antenna to the pins MFOUT and MFIN. In this configuration, two RF-parts may be driven (one after another) by one host processor.

Remark: The CLRC663 has an extra supply pin (SVDD and PVSS as Ground line) for the MFIN and MFOUT pads.
If MFIN pin is not used it should be connected to SVDD or PVSS.
If SVDD pin is not used it should be connected to DVDD or PVDD or any other voltage supply pin.

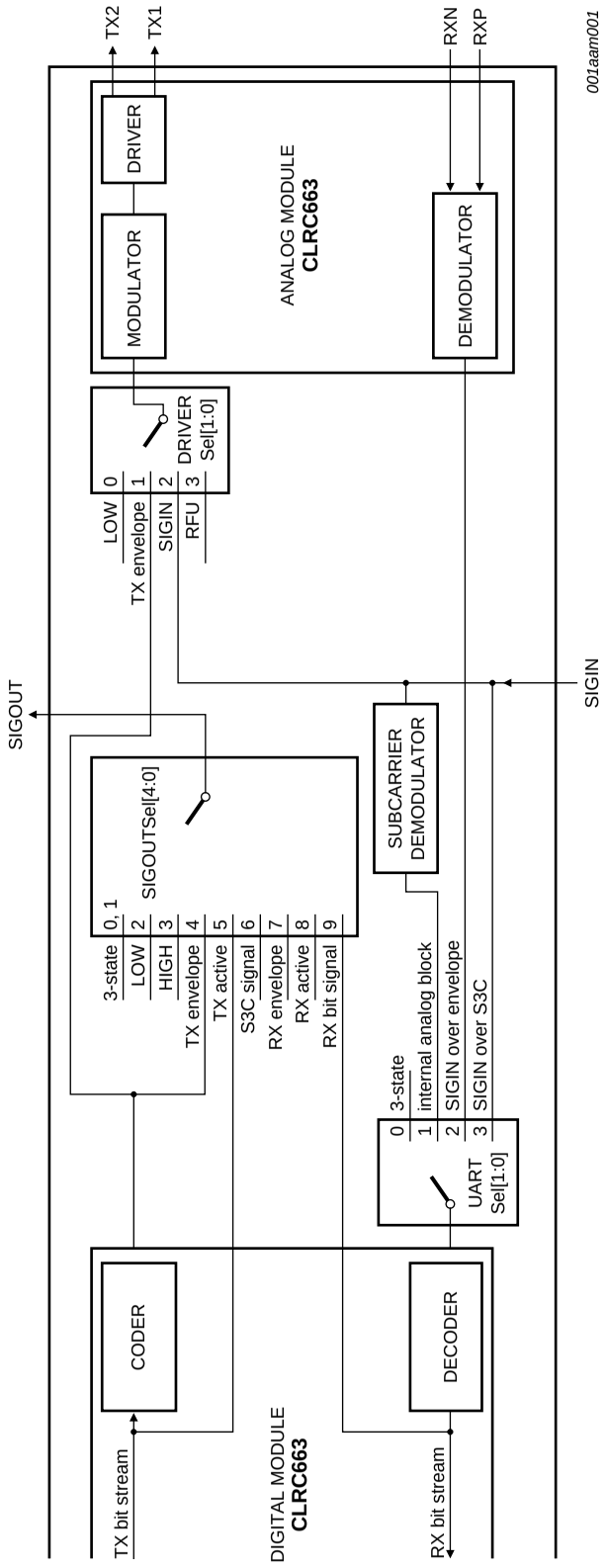


Fig 29. Overview (GPIO0)SIGIN/SIGOUT Signal Routing

12. Memory organization of the EEPROM

12.1 Overview

The CLRC663 has a memory of 8 kB and is organized in sections with pages of 64 bytes.

The following figure show the structure of the EEPROM

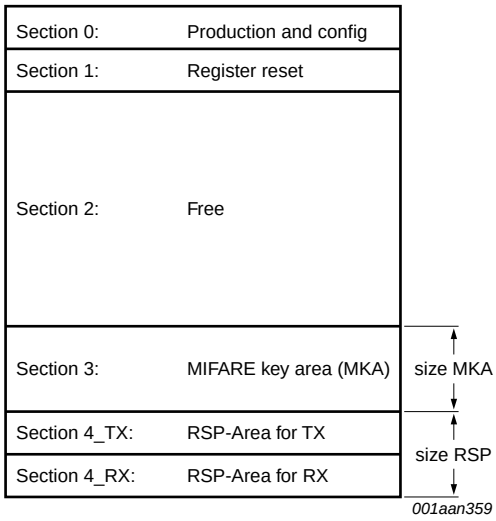


Fig 30. Sector arrangement of the EEPROM

12.2 EEPROM memory organization

Table 225. Table of the EEPROM memory organization

Section	Page	Byte addresses	Access rights	Memory content	See also
0	0	00 to 63	r/w	product information field (read only) and configuration (read and write)	Section 12.2.1
1	1 to 2	64 to 191	r/w	register reset	
2	3 to 95	192 to 6143	r/w	free	
3	96 to 111	6144 to 7167	w	MIFARE key area (WO)	Section 12.2.3
4	112 to 128	7168 to 8191	r	Register Set Protocol (RO)	

Remark: The size of Sections 3 and 4 can be configured.

12.2.1 Production Area

The first page includes production data as well as configuration information.

Table 226. Production area

Page	0	1	2	3	4	5	6	7
0.0	product id		feature lock	version	part ID	batch	part ID batch	
0.1	part ID batch		wafer number	x-pos.	y-pos.	date	date	trimm EE
1.0	trimm LFO	-	-	-	MKA size	RSP size	-	-
1.1	RFU		RFU		-	-	-	-

The size of the MIFARE Key Area (MKA), specifies the number of EE-pages for the MKA.

The size of the Register Set Protocol (RSP), specifies the number of EE-pages for the RSP area. The number of pages is equally divided for use between Tx and Rx.

12.2.2 Configuration Area

The CLRC663 EEPROM has a page size of 64 byte and is r/w.

The second page includes configuration data.

Table 227. Configuration area

Page	0	1	2	3	4	5	6	7
2.0	I2C-address	interface	I2CSAM-address	default prot Rx	default prot Tx	-	Tx CRC present	
2.1	Rx - CRC present		-	-	-	-	-	-
3.0	Tx - Sequence OFF-ON							
3.1	Tx - Sequence ON-OFF							

Only the interface byte as well as the I^2C-address and I^2CSAM-address are selectable.

12.2.2.1 Interface

This section describes the Interface byte configuration.

Table 228. Interface byte

Bit	7	6	5	4	3	2	1	0
	I2C HSP	-	-	I2C-address	boundary scan	host		
access rights	r/w	RFU	RFU	r/w	r/w		r/w	

Table 229. Description of TxDataModWidth bits

Bit	Symbol	Description
7	I2C HSP	when set to 0, the high speed mode is used when set to 1, the high speed + mode is used (default)
6, 5	RFU	-
4	I2C Add	when set to 0, the pins are used (default) when set to 1, the EEPROM is used
3	Boundary Scan	when set to 1, the boundary scan interface is ON (default) when set to 2, the boundary scan is OFF
2 to 0	Host	000b - RS232 001b - I2C 010b - SPI 011b - I2CL 1xx b - pin selection

12.2.3 MIFARE key area

This area is Write Only. The Keys can be loaded into the MIFARE Crypto Unit with the KeyLoadEE command. The size of the MKA can be configured between 0 and 24 (00h - 18h) using the Size_MKA byte in the EE Section 0 (production area + configuration area).

12.2.4 Register set protocol area

The size of this area can be configured between 1 and 31 (01h - 1Fh) using the Size_RSP byte in the EE Section 0 (production area + configuration area).

Half of the RSP Area contains settings for the TX registers (16 bytes). The other half of the Area contains the settings for the RX registers (8 bytes)

e.g. size_RSP = 4

Max. number of Tx settings = ((Size_RSP / 2 pages) × 64 byte / page) / 16 byte / tx_sets = 8 tx_settings

Max. number of Rx settings = ((Size_RSP / 2 pages) × 64 byte / page) / 8 byte / rx_sets = 16 rx_settings

Table 230. Tx and Rx arrangements in the register set protocol area

Section								
Section 4 TX	Tx0		Tx1		TX2		Tx3	
Section 4 TX	Tx4		Tx5		TX6		TX7	
Section 4 Rx	RX0	RX1	RX2	RX3	RX4	RX5	RX6	RX7
Section 4 Rx	RX8	RX9	RX10	RX11	RX12	RX13	RX14	RX15

13. FiFo Buffer

13.1 Overview

An 512 × 8-bit FiFo buffer is implemented in the CLRC663. It buffers the input and output data stream between the host and the internal state machine of the CLRC663. Thus, it is possible to handle data streams with lengths of up to 512 bytes without taking timing constraints into account. The FiFo can also be limited to a size of 255 byte

13.2 Accessing the FiFo buffer

The FiFo-buffer input and output data bus is connected to the register FiFoData_Reg. Writing to this register stores one byte in the FiFo-buffer and increments the internal FiFo-buffer write-pointer. Reading from this register shows the FiFo-buffer contents stored at the FiFo-buffer read-pointer and decrements the FiFo-buffer read-pointer. The distance between the write- and read-pointer can be obtained by reading the register FiFoLength_Reg. If the FiFo is used in 512 byte mode, also the higher bit of FiFoLength in the FiFoControl_Reg register (bit 0 and bit 1) has to be taken into account.

When the µ-Controller starts a command, the CLRC663 may, while the command is in progress, access the FiFo-buffer according to that command. Physically only one FiFo-buffer is implemented, which can be used in input and output direction. Therefore the µ-Controller has to take care, not to access the FiFo buffer in an unintended way.

13.3 Controlling the FiFo buffer

Besides writing to and reading from the FiFo buffer, the FiFo-buffer pointers might be reset by setting the bit FiFoFlash in FiFoControl_Reg to 1. Consequently, the FiFoLevel bits are set to logic 0, the bit ErrIrq in the register Irq0_Reg is cleared, the actually stored bytes are not accessible any more and the FiFo buffer can be filled with another 512 bytes (or 255 bytes if the bit FiFoSize is set to 1) again.

13.4 Status Information about the FiFo buffer

The host may obtain the following data about the FiFo-buffers status:

- Number of bytes already stored in the FiFo-buffer: *FiFoLength* in register *FiFoLength_Reg*
- Warning, that the FiFo-buffer is almost full: *HiAlert* in register *FiFoControl_Reg* according to the value of the water level in register WaterLevel_Reg (Register 0x02 bit [2], Register 0x03 bit[7:0])
- Warning, that the FiFo-buffer is almost empty: *LoAlert* in register *FiFoControl_Reg*
- FiFoOvl bit indicates, that bytes were written to the FiFo buffer although it was already full: *ErrIrq* in register *Irq0_Reg*. *ErrIrq* can be cleared only by setting bit *FiFoFlash* in the register *FiFoControl_Reg*.

The CLRC663 can generate an interrupt signal if:

- *LoAlertIRQEn* in register I*RQ0En_Reg* is set to logic 1 it will activate pin IRQ when *LoAlert* in the register *FiFoControl_Reg* changes to 1.
- *HiAlertIRQEN* in register *IRQ0En_Reg* is set to logic 1 it will activate pin IRQ when *HiAlert* in the register *FiFoControl_Reg* changes to 1.

The bit *HiAlert* is set to logic 1 if maximum *water level* bytes (as set in register *WaterLevel_Reg*) or less can be stored in the FiFo-buffer. It is generated according to the following equation:

$$HiAlert = (FiFoSize - FiFoLength) \leq WaterLevel \quad (1)$$

The bit *LoAlert* is set to logic 1 if *water level* bytes (as set in register *WaterLevel_Reg*) or less are actually stored in the FiFo-buffer. It is generated according to the following equation:

$$LoAlert = FIFOLength \leq WaterLevel \quad (2)$$

14. Timer unit

The external host may use this timer to manage timing relevant tasks. The timer unit may be used in one of the following configurations:

- Time-out counter
- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A time-out during data reception does not influence the reception process automatically). Furthermore, several timer related bits are set and these bits can be used to generate an interrupt.

The CLRC663 has 4 identical timers (Timer 0 - Timer 3). Each timer has an input clock of 13.56 MHz (derived from the 27.12 MHz quartz) and has 16 bits. The reload value for the counter is defined in a range of 0d to 65535d in the register *TnReload_Reg.* Timer 4 also can be used as wake up timer. In this case the internal LPO (Low Power Oscillator) can be used as input clock.

The current value of the timer is indicated by the register *TnCounterVal_Reg*.

If the counter reaches 0 an interrupt will be generated automatically by the next clock indicated by setting the TimerIRq bit in the register CommonIRq_Reg. If enabled, this event can be indicated on the IRQ line. The bit TimerIRq can be set and reset by the host controller. Depending on the configuration the timer will stop at 0h or restart with the value from register TReload_Reg.

The status of the timer is indicated by bit *TnRunning* in register Tcontrol_Reg.

The timer can be manually started by setting *TnRunning* and *TnStartStopNow* in register ControlReg or manually stopped by setting *TnStartStopNow* and clearing *TnRunning* in register *TnControl_Reg*.

Furthermore the timer can be started automatically by setting the bit *TnStart* in the register *TnMode_Reg* to fulfil dedicated protocol requirements automatically.

14.1 Usage timer unit

14.1.1 Time-Out- and Watch-Dog-Counter

Having started the timer by setting *TnReloadValue* the timer unit decrements the *TnCounterValue* Register beginning with a certain start event. If a certain stop event occurs e.g. a bit is received from the card, the timer unit stops (no interrupt is generated).

On the other hand, if no stop event occurs, e.g. the card does not answer in the expected time, the timer unit decrements down to zero and generates a timer interrupt request. This signals the µ-Processor that the expected event has not occurred in the given time T_{Timer}.

14.1.2 Wake-up timer (Timer4)

The wake-up timer can activate the system after a given time. It can start a low power card detection. For the LPCD it is recommended to set *T4AutoWakeUp* and *T4AutoRestart*, to start the Timer and go to Standby. The internal LPO is used as input clock for this timer. If a card is detected stop the Timer and start the communication. If *T4AutoWakeUp* is not set, the IC will not enter Standby mode in case no card is detected. Refer to Section 16.3

14.1.3 Stop watch

The time T_{Timer} [2] between a certain start- and stop event may be measured by the µ-Processor by means of the CLRC663 timer unit. Setting *TReloadValue* the timer starts to decrement. If the defined stop event occurs the timers stops. The time between start and stop can be calculated by µ-Processor

$$\Delta T = (T\ \mathrm{Re}\ load_{value} - Timer_{value}) * T_{Timer} \quad (3)$$

if the timer does not decrements down to zero.

14.1.4 Programmable one-shot timer

The µ-Processor starts the timer unit and waits for the timer interrupt. After the specified time T_{Timer} the interrupt will occur.

14.1.5 Periodical trigger

If the µ-Processor sets bit *TAutoRestart*, it will generate an interrupt request periodically after every T_{Timer}.

2. Refer to Section 27 “Abbreviations”

15. Interrupt request system

The CLRC663 indicates certain events by setting bit *Irq* in the register *Status1Reg* and additionally, if activated, by pin IRQ. The signal on pin IRQ may be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

The following table shows the available interrupt bits, the corresponding source and the condition for its activation. The interrupt bit *TimernIrq* in register *Irq1_Reg* indicates an interrupt set by the timer unit. The setting is done when the timer decrements from 1 down to 0.

The *TxIrq* bit in register *IRq0_Reg* indicates that the transmission is finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit sets the interrupt bit automatically.

The bit *RxIrq* in register *Irq0_Reg* indicates an interrupt when the end of the received data is detected.

The bit *IdleIrq* in register *IRq0_Reg* is set if a command finishes and the content of the command register changes to idle.

The bit *HiAlertIrq* in register *Irq0_Reg* is set to logic 1 if the *HiAlert* bit is set to logic 1, that means the FiFo buffer has reached the level indicated by the bit *WaterLevel*.

The bit *LoAlertIrq* in register *Irq0_Reg* is set to logic 1 if the *LoAlert* bit is set to logic 1, that means the FiFo buffer has reached the level indicated by the bit *WaterLevel*.

The bit *ErrIrq* in register *Irq0_Reg* indicates an error detected by the contactless UART during sending or receiving. This is indicated by any bit set to logic 1 in register *ErrorReg*.

The bit *LPCDIrq* in register *Irq0_Reg* indicates a card detected.

The bit *RxSOFIrq* in register *Irq0_Reg* indicates a detection of a SOF or a subcarrier by the contactless UART during receiving.

The bit *GlobalIRq* in register *Irq1_Reg* indicates an *interrupt occurring at any other interrupt source when enabled.*

Table 231: Interrupt sources

Interrupt bit	Interrupt source	Is set automatically, when
TimerIrq	Timer Unit	the timer counts from 1 to 0
TxIrq	Transmitter	a transmitted data stream ends
RxIrq	Receiver	a received data stream ends
IdleIrq	Command Register	a command execution finishes
HiAlertIrq	FiFo-buffer	the FiFo-buffer is getting full
LoAlertIrq	FiFo-buffer	the FiFo-buffer is getting empty
ErrIrq	contactless UART	an error is detected
LPCDIrq	LPCD	A card was detected when in low power card detection mode
RxSOFIrq	Receiver	Detection of a SOF or a subcarrier
GlobalIrq	all interrupt sources	will be set if an other Irq source is set

16. Clock generation

16.1 Crystal oscillator

The clock applied to the CLRC663 acts as time basis for generation of the carrier sent out at TX and for the quadrature mixer I and Q clock generation as well as for the coder and decoder of the synchronous system. Therefore stability of the clock frequency is an important factor for proper performance. To obtain highest performance, clock jitter has to be as small as possible. This is best achieved by using the internal oscillator buffer with the recommended circuitry.

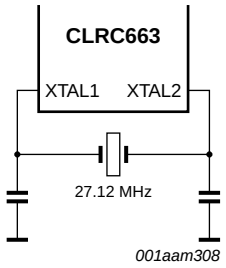


Fig 31. Quartz connection

Table 232: Crystal requirements recommendations

Symbol	Parameter	Conditions	Min	Typ	max	Unit
f_{xtal}	crystal frequency		-	27.12	-	MHz
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation		–250		+250	ppm
ESR	equivalent series resistance		-	50	100	Ω
C_L	load capacitance		-	10	-	pF
P_{xtal}	crystal power dissipation		-	50	100	μW

16.2 IntegerN PLL clock line

The CLRC663 is able to provide a clock with configurable frequency at CLKOUT from 1 MHz to 24 MHz (PLL_Ctrl_Reg and PLL_DIV_Reg). There it can serve as a clock source to a microcontroller which avoids the need of a second crystal oscillator in the reader system. Clock source for the IntegerN-PLL is the 27.12 MHz crystal oscillator. Inside the PLL the input frequency is divided by 2: fin = 13.56 MHz.

Two dividers are determining the output frequency. First a feedback integer-N divider configures the VCO frequency to be N × fin/2 (control signal pll_set_divfb). As supported Feedback Divider Ratios are 23, 27 and 28 VCO frequencies can be 23 × fin / 2 (312 MHz), 27 × fin / 2 (366 MHz) and 28 × fin / 2 (380 MHz). 23 is the recommended value.

The VCO frequency is divided by a factor which is defined by the output divider (pll_set_divout). Of course only a limited accuracy of the output frequencies can be achieved by this approach.Table 233 and Table 234: Shows the accuracy achieved for various frequencies (integer multiples of 1 MHz and some typical RS232 frequencies) and the divider ratios to be used. The register bit ClkOutEn enables the clock at CLKOUT pin.

The following formula can be used to calculate the output frequency:

f_{out} = 13.56 MHz × pll_set_divb /pll_set_divout

Table 233: Setting of feedback divider pll_set_divb [1:0]

Bit 1	Bit 0	Division
0	0	23
0	1	27
1	0	28
1	1	23

Table 234: Setting for the output divider ration pll_set_divout [7:0]

Value	Division
0	8
1	9
2	10
3	11
4	12
5	13
6	14
7	15
8	8
9	9
10	10
...	...
253	253
254	254

Remark: At the value 0 to 7 have special division values.

The following Table 235 shows the recommended divider values for typical clock frequencies.

Table 235. Divider values for selected frequencies using the integerN PLL

Frequency [MHz]	4	6	8	10	12	13	19	20	24	1.8432	3.6864
pll_set_divb	23	27	23	28	23	23	28	28	23	28	28
pll_set_divout	78	61	39	38	26	24	20	19	16	206	103
accuracy [%]	0.04	0.03	0.04	0.08	0.04	0.03	0.08	0.08	0.04	0.01	0.01

Remark: The recommended value for pll_set_divb = 00h (divider value = 23). In this case the internal current consumption of the IntegerN PLL is a minimum.

16.3 Low Power Oscillator (LPO)

The LPO is implemented as a ring oscillator structure. Frequency can be controlled/trimmed by adapting the CCO bias current with lpo_trimm. Target is to achieve a trimming accuracy of 2.5 % with a maximum of 8 trimm-bits for all PVT conditions taking into account also the reference current variations.

With linear trimming behavior following relation is valid for the output frequency:

f_lpo $f_{lpo} = f_{center} + delta\_f \times (80h - lpo\_trimm)$; with f_{center} being the frequency for lpo_trimm in the middle of the range (lpo_trimm = 80h) and delta_f being the trimming step size which must be < 0.05 × f_target (for 2.5 % accuracy).

Trimming will be done by a digital state machine which compares LPO-clock to a reference clock. As reference the 13.56 MHz crystal clock is available. The LPO frequency must be chosen such that a period of 1 ms (=1/1 kHz) can easily be generated with a 2N-counter.

For trimming M periods of the reference clock need to be counted with M = round(13.56 M/f_lpo). A small systematic error due to rounding of M to an integer value is introduced. This error is with 0.06 % much smaller than the targeted trimming accuracy of 2.5 %.

Table 236: Setting of lpo_trimm [7:0]

value	LPO frequency	No. of reference clocks
4	16	848
5	32	424
6	64	212
7	128	106

The LPO can be set to power down with input pin PDOWN/RESET.

17. Power management

17.1 Supply concept

The CLRC663 is supplies of V_{DD} – Supply voltage, PVDD – pad supply and TVDD – Tx power supply. These three voltages are independent and can have different as well as same supply voltage values. e.g. To operate with a 3.3 V supplied Microcontroller, PVDD and V_{DD} shall be 3.3 V, to guarantee maximum field strength TVDD shall be 5 V.

Note: None of this three voltages is allowed to be zero.

Independent of the voltage it is recommended to buffer these supplies with blocking capacitances. V_{DD} and PVDD min 100 nF; TVDD min 100 nF parallel to 1 μF

NOTE: AVDD and DVDD are NO voltage inputs! Buffer them with blocking capacitances of 470 nF each.

17.2 Power reduction mode

17.2.1 Power-down

A hard power-down is enabled with HIGH level on pin PDOWN. This turns off the internal 1.8 V voltage regulators for the analog and digital core Supply as well as the oscillator. All digital input buffers are separated from the input pads and clamped internally (except pin PDOWN itself). The output pins are switched to high impedance.

To leave the power-down mode the level at the pin PDOWN as to be set to LOW. This will start the internal start up sequence. The reader IC is in full mode again when the internal reset sequence is finished, the crystal reaches the point in the oscillation cycle where the oscillation gets stable and the booting sequence is finished.

17.2.2 Standby mode

The standby mode is entered immediately after setting the bit *PowerDown* in the register *Command_Reg* to 1. All internal current sinks are switched off (including the oscillator buffer).

In opposition to the power-down mode, the digital input buffers are not separated by the input pads and keep their functionality. The digital output pins do not change their state.

During standby mode, all registers values, the FiFo's content and the configuration itself will keep its current content.

To leave the standby mode the bit *PowerDown* in the register *Command_Reg* is set to 0. This will start the internal start up sequence. The reader IC is in Full mode again when the internal start up sequence is finished, the crystal reaches the point in the oscillation cycle where the oscillation gets stable and the booting sequence is finished.

17.2.3 Modem OFF mode

When the *ModemOff* bit in the register *Control_Reg* is set to 1 the antenna transmitter and the receiver are switched off.

To leave the modem OFF mode set the *ModemOff* bit in the register *Control_Reg* to 0.

17.3 Low Power Card Detection (LPCD)

The low power card detection is a energy saving modus when the CLRC663 is not used permanently.

The LPCD works in two phases. The standby phase, controlled with the Wake up timer 4, which defines the duration of the standby of the CLRC663. Second phase is the detection-phase. there the values of the I and Q channel are detected and stored in the register map. (LPCD_I_Result_Reg, LPCD_Q_Result_Reg).This time period can be handled with Timer3. The value is compared with the min/max values in the registers (LPCD_IMin_Reg, LPCD_IMax_Reg; LPCD_QMin_Reg, LPCD_QMax_Reg). If it exceeds the limits, a LPCDIrq will be raised.

After the command *LPCD* the standby of the CLRC663 is activated, if selected. The wake-up timer 4 can activate the system after a given time. For the LPCD it is recommended to set *T4AutoWakeUp* and *T4AutoRestart*, to start the timer and then go to standby. If a card is detected the timer stops and the communication can be started. If *T4AutoWakeUp* is not set, the IC will not enter Standby mode in case no card is detected.

17.4 Reset and startup time

A 10 μs constant high level at the Reset pin starts the internal reset procedure.

The following figure shows the internal voltage regulator:

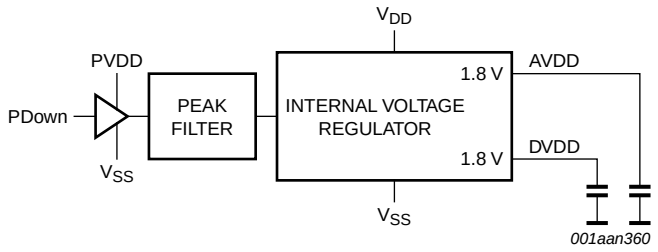


Fig 32. Internal PDown to voltage regulator logic

This internal procedure consists of two phases:

- Power on reset
- Startup time

When the CLRC663 has finished this two phases the reader IC is in Full mode an is ready to be used. Refer to Section 22.1 “Timing characteristics”

18. CLRC663 Command set

18.1 General description

The behavior is determined by a state machine capable to perform a certain set of commands. By writing the according command-code to register Command_Reg the command is executed.

Arguments and/or data necessary to process a command, are exchanged via the FiFo buffer.

18.2 General behavior

- A data transmission of the TxEncoder can be started by a command. When started, the communication is executed as defined in the TxFrameCon register. Therefore a communication frame can consist of a start-symbol, a data-stream, and followed by an end-symbol.
- Each command that needs a certain number of arguments will start processing only when it has received the correct number of arguments via the FiFo buffer.
- The FiFo buffer is not cleared automatically at command start. Therefore, it is also possible to write the command arguments and/or the data bytes into the FiFo buffer and start the command afterwards.
- Each command may be interrupted by the host by writing a new command code into register Command_Reg e.g.: the Idle-Command.

18.3 CLRC663 commands overview

Table 237. Command overview

Command	No.	No.	Parameter	Short description
Idle	0.0000	00h	no	no action, cancels current command execution
LPCD	0.0001	01h	no	low power card detection
LoadKey	0.0010	02h	MIFARE key (6 bytes)	reads a key from FiFo buffer ant puts it into Key buffer
MFAuthent	0.0011	03h	authentication command code (60h, 61h), block address	performs the MIFARE standard authentication in MIFARE read/write mode only
AckReq	0.0100	04h	no	performs a query, an Ack and a Req-Rn for ISO/IEC18000-3 Mode 3
Receive	0.0101	05h	no	activates the receive circuit
Transmit	0.0110	06h	no	transmits data from the FiFo buffer
Transceive	0.0111	07h	no	transmits data from the FiFo buffer and automatically activates the receiver after transmission finished
WriteE2	0.1000	08h	address (2 bytes, 0000h - 1FFFh), data (1 byte)	gets one byte from FiFo buffer and writes it to the internal E2Prom
WriteE2Pages	0.1001	09h	page Address (1 byte, 00h - 7Fh), data (up to 64 bytes)	gets up to 64 bytes from FiFo buffer and writes it to the internal E2Prom
ReadE2	0.1010	0Ah	address (2 bytes, 0000h - 1FFFh), length [1 byte, 01h (= 1 byte) - 00h (= 256 byte)]	reads data from the E2Prom and puts it into the FiFo buffer

Table 237. Command overview *...continued*

Command	No.	No.	Parameter	Short description
LoadReg	0.1100	0Bh	EEAddress (2 bytes, within sector2), RegAdr (1 byte, 0x00 - 0xFF), number of Register to be copied (1 byte, 0x01 - 0xFF).	reads data from the internal E2Prom and initializes the CLRC663 registers
LoadProtocol	0.1101	0Ch	Protocol Number RX (1 byte, 0x00 - 0xFF), Protocol Number TX (1 byte, 0x00 - 0xFF)	reads data from the internal E2Prom and initializes the CLRC663 registers needed for a Protocol change
LoadKeyE2	0.1110	0Eh	KeyNr (1 byte, 0x00 - 0xFF)	copies a key of the E2OProm into the key buffer
StoreKeyE2	0.1111	0Fh	KeyNr (1 byte, 0x00 - 0xFF), one or more MIFARE Keys (á 6 byte)	stores a MIFARE key into the EEPROM
Soft Reset	1.1111	1Fh	no	resets the CLRC663

18.3.1 CLRC663 Command description

18.3.1.1 Idle command

This command indicates that the RC663 is in idle mode. This command is also used to terminate the actual command.

18.3.1.2 LPCD command

This command performs a low power card detection and or an automatic trimming of the LPO. The values of the sampled I and Q channel are stored in the register map. The value is compared with the min/max values in the register. If it exceeds the limits, an LPCD_Irq will be raised. After the command the standby is activated if selected.

18.3.1.3 Load key command

Parameter: MIFARE Key (6 bytes).
Loads a MIFARE Key (6 bytes) for Authentication from the FiFo into the crypto1 unit. Unused bytes remain in the FiFo.

Abort condition: Less than 6 bytes in FiFo.

18.3.1.4 MFAuthent command

This command handles the MIFARE authentication to enable a secure communication to any MIFARE classic card. The following data shall be written to the FiFo before the command can be activated:

- LoadKeyE2
- Authentication command code (60h, 61h)
- Block address
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total, 12 bytes are written to the FiFo.

Remark: When the MFAuthent command is active, any FiFo access is blocked. If there is an access to the FiFo, the bit WrErr in the ErrorReg register is set.

This command terminates automatically when the MIFARE card is authenticated and the bit MFCrypto1On in the Status_Reg register is set to logic 1.

This command does not terminate automatically when the card does not answer, therefore the timer should be initialized to automatic mode. In this case, beside the bit IdleIrq, the bit TimerIrq can be used as termination criteria. During authentication processing the bit RxIrq and bit TxIrq are blocked. The Crypto1On bit is only valid after termination of the authentication command (either after processing the protocol or after writing IDLE to the command register).

In case there is an error during authentication, the bit ProtocolErr in the ErrorReg register is set to logic 1 and the bit Crypto1On in register Status2Reg is set to logic 0.

18.3.1.5 Ack Reqcommand

Performs a Query (Full command must be written into the FiFo); a Ack and a ReqRn command. All answer of the command will be written into the FiFo. The error flag is copied after the answer into the FiFo.

This command terminates automatically when finished and the active command is idle.

18.3.1.6 Receive command

The CLRC663 activates the receiver path and waits for any data stream to be received. The correct settings have to be chosen before starting this command.

This command terminates automatically when the received data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected framing and speed.

Remark: If the bit RxMultiple in the RxModeReg register is set to logic 1, the Receive command does not terminate automatically. It has to be terminated by activating any other command in the CommandReg register.

18.3.1.7 Transceive command

This command transmits data from the FiFo and receives data from the RF field conce. The first action is transmitting and after a transmission the command is changed to receive a data stream.

Each transmission process starts by writing the command into register CommandReg e.g. the command idle.

Remark: If the bit RxMultiple in register RxModeReg is set to logic 1, this command will never leave the receiving state, because the receiving will not be cancelled automatically.

18.3.1.8 Transmit command

The content of the FiFo is transmitted immediately after starting the command. Before transmitting the FiFo content all relevant register have to be set to transmit data.

This command terminates automatically when the FiFo gets empty. It can be terminated by any other command written to the command register.

18.3.1.9 WriteE2 command

Parameter: address (2 byte), data (1 byte)

This command writes one byte into the EEPROM. If the FiFo contains no data, the command will wait until the data is available

Abort condition: insufficient parameter in FiFo; Address-parameter outside of range

18.3.1.10 WriteE2PAGE command

Parameter: Page address (1 byte), data (up to 64 byte)

This command writes up to 64 bytes into the EEPROM. The addresses are not allowed to wrap over a page border. If this is the case, this additional data be ignored and stays in the FiFo. The programming starts after 64 bytes are read from the FiFo or the FiFo is empty.

Abort condition: Insufficient parameters in FiFo; Page address parameter outside of range

18.3.1.11 ReadE2 command

Parameter: address (2 byte); length (1 byte).

Reads up to 256 bytes from the EEPROM to the FiFo. If a read operation exceeds the address 0x1FFF, the read operation continues from address 0x0000.

Abort condition: Insufficient parameter in FiFo; Address parameter outside of range.

18.3.1.12 LoadReg command

Parameter: address (2 byte, within the free sectors); register address (1 byte), number of register to be copied (1 byte)
Read a defined number of bytes from the EEPROM and copies the value into the Register set, beginning at the given RegAdr.

Abort condition: Insufficient parameter in FiFo; Address parameter outside of range.

18.3.1.13 LoadProtocol command

Parameter: Protocol Number RX (1 byte), Protocol Number TX (1 byte).

Read out the EEPROM and copies the value to the RX-Protected area and to the TX protected area. These are all important registers to a Protocol selection.

Abort condition: Insufficient parameter in FiFo

18.3.1.14 LoadKeyE2 command

Parameter: key number (1 byte)
Load a MIFARE key for authentication from the EEPROM into the crypto1 unit.

Abort condition: Insufficient parameter in FiFo; KeyNr is outside the MKA.

18.3.1.15 StoreKeyE2 command

Parameter: key number (1 byte), one or more MIFARE Keys (a 6 bytes).
Stores MIFARE Keys into the EEPROM. If an incomplete Key (less than 6 bytes) is written into the FiFo, this key will be ignored and will remain in the FiFo.

Abort condition: Insufficient parameter in FiFo; KeyNr is outside the MKA;

18.3.1.16 Soft Reset command

Parameter: No,
This command is performing a soft rest. During this command the default values for the register set will be read from the EEPROM and stored in the register set.

19. Limiting values

Table 238. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage		–0.5	+5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage		–0.5	+5.5	V
P_{tot}	total power dissipation	per package; Umax * Imax	-	1125	mW
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V

20. Recommended operating conditions

Table 239. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			3	5	5.5	V
$V_{DD(TVDD)}$	TVDD supply voltage		[1]	3	5	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage			3	5	5.5	V
T_{amb}	ambient temperature			–25		+85	°C

[1] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DD}.

21. Thermal characteristics

Table 240. Thermal characteristics

Symbol	Parameter	Conditions	Package	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB	HVQFN32	40	K/W

22. Characteristics

Table 241. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics I/O Pin Characteristics IF3-SDA in I^2C configuration						
I_{LI}	input leakage current	output disabled	-	2	100	nA
V_{IL}	LOW-level input voltage		–0.5	-	$0.3xV_{DD(PVDD)}$	V
V_{IH}	HIGH-level input voltage		$0.7xV_{DD(PVDD)}$	-	$V_{DD(PVDD)}$ + 0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.3	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; Standard Mode, Fast mode	4	-	-	mA
		V_{OL} = 0.6 V; Standard Mode, Fast mode	6	-	-	mA

Table 241. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{f(o)}$	output fall time	Standard mode, Fast mode, C_L < 400 pF	-	-	250	ns
		Fast mode +; C_L < 550 pF	-	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	-	50	ns
C_i	input capacitance		-	3.5	5	pF
C_L	load capacitance	Standard mode	-	-	400	pF
		Fast mode	-	-	550	pF
Core supply Pin AVDD/DVDD						
V_{DDA}	analog supply voltage		-	1.8	-	V
V_{DDD}	digital supply voltage		-	1.8	-	V
C_{Load}	load Capacitance	AVDD	220	470	-	nF
C_{Load}	load Capacitance	DVDD	220	470	-	nF
Current Consumption						
I_{pd}	power-down current	PDOWN pin pulled HIGH [1]	-	8	40	nA
I_{stb}	standby current	Standby bit = 1	-	3	6	µA
I_{DD}	supply current		-	17	20	mA
		modem off	-	0.45	0.5	mA
$I_{DD(TVDD)}$	TVDD supply current		-	100	200	mA
I/O Pin Characteristics SIGIN, SIGOUT, CLKOUT, IFSEL0, IFSEL1, TCK, TMS, TDI, TDO, IRQ, IF0, IF1, IF2, SCL2, SDA2						
I_{LI}	Input leakage current	output disabled	-	50	500	nA
V_{IL}	LOW-level input voltage		–0.5	-	$0.3xV_{DD(PVDD)}$	V
V_{IH}	HIGH-level input voltage		$0.7xV_{DD(PVDD)}$	-	$V_{DD(PVDD)}$ + 0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = <tbd> mA, $V_{DD(PVDD)}$ = 5.0 V	-	-	0.4	V
		I_{OL} = <tbd> mA, $V_{DD(PVDD)}$ = 3.3 V	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OL} = <tbd> mA, $V_{DD(PVDD)}$ = 5.0 V	4.6	-	-	V
		I_{OL} = <tbd> mA, $V_{DD(PVDD)}$ = 3.3 V	2.9	-	-	V
C_i	input capacitance		-	2.5	4.5	pF
Pull-up resistance for TCK, TMS, TDI, IF2						
R_{pu}	pull-up resistance		50	72	120	kΩ
Pin Characteristics AUX 1, AUX 2						
V_o	output voltage rage		0	-	1.8	V
C_L	load capacitance		-	-	400	pF
Pin Characteristics RXP, RXN						
V_i	input voltage		0	-	1.8	V
C_i	input capacitance		2	3.5	5	pF
V_{mod}	modulation voltage		-	2.5	-	V

Table 241. Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Vpp	Max Range of Signal on RxP, RXN			-	-	1.65	V
Pins TX1 and TX2							
V_o	output voltage			$V_{ss(TVss)}$	-	$V_{DD(TVDD)}$	V
R_o	output resistance			-	1.5	-	Ω
Current consumption							
I_{pd}	power-down current			-	8	200	nA
	Standby current		[1]	-	3	6	μA
I_{LPCD}	LPCD sleep current		[1]	-	3	6	μA
I_{VDD}	Supply current			-	17	20	mA
I_{VDD} modem off	supply current, transceiver off			-	0.45	0.5	mA
$I_{DD(PVDD)}$	PVDD supply current		[2]	<tbd>	<tbd>	<tbd>	mA
$I_{DD(TVDD)}$	TVDD supply current		[3][4][5]	-	100	200	mA
Clock frequency Pin CLKOUT							
f_{clk}	clock frequency			-	27.12	-	MHz
δ_{clk}	clock duty cycle			-	50	-	%
Crystal oscillator							
$V_{o(p-p)}$	peak-to-peak output voltage	pin XTAL1		-	1	-	V
V_i	input voltage	pin Xtal1		0	-	1.8	V
C_i	input capacitance	pin XTAL1		-	3	-	pF
		pin XTAL2		-	3	-	pF
Typical input requirements							
f_{xtal}	crystal frequency			-	27.12	-	MHz
ESR	equivalent series resistance			-	50	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	50	100	μW

[1] I_{pd} is the total current for all supplies.

[2] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[3] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[4] During typical circuit operation, the overall current is below 100 mA.

[5] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

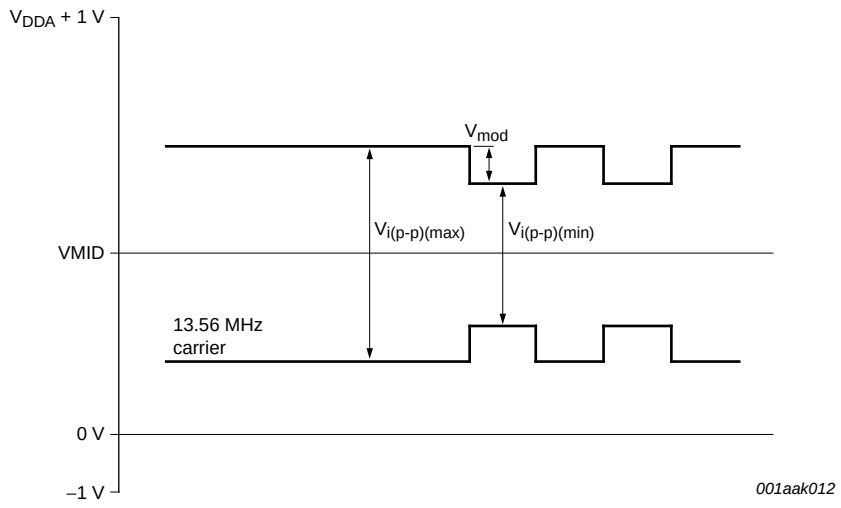


Fig 33. Pin RX input voltage range

22.1 Timing characteristics

Table 242. SPI timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time		50	-	-	ns
t_{SCKH}	SCK HIGH time		50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time		0	-	-	ns
t_{NSSH}	NSS HIGH time	before communication	50	-	-	ns

Table 243. I^2C-bus timing in Fast mode and Fast mode Plus

Symbol	Parameter	Conditions	Fast mode		Fast mode Plus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	400	0	1000	kHz
$t_{HD;STA}$	hold time (repeated) START condition	after this period, the first clock pulse is generated	600	-	260		ns
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	260		ns
$t_{SU;STO}$	set-up time for STOP condition		600	-	260		ns
t_{LOW}	LOW period of the SCL clock		1300	-	500		ns
t_{HIGH}	HIGH period of the SCL clock		600	-	260		ns

Table 243. I^2C-bus timing in Fast mode and Fast mode Plus *...continued*

Symbol	Parameter	Conditions	Fast mode		Fast mode Plus		Unit
			Min	Max	Min	Max	
$t_{HD;DAT}$	data hold time		0	900		450	ns
$t_{SU;DAT}$	data set-up time		100	-			ns
t_r	rise time	SCL signal	20	300		120	ns
t_f	fall time	SCL signal	20	300		120	ns
t_r	rise time	SDA and SCL signals	20	300		120	ns
t_f	fall time	SDA and SCL signals	20	300		120	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	0.5		µs

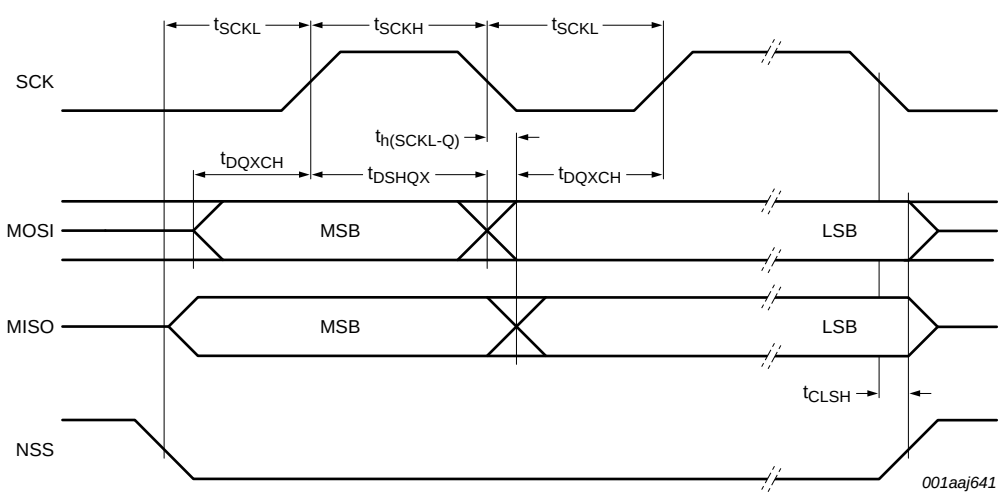


Fig 34. Timing diagram for SPI

Remark: To send more bytes in one data stream the NSS signal must be LOW during the send process. To send more than one data stream the NSS signal must be HIGH between each data stream.

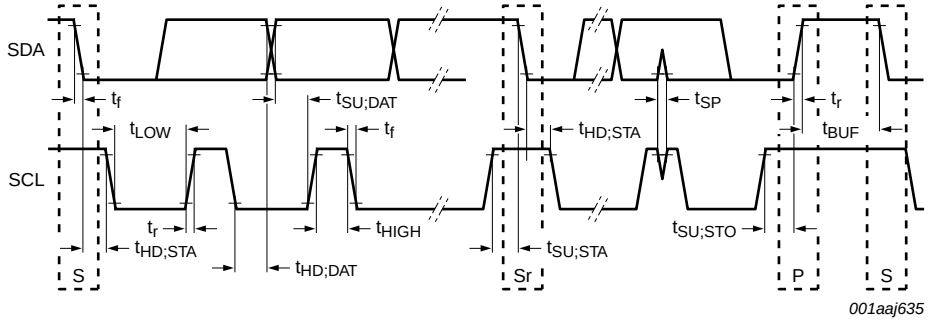


Fig 35. Timing for fast and standard mode devices on the I^2C-bus

23. Application information

A typical application diagram using a complementary antenna connection to the CLRC663 is shown in Figure 36.

The antenna tuning and RF part matching is described in the application note Ref. 1 and Ref. 2.

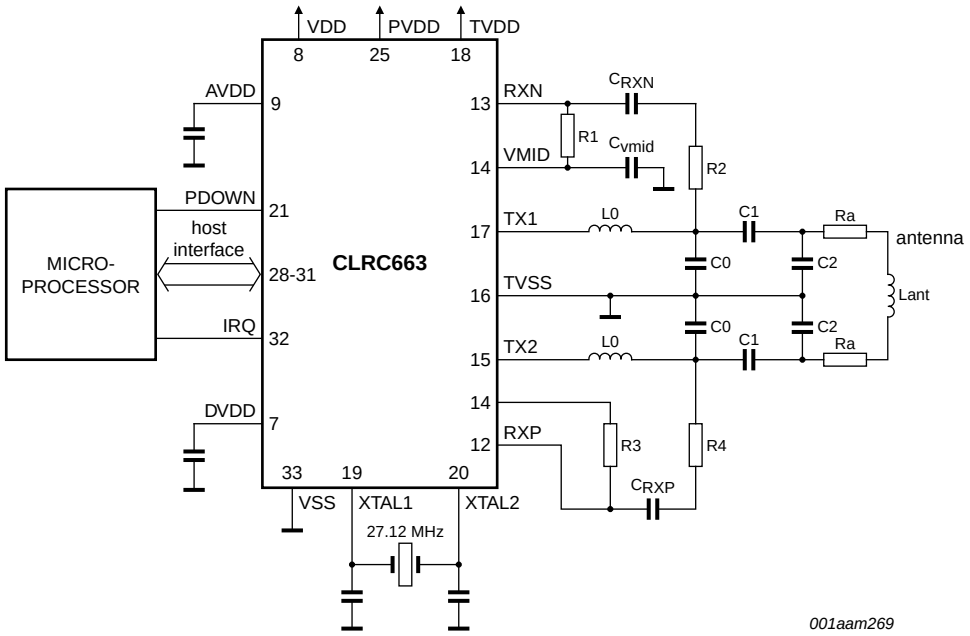


Fig 36. Typical application antenna circuit diagram

23.1 Circuit description

The matching circuit consists of an EMC low pass filter (L0 and C0), a matching circuitry (C1 and C2), and a receiving circuits (R1 = R3, R2 = R4, C3 = C5 and C4 = C6;), and the antenna itself.

For more detailed information about designing and tuning an antenna please refer to the Application notes

- MICORE reader IC family; Directly Matched Antenna Design, Ref. 1 and
- MIFARE (14443A) 13.56 MHz RFID Proximity Antennas, Ref. 2.

23.1.1 EMC low pass filter

The MIFARE system operates at a frequency of 13.56 MHz. This frequency is generated by a quartz oscillator to clock the CLRC663 and is also the basis for driving the antenna with the 13.56 MHz energy carrier. This will not only cause emitted power at 13.56 MHz but will also emit power at higher harmonics. The international EMC regulations define the amplitude of the emitted power in a broad frequency range. Thus, an appropriate filtering of the output signal is necessary to fulfil these regulations.

A multi-layer board is recommended to implement a low pass filter as shown in the circuit above. The low pass filter consists of the components L0 and C0. The recommended values are given in the above mentioned application notes.

Remark: To achieve best performance all components shall have at least the quality of the recommended ones.

Remark: The layout has a major influence on the overall performance of the filter.

23.1.2 Antenna matching

Due to the impedance transformation of the given low pass filter, the antenna coil has to be matched to a certain impedance. The matching elements C1 and C2 can be estimated and have to be fine tuned depending on the design of the antenna coil.

The correct impedance matching is important to provide the optimum performance. The overall quality factor has to be considered to guarantee a proper ISO/IEC 14443 communication scheme. Environmental influences have to considered as well as common EMC design rules.

For details refer to the above mentioned application notes.

Remark: Do not exceed the current limits I_{TVDD}, otherwise the chip might be destroyed.

Remark: The overall 13.56 MHz RFID proximity antenna design with the CLRC663 chip is straight forward and doesn't require a special RF-know how. However, all relevant parameters have to be considered to guarantee an overall optimum performance together with international EMC compliance.

23.1.3 Receiving circuit

The internal receiving concept of the CLRC663 makes use both side-bands of the sub-carrier load modulation of the card response via a differential receiving concept (RXP,RXN). No external filtering is required.

It is recommended to use the internally generated VMID potential as the input potential of pin RX. This DC voltage level of VMID has to be coupled to the Rx-pins via R2 and R4. To provide a stable DC reference voltage capacitances C4, C6 has to be connected between VMID and ground. Refer to Figure 36

Considering the (AC) voltage limits at the Rx-pins the AC voltage divider of R1 + C3 and R2 as well as R3 + C5 and R4 has to be designed. Depending on the antenna coil design and the impedance matching the voltage at the antenna coil varies from antenna design to antenna design. Therefore the recommended way to design the receiving circuit is to use the given values for R1(= R3), R2 (= R4), and C3 (= C5) from the above mentioned application note, and adjust the voltage at the RX-pins by varying R1(= R3) within the given limits.

Remark: R2 and R4 are AC-wise connected to ground (via C4 and C6).

23.1.4 Antenna coil

The precise calculation of the antenna coils' inductance is not practicable but the inductance can be **estimated** using the following formula. We recommend designing an antenna either with a circular or rectangular shape.

$$L_1 = 2 \cdot I_1 \cdot \left(ln \langle \frac{I_1}{D_1} \rangle - K \right) N_1^{1,8} \quad (4)$$

- I_1 - Length in cm of one turn of the conductor loop
- D_1 - Diameter of the wire or width of the PCB conductor respectively
- K - Antenna shape factor (K = 1,07 for circular antennas and K = 1,47 for square antennas)
- L_1 - Inductance in nH
- N_1 - Number of turns
- Ln: Natural logarithm function

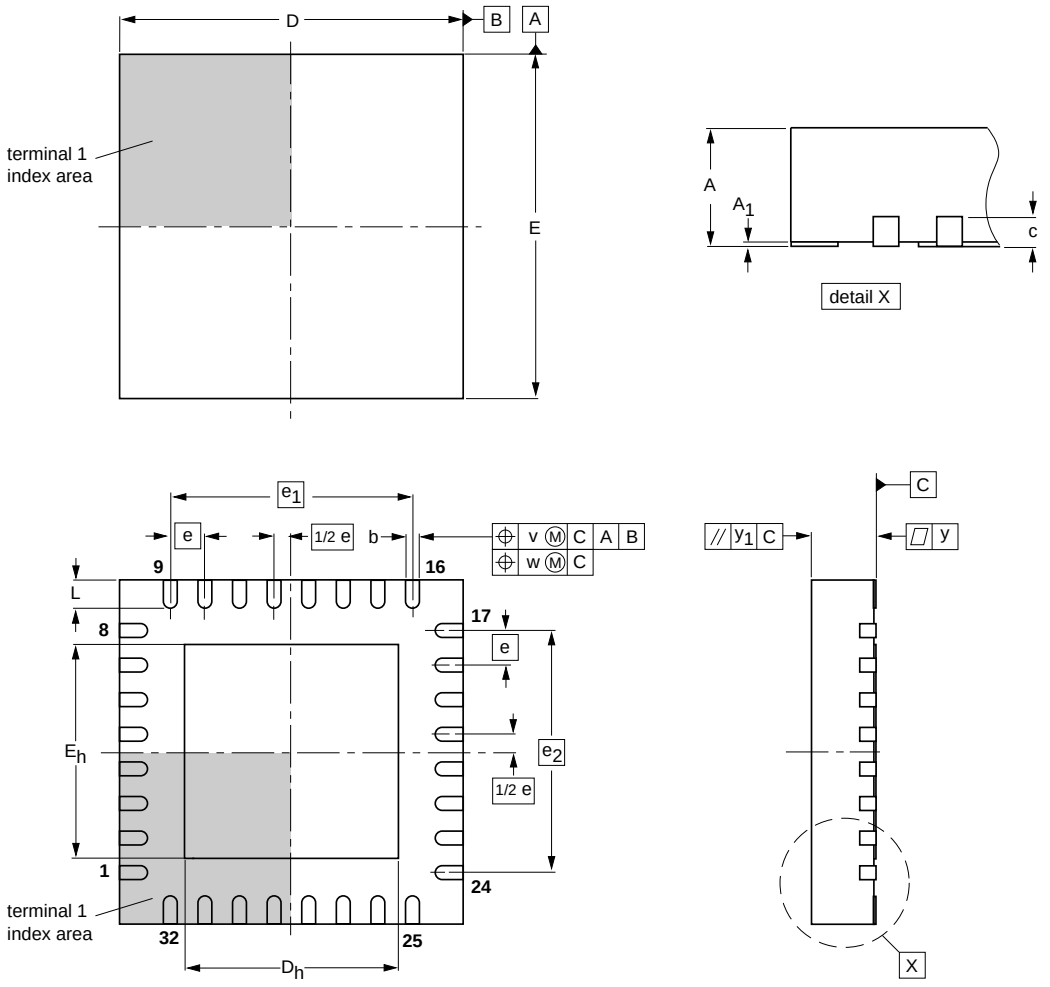
The actual values of the antenna inductance, resistance, and capacitance at 13.56 MHz depend on various parameters such as:

- antenna construction (Type of PCB)
- thickness of conductor
- distance between the windings
- shielding layer
- metal or ferrite in the near environment

Therefore a measurement of those parameters under real life conditions, or at least a rough measurement and a tuning procedure is highly recommended to guarantee a reasonable performance. For details refer to the above mentioned application notes.

24. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 37. Package outline SOT617-1 (HVQFN32)

Detailed package information can be found at
http://www.nxp.com/package/SOT617-1.html.

25. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*. MSL for this package is level 2 which means 260 °C convection reflow temperature.

Dry pack is required.

1 year out-of-pack floor life at maximum ambient temperature 30 °C/ 85 % RH.

26. Packing information

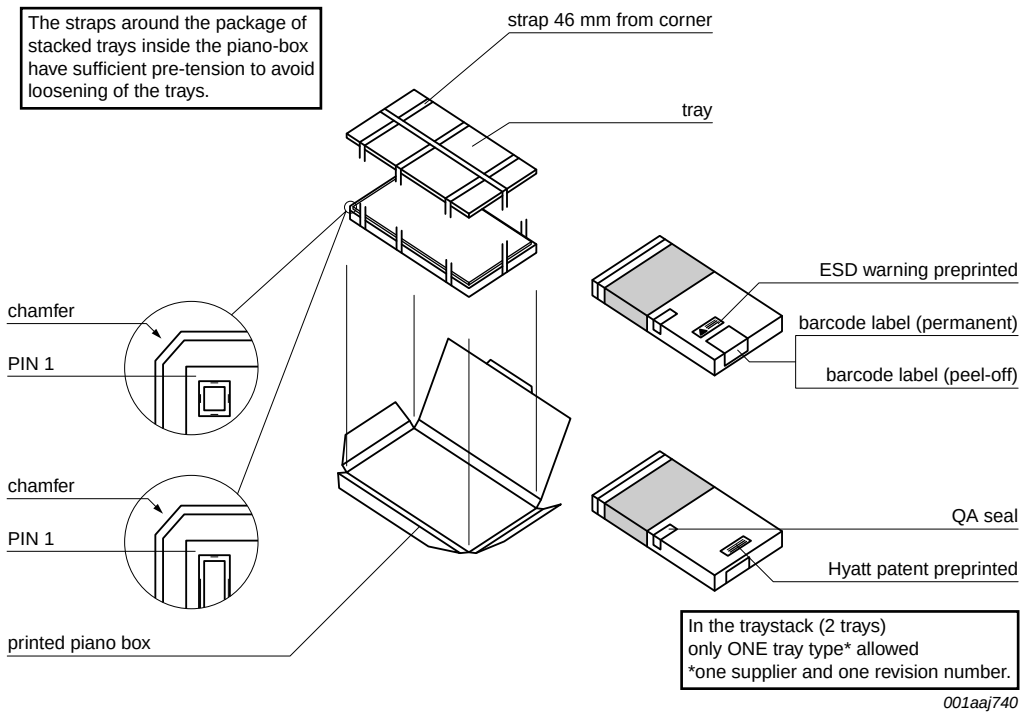


Fig 38. Packing information 1 tray

27. Abbreviations

Table 244. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
CW	Continuous Wave
EGT	Extra Guard Time
EMC	Electro Magnetic Coupling
EMD	Electro Magnetic Disturbance
EOF	End Of Frame
EPC	Electronic Product Code
ETU	Elementary Time Unit
GPIO	General Purpose Input/Output
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LFO	Low Frequency Oscillator
LPCD	Low Power Card Detection
LSB	Least Significant Bit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
NRZ	Not Return to Zero
NSS	Not Slave Select
OTP	One Time Programmable
PCD	Proximity Coupling Device (Reader)
PLL	Phase-Locked Loop
RTZ	Return To Zero
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
SW	SoftWare
T_{Timer}	Timing of the clk period (1/clk period)
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter
UID	Unique IDentification
VCO	Voltage Controlled Oscillator

28. References

[1] **Application note —** *MFRC52x Reader IC Family Directly Matched Antenna Design*

[2] **Application note —** *MIFARE (ISO/IEC 14443 A) 13.56 MHz RFID Proximity Antennas*

[3] **BSDL File —** *Boundary scan description language file of the CLRC663*

29. Revision history

Table 245. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CLRC663 v.2.0	20110615	Preliminary data sheet	-	CLRC663 v.1.0
Modifications:	• General update			
CLRC663 v.1.0	20110308	Objective data sheet	-	-

30. Legal information

30.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 15 June 2011
171120