mosaic
semiconductor, inc.

11403 West Bernado Court, Suite 100, San Diego, CA 92127.
Tel No: (619) 674 2233, Fax No: (619) 674 2230

8M x 8 SRAM MODULE

SYS88000RKX - 70/85/10/12

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Description

The SYS88000RKX is a plastic 64Mbit Static RAM Module housed in a standard 38 pin Single In-Line package organised as 8M x 8 with access times of 70, 85,100, or 120 ns.

The module is constructed using sixteen 512Kx8 SRAMs in TSOPII packages mounted onto both sides of an FR4 epoxy substrate. This offers an extremely high PCB packing density.

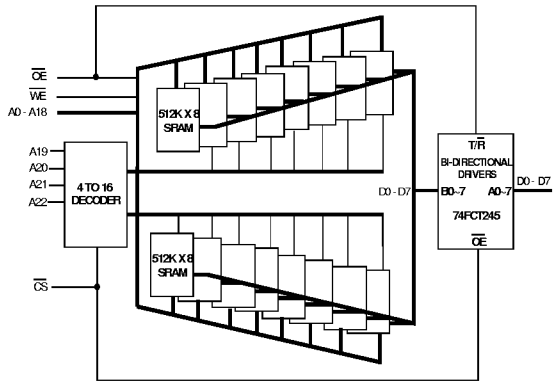
The device is offered in standard and low power versions, with the -L module having a low voltage data retention mode for battery backed applications. On board buffering is provided to reduce output capacitance.

Note: $\overline{CS}$ and $\overline{OE}$ on the module, should be used with care to avoid on and off board bus contention.

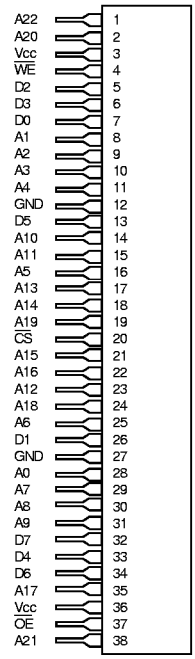
Features

- Access Times of 70/85/100/120 ns.
- Low Power Disapation:
  Operating 935 mW (Max.)
  Standby -L Version 11 mW (Max.)
- 5 Volt Supply ± 10%.
- Completely Static Operation.
- Equal Access and Cycle Times.
- Low Voltage V_{CC} Data Retention.
- On-board Decoding & Capacitors.
- 38 Pin Single-In-Line package.
- Upgrade from SYS84000RKX (32Mbit).

Block Diagram



Pin Definition



Pin Functions

Address Inputs	**A0 ~ A22**
Data Input/Output	**D0 ~ D7**
Chip Select	**$\overline{CS}$**
Write Enable	**$\overline{WE}$**
Output Enable	**$\overline{OE}$**
No Connect	**NC**
Power (+5V)	**V_{CC}**
Ground	**GND**

Package Details

Plastic 38 pin Single-In-Line (SIP)

Absolute Maximum Ratings (1)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Voltage on any pin relative to V_{SS}	V_T (2)	-0.3	-	7.0	V
Power Dissipation	P_T	-	1.0	-	W
Storage Temperature	T_{STG}	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

Parameter		*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-0.3	-	0.8	V
Operating Temperature	(Commercial)	T_A	0	-	70	°C
	(Industrial)	T_{AI}	-40	-	85	°C

DC Electrical Characteristics (V_{CC}=5V±10%) TA 0 to 70 °C

Parameter		*Symbol*	*Test Condition*	*Min*	*Typ*	*max*	*Unit*
I/P Leakage Current	Address,$\overline{OE}$,$\overline{WE}$	I_{LI}	$0V \le V_{IN} \le V_{CC}$	-16	-	16	µA
Output Leakage Current		I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	-16	-	16	µA
Operating Current		I_{CC1}	Min. Cycle, $\overline{CS}$ = V_{IL}, $V_{IL} \le V_{IN} \le V_{IH}$	-	-	170	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$ = V_{IH}	-	-	48	mA
	CMOS levels	I_{SB2}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2 \le V_{IN} \le V_{CC}$-0.2V	-	-	32	mA
	-L Version (CMOS)	I_{SB3}	$\overline{CS} \ge V_{CC}$-0.2V, $0.2 \le V_{IN} \le V_{CC}$-0.2V	-	-	2	mA
Output Voltage		V_{OL}	I_{OL} = 8.0mA	-	-	0.4	V
		V_{OH}	I_{OH} = -4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Add 800mA to -L CMOS standby currents to obtain industrial temp range parameters.

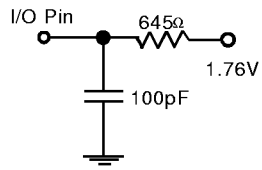
Capacitance (V_{CC}=5V±10%, T_A=25°C) Note: Capacitance calculated, not measured.

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance (Address,$\overline{OE}$,$\overline{WE}$)	C_{IN1}	V_{IN} = 0V	128	pF
I/P Capacitance (other)	C_{IN2}	V_{IN} = 0V	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	160	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load



Operation Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*DATA PINS*	*SUPPLY CURRENT*	*MODE*
H	X	X	High Impedance	I_{SB1} , I_{SB2} , I_{SB3}, I_{SB4}	Standby
L	**L**	**L**	**Invalid State**	~	**Invalid**
L	L	H	Data Out	I_{CC1}	Read
L	H	L	Data In	I_{CC1}	Write
L	H	H	High-Impedance	I_{CC1}	High-Z

Notes : H = V_{IH} : L =V_{IL} : X = V_{IH} or V_{IL}
$\overline{OE}$ must not be tied low permanently.

Low V_{cc} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ(1)*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR1} (2)	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}$-0.2V	-	-	1.2	mA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5.0	-	-	ms

Notes (1) Typical figures are measured at 25°C.
(2) This parameter is guaranteed not tested.
(3) Add 840mA to -L CMOS standby currents to obtain industrial temp range parameters.

AC OPERATING CONDITIONS

Read Cycle

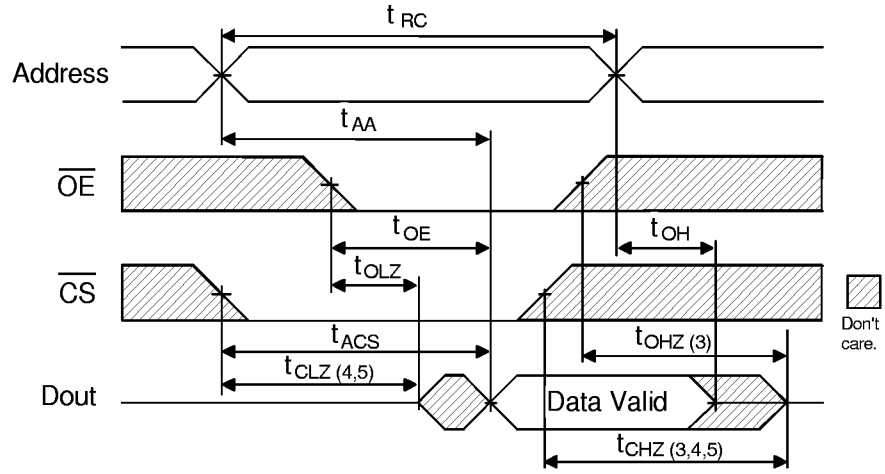
		-70		-85		-10		-12		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	70	-	85	-	100	-	120	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	-	120	ns
Chip Select Access Time	t_{ACS}	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	40	-	50	-	55	-	60	ns
Output Hold from Address Change	t_{OH}	11.5	-	11.5	-	11.5	-	11.5	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	1.5	-	1.5	-	1.5	-	1.5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	1.5	-	1.5	-	1.5	-	1.5	-	ns
Chip Deselection to O/P in High Z	t_{CHZ}	0	5	0	5	0	5	0	5	ns
Output Disable to Output in High Z	t_{OHZ}	0	5	0	5	0	5	0	5	ns

Write Cycle

			-70		-85		-10		-12		
Parameter		*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time		t_{WC}	70	-	85	-	100	-	120	-	ns
Chip Selection to End of Write		t_{CW}	60	-	75	-	80	-	100	-	ns
Address Valid to End of Write		t_{AW}	60	-	75	-	80	-	100	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width		t_{WP}	50	-	60	-	70	-	70	-	ns
Write Recovery Time		t_{WR}	5	-	5	-	5	-	5	-	ns
Write to Output in High Z	***	t_{WHZ}	0	30	0	35	0	40	0	40	ns
Data to Write Time Overlap		t_{DW}	35	-	40	-	45	-	45	-	ns
Data Hold from Write Time		t_{DH}	0	-	0	-	0	-	0	-	ns
Output active from end of write	***	t_{OW}	5	-	5	-	5	-	5	-	ns

*** Theses signals are the internal Ram signals on the module and are included to assist control signal timing.

Read Cycle Timing Waveform (1,2)



AC Read Characteristics Notes

(1) $\overline{WE}$ is High for Read Cycle.

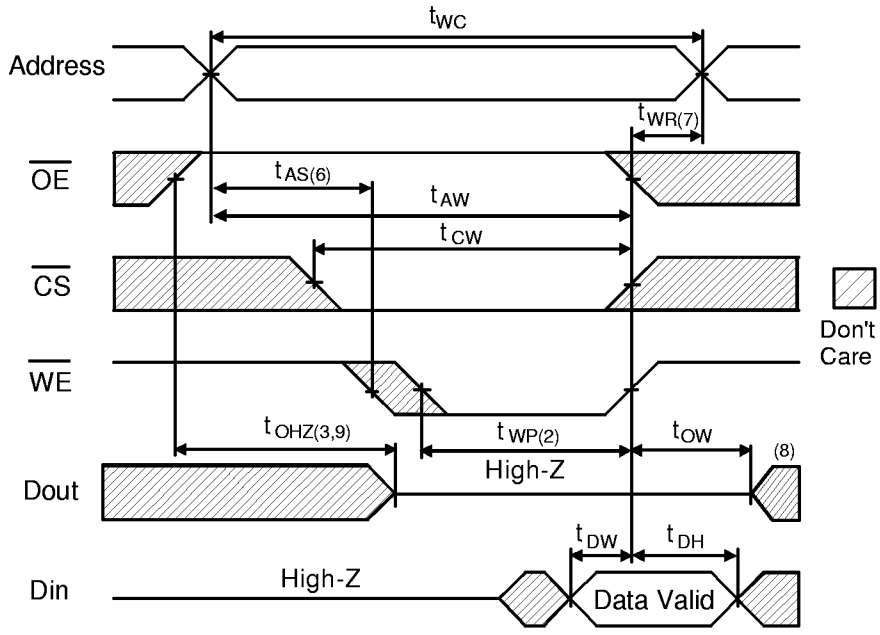
(2) All read cycle timing is referenced from the last valid address to the first transition address.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels.

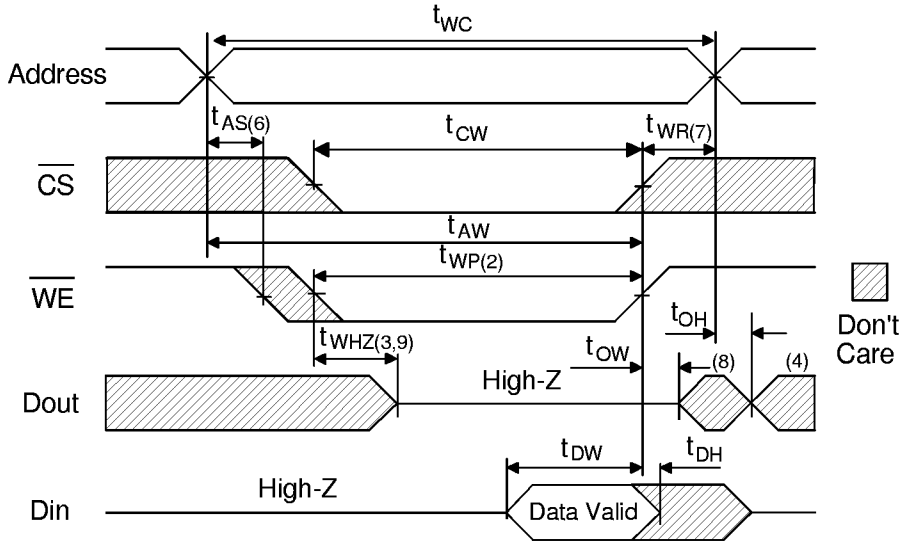
(4) At any given temperature and voltage condition, t_{CHZ} (max) is less than t_{CLZ} (min) both for a given module and from module to module.

(5) These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform (1,4)



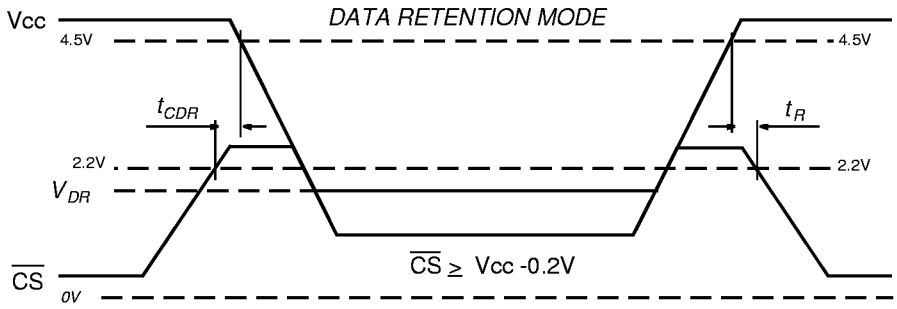
Write Cycle No.2 Timing Waveform (1,5)



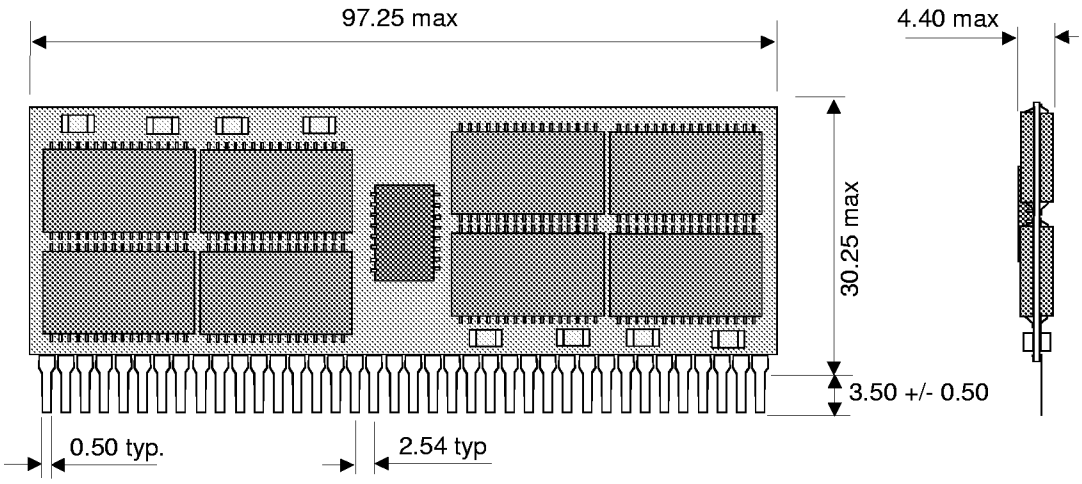
AC Write Characteristics Notes

(1) All write cycle timing is referenced from the last valid address to the first transition address.
(2) All writes occur during the overlap of $\overline{CS}$ and $\overline{WE}$ low.
(3) If $\overline{OE}$, $\overline{CS}$, and $\overline{WE}$ are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
(4) Dout is the Read data of the new address.
(5) $\overline{OE}$ is continuously low.
(6) Address is valid prior to or coincident with $\overline{CS}$ and $\overline{WE}$ low, too avoid inadvertant writes.
(7) $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
(8) When $\overline{CS}$ is low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
(9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Data Retention Waveform



Package Information Dimensions in mm



Ordering Information

SYS88000RKXLI - 70

Speed	70	=	70ns
	85	=	85ns
	10	=	100ns
	12	=	120ns
Temperature Range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
Power Consumption	Blank	=	Standard
	L	=	Low Power
Package	RKX	=	Plastic 38 pin SIP
Organization	88000	=	8M x 8
Memory Type	SYS	=	Static RAM

Note :

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantibility or fitness for a particular purpose.

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Products are not authorised for use as critical components in life support devices without the express written approval of a company director