QUALITY SEMICONDUCTOR, INC.

16-Bit Register with Asynchronous Reset

QS74FCT2X273T
QS74FCT2X2273T

FEATURES/BENEFITS

- Function compatible to the 74F273
- 74FCT273 and 74ABT273
- CMOS power levels: <7.5 mW static
- Available in 40-Pin QVSOP
- Undershoot clamp diodes on all inputs

FCT-T 2X273T

- JEDEC-FCT spec compatible
- Fastest CMOS logic family available
- t_{PD} = 5.2ns
- I_{OL} = 48 mA
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V

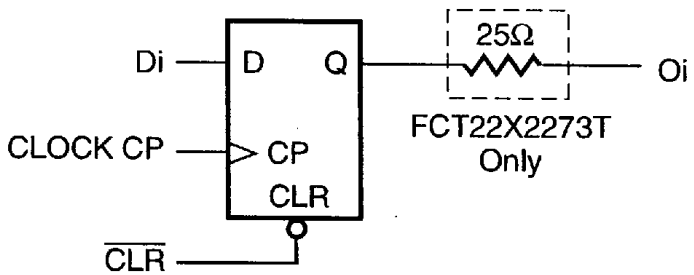
FCT-T 2X2273T Advance Information

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- t_{PD} =5.2ns
- I_{OL} = 12 mA

DESCRIPTION

The QSFCT2X273T and QSFCT2X2273T are high-speed CMOS TTL-compatible registers with an asynchronous reset input. They are 16-bit registers with a buffered common clock and a buffered output drive. The QSFCT2X2273T is a 25Ω resistor output version useful for driving transmission lines and reducing system noice. Data is stored in the register on the rising edge of the clock. The high output current I_{OL} and I_{OH} drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS
(All Pins Top View)

QVSOP

$\overline{CLR}$0	1	40	Vcc
O0	2	39	O7
D0	3	38	D7
D1	4	37	D6
O1	5	36	O6
O2	6	35	O5
D2	7	34	D5
D3	8	33	D4
O3	9	32	O4
GND	10	31	CP0
$\overline{CLR}$1	11	30	Vcc
O8	12	29	O15
D8	13	28	D15
D9	14	27	D14
O9	15	26	O14
O10	16	25	O13
D10	17	24	D13
D11	18	23	D12
O11	19	22	O12
GND	20	21	CP1

PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Oi	O	Data Outputs
CP0	I	Clock Input D/O7-D/O0
CP1	I	Clock Input D/O15-D/O8
$\overline{CLR}$0	I	Clear Input D/O7-D/O0
$\overline{CLR}$1	I	Clear Input D/O15-D/O8

FUNCTION TABLE

Inputs			Internal Q	Outputs	
$\overline{CLR}$	CP	Di	Value	Oi	Function
L	X	X	L	L	Clear Register
H	↑	L	L	L	Load Input Data
H	↑	H	H	H	Load Input Data

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20 mA
DC Output Diode Current with $V_{OUT} < 0$	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	1.2 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	Typ	Unit
Input pins	4	pF
Output pins	6	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	3.0	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Qccd	Supply Current per Input per MHz	Vcc = Max., Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Qccd is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	Vcc = Max., 0 ≤ V_{IN} < Vcc	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	Vcc = Max., 0 ≤ V_{OUT} ≤ Vcc	—	—	5	µA
I_{OS}	Short Circuit Current	Vcc = Max., V_{OUT} = GND(2,3)	–60	—	–225	mA
I_{OR}	Current Drive (FCT2X2273-25Ω)	V_{CC} = Min,. V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	Vcc = Min., I_{IN} = –18 mA(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	Vcc = Min. I_{OH} = –15 mA	2.4	—	—	V
V_{OL}	Output LOW Voltage (FCT2X273)	Vcc = Min. I_{OL} = 48 mA	—	—	0.50	V
V_{OL}	Output LOW Voltage (FCT2X2273-25Ω)	Vcc = Min. I_{OL} = 12 mA	—	—	0.50	V
R_{OUT}	Output Resistance (FCT2X2273-25Ω)	V_{CC} = Min. I_{OL} = 12 mA	20	28	40	Ω

Notes:

1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

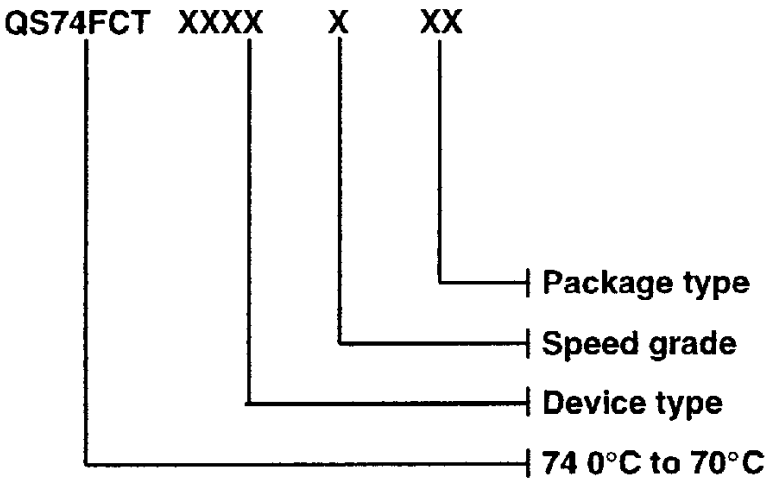
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	2X273A 2X2273A		2X273C 2X2273C		Unit
		Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay CP, $\overline{CLR}$ to Oi (273)	2	7.2	2	5.2	ns
t_{PHL} t_{PLH}	Propagation Delay CP, $\overline{CLR}$ to Oi (2273)	2	7.2	2	5.2	ns
t_S	Data Setup Time Di to CP	2	—	1.5	—	ns
t_H	Data Hold Time Time Di to CP	1.5	—	1	—	ns
t_{WCP}	Clock Pulse Width[2] HIGH or LOW	6	—	4	—	ns
t_{WCLR}	$\overline{CLR}$ Pulse Width[2] HIGH or LOW	6	—	5	—	ns
t_{REC}	$\overline{CLR}$ Recovery Time[2] $\overline{CLR}$ to CP	2	—	1.5	—	ns

Notes:
1. Minimums guaranteed but not tested for all parameters except t_S and t_H.
2. These parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

ORDERING INFORMATION



Device Type:

2X273, 2X2273

Speed Grades:

A

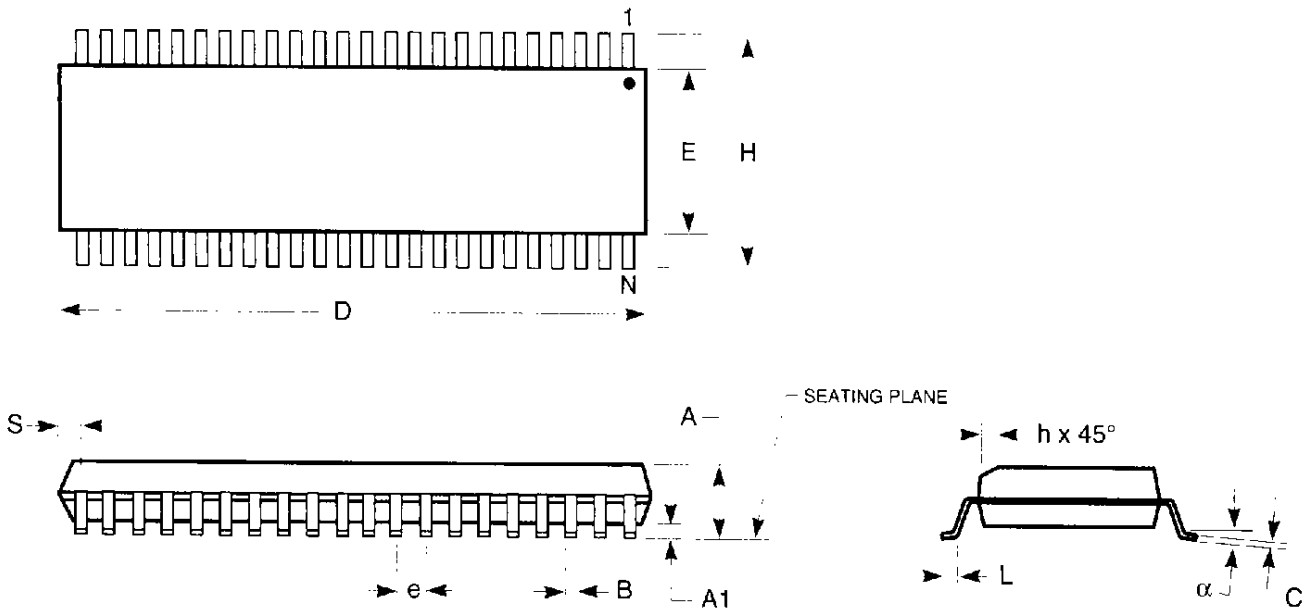
C

Package Type:

40 pin QVSOP (Q2)

150-MIL QVSOP™ - Package Code Q1/Q2

150-Mil Wide Plastic Small Outline Gull-Wing



JEDEC#	MO-154BB			MO-154AB		
DWG#	PSS-40A (Q2)			PSS-48A (Q1)		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.059	0.065	0.069	0.059	0.065	0.069
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.0067	0.008	0.009	0.0051	0.0063	0.008
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.386	0.390	0.394	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157
e	0.0197 BSC, 0.5mm			0.0157 BSC, 0.4mm		
H	0.228	0.236	0.244	0.228	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.020	0.024	0.030	0.020	0.024	0.030
N	40			48		
α	0°	5°	8°	0°	5°	8°
S	0.006	0.008	0.010	0.012	0.014	0.016

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.003 in. maximum.