PCF/PCC0330; 0450; 0700; 1100 GATE ARRAY FAMILY

GENERAL DESCRIPTION

The PCXXXXX gate array family offers the circuit designer the facility to create a semi-custom circuit with a unique set of CAD (Computer-Aided Design) tools in a well established CMOS process. The PCFXXXX gate arrays described in this data sheet are of the "standard" version (standard ambient temperature range: −40 to + 85 °C). The type numbers are PCF0330, PCF0450, PCF0700 and PCF1100.

Occasional references are made to an "extended" version, the PCCXXXX, which is characterized by a wider operating temperature range (extended ambient temperature range: −55 to + 125 °C). The type numbers are PCC0330, PCC0450, PCC0700 and PCC1100.

The basis for the design procedure is formed by a logic network description, which outlines the required logic in terms of basic functions.

A simulation control language offers the ability to verify the logic, simulate it with the actual propagation delay times and generate the test patterns.

The network and cell placement procedure is put in for the automatic routeing program, INGATE (INterconnect GATEs), which also makes the connections automatically to the bonding pad and I/O cells.

The mask pattern tape of the two final masks is generated directly by INGATE. This extensive CAD procedure, using readily available pre-processed slices, offers the designer a very fast turn-around time for the first LSI prototypes.

purple binder, tab 5

Features

- Fast development time
- A set of CAD tools enables the customer to make his own design, from logic to mask-pattern tape
- Low-power CMOS technology with wide supply voltage range, high noise-immunity and high-speed operations
- Supply voltage range 3 to 15 V
- High gate utilization of at least 90%
- HE4000B family compatible

The PCXXXXX family characteristics

		PCF0330 PCC0330	PCF0450 PCC0450	PCF0700 PCC0700	PCF1100 PCC1100
Gate equivalents (2-input)		330	448	704	1116
Cell units		165	224	352	558
Rows of cell units		11	14	16	18
Cell units per row		15	16	22	31
Horizontal mask-programmable interconnection strips					
above top row of cell units	max.	5	5	5	6
between cell units	max.	10	9	10	13
below bottom row of cell units	max.	5	5	5	6
Bonding pads	max.	40	28	40	68
Input/output stages with choice of		38	26	38	66
3-state I/O	max.	34	26	38	66
drivers	max.	38	14	22	66
buffers	max.	38	12	16	66
Schmitt-triggers	max.	34	8	10	66
Pin pull-up/pull-down resistors	max.	34	26	34	66
Chip size		13,6 mm^2	14,6 mm^2	21,9 mm^2	40,0 mm^2
Chip dimensions	x	3,52 mm	3,45 mm	4,44 mm	6,25 mm
	y	3,87 mm	4,24 mm	4,94 mm	6,40 mm
Gate delays					
at V_{DD} = 5 V	max.	16 ns	16 ns	16 ns	16 ns
	typ.	8 ns	8 ns	8 ns	8 ns
at V_{DD} = 10 V	max.	6,4 ns	6,4 ns	6,4 ns	6,4 ns
	typ.	3,2 ns	3,2 ns	3,2 ns	3,2 ns
at V_{DD} = 15 V	max.	4 ns	4 ns	4 ns	4 ns
	typ.	2 ns	2 ns	2 ns	2 ns
Maximum toggle frequency					
at V_{DD} = 5 V	min.	6 MHz	6 MHz	6 MHz	6 MHz
at V_{DD} = 10 V	min.	12 MHz	12 MHz	12 MHz	12 MHz
at V_{DD} = 15 V	min.	15 MHz	15 MHz	15 MHz	15 MHz

PACKAGE OUTLINES

The table shows the package codes for the outlines in which the gate arrays are available.

package type	no. of pins	package code			
		PCF0330 PCC0330	PCF0450 PCC0450	PCF0700 PCC0700	PCF1100 PCC1100
Plastic DIL	8	SOT-97C.2*	SOT-97C.2*	–	–
	16	SOT-38Z.2	–	–	–
	18	SOT-102F.6	SOT-102F.6	–	–
	20	–	SOT-146C.1	–	–
	22	SOT-116C.2	–	SOT-116C.2	
	24	SOT-101C.9	SOT-101E.9	SOT-101E.10	–
	28	SOT-117C.14	SOT-117C.14	SOT-117D.16*	–
	40	SOT-129C.1	–	SOT-129C.2	SOT-129C.3
Plastic SO	16	–	SOT-162AC.4	–	–
	20	–	SOT-163AC.4	–	–
	24	–	SOT-137AC.1	–	–
	28	–	SOT-136AC.4	SOT-136AC.5	–
Plastic VSO	40	–	–	SOT-158A.3*	–
Leaded chip carrier	68*	–	–	–	–
Ceramic (cerdip)	14	SOT-73C*	SOT-73C*	–	–
	16	SOT-74C	SOT-74C	–	–
	18	–	SOT-133B	–	–
	20	SOT-152B	SOT-152B	–	–
	22	SOT-134A.1	SOT-134A.1	SOT-134A.1	–
	24	SOT-94A	SOT-94A	SOT-94A	–
	28	SOT-135A	SOT-135A	SOT-135A	–
	40	SOT-145A.3	–	SOT-145A.7	SOT-145A.4
Metal-ceramic (cerdil)	8	SOT-153B.0*	SOT-153B.0*	–	–
	14	SOT-83B.0	SOT-83B.0	–	–
	16	SOT-84B.0	SOT-84B.4	–	–
	18	SOT-85B.0	SOT-85B.0	SOT-85B.0	–
	20	SOT-154B.0	SOT-154B.0	–	–
	22	SOT-118B.0	SOT-118B.0	SOT-118B.0	–
	24	SOT-86A.0	SOT-86A.0	SOT-86A.4	–
	28	SOT-87A.0	SOT-87A.0	SOT-87A.4	SOT-87B.6*
	40	SOT-88A.4	–	SOT-88A.4	SOT-88B.5
Plug-in	64*	–	–	–	–
Leadless chip carrier	28*	–	–	–	–
	44*	–	–	–	–
	68*	–	–	–	–

* Not yet available.

A.C. and dynamic features

V_{SS} = 0 V; T_{amb} = 25 °C

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Maximum toggle frequency flip-flop GT00	5	f_{max}	6	12	–	MHz
	10	f_{max}	12	24	–	MHz
	15	f_{max}	15	30	–	MHz
Propagation delays 2-input gate; fan-out = 2	5	t_{PHL} = t_{PLH}	–	8	16	ns
	10		–	3,2	6,4	ns
	15		–	2	4	ns

The maximum system frequency depends on the number of gates in sequence. The average minimum frequencies are 3 MHz at V_{DD} = 5 V, 6 MHz at V_{DD} = 10 V and 9 MHz at V_{DD} = 15 V.

FAMILY SPECIFICATIONS

These specifications cover the common electrical characteristics of the entire PCXXXXX family, unless otherwise specified in the individual device data sheet. The CMOS PCXXXXX family devices will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} of 5, 10 and 15 V. Because of the wide operating voltage range, power supply regulation is less critical than with other types of logic. The lower limit of the supply voltage is 3 V, or as determined by the required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 12,5 V or 15 V or as determined by power dissipation constraints or interface to other logic. Inputs and outputs are protected against electrostatic effects in a wide variety of device handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

SUPPLY VOLTAGE

	rating	operating voltage
PCXXXXXB	–0,5 to 18	3 to 15,0 V
PCXXXXXV	–0,5 to 18	3 to 12,5 V

The family specifications are given in the following sections: RATINGS, D.C. CHARACTERISTICS and A.C. CHARACTERISTICS.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to + 18	V
Voltage on any input			
when pin pull up/down resistors are:			
used	V_I	−0,5 to V_{DD} + 0,5	V
not used	V_I	−0,5 to + 18	V
D.C. current into any input or output	± I	max. 10	mA
Power dissipation per output	P	max. 100	mW
Power dissipation per package			
for standard temperature range: −40 to + 85 °C (PCFXXXX)			
plastic and ceramic DIL			
for T_{amb} = −40 to + 60 °C	P_{tot}	max. 400	mW
for T_{amb} = +60 to + 85 °C	P_{tot}	derate linearly with 8 mW/K to 200 mW	
plastic mini-pack (SO)			
for T_{amb} = −40 to + 70 °C	P_{tot}	max. 200	mW
for T_{amb} = +70 to + 85 °C	P_{tot}	derate linearly with 5 mW/K to 125 mW	
for extended temperature range: −55 to + 125 °C (PCCXXXX)			
ceramic DIL			
for T_{amb} = −55 to + 100 °C	P_{tot}	max. 400	mW
for T_{amb} = +100 to + 125 °C	P_{tot}	derate linearly with 8 mW/K to 200 mW	
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range			
standard (PCFXXXX)	T_{amb}	−40 to + 85	°C
extended (PCCXXXX)	T_{amb}	−55 to + 125	°C

DEVELOPMENT SAMPLE DATA

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the V-version, because of its reduced supply voltage range (viz 3 to 12,5 V).

D.C. CHARACTERISTICS

V_{SS} = 0 V; for all devices unless otherwise specified

parameter	T_{amb}	V_{DD} V	symbol	T_{amb} (°C)* low min.	low max.	+25 min.	+25 max.	high min.	high max.	unit	conditions
Quiescent device current	stand.	5	I_{DD}	–	50	–	50	–	375	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
		10	I_{DD}	–	100	–	100	–	750	μA	
		15	I_{DD}	–	200	–	200	–	1500	μA	
Quiescent device current	ext.	5	I_{DD}	–	15	–	15	–	375	μA	
		10	I_{DD}	–	25	–	25	–	750	μA	
		15	I_{DD}	–	50	–	50	–	1500	μA	
Output voltage LOW	all	5	V_{OL}	–	0,05	–	0,05	–	0,05	V	$V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA
		10	V_{OL}	–	0,05	–	0,05	–	0,05	V	
		15	V_{OL}	–	0,05	–	0,05	–	0,05	V	
Output voltage HIGH	all	5	V_{OH}	4,95	–	4,95	–	4,95	–	V	
		10	V_{OH}	9,95	–	9,95	–	9,95	–	V	
		15	V_{OH}	14,95	–	14,95	–	14,95	–	V	
Input voltage LOW: INPI, INPB	all	5	V_{IL}	–	1,5	–	1,5	–	1,5	V	V_O = 0,5 V or 4,5 V; V_O = 1,0 V or 9,0 V; V_O = 1,5 V or 13,5 V; $\|I_O\| < 1$ μA
		10	V_{IL}	–	3,0	–	3,0	–	3,0	V	
		15	V_{IL}	–	4,0	–	4,0	–	4,0	V	
Input voltage HIGH: INPI, INPB	all	5	V_{IH}	3,5	–	3,5	–	3,5	–	V	
		10	V_{IH}	7,0	–	7,0	–	7,0	–	V	
		15	V_{IH}	11,0	–	11,0	–	11,0	–	V	
Input voltage LOW: INPD, INPA, INPS	all	5	V_{IL}	–	1,0	–	1,0	–	1,0	V	V_O = 0,5 V or 4,5 V; V_O = 1,0 V or 9,0 V; V_O = 1,5 V or 13,5 V; $\|I_O\| < 1$ μA
		10	V_{IL}	–	2,0	–	2,0	–	2,0	V	
		15	V_{IL}	–	2,5	–	2,5	–	2,5	V	
Input voltage HIGH: INPD, INPA, INPS	all	5	V_{IH}	4,0	–	4,0	–	4,0	–	V	
		10	V_{IH}	8,0	–	8,0	–	8,0	–	V	
		15	V_{IH}	12,5	–	12,5	–	12,5	–	V	

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS (continued)

parameter	T_{amb}	V_{DD} V	symbol	T_{amb} (°C)* low min.	low max.	+25 min.	+25 max.	high min.	high max.	unit	conditions
Output (sink) current LOW driver outputs	stand.	5	I_{OL}	1,1	—	0,9	—	0,7	—	mA	V_O = 0,4 V; V_I = 0 or 5 V
		10	I_{OL}	4,0	—	3,3	—	2,6	—	mA	V_O = 0,5 V; V_I = 0 or 10 V
		15	I_{OL}	12,0	—	10,0	—	8,0	—	mA	V_O = 1,5 V; V_I = 0 or 15 V
Output (sink) current LOW driver outputs	ext.	5	I_{OL}	1,2	—	0,9	—	0,6	—	mA	
		10	I_{OL}	4,2	—	3,3	—	2,2	—	mA	
		15	I_{OL}	13,0	—	10,0	—	6,7	—	mA	
Output (sink) current LOW buffer outputs	stand.	5	I_{OL}	2,2	—	1,8	—	1,4	—	mA	
		10	I_{OL}	8,0	—	6,6	—	5,6	—	mA	
		15	I_{OL}	24,0	—	20,0	—	16,0	—	mA	
Output (sink) current LOW buffer outputs	ext.	5	I_{OL}	2,4	—	1,8	—	1,2	—	mA	
		10	I_{OL}	8,4	—	6,6	—	4,4	—	mA	
		15	I_{OL}	26,0	—	20,0	—	13,4	—	mA	
Output (source) current HIGH	stand.	5	$-I_{OH}$	1,1	—	0,9	—	0,7	—	mA	V_O = 4,6 V; V_I = 0 or 5 V
		10	$-I_{OH}$	3,1	—	2,6	—	2,0	—	mA	V_O = 9,5 V; V_I = 0 or 10 V
		15	$-I_{OH}$	12,0	—	10,0	—	8,0	—	mA	V_O = 13,5 V; V_I = 0 or 15 V
Output (source) current HIGH	ext.	5	$-I_{OH}$	1,2	—	0,9	—	0,6	—	mA	
		10	$-I_{OH}$	3,5	—	2,6	—	1,7	—	mA	
		15	$-I_{OH}$	13,0	—	10,0	—	6,7	—	mA	

* T_{amb} low: −40 °C for standard temperature range
−55 °C for extended temperature range
T_{amb} high: +85 °C for standard temperature range
+125 °C for extended temperature range

D.C. CHARACTERISTICS (continued)

V_{SS} = 0 V; for all devices unless otherwise specified

parameter	T_{amb}	V_{DD}	symbol	T_{amb} (°C)*						unit	conditions
				low		+ 25		high			
		V		min.	max.	min.	max.	min.	max.		
Input leakage current	stand.	10	$\pm I_{IN}$	—	0,3	—	0,3	—	1,0	μA	V_I = 0 or 10 V
		15	$\pm I_{IN}$	—	0,3	—	0,3	—	1,0	μA	V_I = 0 or 15 V
Input leakage current	ext.	10	$\pm I_{IN}$	—	0,1	—	0,1	—	1,0	μA	
		15	$\pm I_{IN}$	—	0,1	—	0,1	—	1,0	μA	
3-state output and open N-channel output leakage current HIGH	stand.	10	I_{OZH}	—	1,6	—	1,6	—	12,0	μA	output returned to V_{DD}
		15	I_{OZH}	—	1,6	—	1,6	—	12,0	μA	output returned to V_{DD}
3-state output and open N-channel output leakage current HIGH	ext.	10	I_{OZH}	—	0,4	—	0,4	—	5,0	μA	output returned to V_{DD}
		15	I_{OZH}	—	0,4	—	0,4	—	5,0	μA	output returned to V_{DD}
3-state output and open P-channel output leakage current LOW	stand.	10	$-I_{OZL}$	—	1,6	—	1,6	—	12,0	μA	output returned to V_{SS}
		15	$-I_{OZL}$	—	1,6	—	1,6	—	12,0	μA	output returned to V_{SS}
3-state output and open P-channel output leakage current LOW	ext.	10	$-I_{OZL}$	—	0,4	—	0,4	—	5,0	μA	output returned to V_{SS}
		15	$-I_{OZL}$	—	0,4	—	0,4	—	5,0	μA	output returned to V_{SS}

D.C. CHARACTERISTICS (continued)

parameter	T_{amb}	V_{DD} V	symbol	T_{amb} (°C)*						unit	conditions
				low		+ 25		high			
				min.	max.	min.	max.	min.	max.		
Hysteresis voltage input INPS		5	V_H	–	–	0,2 typ.		–	–	V	
		10	V_H	–	–	0,6 typ.		–	–	V	
		15	V_H	–	–	0,8 typ.		–	–	V	

* T_{amb} low: −40 °C for standard temperature range
−55 °C for extended temperature range
T_{amb} high: +85 °C for standard temperature range
+125 °C for extended temperature range

Notes

1. Pull up/down resistors (pin) typical 7 to 78 kΩ; see also section "PERIPHERY".
2. I_{DD} current limits have to be adapted when pull-up/pull-down resistors are used.
3. If a rather low value pull-up/pull-down resistor is used in combination with open N-channel or P-channel output stages the following has to be taken into account (see also table).

   For functional tests, only a voltage drop across the output transistor is required, which is lower than 1/8 of the supply voltage.

   The V_{OL} and V_{OH} levels can be calculated by using the specified I_{OL} and I_{OH} currents relative to the current supplied by the pull-up/pull-down resistor (the spread of the resistor-value is a factor 2).

   Table: minimum applicable pull-up/pull-down resistor versus supply voltage.

V_{DD} (V)	minimum pull-up resistor		minimum pull-down resistor
	open N-channel driver output	open N-channel buffer output	open P-channel output
3	33 kΩ	17 kΩ	33 kΩ
4	12 kΩ	7 kΩ	12 kΩ
5 to 15	7 kΩ	7 kΩ	7 kΩ

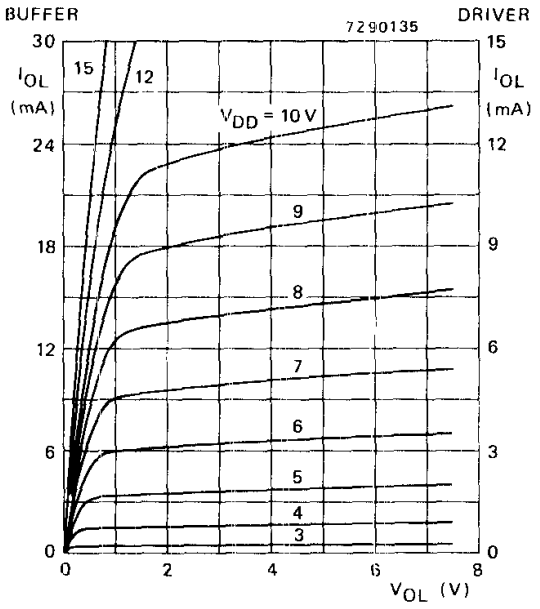


Fig. 5 Minimum output current LOW as a function of the output voltage LOW; buffer and driver outputs.

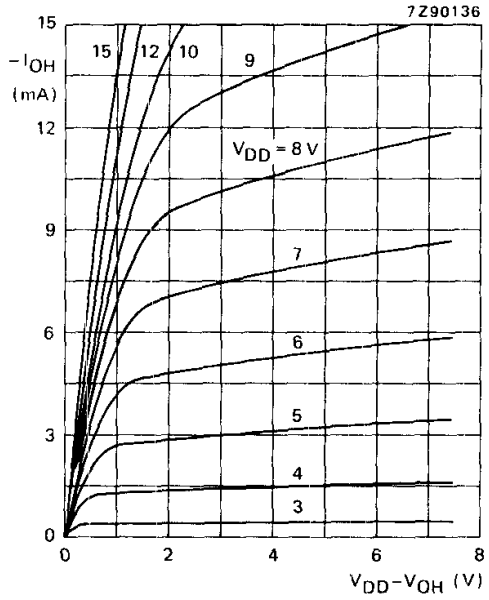


Fig. 6 Minimum output current HIGH as a function of the supply voltage minus the output voltage HIGH.

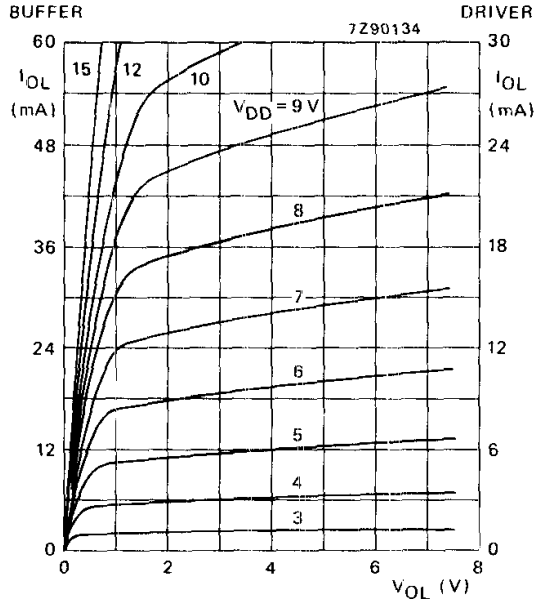


Fig. 7 Typical output current LOW as a function of the output voltage LOW; buffer and driver outputs.

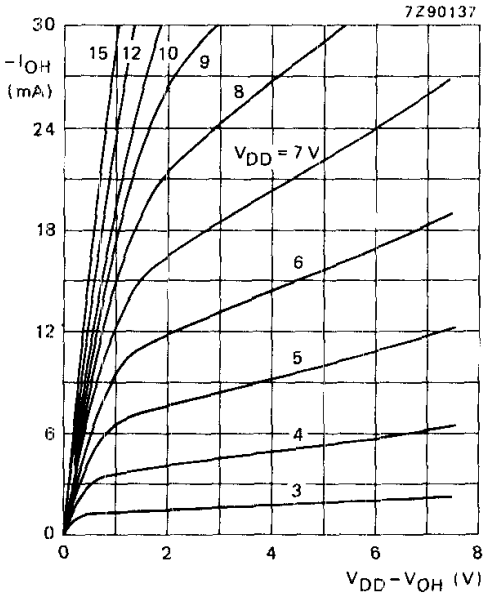


Fig. 8 Typical output current HIGH as a function of the supply voltage minus the output voltage HIGH.

A.C. CHARACTERISTICS

Clock input rise and fall times (t_r, t_f)

The upper limits on t_r and t_f vary widely from device to device and with supply voltage. Unless otherwise specified in the individual data sheets, it is recommended that input rise and fall times be less than 15 μs for V_{DD} = 5 V; 4 μs for V_{DD} = 10 V; 1 μs for V_{DD} = 15 V. However, when the Schmitt-trigger input INPS is used, the device is highly tolerant to slow clock rise and fall times.

Output transition times

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns; C_L = 50 pF

parameter	V_{DD} V	symbol	min.	typ.	max.	unit
Output transition times	5	t_{THL}	–	60	120	ns
driver outputs	10	t_{THL}	–	30	60	ns
HIGH to LOW	15	t_{THL}	–	20	40	ns
Output transition times	5	t_{THL}	–	30	60	ns
buffer outputs	10	t_{THL}	–	15	30	ns
HIGH to LOW	15	t_{THL}	–	10	20	ns
Output transition times	5	t_{TLH}	–	40	80	ns
buffer outputs	10	t_{TLH}	–	18	36	ns
LOW to HIGH	15	t_{TLH}	–	12	24	ns

Temperature coefficient (typical values)

Propagation delays	+ 0,35 %/K
Output transition times	+ 0,35 %/K

Input capacitance

Maximum input capacitance

for plastic and metal-ceramic (cerdil) DIL up to 40 pins	C_I = 7,5 pF
for ceramic (cerdip) DIL up to 28 pins	C_I = 10 pF
for ceramic (cerdip) DIL 40 pins	C_I = 18 pF

DEVELOPMENT SAMPLE DATA

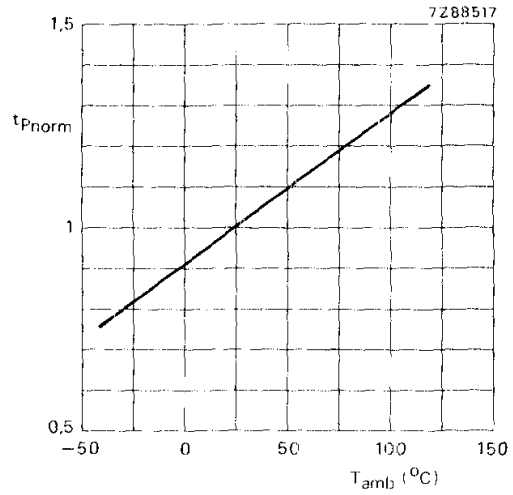


Fig. 1 Normalized propagation delay (t_{Pnorm}) as a function of the ambient temperature.

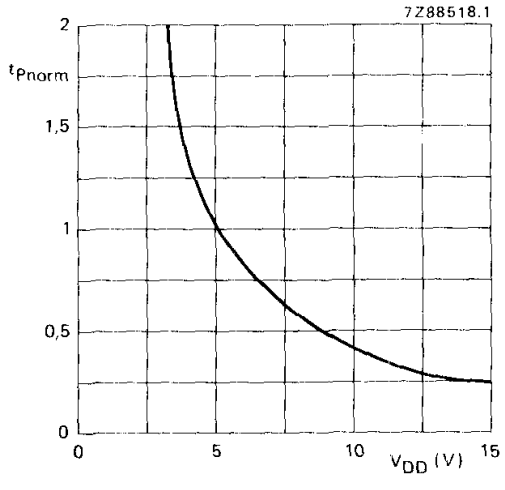


Fig. 2 Normalized propagation delay (t_{Pnorm}) as a function of the supply voltage.

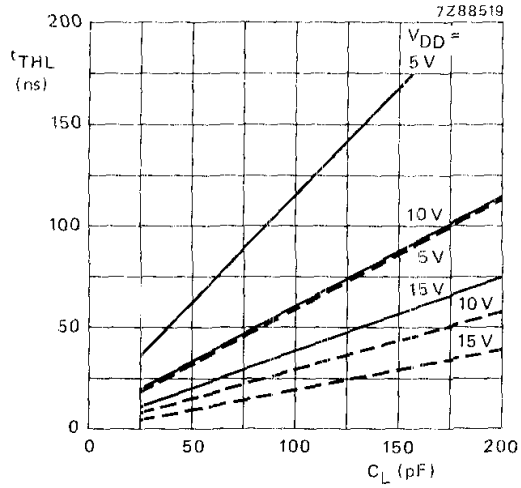


Fig. 3 Output transition time (HIGH-to-LOW) as a function of the load capacitance.

——— driver output
– – – buffer output

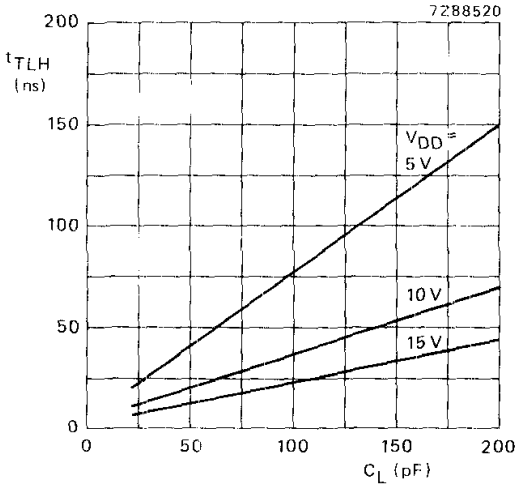


Fig. 4 Output transition time (LOW-to-HIGH) as a function of the load capacitance for driver and buffer outputs.

PHYSICAL STRUCTURE OF THE GATE ARRAY

The basic layout of the PCXXXXX chip is shown in Fig. 9.

The active area of the chip consists of identical units, located in rows. A standard interconnection area is situated between the rows with pre-defined vertical poly-silicon lines and a height that allows for ten completely independent horizontal metal strips. Figure 10 shows some units and their interconnections.

The elements for the I/O cells are located in the border region of the chip between the bonding pads.

The contact and the metal masks for the I/O cells are automatically generated when a pad is assigned to a particular I/O function. Placement of a cell from the cell library on a row, automatically generates the last two masks belonging to that cell, which transforms the standard unit into the required logic cell called from the library.

Finally, the INGATE program generates the contact and metal masks, which interconnect the logic cells, without error, conform to the network description that outlined the logic.

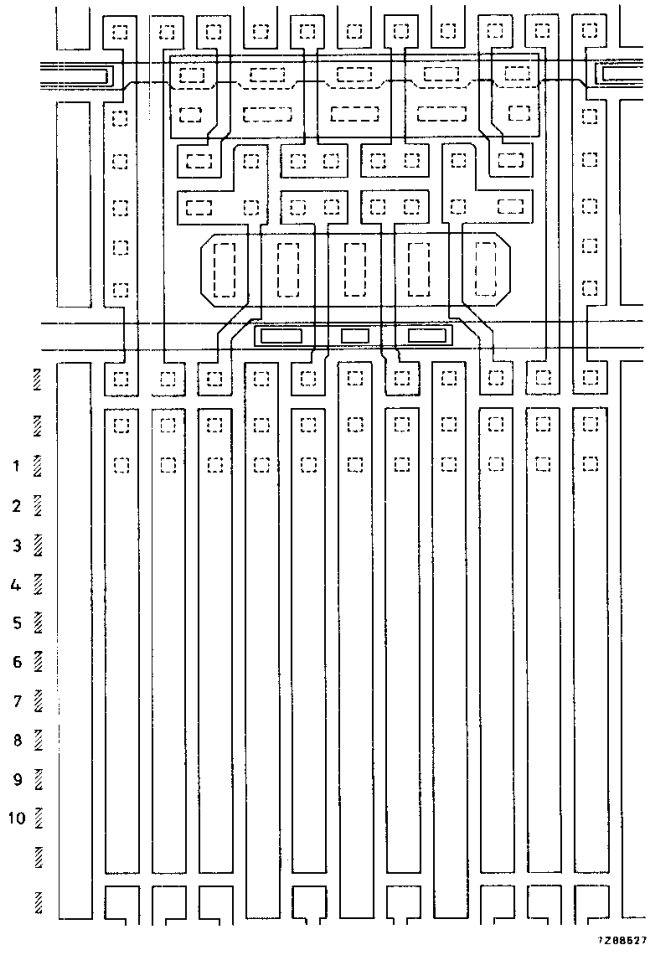
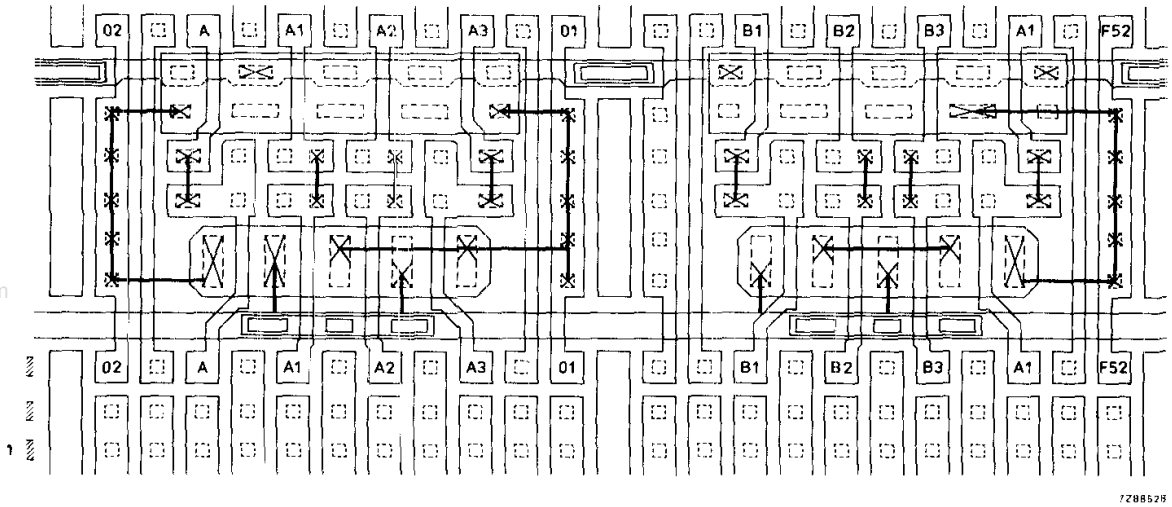
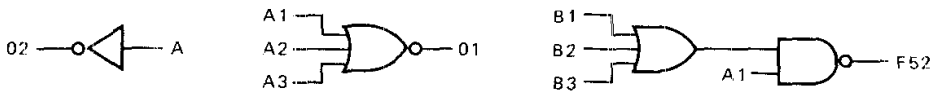


Fig. 9 Basic chip layout of unit with interconnect area.





inverter NOR complex function; $\overline{A1 \cdot (B1 + B2 + B3)}$ 7Z88526

Fig. 10 Some examples of library cells.

CELL LIBRARY

To simplify the design procedure, a library of approximately sixty pre-designed, fully-characterized cells is available as part of the CAD facilities.

The library logic elements, function and number of the equivalent gate count are shown in Tables 1 and 2.

It is a special feature of the PCXXXXX cell unit that the N and P-channel gates are not pre-connected, which makes it possible to give them different potentials. In this way, transmission gates can be made, which is a very attractive facility in CMOS circuit design. Compared with the normal gate flip-flops, transmission gate flip-flops are not only faster, but use only 50% of the physical area (GT00).

DEVELOPMENT SAMPLE DATA

Table 1 Array cell library

library identification code	logic element	function	number of units	number of equiv. gates	remarks
inverters/buffers					
GIN1	inverter	$\overline{A}$	1/4	1/2	max. 2 in one unit
GIN2	array driver inverting	$\overline{A}$	1/2	1	2 times size GIN1
GIN3	array driver inverting	$\overline{A}$	3/4	1 + 1/2	3 times size GIN1
GIN4	array driver inverting	$\overline{A}$	1	2	4 times size GIN1
GIN6	array driver inverting	$\overline{A}$	1 + 1/2	3	6 times size GIN1
GIN8	array driver inverting	$\overline{A}$	2	4	8 times size GIN1
GIN12	array driver inverting	$\overline{A}$	3	6	12 times size GIN1
GB12	array buffer non-inverting	A	1	2	2 times size GIN1
GB13	array buffer non-inverting	A	1	2	3 times size GIN1
NAND/AND gates					
GNAND2	2-input NAND	$\overline{A1 \circ A2}$	1/2	1	
GNAND3	3-input NAND	$\overline{A1 \circ A2 \cdot A3}$	3/4	1 + 1/2	
GNAND4	4-input NAND	$\overline{A1 \cdot A2 \cdot A3 \cdot A4}$	1	2	
GAND2	2-input AND	$A1 \cdot A2$	1	2	output GIN2
GAND3	3-input AND	$A1 \circ A2 \cdot A3$	1	2	
OR/NOR gates					
GNOR2	2-input NOR	$\overline{A1 + A2}$	1/2	1	
GNOR3	3-input NOR	$\overline{A1 + A2 + A3}$	3/4	1 + 1/2	
GNOR4	4-input NOR	$\overline{A1 + A2 + A3 + A4}$	1	2	
GOR2	2-input OR	$A1 + A2$	1	2	output GIN2
GOR3	3-input OR	$A1 + A2 + A3$	1	2	
complex logic functions					
GF01	complex function	$\overline{A1 + B1 \cdot B2}$	1	2	
GF02		$\overline{A1 + B1 \cdot B1 \cdot B3}$	1	2	
GF03		$\overline{A1 \circ A2 + B1 \cdot B2}$	1	2	
GF06		$\overline{A1 + A2 + B1 \cdot B2}$	1	2	
GF15		$\overline{A1 + B1 \circ (C1 + C2)}$	1	2	
GF51		$\overline{A1 \cdot (B1 + B2)}$	1	2	
GF52		$\overline{A1 \cdot (B1 + B2 + B3)}$	1	2	
GF53		$\overline{(A1 + A2) \cdot (B1 + B2)}$	1	2	
GF56		$\overline{A1 \circ A2 \cdot (B1 + B2)}$	1	2	
GF65		$\overline{A1 \cdot (B1 + C1 \cdot C2)}$	1	2	
GXOR1	EXCLUSIVE-OR	$\overline{A \cdot B + \overline{A} \cdot \overline{B}}$	1	2	unbuffered
GXNOR1	EXCLUSIVE-NOR	$\overline{A \cdot B + \overline{A} \cdot \overline{B}}$	1	2	unbuffered
GXOR2	EXCLUSIVE-OR	$A \cdot B + \overline{A} \cdot \overline{B}$	1	2	buffered
GXNOR2	EXCLUSIVE-NOR	$\overline{A \cdot B + \overline{A} \cdot \overline{B}}$	1	2	buffered
GXOR3	EXCLUSIVE-OR	$A \cdot B + \overline{A} \cdot \overline{B}$	2	4	

Table 1 Array cell library (continued)

library identification code	logic element	function	number of units	number of equiv. gates	remarks
transmission gate latches					
GTL0	strobed D-LATCH without SET and RESET		1	2	
GTLRP	strobed D-LATCH with RESET		1 + 1/2	3	pos. triggered
GTLRN	strobed D-LATCH with RESET		1 + 1/2	3	neg. triggered
GTLSP	strobed D-LATCH with SET		1 + 1/2	3	pos. triggered
GTLSN	strobed D-LATCH with SET		1 + 1/2	3	neg. triggered
GTL2	strobed D-LATCH with SET and RESET		1 + 1/2	3	
compound latches					
GGM0	MASTER module without SET and RESET		2	4	
GGMR	MASTER module with RESET		2	4	all positive
GGMS	MASTER module with SET		2	4	triggered
GGM2	MASTER module with SET and RESET		2	4	
GGS0	SLAVE module without SET and RESET		2	4	
GGSR	SLAVE module with RESET		2	4	all negative
GGSS	SLAVE module with SET		2	4	triggered
GGS2	SLAVE module with SET and RESET		2	4	
transmission gate master-slave flip-flop (MS-D-FF)					
GT00	MS-D-FF without SET and RESET		2	4	
GTROP	MS-D-FF with RESET on MASTER		2 + 1/2	5	pos. triggered
GTRON	MS-D-FF with RESET on MASTER		2 + 1/2	5	neg. triggered
GTRRP	MS-D-FF with RESET on MASTER and SLAVE		3	6	pos. triggered
GTRRN	MS-D-FF with RESET on MASTER and SLAVE		3	6	neg. triggered
GTSSP	MS-D-FF with SET on MASTER and SLAVE		3	6	pos. triggered
GTSSN	MS-D-FF with SET on MASTER and SLAVE		3	6	neg. triggered
GT22	MS-D-FF with SET and RESET on MASTER and SLAVE		3	6	
compound master-slave flip-flops					
GG00	MS-RS-FF without SET and RESET		4	8	
GGRO	MS-RS-FF with RESET on MASTER		4	8	all negative
GGRR	MS-RS-FF with RESET on MASTER and SLAVE		4	8	triggered

COMPUTER-AIDED DESIGN FACILITIES

The comprehensive CAD facilities for CMOS custom design, in use since the early 1970s, have been tailored to form an integrated design system for semi-custom gate arrays. This re-styled design consists of CAD tools for:

- logic simulation
- automatic wiring
- mask-making
- test-pattern verification
- testing

The flow-chart through this integrated design system is shown in Fig. 11 and the facilities are such to enable GUARANTEE THAT THE CUSTOMIZED MASK CONTAINS THE LOGIC GIVEN IN THE NETWORK DESCRIPTION.

This logic simulation of the customer's prescribed network ensures that there is no bread-boarding, hand layout (digitizing), etc., which results in time-saving and obviates the need to learn tedious layout rules.

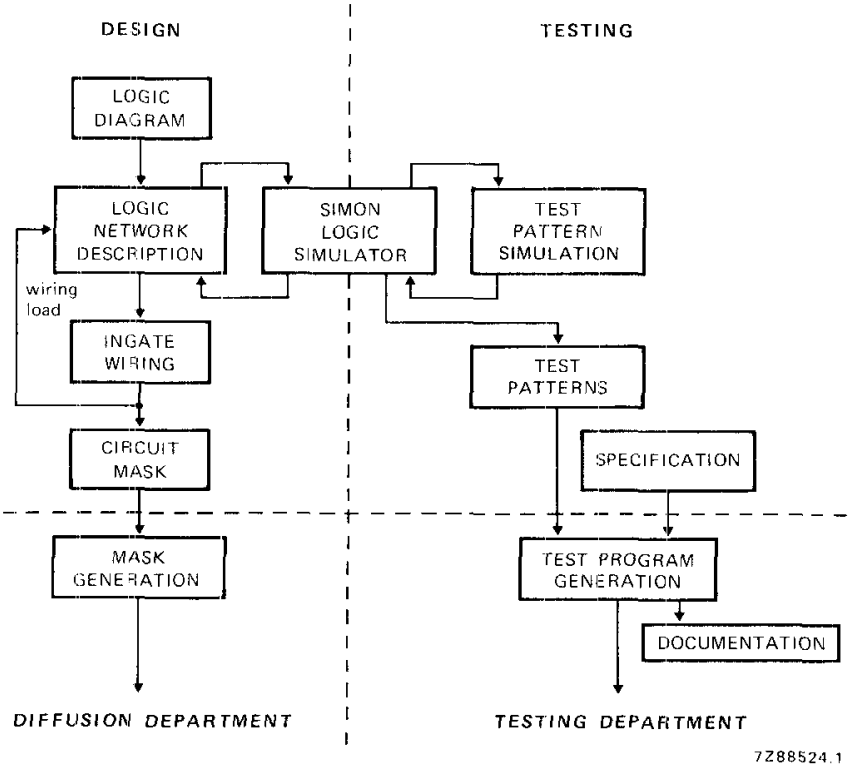


Fig. 11 CAD flow-chart.

Designing a Gate Array Chip

The design of a gate array chip can be subdivided into several steps, which logically succeed each other, but can sometimes be performed in parallel.

Logic network description

This transfers the user specification into a logic network description, using the gate array cells from the cell library.

The cell library contains several logic functions, ranging from simple logic gates (AND, NAND, etc.) to more complex flip-flop functions. For each cell, the logic function and timing are known. A macro-facility is available for user convenience.

SIMON — Logic simulation

This step checks the logical behaviour of the described network against the user specification. The well-proven logic simulator, SIMON, is used to simulate the response of the network on the user-supplied input stimuli. SIMON is an event-driven logic simulator with variable gate delay and uses five logic values (HIGH, LOW, UNKNOWN, etc.).

If the response of the simulated network does not comply with the user specification, the network has to be corrected and simulated again.

INGATE, cell placement and routeing

The INGATE step takes care of cell placement and automatic routeing in accordance with the logic network description. The gate array cells used in the network have to be placed on the chip area in rows. The special construction of the cells results in very efficient use of the available chip area. The INGATE program calculates the wiring for the entire chip using only two mask steps (contacts and aluminium). User interaction is possible and useful for extremely dense circuits.

When large signal tracks occur on a chip, the capacitance of these can increase the fan-out driven by a gate output. This extra fan-out is computed in the INGATE program and can be fed back for use in the SIMON program to calculate the extra delay values that are necessary.

Mask-making

The INGATE program interfaces directly with the CIRCUIT MASK program, which produces the control tapes for the mask generators for the two masks.

Testing

The logic simulator enables the fault coverage and efficiency of the user-supplied test sequences to be determined. The program interfaces with a test generation program that adds the d.c. parametric test and generates the control tapes to enable testing on any of the equipment used in the CAD program.

This equipment includes the following:

- Sentry VII/SSIO
- Macrodata
- Philips LOCMOS testers 1650TG
- Tektronix S3260 series

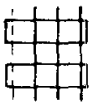
Table 2 Cell functions

Inverters/buffers

GIN1	INVERTER	A1 — F	$F=\overline{A1}$
GIN2	ARRAY DRIVER	A1 — F	$F=\overline{A1}$
GIN3	ARRAY DRIVER	A1 — F	$F=\overline{A1}$
GIN4	ARRAY DRIVER	A1 — F	$F=\overline{A1}$
GB12	NON-INVERTING BUFFER	A1 — F	F=A1
GB13	NON-INVERTING BUFFER	A1 — F	F=A1

Table 2 Cell functions (continued)

AND/NAND gates

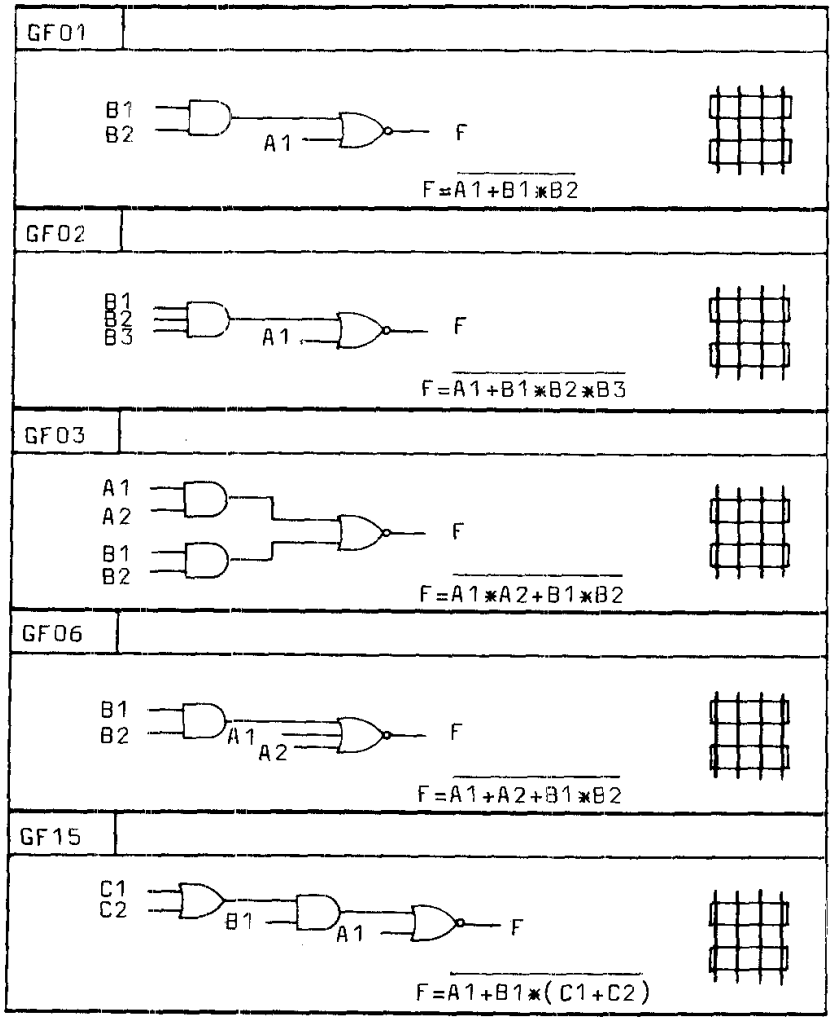
GNAND2	2-INPUT NAND		
	A1 A2 — F	$F=\overline{A1*A2}$	
GNAND3	3-INPUT NAND		
	A1 A2 A3 — F	$F=\overline{A1*A2*A3}$	
GNAND4	4-INPUT NAND		
	A1 A2 A3 A4 — F	$F=\overline{A1*A2*A3*A4}$	
GAND2	2-INPUT AND		
	A1 A2 — F	$F=A1*A2$	
GAND3	3-INPUT AND		
	A1 A2 A3 — F	$F=A1*A2*A3$	

OR/NOR gates

GNOR2	2-INPUT NOR		
	A1, A2	F	$F=\overline{A1+A2}$
GNOR3	3-INPUT NOR		
	A1, A2, A3	F	$F=\overline{A1+A2+A3}$
GNOR4	4-INPUT NOR		
	A1, A2, A3, A4	F	$F=\overline{A1+A2+A3+A4}$
GOR2	2-INPUT OR		
	A1, A2	F	$F=A1+A2$
GOR3	3-INPUT OR		
	A1, A2, A3	F	$F=A1+A2+A3$

Table 2 Cell functions (continued)

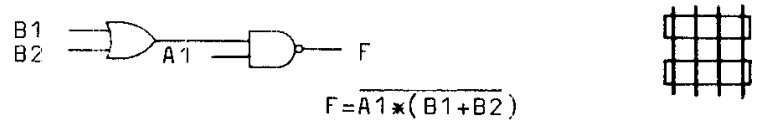
Complex logic



Complex logic (continued)

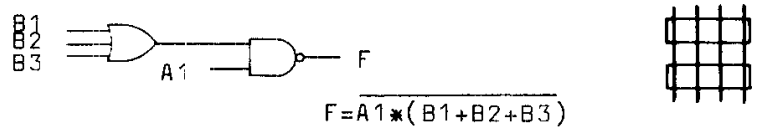
DEVELOPMENT SAMPLE DATA

GF51



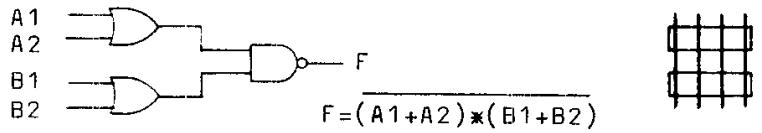
$F=\overline{A1*(B1+B2)}$

GF52



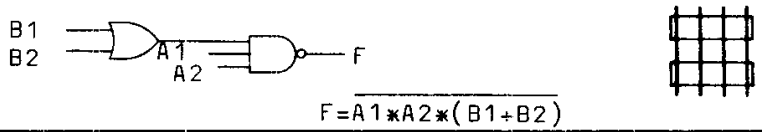
$F=\overline{A1*(B1+B2+B3)}$

GF53



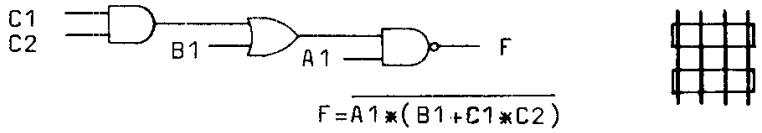
$F=\overline{(A1+A2)*(B1+B2)}$

GF56



$F=\overline{A1*A2*(B1+B2)}$

GF65

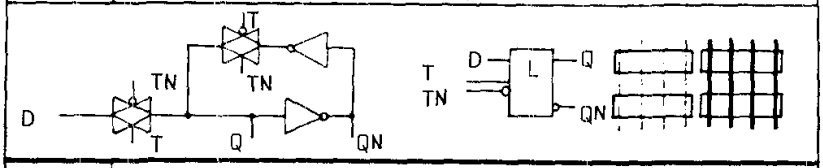


$F=\overline{A1*(B1+C1*C2)}$

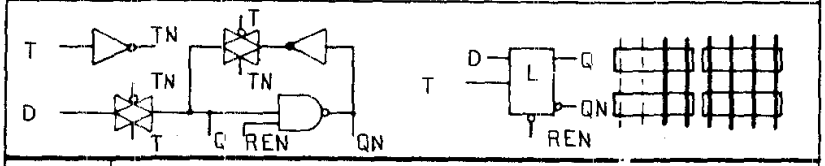
Table 2 Cell functions (continued)

Transmission gate latches

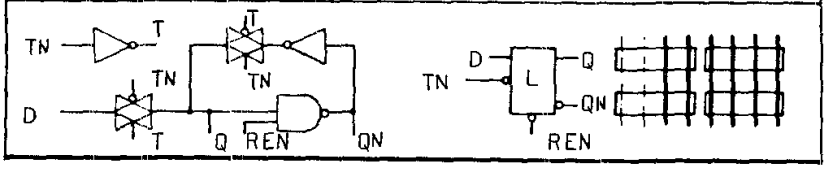
GTLD	STROBED D-LATCH WITHOUT SET AND RESET



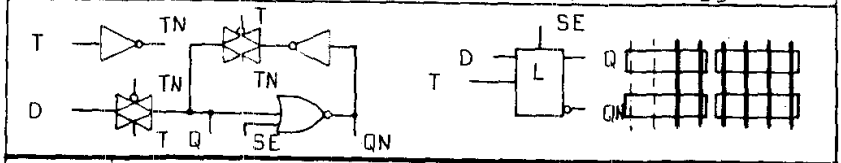
GTLRP	STROBED D-LATCH WITH RESET pos. triggered



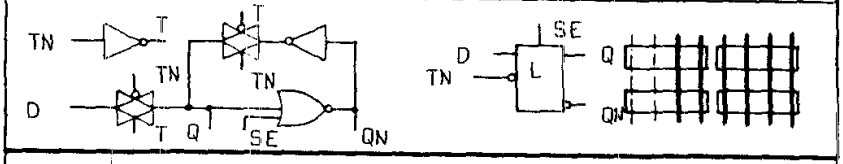
GTLRN	STROBED D-LATCH WITH RESET neg. triggered



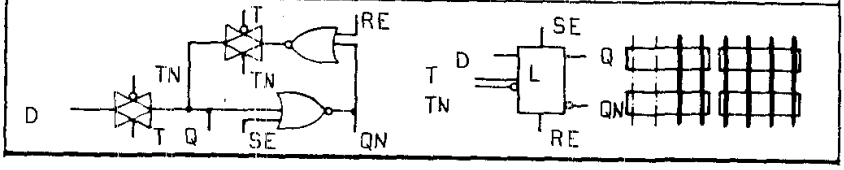
GTLSP	STROBED D-LATCH WITH SET pos. triggered



GTLSN	STROBED D-LATCH WITH SET neg. triggered

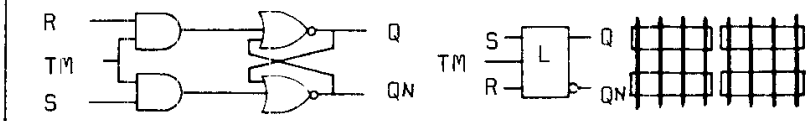


GTL2	STROBED D-LATCH WITH SET AND RESET

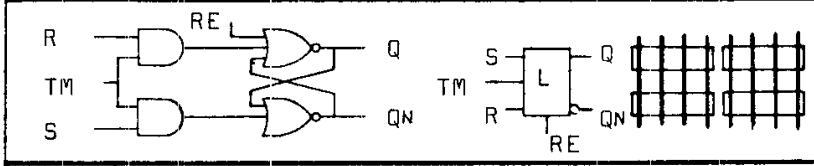


Compound latches

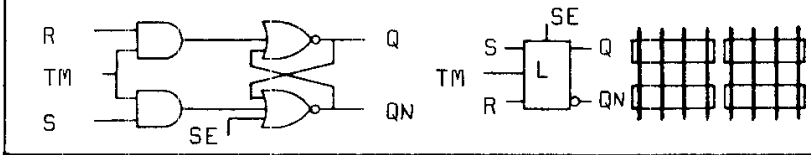
GGMO	MASTER MODULE WITHOUT SET AND RESET



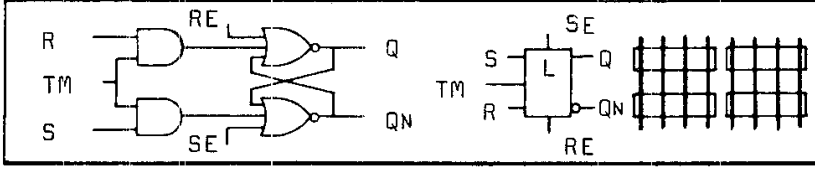
GGMR	MASTER MODULE WITH RESET



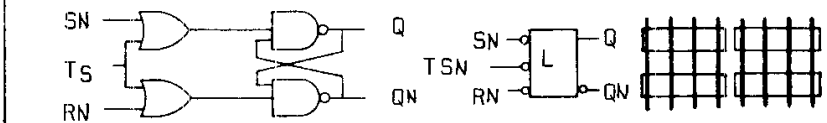
GGMS	MASTER MODULE WITH SET



GGM2	MASTER MODULE WITH SET AND RESET



GGSO	SLAVE MODULE WITHOUT SET AND RESET



GGSR	SLAVE MODULE WITH RESET

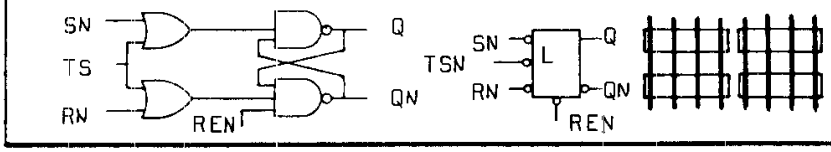
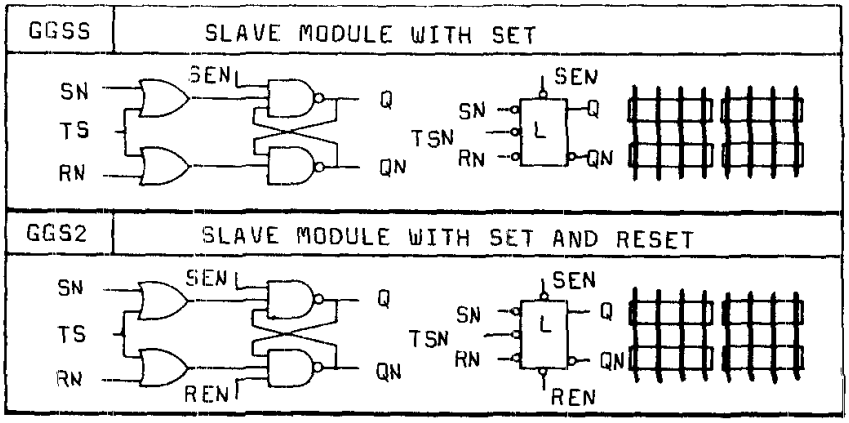
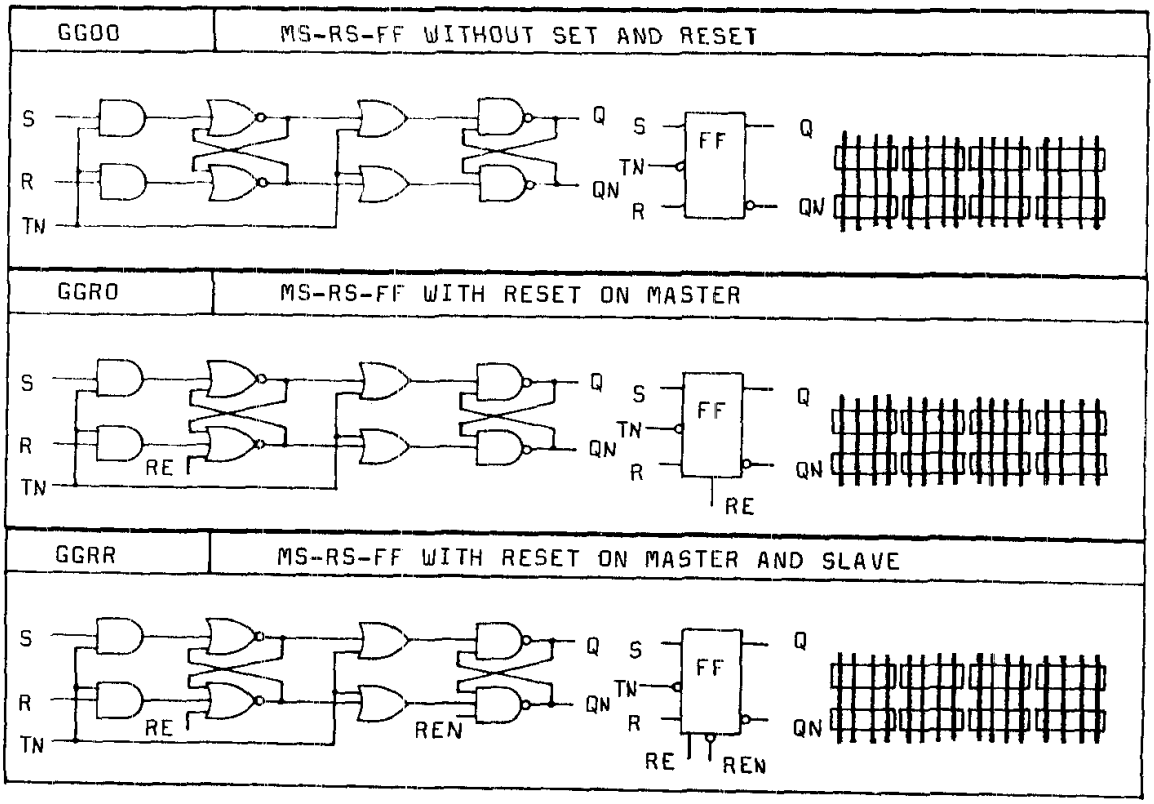


Table 2 Cell function (continued)

Compound latches (continued)

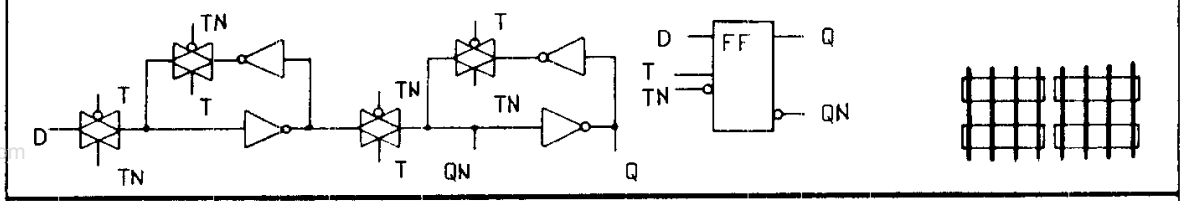


Compound master-slave flip-flops

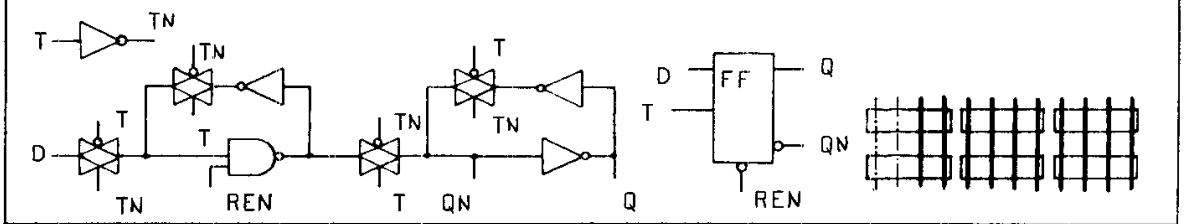


Transmission gate master-slave flip-flops

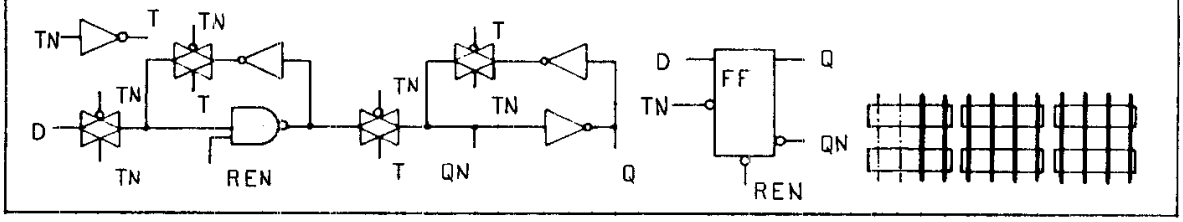
GT00	MS-D-FF WITHOUT SET AND RESET



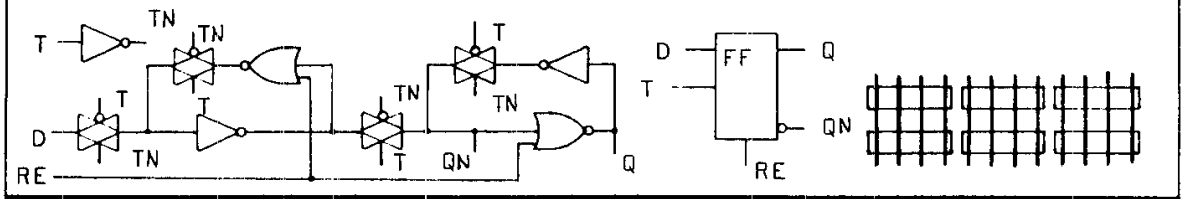
GTROP	MS-D-FF WITH RESET ON MASTER pos. triggered



GTRON	MS-D-FF WITH RESET ON MASTER neg. triggered



GTRRP	MS-D-FF WITH RESET ON MASTER AND SLAVE pos. triggered



GTRRN	MS-D-FF WITH RESET ON MASTER AND SLAVE neg. triggered

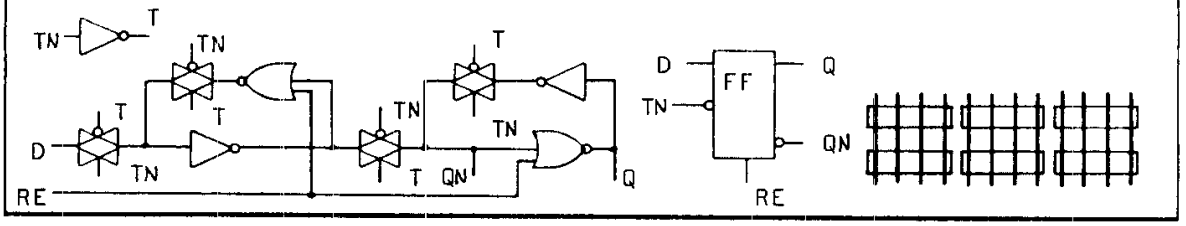
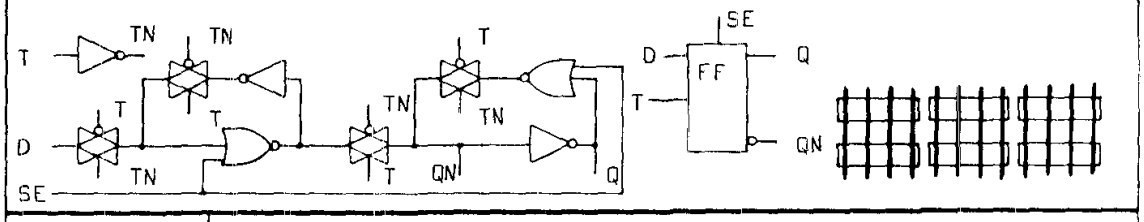


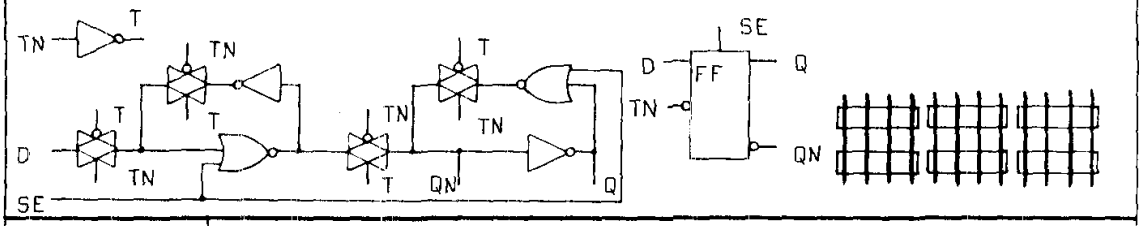
Table 2 Cell functions (continued)

Transmission gate master-slave flip-flops (continued)

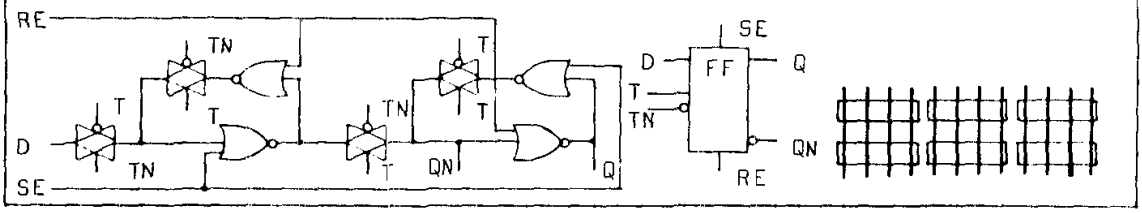
GTSSP	MS-D-FF WITH SET ON MASTER AND SLAVE pos. triggered



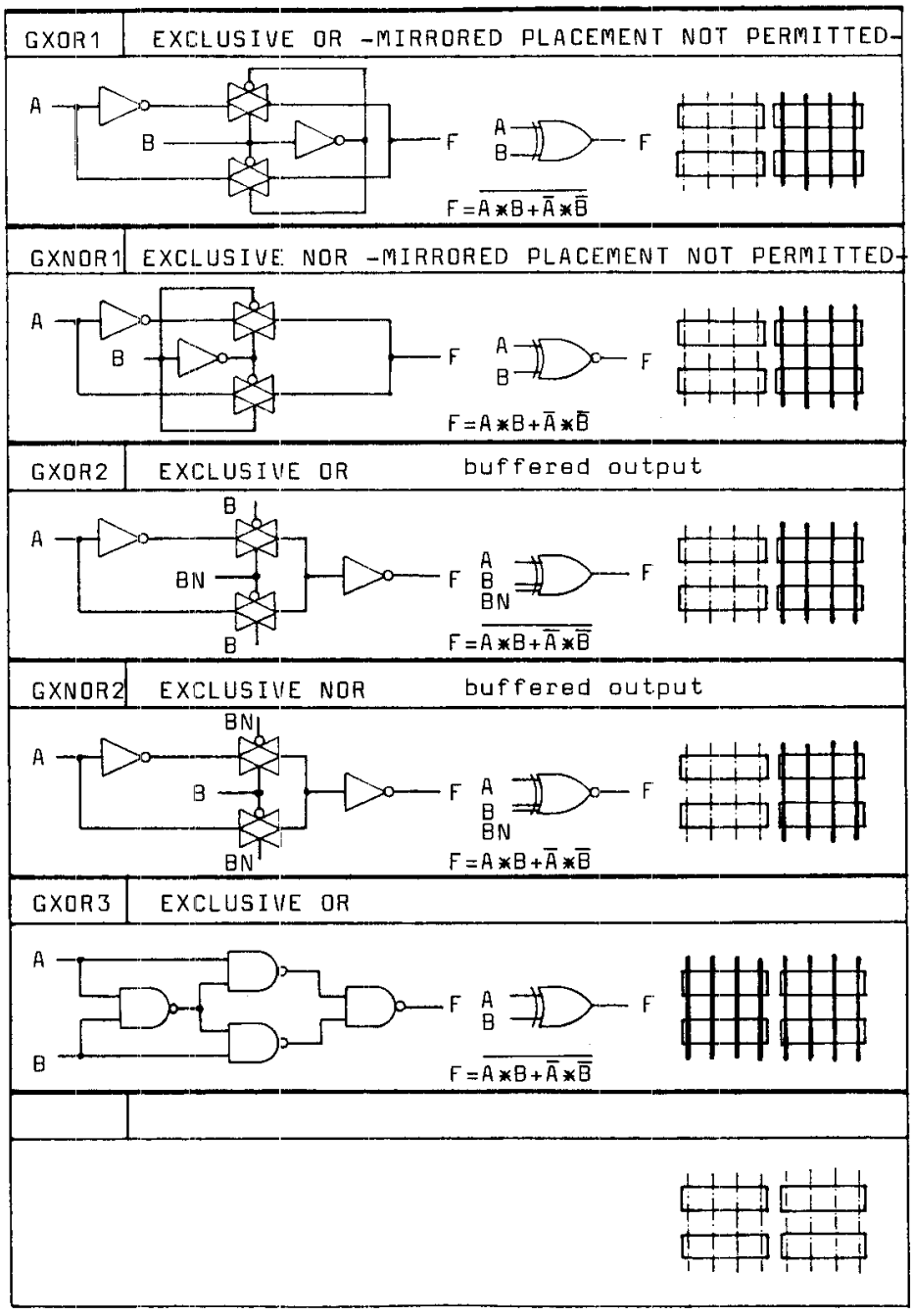
GTSSN	MS-D-FF WITH SET ON MASTER AND SLAVE neg. triggered



GT22	MS-D-FF WITH SET AND RESET ON MASTER AND SLAVE



EXCLUSIVE-OR/NOR



PERIPHERY

To provide a versatile interface, the PCXXXXX has input/output blocks and Schmitt-trigger inputs available. These peripheral elements can be configured to match the input or the output requirements of a wide variety of logic families. Accordingly, a bonding pad may have assigned to it one of the following functions:

- Input stage, including an input protection circuit (series resistor and single diode clamp to V_{SS}). The recommended maximum load is 20 array gates, or 10 array gates for optimum speed performance. Because the input voltage is not clamped to V_{DD}, input voltages greater than the supply voltage are possible, thus allowing voltage-level shifting.
- Schmitt-trigger input stage for noise rejection, pulse shaping, or the suppression of spurious oscillations associates with slow input clock transitions. The recommended maximum load is 10 array gates, or 5 for optimum speed performance.
- Complementary (push-pull) output with driver or buffer performance capability.
- 3-state output with driver or buffer performance capability for bus-line applications.
- Transceiver input/output stage, i.e. a combination of 3-state output and input or Schmitt-trigger stage.
- Open-drain N-channel or P-channel output transistor.
- Direct access to array cells; this enables the user to get direct access to any one (or more in parallel) input of any cell.

In addition, a pull-up/pull-down resistor may be added to any input or output stage. The values available is the range from 7 to 78 kΩ (see note 2 on next page).

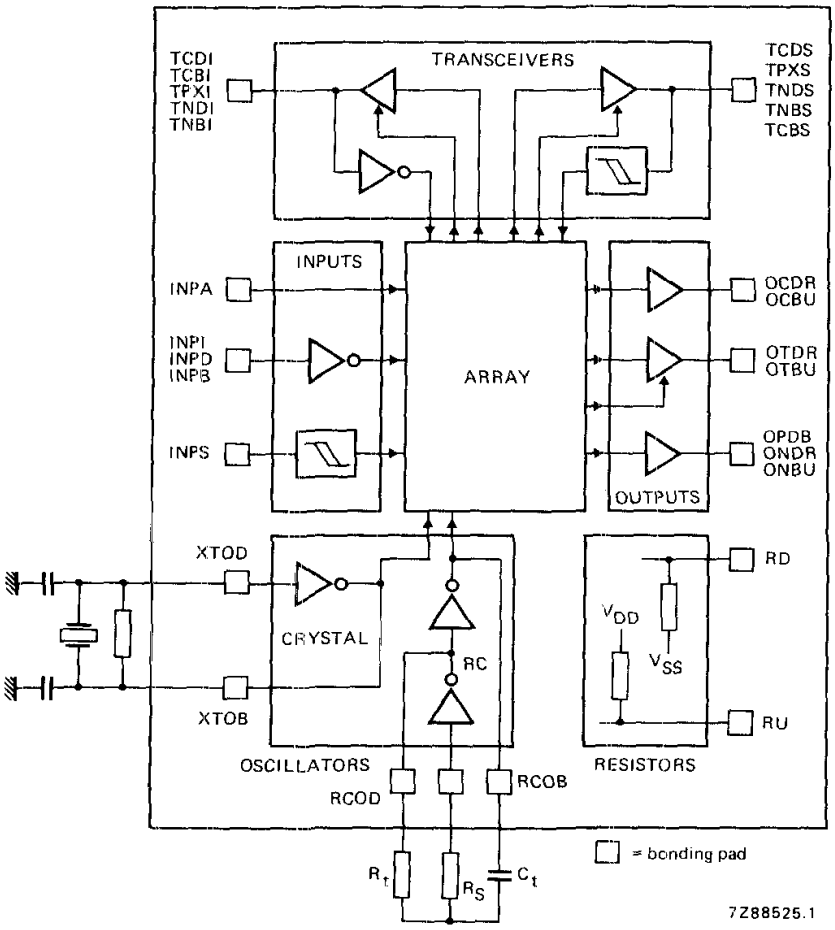


Fig. 12 Possible configurations of each input/output cell.

PERIPHERY (continued)

element	bonding pad code	function
transceivers		
with inverter inputs	TCDI	complementary driver output
	TCBI	complementary buffer output
	TPXI	open drain P-channel driver output
	TNDI	open drain N-channel driver output
	TNBI	open drain N-channel buffer output
with Schmitt-trigger	TCDS	complementary driver output
	TPXS	open drain P-channel driver output
	TNDS	open drain N-channel driver output
	TNBS	open drain N-channel buffer output
	TCBS	complementary buffer output
Inputs		
	INPA	direct access to array
	INPI	inverter
	INPD	driver
	INPB	buffer
	INPS	Schmitt-trigger
Outputs (note 1)		
	OCDR	complementary driver
	OCBU	complementary buffer
	OTDR	3-state driver
	OTBU	3-state buffer
	OPDB	open drain P-channel driver
	ONDR	open drain N-channel driver
	ONBU	open drain N-channel buffer
Oscillator		
crystal	XTOD	oscillator with driver stage
	XTOB	oscillator with buffer stage
RC ($f = \frac{1}{2{,}3\ R_t C_t}$)	RCOD	oscillator with driver stage
	RCOB	oscillator with buffer stage
Resistors (note 2)		
	RD . .	pull-down resistor
	RU . .	pull-up resistor

DEVELOPMENT SAMPLE DATA

Notes

1. Fan-out of driver: 2 LSTTL loads.
   Fan-out of buffer: 4 LSTTL loads.

2. Typical resistor values:

RU05/RD05	7 kΩ	RU60/RD60	64 kΩ
RU10/RD10	12 kΩ	RU65/RD65	68 kΩ
RU15/RD15	17 kΩ	RU70/RD70	73 kΩ
RD30	33 kΩ	RU75/RD75	78 kΩ

GATE DELAYS

Nominal Propagation Delay

Examples are given of the nominal propagation delay times of several library cells in Figs 13, 14 and 15, these being calculated from the delay figures given in the individual macro descriptions. These graphs are intended to provide quick-reference data to enable the designer to make an estimate of the critical a.c. path without having built or simulated a network.

Accurate delay figures can only be obtained after incorporating the wiring length load automatically calculated by INGATE (i.e. the result of the automatic routeing program).
A maximum delay is obtained by multiplying the nominal value by 2,2.

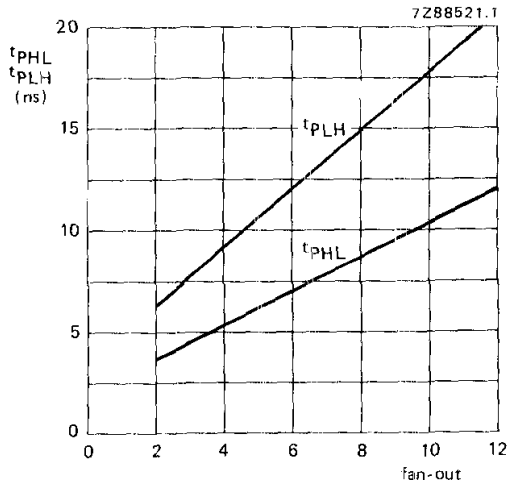


Fig. 13 Nominal propagation delay as a function of the fan-out; GIN1; V_{DD} = 5 V.

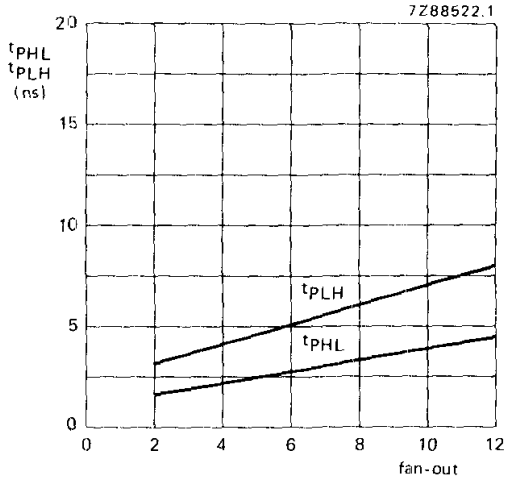


Fig. 14 Nominal propagation delay as a function of the fan-out; GIN4; V_{DD} = 5 V.

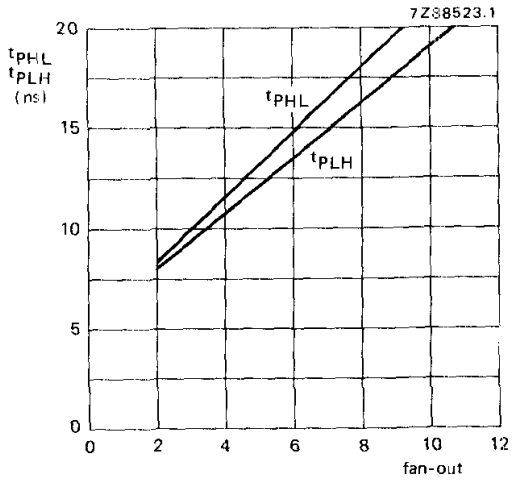


Fig. 15 Nominal propagation delay as a function of the fan-out; GNAND2; V_{DD} = 5 V.

DESIGN PROCEDURE

Gate count

The following step-by-step procedure is intended to guide the designer in determining the correct gate count.

- Simplify the logic circuit.
- Prepare a detailed logic drawing using only library cells provided in this data sheet.
- Expand all MSI functions to the level of gates and flip-flops (see e.g. the logic diagrams HE4000B family).
- Eliminate all unused functions and simplify the complex functions. Standard off-the-shelf products e.g. up/down counters, programmable counters and latches are often devices for considerable simplification.
- Partition the logic into several sections based on the pattern of interconnecting wiring. Circuits with numerous interconnections should be grouped together and interconnections between groups should be kept to a minimum.
- Examine the logic to see if complex functions can be used to reduce the gate count. Reduction can be achieved by using GF . . functions and eliminating unnecessary inversions.
- Rearrange the logic into the library cells provided in this data sheet. When fan-out is more than 10 to 15, add or use buffers to minimize delays.
- Use this simplified logic drawing for a gate count.
- One "equivalent gate" is a 2-input device.
- A rough estimate count can quickly be made by using HE4000B family gate count table.
- Extensive random interconnection e.g. 'wild' combinative logic yields a lower utilization factor than regular sequential logic. Regular LSI functions, such as memories or long shift registers, may lead to inefficient use of a gate array.

Gate Count for HE4000B family

A gate count is given below of 98 different devices that are described in the Handbook LOCMOS HE4000B family.

Only the gates to be implemented in the array area are given.
The connections to the 'outside world' are via the inputs or outputs located in the border area (among the bonding pads).
The numbers within brackets apply when compound master-slave flip-flops (i.e. devices built-up with gates instead of transmission elements) are used.

DESIGN PROCEDURE (continued)

Preliminary list (use for indication only)

type number	number of equiv. gates	type number	number of equiv. gates
HEF4000B	4	HEF4075B	6
HEF4001UB	4	HEF4076B	30 (50)
HEF4002B	4	HEF4077B	12
HEF4006B	76 (148)	HEF4078B	6
HEF4007B	▲	HEF4081B	8
HEF4008B	45	HEF4082B	4
HEF4011UB	4	HEF4085B	8
HEF4012B	4	HEF4086B	8
HEF4013B	14 (18)	HEF4093B	▲
HEF4014B	57 (89)	HEF4094B	54 (104)
HEF4015B	41 (65)	HEF4502B	6
HEF4017B	38 (54)	HEF4508B	12 (20)
HEF4018B	57 (67)	HEF4510B	82 (93)
HEF4019B	8	HEF4511B	49 (60)
HEF4020B	70 (112)	HEF4512B	26
HEF4021B	73 (89)	HEF4514B	60
HEF4022B	31 (43)	HEF4515B	60
HEF4023B	6	HEF4516B	82 (93)
HEF4024B	35 (56)	HEF4517B	552 (1064)
HEF4025B	6	HEF4518B	58 (98)
HEF4027B	22 (24)	HEF4519B	27
HEF4028B	23	HEF4520B	54 (94)
HEF4029B	75 (86)	HEF4521B*	128 (200
HEF4030B	12	HEF4522B	62 (70)
HEF4031B	277 (554)	HEF4526B	62 (70)
HEF4035B	46 (58)	HEF4527B	60 (72)
HEF4040B	61 (96)	HEF4528B	—
HEF4041B	▲	HEF4531B	36
HEF4042B	11 (23)	HEF4532B	24
HEF4043B	8	HEF4534B	—
HEF4044B	8	HEF4539B	24
HEF4047B	—	HEF4541B**	100 (148)
HEF4049B	▲	HEF4543B	65
HEF4050B	▲	HEF4555B	16
HEF4068B	6	HEF4556B	16
HEF4069UB	▲	HEF4557B	360 (560)
HEF4070B	12	HEF4585B	40
HEF4071B	8	HEF4724B	52 (68)
HEF4072B	6	HEF4731B; V	1064 (2138)
HEF4073B	6	HEF4737B; V	—

* Excluding V'_{DD} and V'_{SS}.
** Excluding power-on reset.
▲ Located in the periphery.

type number	number of equiv. gates	type number	number of equiv. gates
HEF40097B	▲	HEF40193B	68 (84)
HEF40098B	▲	HEF40194B	64 (80)
HEF40106B	▲	HEF40195B	40 (56)
HEF40160B	54 (70)	HEF40240B	▲
HEF40161B	54 (70)	HEF40244B	▲
HEF40162B	52 (78)	HEF40245B	▲
HEF40163B	52 (78)	HEF40373B	16 (32)
HEF40174B	34 (52)	HEF40374B	32 (64)
HEF40175B	24 (36)		
HEF40192B	68 (84)		

DEVELOPMENT SAMPLE DATA

▲ Located in the periphery.