CYM9275
CYM9276A
CYM9277B
CYM9278

64K x 36 SRAM Module
128K x 36 SRAM Module
256K x 36 SRAM Module
512K x 36 SRAM Module

Features

- **Operates at 133 MHz**
- **Uses 64K x 18 / 128K x 18 or 256K x 18 high-performance synchronous SRAMs**
- **144-Position Angled DIMM from Berg p/n 61178**
- **3.3V inputs/data outputs**

Functional Description

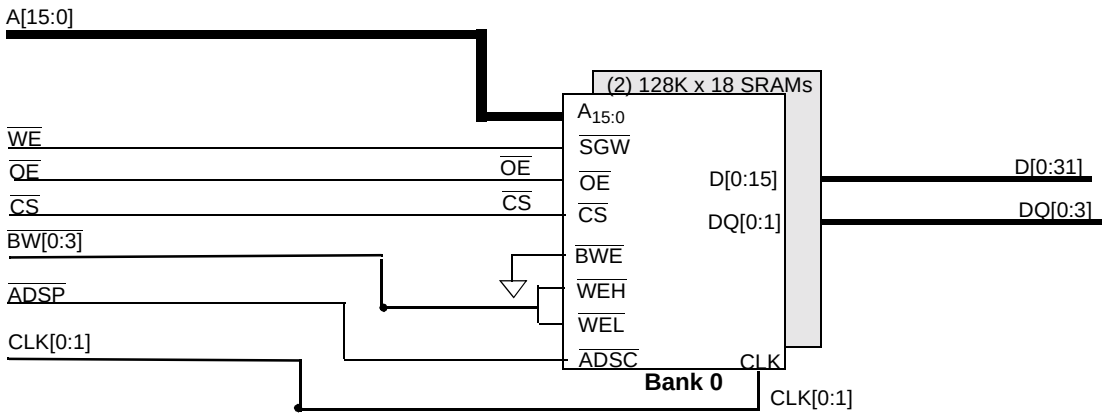
The CYM9275, CYM9276A, CYM9277B, and the CYM9278 are high-performance synchronous pipelined memory modules organized as 64K, 128K, 256K, 512K by 36 bits. These modules are constructed using either 128K x 18 SRAMs (9275, 9276A, 9277B) or 256K x 18 SRAMs (9278) in plastic surface mount packages on an epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

The modules are configured as single banks or multiple banks depending on the SRAM used to make the module. Separate clock are provided for each of the banks. Separate clocks are provided for each of the SRAMs.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

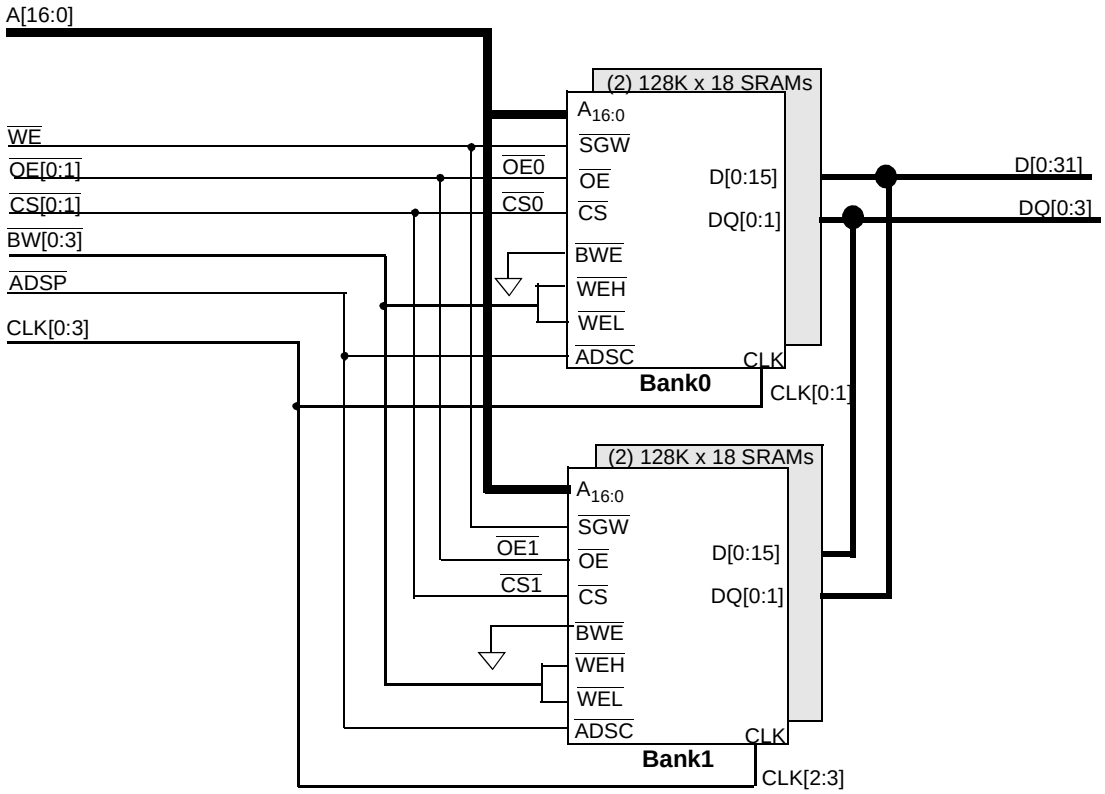
All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 30 micro-inches of gold flash.

Logic Block Diagram - CYM9275



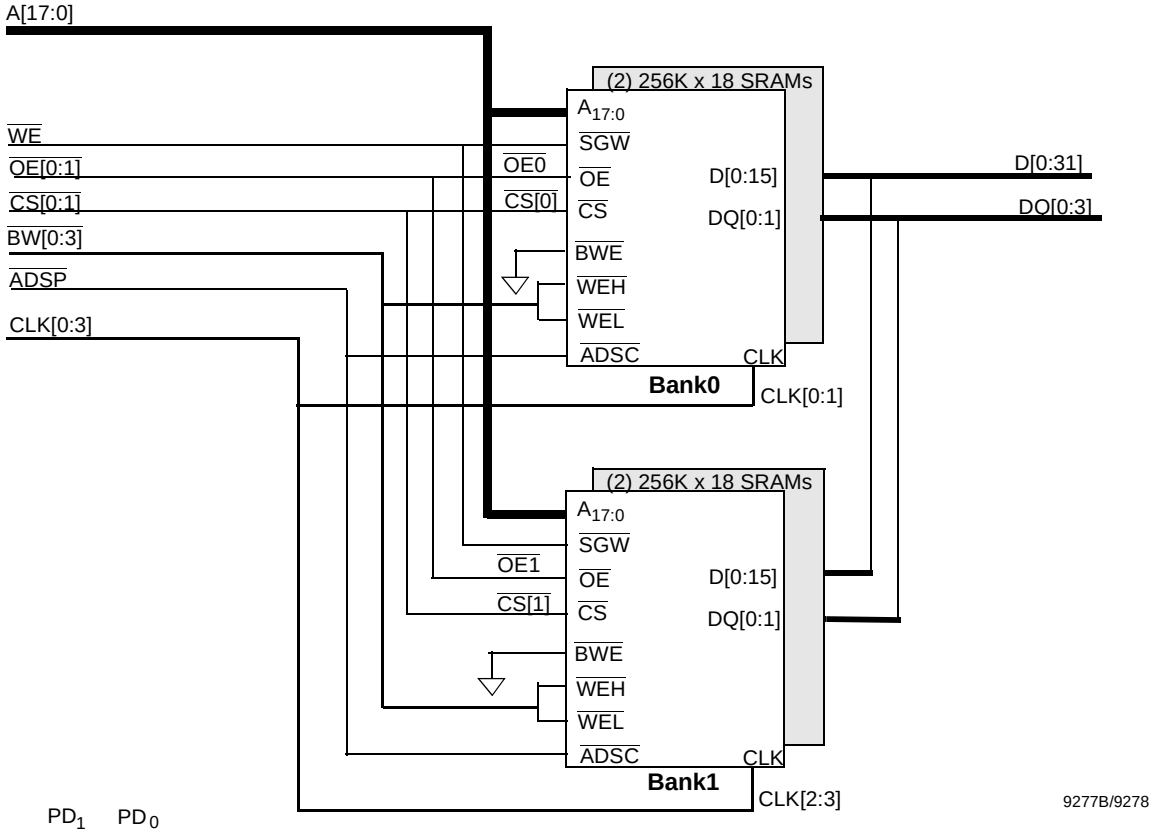
	PD_1	PD_0	
64Kx36	GND	NC	**Bank0**

Logic Block Diagram - CYM9276A



	PD_1	PD_0	
128Kx36	NC	GND	**Bank0**

Logic Block Diagram - CYM9277B / CYM9278



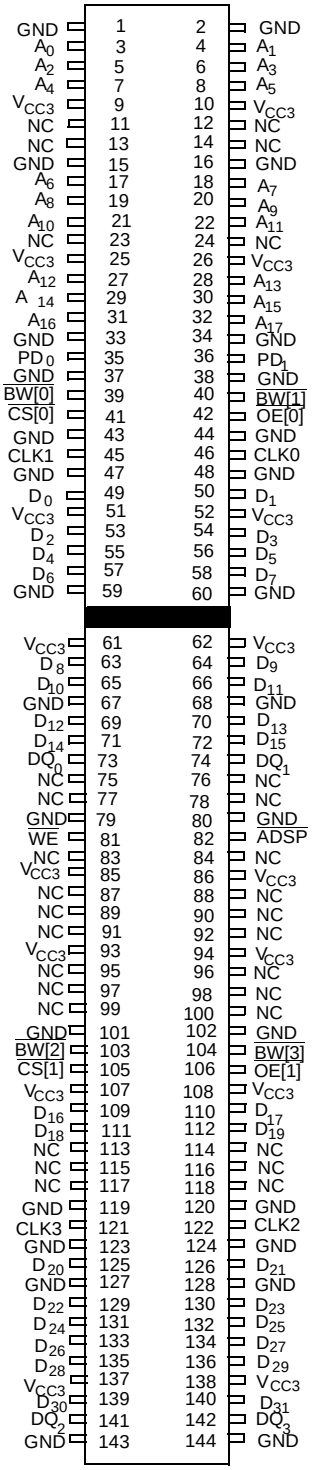
	PD_1	PD_0	
256KX36	GND	GND	**Bank0**
512KX36	NC	NC	**Bank0 and 1**

Selection Guide

	Synchronous Cache Module							
	CYM9275		CYM9276A		CYM9277B		CYM9278	
Part Number	**133**	**100**	**133**	**100**	**133**	**100**	**133**	**100**
Module Size	64 K x 72		128 K x 72		256 K x 72		512 K x 72	
SRAMs Used	4 of 128K x 18 (High address bit tied Off)		8 of 128K x 18 (High address bit tied Off)		8 of 128K x 18		8 of 256K x 18	
System Clock (MHz)	133	100	133	100	133	100	133	100
Data t_{CO}	4.5 ns	5.5 ns	4.5 ns	5.5 ns	4.5 ns	5.5 ns	4.5 ns	5.5 ns

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



Pin Definitions

Signal	Description
V_{CC3}	3V Supply
GND	Ground
A[17:0]	Addresses from processor
$\overline{ADSP}$	Address strobe from the processor
$\overline{OE}$[1:0]	Output Enables for each of the banks
$\overline{BW}$[0:3]	Byte writes
$\overline{WE}$	Global Write
$\overline{CS}$[1:0]	Chip Select for the two banks
PD_0–PD_1	Presence Detect output pins
D[31:0]	Data lines from processor
DQ[3:0]	Data Parity lines from processor
CLK[0:3]	Clock lines to the module
NC	Signal not connected on module
RSVD	Reserved

Presence Detect Pins

	PD_1	**PD_0**
CYM9275 – 64K x 36	GND	NC
CYM9276A – 128K x 36	NC	GND
CYM9277B – 256K x 36	GND	GND
CYM9278 – 512K x 36	NC	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature
with Power Applied..... –0°C to +70°C

3.3V Supply Voltage to Ground Potential..... –0.5V to +4.5V

DC Voltage Applied to Outputs
in High Z State ..... –0.5V to +4.6V

DC Input Voltage ..... –0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 5%

Electrical Characteristics Over the Operating Range

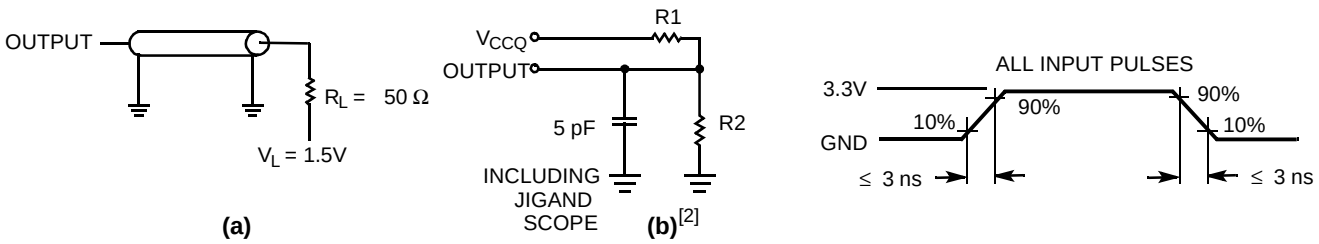
Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = –4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 8 mA		0.4	V
$I_{CC\ (9275)}$	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		350	mA
$I_{CC\ (9276A)}$	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		500	mA
$I_{CC\ (9277B)}$	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		1000	mA
$I_{CC\ (9278)}$	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		1200	mA

Capacitance[1]

Parameter	Description	Test Conditions	Part No.	Max.	Unit
C_A	Address Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9275	12	pF
			9276A	7	
			9277B	14	
			9278	20	
C_I	Control Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9275	12	
			9276A	8	
			9277B	16	
			9278	20	
C_O	Input / Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9275	9	
			9276A	5	
			9277B	10	
			9278	16	
C_{CLK}	Clock Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9275	6	
			9276A	3	
			9277B	3	
			9278	5	

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3]



Switching Characteristics Over the Operating Range

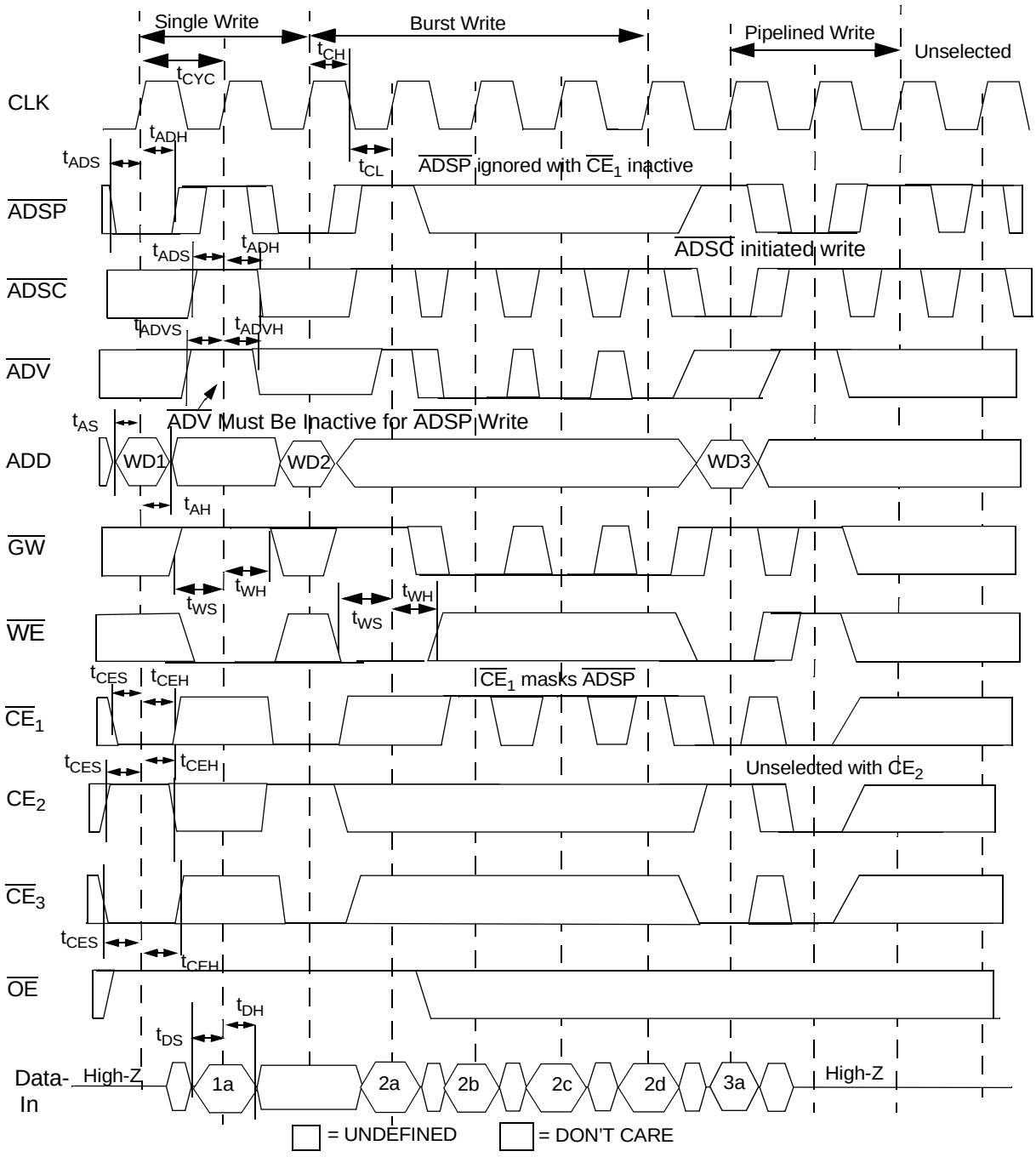
Parameter	Description	CYM9275/76A/77B/78				Unit
		133 MHz		100 MHz		
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	7.5		10		ns
t_{CH}	Clock HIGH	1.9		3.5		ns
t_{CL}	Clock LOW	1.9		3.5		ns
t_{AS}	Address Set-Up Before CLK Rise	2		2		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		4.5		5.5	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2		3.1		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0. 5		0.5		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2		2		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2		2		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	2		2		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[4]		7		7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		4.5		5.5	ns

Notes:

2. Resistor values for V_{CCQ} = 3.3V are R1 = 317Ω and R2 = 351 Ω.
3. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads. All measurements are made at room temperature.
4. t_{EOZ} is specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

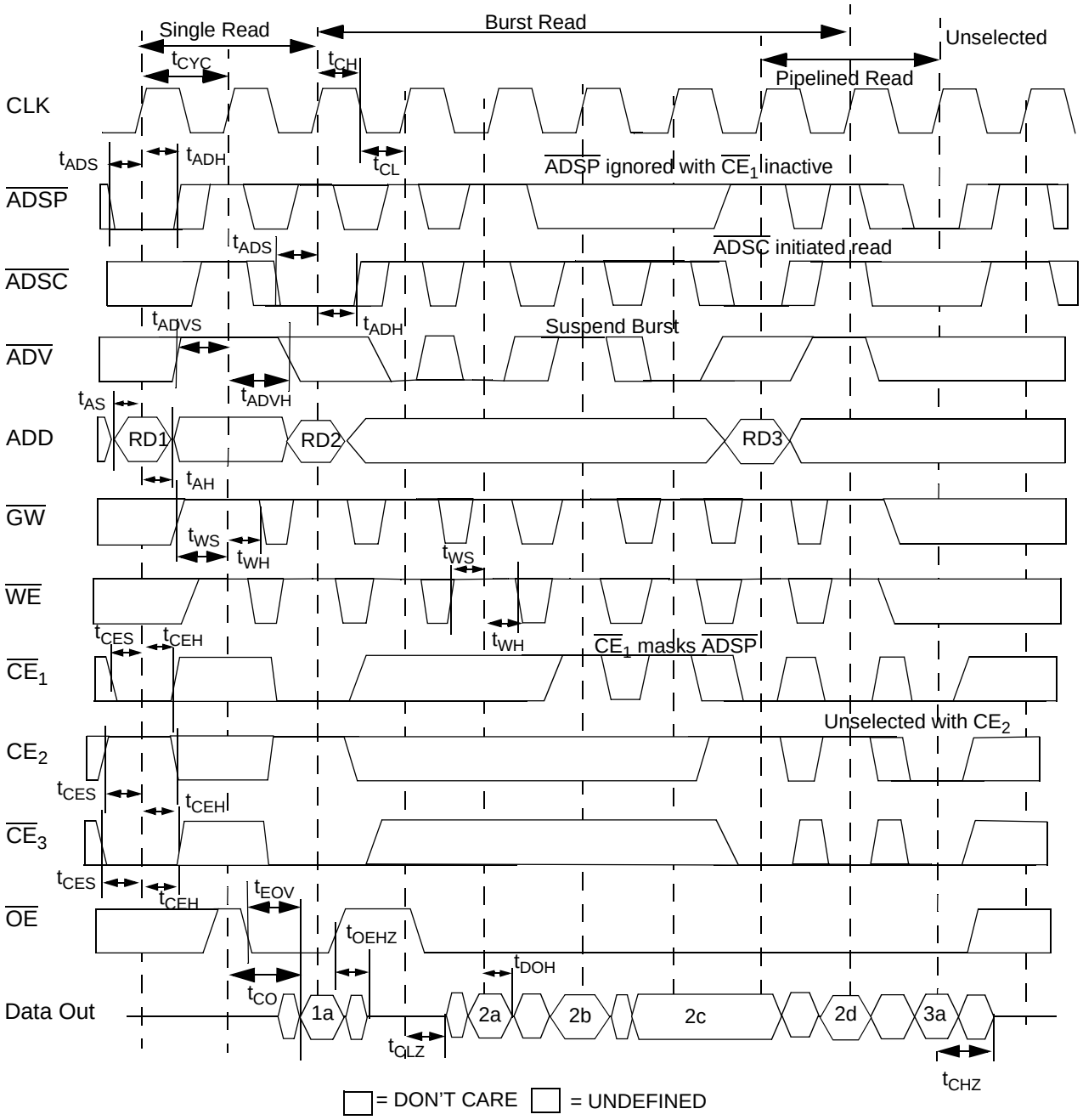
Switching Waveforms

Write



Switching Waveforms (continued)

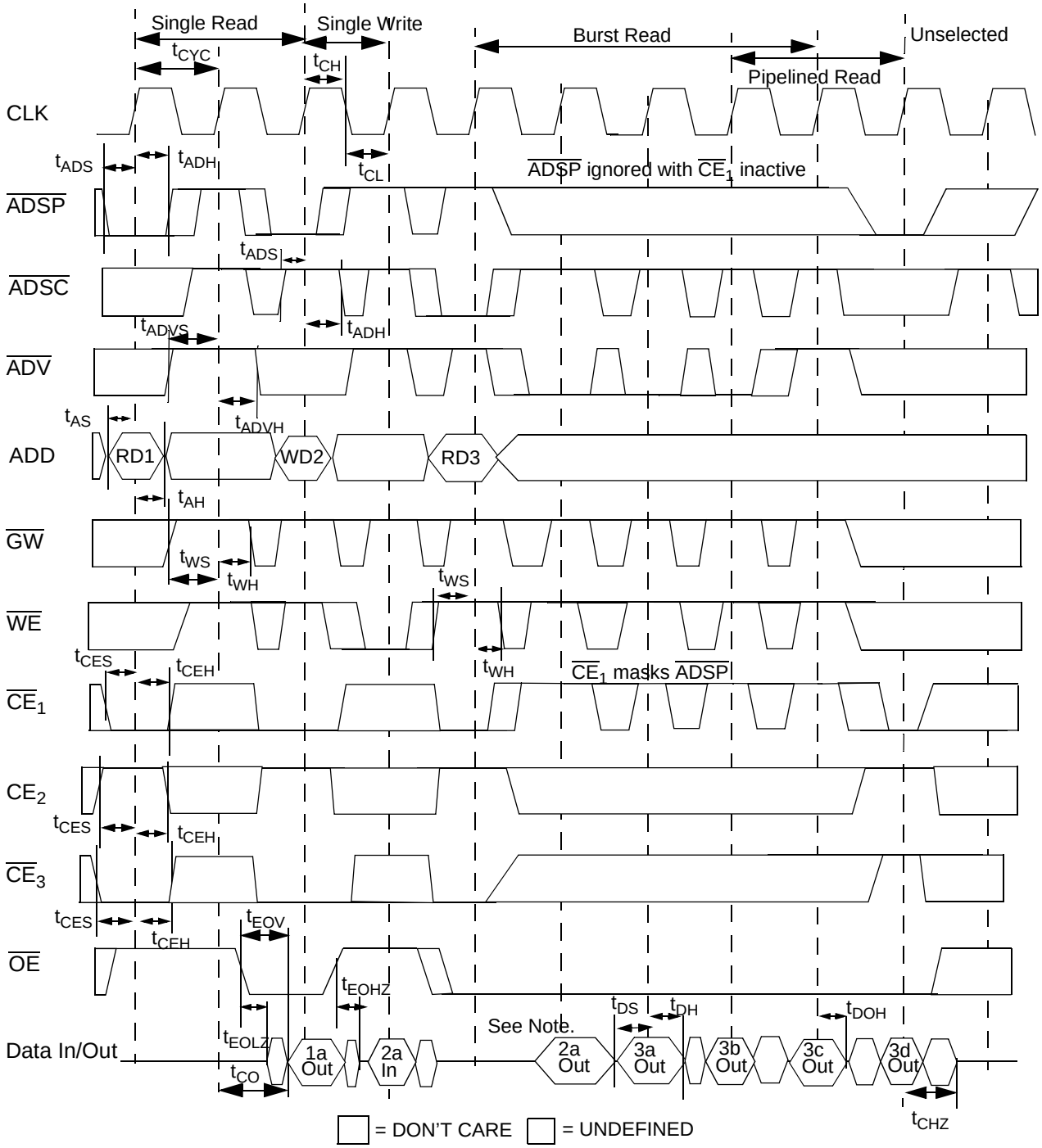
Read [5, 6, 7]



Notes:
5. OE is LOW throughout this operation.
6. If ADSP is asserted while CS is HIGH, ADSP will be ignored.
7. ADSP has no effect on ADV, WL, and WH if CS is HIGH.

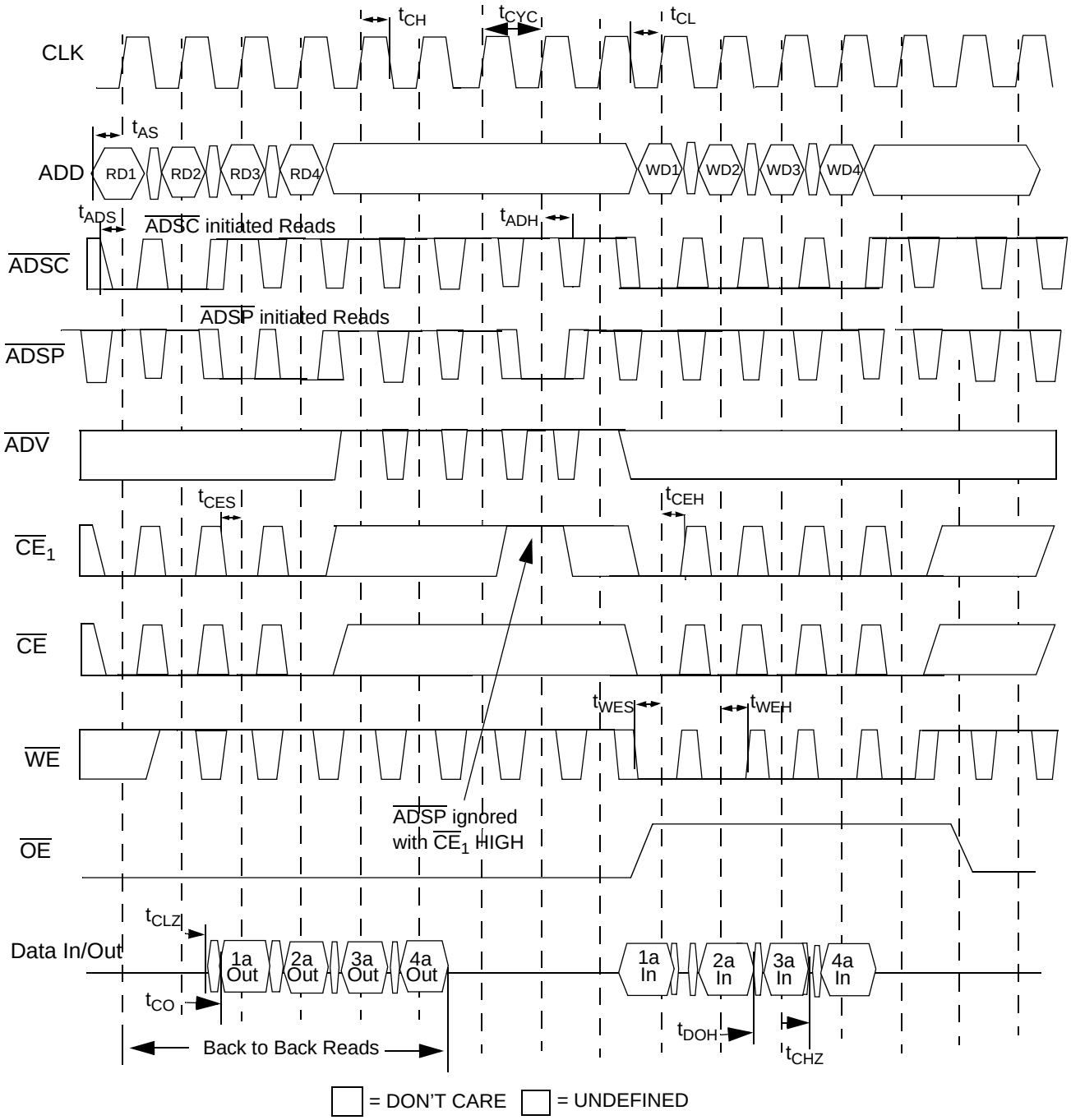
Switching Waveforms (continued)

Read / Write



Switching Waveforms (continued)

Pipeline Timing



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
100	CYM9275PM-100C	PM45	144-Pin Dual-Readout SIMM (DIMM)	Sync 64K x 72	Commercial
	CYM9276APM-100C	PM45	144-Pin Dual-Readout SIMM (SIMM)	Sync 128K x 72	
	CYM9277BPM-100C	PM46	144-Pin Dual-Readout SIMM (DIMM)	Sync 256K x 72	
	CYM9278PM-100C	PM46	144-Pin Dual-Readout SIMM (DIMM)	Sync 512K x 72	
133	CYM9275PM-133C	PM45	144-Pin Dual-Readout SIMM (DIMM)	Sync 64K x 72	
	CYM9276APM-133C	PM45	144-Pin Dual-Readout SIMM (SIMM)	Sync 128K x 72	
	CYM9277BPM-133C	PM46	144-Pin Dual-Readout SIMM (DIMM)	Sync 256K x 72	
	CYM9278PM-133C	PM46	144-Pin Dual-Readout SIMM (DIMM)	Sync 512K x 72	

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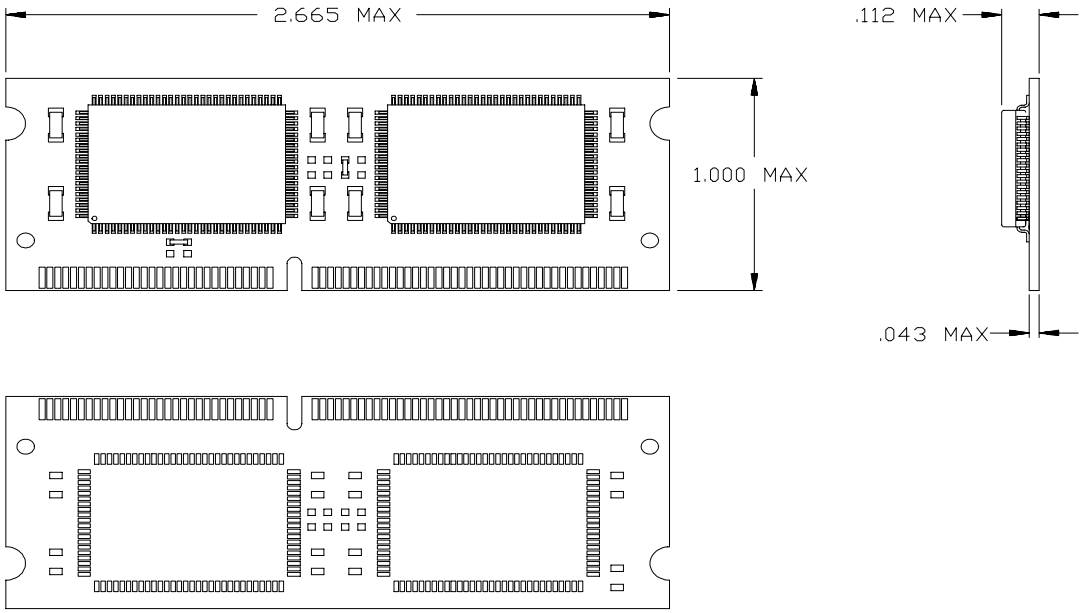
Package Diagrams

144-Pin Single-Sided DIMM PM45



Package Diagrams

144-Pin Dual-Sided DIMM PM46