

UT54ACS253/UT54ACTS253

Radiation-Hardened

Dual 4-Input Multiplexers, Three-State Outputs

FEATURES

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- 1.2μ radiation-hardened CMOS
 - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
 - 16-pin DIP
 - 16-lead flatpack

DESCRIPTION

The UT54ACS253 and the UT54ACTS253 are 1-line to 4-line multiplexers that contain drivers to supply full binary decoding. Separate output control inputs are provided for each of the two four-line sections.

Use the three-state outputs to drive data lines in bus-organized systems. With all but one of the common outputs disabled the low-impedance of the single enable output will drive the bus line to a high or low logic level. Each output has its own strobe (G).

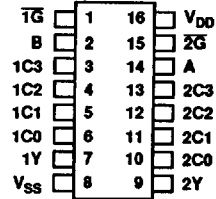
The devices are characterized over full military temperature range of -55°C to +125°C.

FUNCTION TABLE

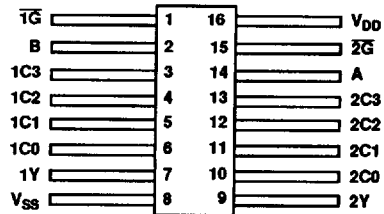
SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	\bar{G}	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

PINOUTS

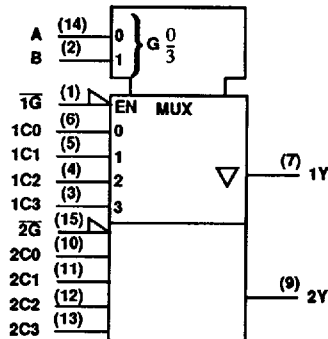
16-Pin DIP
Top View



16-Lead Flatpack
Top View



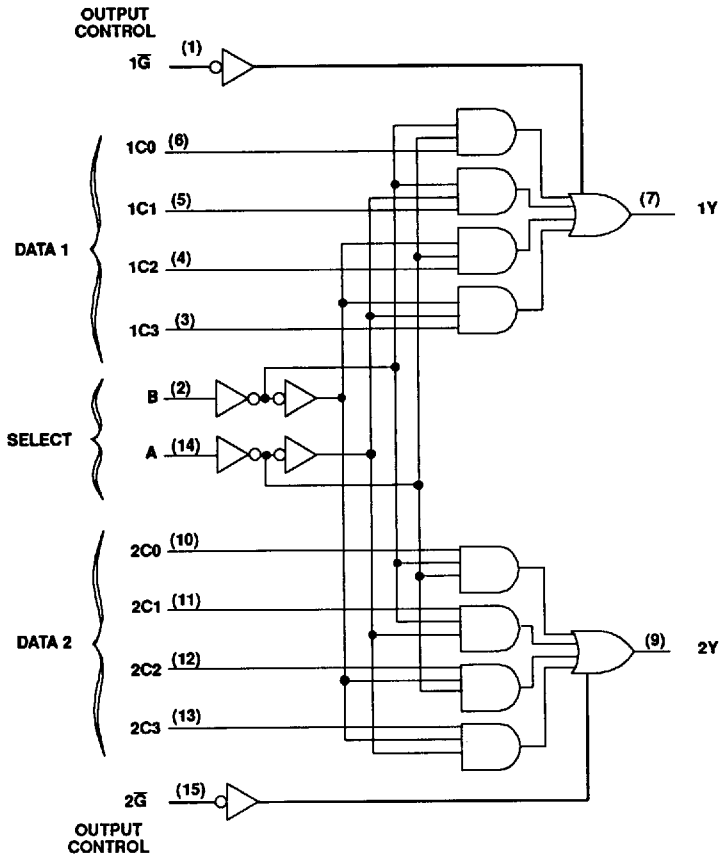
LOGIC SYMBOL



Note:

1. These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS ¹

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU & SEL Threshold ²	80	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

- 1. Logic will not latchup during radiation exposure within the limits defined in the table.
- 2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	20	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

- 1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS ⁷ $(V_{DD} = 5.0V \pm 10\%; V_{SS} = 0V, -55^{\circ}C < T_C < +125^{\circ}C)$

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3 V_{DD}	V
V_{IH}	High-level input voltage ¹ ACTS ACS		.5 V_{DD} .7 V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	μ A
V_{OL}	Low-level output voltage ³ ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
V_{OH}	High-level output voltage ³ ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$.7 V_{DD} $V_{DD} - 0.25$		V
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ and V_{SS}	-20	20	μ A
I_{OS}	Short-circuit output current ^{2,4} ACTS/ACS	$V_O = V_{DD}$ and V_{SS}	-200	200	mA
P_{total}	Power dissipation ^{8,9}	$C_L = 50pF$		2.1	mW/ MHz
I_{DDQ}	Quiescent Supply Current	$V_{DD} = 5.5V$		10	μ A
C_{IN}	Input capacitance ⁵	$f = 1MHz @ 0V$		15	pF
C_{OUT}	Output capacitance ⁵	$f = 1MHz @ 0V$		15	pF

Notes:

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(\min) + 20\%$, -0% ; $V_{IL} = V_{IL}(\max) + 0\%$, -50% , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(\min)$ and $V_{IL}(\max)$.
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density $\leq 5.0ES$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose $\leq 1E6$ rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

AC ELECTRICAL CHARACTERISTICS ²

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V$ ¹, $-55^{\circ}C < T_C < +125^{\circ}C$)

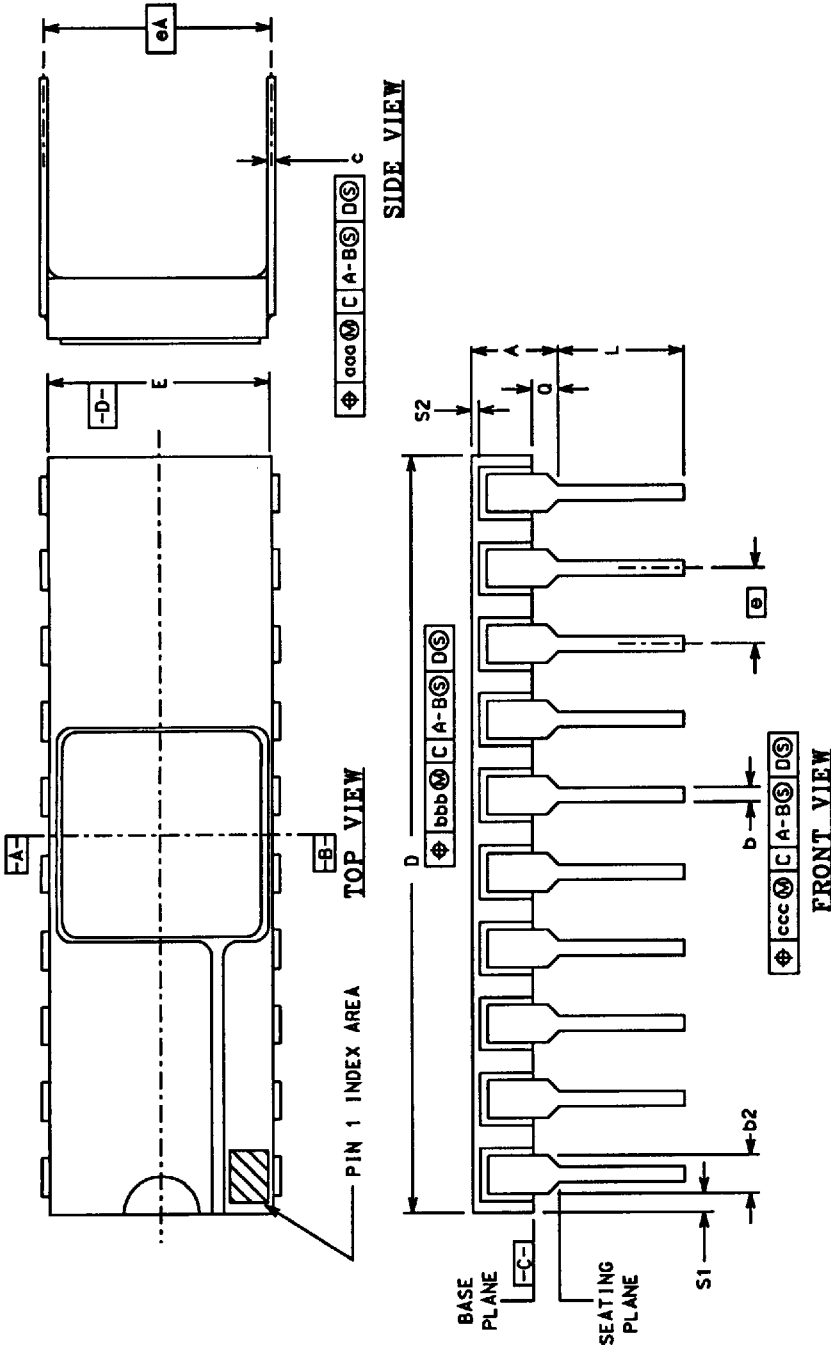
SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t _{PLH}	Select to output Y _n	2	12	ns
t _{PHL}	Select to output Y _n	2	16	ns
t _{PLH}	Data to output Y _n	2	14	ns
t _{PHL}	Data to output Y _n	2	16	ns
t _{PZH}	\bar{G} low to Y _n active	2	12	ns
t _{PZL}	\bar{G} low to Y _n active	1	12	ns
t _{PHZ}	\bar{G} high to Y _n three-state	2	11	ns
t _{PLZ}	\bar{G} high to Y _n three-state	2	10	ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose $\leq 1E6$ rads(Si).

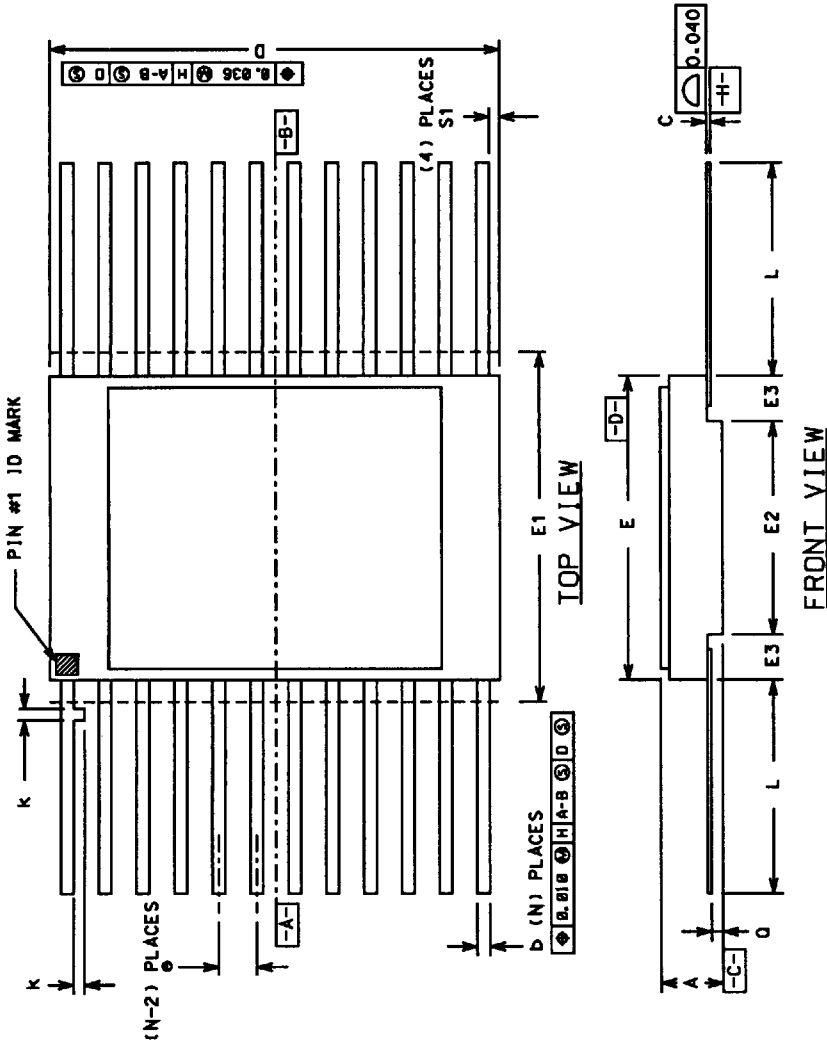
2.0 RAD-HARD MSI PACKAGES

Side-Brazed Packages



PKG CONFIG	MIL-STD- 1835 Dwg CONF C	DIMENSION SYMBOLS														
		A	b	b2	c	D	E	e	eA	L	Q	S1	S2	ddd	bbb	ccc
-01	14 D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-02	16 D-2	0.200	0.014	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-03	20 D-8	0.200	0.026	0.065	0.018	1.060	0.310	0.100	0.300	0.200	0.070	0.005	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.125	0.015	0.005	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.125	0.015	0.005	0.005	0.015	0.030	0.010
			0.014	0.045	0.008		0.220	0.100	0.300	0.125	0.015	0.005	0.005	0.015	0.030	0.010

Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS														
			A	b	c	D	E	E1	E2	E3	e	k	L	O	S1		
-03	14	F-2A	0.115	0.022	0.009	0.390	0.260	0.290	---	---	0.130	0.030	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.235	---	---	---	---	---	BSC	0.008	0.270	0.026	0.005
-04	16	F-5A	0.115	0.022	0.009	0.440	0.285	0.315	---	---	0.130	0.030	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	---	---	---	---	BSC	0.008	0.250	0.026	0.005
-05	20	F-9A	0.115	0.022	0.009	0.540	0.300	0.330	---	---	0.130	0.030	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	---	---	---	---	BSC	0.008	0.250	0.026	0.000