AMI SEMICONDUCTORS

SX041

WavePlex™ Wireless Products

Product Description

January, 1996

Spread Spectrum Transmitter

General Description

The SX041 Spread Spectrum Transmitter (STX) is a highly programmable baseband CMOS integrated circuit that simplifies the design of direct sequence spread spectrum modems. Used to create very low cost transmit-only remote wireless links, the SX041 is designed to interface easily with the SX042 Receiver or the SX043 Transceiver such that multiple SX041 nodes can supply data to a single SX042 or SX043 collector host. Connected to a standard 8 bit microcontroller data bus, the STX allows the user to manage internal STX functions including the type and length of PN codes, data rates, chipping rates, preamble, transmission protocols, power levels, and type of redundancy checks, as well as manage the external circuitry for signal transmission.

Features

- All baseband digital circuitry for direct sequence coded transmissions
- PN clock programmable up to 64M chips per second
- Easy node link interface to AMI's SX042 or SX043
- Psuedorandom noise rates up to 64M chips per second
- Programmable up to 30dB processing gain; PN code lengths from 3 to 2047 chips
- Data and PN code streams available either separately or combined
- Supports BPSK, DBPSK, QPSK, and DPQSK modulation schemes
- Supports RF transmission in any frequency band
- CRC-32 or CRC-16 redundancy checking available
- Selectable code scrambling for spectral whitening (127 bit data scrambler)
- Address/data bus timing allows interface to many popular 8 bit microcontrollers
- Supports packetized synchronous protocol (HDLC)
- 16 Byte data FIFOs reduces interrupt overhead
- Low power 3.3 volt (5 volt option available)
- Power-down modes for minimum power usage

Figure 1: BLOCK DIAGRAM

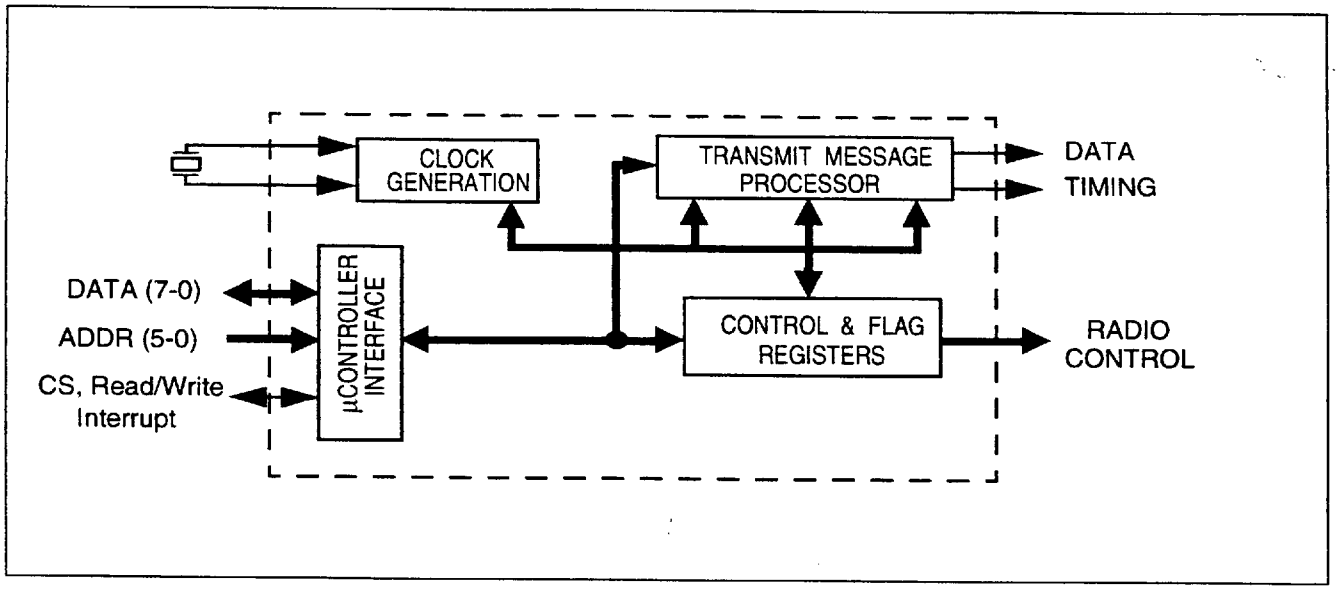
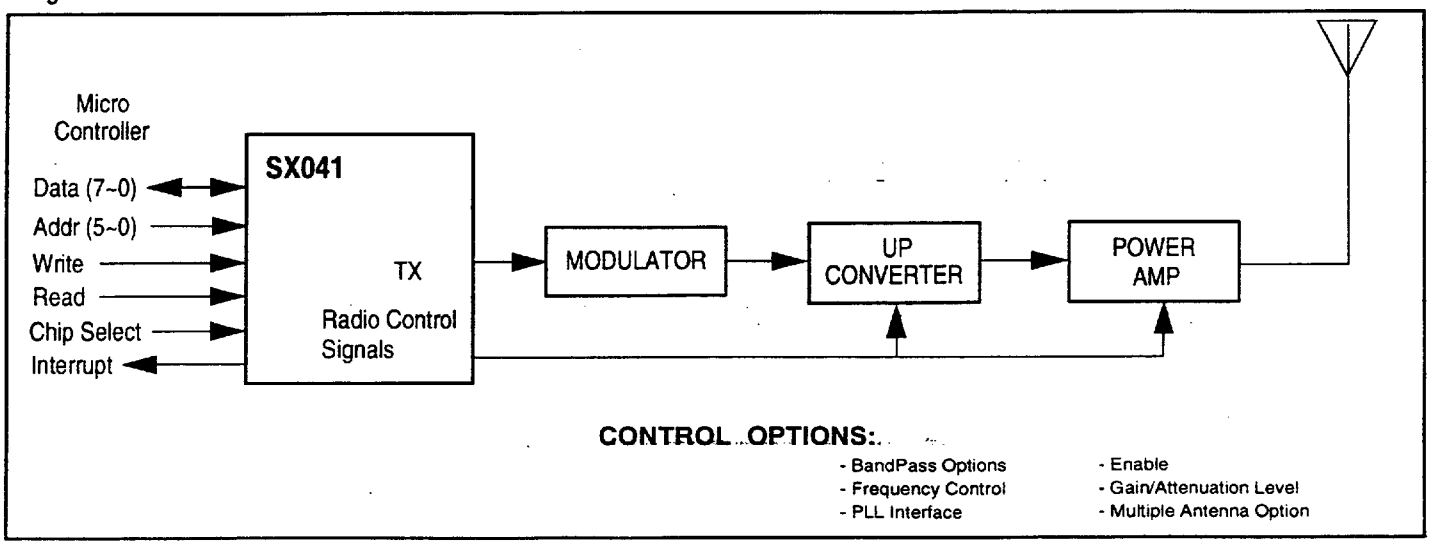


Figure 2. SYSTEM INTERFACE DIAGRAM



Functional Block Overview

The STX Block Diagram in Figure 1 details the major functional blocks of the device. The microcontroller manages the Transmit Message Processors independently through various control and flag registers on the IC.

The microcontroller can also use registers in the STX to control various radio functions. Figure 2 above represents the full radio implementation using the STX.

MICROCONTROLLER INTERFACE: The device has a simple bus interface consisting of a bi-directional tri-state eight-bit data bus , a seven-bit address bus, read, write, and chip select inputs, and a general interrupt output. Target microcontrollers for this interface include the 68HC11, 68HC05, 6502, Z8, 8051, 16C5x, and 16C7x.

Power Manager: The microcontroller can put the IC into Standby Mode (a minimum power state) or select on and off.

CONTROL AND FLAG REGISTERS: The STX has 45 registers available to the microcontroller. These registers allow programmable control over most characteristics of the transmit channel (See Control Options in Figures 3), as well as off-chip control of the radio portion of the design. (See Control Options in Figure 2)

The SX041 includes a programmable 8 to 48 bit variable RF synthesizer interface. This interface supports any of the three popular serial data transfer styles in RF synthesizers: pulsed transfer, active enable transfer, or clock and data only. It can also be set to a fourth 'user defined' mode. Extra control lines are also available for external circuits that require gain or attenuation level selection, pass band range selection, multiple antenna selection, etc..

CLOCK GENERATION: This is shown as part of the Transmit Message Processor in Figure 3. The clock generation circuit can be programmed to support crystals from 1MHz to 16MHz or can be driven by an external clock line. The 64MHz clock required for the maximum chipping rate and the 4MHz Tx_CLK signal are created in this block. Control options allow other programmable clocking levels and various 'divide by n' registers are provided.

Tx PN Code Generator: The STX provides two PN code registers (Code A and Code B), an offset register, and control registers for the creation of various usable maximal length codes and Gold codes. PN code lengths are "OFF", 3, 7, 11, 15, 31, 63, 127, 255, 511, 1027, and 2047. The 11-bit code is the Barker code (Wireless LAN specification IEEE P802.11). Outputs available are the Barker Code, Code A, Code B, or an A+B Gold Code. Disabling the PN code to create a narrowband transmission is also possible.

Tx FIFO: Byte-wide data from the microcontroller is placed in a 16-byte deep FIFO. The 'FIFO near-empty' detect level can be programmed at bytes 0, 2, 4, or 8.

The IC can also be programmed to either abort or end the message in an empty FIFO situation.

Packet Generator: The Packet Generator controls whether or not the data is sent in packets, and what, if any, preamble and end protocols are added by the STX. The

user may choose to set the packet structure in the controller and then disable the on-chip packet capabilities.

In Packet Mode, the STX can generate a repeating preamble code, HDLC protocols, destination address and control commands, CRC-16 or CRC-32 error detection coding, and end codes as selected by the control registers. A packet mode frame format is shown below:

START FLAG	ADDRESS	CONTROL	INFORMATION	CRC	END FLAG
8 bits	8 bits	8 bits	8 * N bits (any length)	16/32 bits	8 bits

The packet mode uses the HDLC algorithm for automatically inserting a zero after any five ones in the address, control, information, and CRC fields of the message.

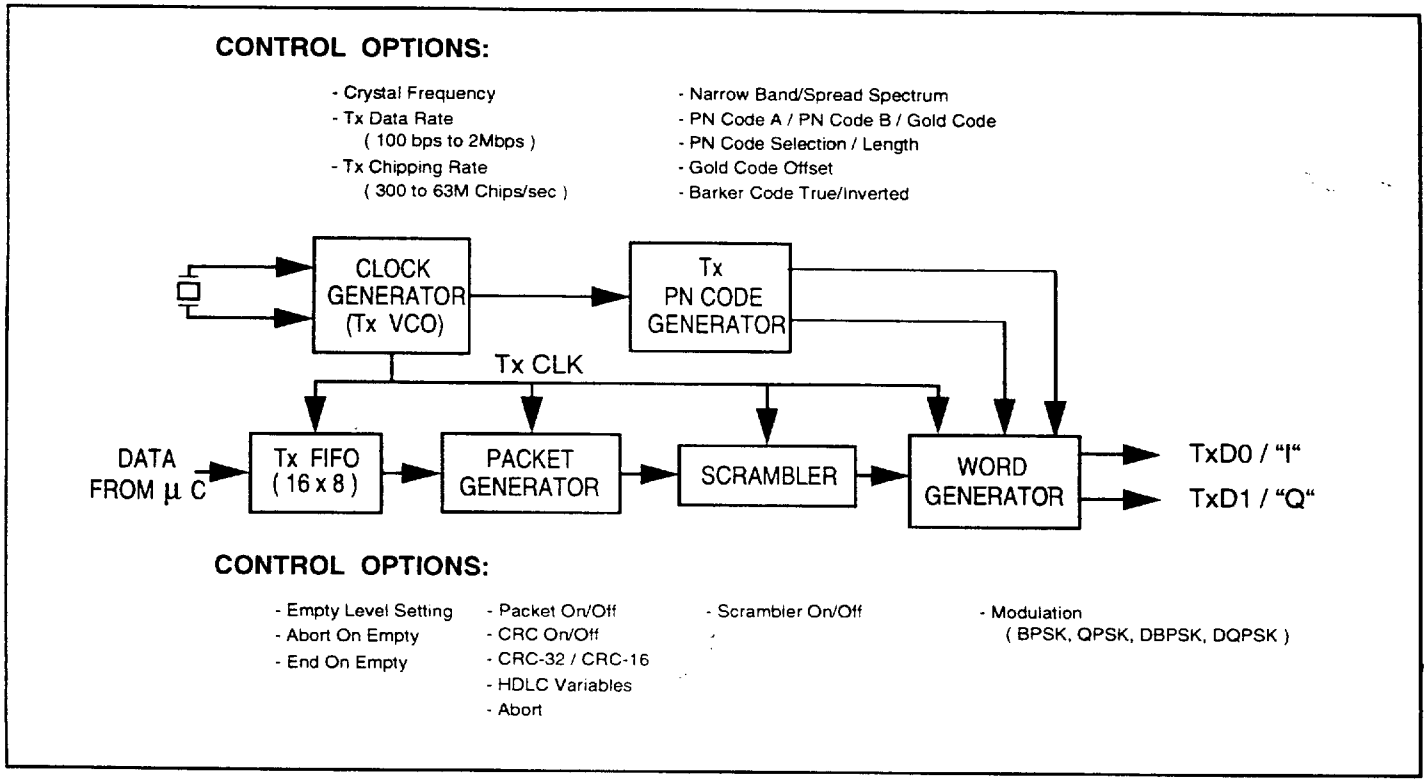
A data underrun (FIFO empty) usually signals that the message is complete, but can be programmed to interpret this condition as an ABORT.

Scrambler: The scrambler is a linear feedback shift register that randomizes the data over a length of 127 bits. The scrambler can be programmed on or off.

Word Generator: The word generator synchronizes the data with the start of the PN code (EPOCH clock) and mixes the PN code with the data transmission. The PN code is running at a much higher frequency than the transmitted data rate, and is sequenced completely once during each data bit period. It is then repeated for each subsequent data bit.

Data can be presented for BPSK, QPSK, Differential BPSK, or Differential QPSK modulation formats. Outputs TxD0 and TxD1, combined with the Tx PN signal, provide the required binary information for the external modulation circuit selected.

Figure 3. TRANSMIT MESSAGE PROCESSOR



Data Rates

The SX041 can achieve data rates dependent on the PN code lengths used. These are shown below for each modulation scheme (nominal).

BPSK and DBPSK:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15, 31, 63	1 M	1 M
127	500 K	500 K
255	250 K	250 K
511	125 K	125 K
1023	62.5 K	62.5 K
2047	31 K	31 K

QPSK, DQPSK:

PN Code Length	Maximum Data Rate bits/sec	Maximum Symbol Rate symbols/sec
3, 7, 11*, 15, 31, 63	2 M	1 M
127	1 M	500 K
255	500 K	250 K
511	250 K	125 K
1023	125 K	62.5 K
2047	62.5 K	31 K

* The 11 bit Barker code (1, -1, 1, 1, -1, 1, 1, 1, -1, -1, -1).

Pin Description

NAME:	TYPE:	FUNCTION:
AGND1	Analog ground	
GND1	ground	
VDD1	Vdd	
OSC1	input	Crystal Oscillator or external reference input. This input is divided by OSCDIV to generate the reference clock for the transmit PLL.
OSC2	padosc	Crystal Osc output.
PLL[0:3]	output	Off-Chip PLL programming; bit0, Enable1; bit1, Sclk; bit2, Enable0; bit3, Sdata.
TXD0	output	Transmit data "I" output.
TXD1	output	Transmit data "Q" output.
GND2	ground	
EXT[0:3]	output	External Control port (lower bits), User Defined Functions for radio control.
VDD2	Vdd	
INT	output	Active high. Initiates an interrupt to the microprocessor.
RESET	input	Active low. Sets all registers to default values and forces the SX041 into its standby state.
CS	input	Active low. Selects the chip for reading and writing via the uP interface
RD	input	Active low. Initiates a read operation via the uP interface.
WR	input	Active low. Initiates a write operation via the uP interface.
GND3	ground	
DATA[0:7]	BiDirection	uP Interface data bus.
ADDR[0:6]	input	uP Interface address bus.
VDD3	Vdd	
GND4	ground	
TEST	I/O	Test pin only.
AGND2	Analog ground	

NAME:	TYPE:	FUNCTION:
AVDD2	Analog VDD	
RBIAS	Analog Input	Current reference for DACs and analog buffers. Nominal resistor value of 20K ohm to AGND3 at 3.3 volt VDD and 30K ohm at 5 volt VDD.
VREF	Analog Input	Reference voltage for DACs. Value is mid-scale between VDD and GND
AGND3	Analog ground	
AVDD3	Analog VDD	
AVDD1	Analog VDD	
VCO1	Analog I/O	Transmit VCO voltage control input.