DOUBLE DATA RATE (DDR) SDRAM

FEATURES

- PC2100, PC2700 and PC3200 compatible
- VDD = +2.5V ±0.2V, VDDQ = +2.5V ±0.2V (For –6A & -75A)
- VDD = +2.6V ±0.1V, VDDQ = +2.6V ±0.1V (For -5B)
- Bi-directional data strobe (DQS) transmitted/ received with data, i.e. source-synchronous data capture (x16 has two: LDQS and UDQS – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two: LDM and UDM – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh
- Longer lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2 compatible)
- These devices are optimized for single rank DIMM applications

Options: Designation:

Family:
SpecTek Memory — SAA

Configuration:
128 Meg x 4 (32 Meg x 4 x 4 banks) — 128M4
64 Meg x 8 (16 Meg x 8 x 4 banks) — 64M8
32 Meg x 16 (8 Meg x 16 x 4 banks) — 32M16

Design ID:
DDR2 512 Megabit Design — Tx7x
(Call SpecTek Sales for details on availability of "x" placeholders)

Voltage and refresh:
2.5V, Auto Refresh — V8
2.5V, Self or Auto Refresh — R8

Package Types:
66-pin Plastic TSOP, OCPL (400 mil width, 0.65mm pin pitch) — TW
60-ball (10mm x 12.5mm) FBGA — FN

Timing – Cycle Time:
5ns @ CL=3 (PC3200 or DDR400B) — -5B
6ns @ CL = 2.5 (PC2700 or DDR333) — -6A
7.5ns @ CL = 2.5 (PC2100 or DDR266) — -75A

Part number example: SAA64M8T27BV8TW-6A
(For part numbers prior to December 2004, refer to page 12 for decoding.)

PIN ASSIGNMENT (TOP VIEW) 66-PIN TSOP

x4	x8	x16			x16	x8	x4
VDD	VDD	VDD	1	66	VSS	VSS	VSS
NF	DQ0	DQ0	2	65	DQ15	DQ7	NF
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NF	DQ2	DQ4	8	59	DQ11	DQ5	NF
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	DNU	DNU	DNU
VDD	VDD	VDD	18	49	VREF	VREF	VREF
DNU	DNU	DNU	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
WE#	WE#	WE#	21	46	CK#	CK#	CK#
CAS#	CAS#	CAS#	22	45	CK	CK	CK
RAS#	RAS#	RAS#	23	44	CKE	CKE	CKE
CS#	CS#	CS#	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addressing	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	4K (A0–A9, A11, A12)	2K (A0–A9, A11)	1K (A0–A9)

GENERAL DESCRIPTION

The 512Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512Mb DDR SDRAM uses a double-data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bi-directional data strobe (DQS or LDQS/UDQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The 512Mb DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All full drive strength outputs are SSTL_2, Class II compatible.

NOTE 1: The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.

NOTE 2: Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
Additionally, the x16 is divided in to two bytes — the lower byte and upper byte. For the lower byte (DQ0 through DQ7) DM refers to LDM and DQS refers to LDQS; and for the upper byte (DQ8 through DQ15) DM refers to UDM and DQS refers to UDQS.

ABSOLUTE MAXIMUM RATINGS*

(Voltages Relative to VSS)

V_{DD} Supply	-1V to +3.6V
$V_{DD}Q$ Supply	-1V to +3.6V
V_{REF} and Inputs	-1V to +3.6V
I/O Pins	-0.5V to $V_{DD}Q$ +0.5V
Operating Temperature, T_A (ambient)	10°C to +70°C
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(For test conditions see note 53)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (For -6A & -75A)	VDD	2.3	2.7	V	41
I/O Supply Voltage (For -6A & -75A)	VDDQ	2.3	2.7	V	41, 44
Supply Voltage (For -5B)	VDD	2.5	2.7	V	41
I/O Supply Voltage (For -5B)	VDDQ	2.5	2.7	V	41, 44
I/O Reference Voltage	VREF	0.49 X VDDQ	0.51 X VDDQ	V	6, 44
I/O Termination Voltage (system)	VTT	VREF – 0.04	VREF + 0.04	V	7, 44
Input High (Logic 1) Voltage	VIH (DC)	VREF + 0.15	VDD + 0.3	V	28
Input Low (Logic 0) Voltage	VIL (DC)	-0.3	VREF – 0.15	V	28
Clock Input Voltage Level; CK and CK#	VIN	-0.3	VDDQ + 0.3	V	
Clock Input Differential Voltage; CK and CK#	VID	0.36	VDDQ + 0.6	V	8
Clock Input Crossing Point Voltage; CK and CK#	VIX	1.15	1.35	V	9
INPUT LEAKAGE CURRENT Any input, 0V ≤ VIN ≤ VDD, VREF pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	II	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	-7	7	µA	
OUTPUT LEVELS: Full drive option - x4 , x8, x16 High Current (VOUT = VDDQ-0.373V, minimum VREF, minimum VTT) Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)	IOH	-16.8	--	mA	37, 39
	IOL	16.8	--	mA	
OUTPUT LEVELS: Reduced drive option - x16 only High Current (VOUT = VDDQ-0.763V, minimum VREF, minimum VTT) Low Current (VOUT = 0.763V, maximum VREF, maximum VTT)	IOHR	-9	--	mA	38, 39
	IOLR	9	--	mA	

AC INPUT OPERATING CONDITIONS

(For test conditions see note 53)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH (AC)	VREF + 0.310	--	V	14, 28, 40
Input Low (Logic 0) Voltage	VIL (AC)	--	VREF – 0.310	V	14, 28, 40
Clock Input Differential Voltage; CK and CK#	VID (AC)	0.7	VDDQ + 0.6	V	8
Clock Input Crossing Point Voltage; CK and CK#	VIX (AC)	0.5 X VDDQ – 0.2	0.5 X VDDQ + 0.2	V	9
I/O Reference Voltage	VREF (AC)	0.49 X VDDQ	0.51 X VDDQ	V	6

CAPACITANCE (x4, x8)

(For test conditions see note 53)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQs, DQS, DM	DCIO	--	0.50	pF	24
Delta Input Capacitance: Command and Address	DCI1	--	0.50	pF	29
Delta Input Capacitance: CK, CK#	DCI2	--	0.25	pF	29
Input/Output Capacitance: DQs, DQS, DM	CIO	4.0	5.0	pF	
Input Capacitance: Command and Address	CI1	2.0	3.0	pF	
Input Capacitance: CK, CK#	CI2	2.0	3.0	pF	
Input Capacitance: CKE	CI3	2.0	3.0	pF	

IDD SPECIFICATIONS AND CONDITIONS (x4, x8)

(For test conditions see note 53)

PARAMETER/CONDITION		SYMBOL	-5B	-6A	-75	UNITS	NOTES
OPERATING CURRENT: One bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;		IDD0	155	135	120	mA	22, 48
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	185	160	135	mA	22, 48
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; tCK = tCK(MIN); CKE=LOW;	Standard 'V' parts	IDD2P	10	10	10	mA	23, 32, 50
	Self Refresh 'R' parts	IDD2P	6	3	5	mA	23, 32, 50
PRECHARGE FLOATING STANDBY CURRENT: CS# = HIGH; All banks idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	55	50	50	mA	51
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	45	35	25	mA	23, 32, 50
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.		IDD3N	60	55	65	mA	22
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	190	170	155	mA	22, 48
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	190	155	130	mA	22
AUTO REFRESH CURRENT	tRC = tRFC (MIN)	IDD5	345	260	260	mA	22, 50
SELF REFRESH CURRENT (Part number 'R' only)		IDD6	6	5	4	mA	11
OPERATING CURRENT: Four bank interleaving READs (BL = 4) with auto precharge, tRC = tRC (MIN); tCK = tRC (MIN); Address and control inputs change only during Active, READ, or WRITE commands.		IDD7	450	400	335	mA	22, 49

CAPACITANCE (x16)

(For test conditions see note 53)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQ0 – DQ7, LDQS, LDM	DC_{IOL}	--	0.50	pF	24
Delta Input/Output Capacitance: DQ8-DQ15, UDQS, UDM	DC_{IOU}	--	0.50	pF	24
Delta Input Capacitance: Command and Address	DC_{I1}	--	0.50	pF	29
Delta Input Capacitance: CK, CK#	DC_{I2}	--	0.25	pF	29
Input/Output Capacitance: DQs, LDQS, UDQS, LDM, UDM	C_{IO}	4.0	5.0	pF	
Input Capacitance: Command and Address	C_{I1}	2.0	3.0	pF	
Input Capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input Capacitance: CKE	C_{I3}	2.0	3.0	pF	

I_{DD} SPECIFICATIONS AND CONDITIONS (x16)

(For test conditions see note 53)

PARAMETER/CONDITION		SYMBOL	-5B	-6A	-75	UNITS	NOTES
OPERATING CURRENT: One bank; Active-Precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;		I_{DD0}	155	135	120	mA	22, 48
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	185	160	145	mA	22, 48
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $^tCK = {}^tCK$(MIN); CKE=LOW;	Standard 'V' parts	I_{DD2P}	10	10	10	mA	23, 32, 50
	Self Refresh 'R' parts	I_{DD2P}	6	3	5	mA	23, 32, 50
PRECHARGE FLOATING STANDBY CURRENT: CS# = HIGH; All banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM		I_{DD2F}	55	55	55	mA	51
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD3P}	45	35	25	mA	23, 32, 50
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank; Active-Precharge; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.		I_{DD3N}	60	65	65	mA	22
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); I_{OUT} = 0Ma		I_{DD4R}	210	190	180	mA	22, 48
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	190	165	155	mA	22
AUTO REFRESH CURRENT	^tRC = tRFC (MIN)	I_{DD5}	345	260	260	mA	22, 50
SELF REFRESH CURRENT (Part number 'R' only)		I_{DD6}	6	5	4	mA	11
OPERATING CURRENT: Four bank interleaving READs (BL = 4) with auto precharge, $^tRC = {}^tRC$ (MIN); $^tCK = {}^tRC$ (MIN); Address and control inputs change only during Active, READ, or WRITE commands.		I_{DD7}	405	400	335	mA	22, 49

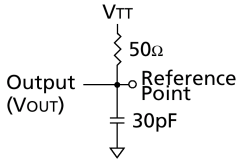
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(For test conditions see note 53)

AC CHARACTERISTICS			-5B		-6A		-75			
PARAMETER		SYMBOL	MIN	MIN	MAX	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#		tAC	-0.70	+0.70	-0.70	+0.70	-0.75	+0.75	ns	
CK high-level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30
CK low-level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30
Clock cycle time	CL = 3	tCK	5.0	7.5					ns	52
	CL = 2.5	tCK			6.0	13	7.5	13	ns	52
DQ and DM input hold time relative to DQS		tDH	0.40		0.45		0.5		ns	26, 31
DQ and DM input setup time relative to DQS		tDS	0.40		0.45		0.5		ns	26, 31
DQ and DM input pulse width (for each input)		tDIPW	1.75		1.75		1.75		ns	31
Access window of DQS from CK/CK#		tDQSCK	-0.60	+0.60	-0.60	+0.60	-0.75	+0.75	ns	
DQS input high pulse width		tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width		tDQSL	0.35		0.35		0.35		tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		tDQSQ		0.40		0.45		0.5	ns	25, 26
Write command to first DQS latching transition		tDQSS	0.72	1.28	0.75	1.25	0.75	1.25	tCK	
DQS falling edge to CK rising – setup time		tDSS	0.2		0.2		0.2		tCK	
DQS falling edge from CK rising – hold time		tDSH	0.2		0.2		0.2		tCK	
Half clock period		tHP	tCH, tCL		tCH, tCL		tCH, tCL		ns	34
Data-out high-impedance window from CK/CK#		tHZ		+0.70		+0.70		+0.75	ns	18
Data-out low-impedance window from CK/CK#		tLZ	-0.70		-0.70		-0.75		ns	18
Address and control input hold time (fast slew rate)		tIH_f	0.6		0.75		.90		ns	14
Address and control input setup time (fast slew rate)		tIS_f	0.6		0.75		.90		ns	14
Address and control input hold time (slow slew rate)		tIH_s	0.7		0.80		1		ns	14
Address and control input setup time (slow slew rate)		tIS_s	0.7		0.80		1		ns	14
LOAD MODE REGISTER command cycle time		tMRD	10		12		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		tQH	tHP – tQHS		tHP – tQHS		tHP – tQHS		ns	25, 26
Data hold skew factor		tQHS		0.5		0.6		0.75	ns	
ACTIVE to READ with Auto precharge command		tRAP	NA		NA		NA		ns	46
ACTIVE to PRECHARGE command		tRAS	40	16,000	42	16,000	45	16,000	ns	35
ACTIVE to ACTIVE/AUTO REFRESH command period		tRC	55		60		65		ns	
AUTO REFRESH command period		tRFC	70		72		75		ns	50
ACTIVE to READ or WRITE delay		tRCD	15		18		20		ns	
PRECHARGE command period		tRP	15		18		20		ns	
DQS read preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	42
DQS read postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE bank *a* to ACTIVE bank *b* command		tRRD	10		12		15		ns	
DQS write preamble		tWPRE	0.25		0.25		0.25		tCK	
DQS write preamble setup time		tWPRES	0		0		0		ns	20, 21
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	19
Write recovery time		tWR	15		15		15		ns	
Internal WRITE to READ command delay		tWTR	2		1		1		tCK	
Data valid output window		na	tQH - tDQSQ		tQH - tDQSQ		tQH - tDQSQ		ns	25
REFRESH to REFRESH command interval		tREFC		70.3		70.3		70.3	µs	23
Average periodic refresh interval		tREFI		7.8		7.8		7.8	µs	23
Terminating voltage delay to Vdd		tVTD	0		0		0		ns	
Exit SELF REFRESH to non-READ command (Part number R only)		tXSNR	75		75		75		ns	
Exit SELF REFRESH to READ command (Part number R only)		tXSRD	200		200		200		tCK	

NOTES

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load: properly initialized, and is averaged at the defined cycle rate.
4. AC timing and I_{DD} tests may use a V_{IL}- to-V_{IH} swing

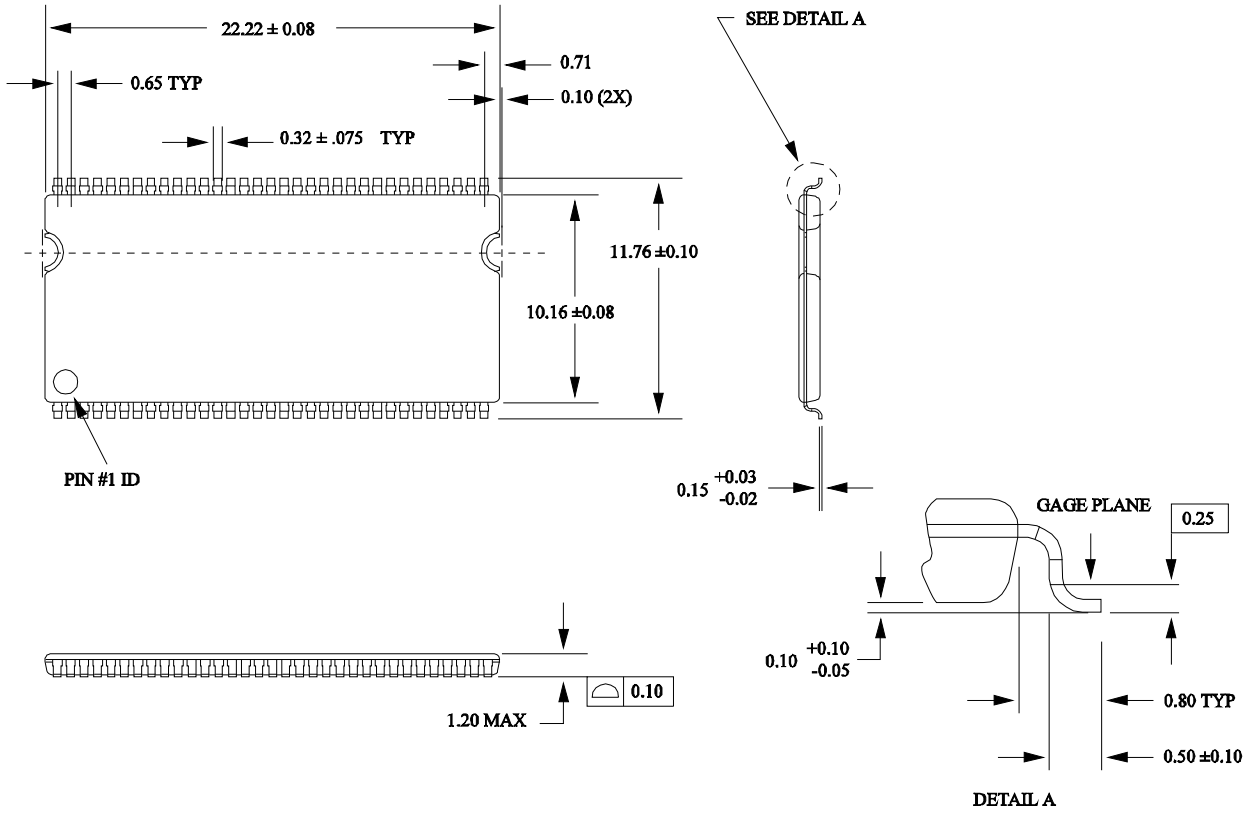


of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The AC and DC input level specifications areas defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
9. The value of V_{IX} is expected to equal V_{DDQ}/2 of the transmitting device and must track variations in the DC level of the same.
10. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2.5 for –65A and –75A (CL=3 for –5B) with the outputs open.
11. Enables on-chip refresh and address counters.
12. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
13. This parameter is sampled. V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V, VREF = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT}(DC) = V_{DDQ}/2, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
14. Command/Address input slew rate = 0.5V/ns. For slew rates of 1V/ns and faster, ^{t}IS and ^{t}IH are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: ^{t}IS have an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. ^{t}IH has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
15. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is VREF.
16. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x V_{DDQ} is recognized as LOW.
17. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
18. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
21. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
22. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
23. The refresh period 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

25. The valid data window is derived by achieving other specifications - ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
26. Referenced to each output group: x4 = DQS with DQ0-DQ3; x8 = DQS with DQ0-DQ7; x16 = LDQS with DQ0-DQ7 and UDQS with DQ8-DQ15.
27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
28. To maintain a valid level, the transitioning edge of the input must:
    a) Sustain a constant slew rate from the Current AC level through to the target AC level, VIL(AC) VIH(AC).
    b) Reach at least the target AC level.
    c) After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
29. The Input capacitance per pin group will not differ by more than this maximum amount for any given device.
30. CK and CK# input slew rate must be $\geq$1V/ns.
31. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
32. VDD must not vary more than 4% if CKE is not active while any bank is active.
33. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
34. ^{t}HP min is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
35. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal precharge command being issued.
36. Applies to x16 only. First DQS (LDQS or UDQS) to transition to last DQ (DQ0-DQ15) to transition valid. Initial JEDEC specifications suggested this to be same as ^{t}DQSQ.
37. Note 37 is not used.
38. Note 38 is not used.
39. Note 39 is not used.
40. VIH overshoot: VIH(MAX) = VDDQ+1.5V for a pulse width $\leq$ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL(MIN) = -1.5V for a pulse width $\leq$ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
41. VDD and VDDQ must track each other.
42. Note 42 is not used.
43. Note 43 is not used.
44. During initialization, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power up, even if VDD /VDDQ are 0 volts, provided a minimum of 42 ohms of series resistance is used between the VTT supply and the input pin.
45. Note 45 is not used.
46. ^{t}RAP $\geq$ ^{t}RCD.
47. Note 47 is not used.
48. Random addressing changing 50% of data changing at every transfer.
49. Random addressing changing 100% of data changing at every transfer.
50. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
51. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is “worst case.”
52. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
53. For -6A & -75A;
    10°C < TA < +70°C; VDD/VDDQ = +2.5V ±0.2V.
    For -5B;
    10°C < TA < +70°C; VDD/VDDQ = +2.6V ±0.1V.

66-Pin Plastic TSOP (400mil)



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical here noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Ball Assignment (Top View) 60-Ball FBGA

x4 (Top View)

1	2	3	4	5	6	7	8	9
VSSQ	NF	VSS		A		VDD	NF	VDDQ
NC	VDDQ	DQ3		B		DQ0	VSSQ	NC
NC	VSSQ	NF		C		NF	VDDQ	NC
NC	VDDQ	DQ2		D		DQ1	VSSQ	NC
NC	VSSQ	DQS		E		NC	VDDQ	NC
VREF	VSS	DM		F		NC	VDD	DNU
	CK	CK#		G		WE#	CAS#	
	A12	CKE		H		RAS#	CS#	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10	
	A6	A5		L		A2	A1	
	A4	VSS		M		VDD	A3	

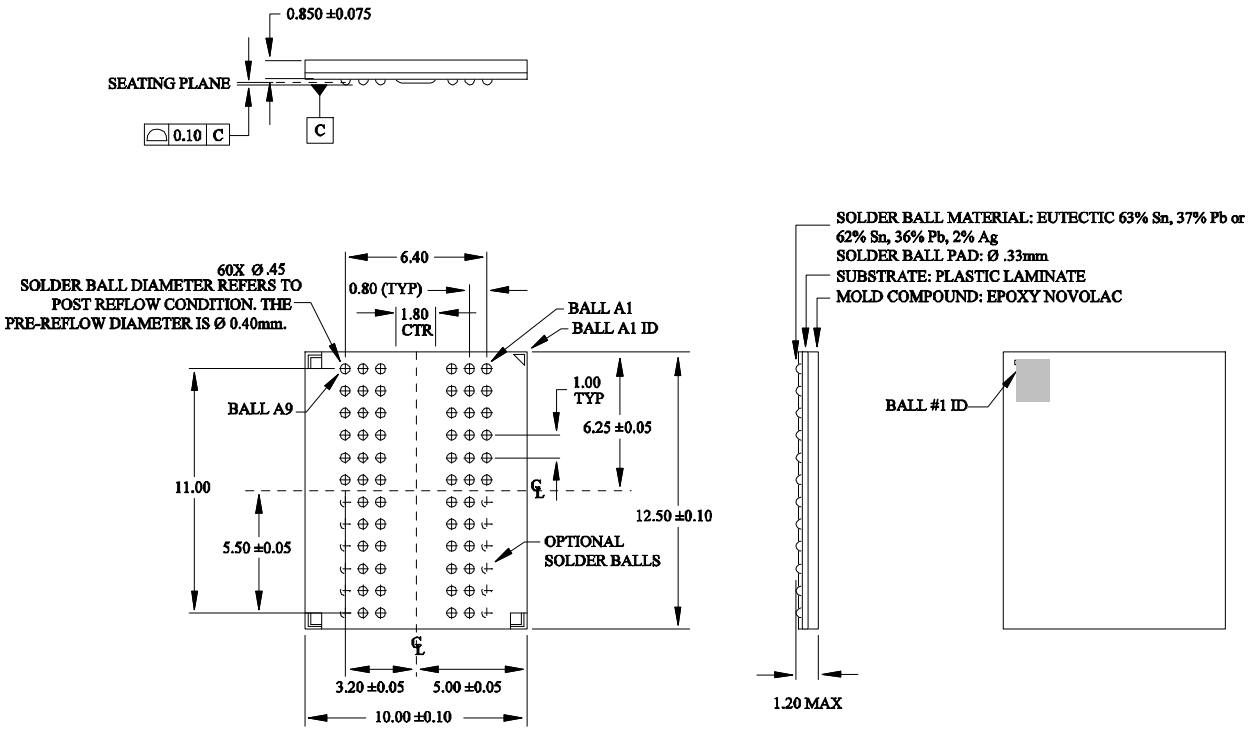
x8 (Top View)

1	2	3	4	5	6	7	8	9
VSSQ	DQ7	VSS		A		VDD	DQ0	VDDQ
NC	VDDQ	DQ6		B		DQ1	VSSQ	NC
NC	VSSQ	DQ5		C		DQ2	VDDQ	NC
NC	VDDQ	DQ4		D		DQ3	VSSQ	NC
NC	VSSQ	DQS		E		NC	VDDQ	NC
VREF	VSS	DM		F		NC	VDD	DNU
	CK	CK#		G		WE#	CAS#	
	A12	CKE		H		RAS#	CS#	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10	
	A6	A5		L		A2	A1	
	A4	VSS		M		VDD	A3	

x16 (Top View)

1	2	3	4	5	6	7	8	9
VSSQ	DQ15	VSS		A		VDD	DQ0	VDDQ
DQ14	VDDQ	DQ13		B		DQ2	VSSQ	DQ1
DQ12	VSSQ	DQ11		C		DQ4	VDDQ	DQ3
DQ10	VDDQ	DQ9		D		DQ6	VSSQ	DQ5
DQ8	VSSQ	UDQS		E		LDQS	VDDQ	DQ7
VREF	VSS	UDM		F		LDM	VDD	DNU
	CK	CK#		G		WE#	CAS#	
	A12	CKE		H		RAS#	CS#	
	A11	A9		J		BA1	BA0	
	A8	A7		K		A0	A10	
	A6	A5		L		A2	A1	
	A4	VSS		M		VDD	A3	

60-Ball FBGA (10mm x 12.5mm)



NOTE:
All dimensions in millimeters.

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512Mb: x4, x8, x16 DDR SDRAM
Rev: 11/24/2004

PART NUMBERS FOR PRODUCT PRIOR TO DECEMBER 2004

OPTIONS	MARKING
• Configuration	
128 Meg x 4 (32 Meg x 4 x 4 banks)	S40128
64 Meg x 8 (16 Meg x 8 x 4 banks)	S80064
32 Meg x 16 (8 Meg x 16 x 4 banks)	S160032
• Voltage and refresh	
2.5V, Auto Refresh	VM
2.5V, Self or Auto Refresh	RM
• Parent Device Configuration	
128 Meg x 4	K
64 Meg x 8	J
32 Meg x 16	L
• Package	
66-pin Plastic TSOP, OCPL (400 mil width, 0.65mm pin pitch)	TW
60-ball (10mm x 12.5mm) FBGA	FN
• Timing – Cycle Time	
5ns @ CL=3 (PC3200 or DDR400B)	-5B
6ns @ CL = 2.5 (PC2700 or DDR333)	-6A
7.5ns @ CL = 2.5 (PC2100 or DDR266)	-75A

(Example part number: S80064VMJTW-6A)

http://www.spectek.com/menus/part_guides.asp