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Laboratory Report

Development specification of the PCB2391 biphase echo canceller

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Abstract

The PCB2391 is a CMOS integrated circuit forming an Integrated Services Digital Network (ISDN) two wire full duplex transmission system.

Keywords
echocanceller
biphase line code
digital subscriber loop

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1. Introduction

1.1. Features

* ISDN basic access transmission over single twisted pair using biphase line code and echo canceller techniques.

* 2B+D transmission capability, for full ISDN access, or B+D.

* 18 dB attenuation at 100 kHz allowed, which is equal to t.b.f. dB signal attenuation.

* Line polarity independent.

* Full activation/deactivation procedures to control power down mode.

* Optimized for connections from PBX, remote multiplexers, or public exchanges to nearby subscribers.

* Full integration of all lower layer 2 bit functions (HDLC) fully in accordance to ECMA-40 to allow cheap applications in TE as well as in linecard applications.

* Low power dissipation, operational < 100 mW
  power down < 40 mW.

* Data/address multiplexed microcontroller interface.

* Maintenance functions implemented.

* Error detection to monitor line transmission performance.

* 2.048 Mbit/s terminal highway interface.

* Synchronisation signal for switched mode power supply to minimize power supply noise.

* Boundary scan test.

1.2. Ordering information

TYPE NUMBER	TEMPERATURE RANGE ^{0}C	PACKAGE
PCB2391	-10 .. 75°C	PLCC 44
PCB2391	-10 .. 75°C	CERDIL 40

1.3. Signal description

1.3.1. PLCC 44 package

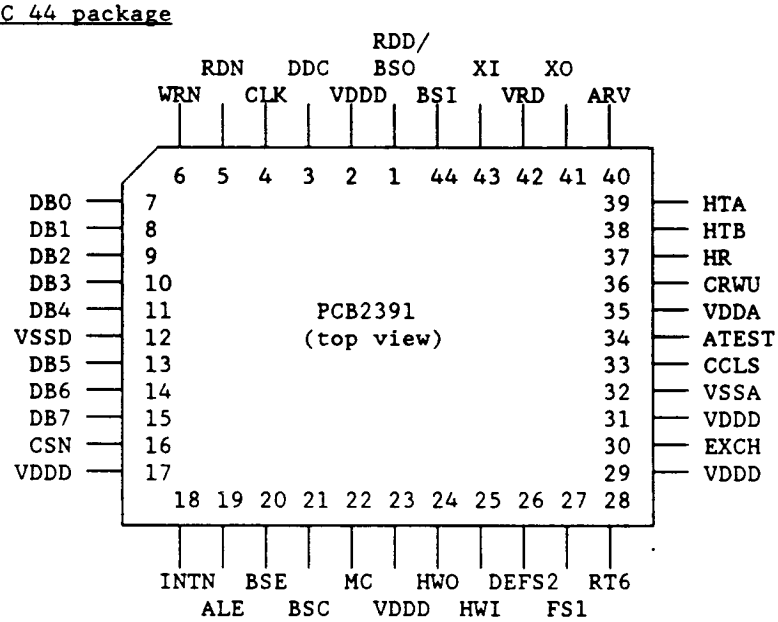


Figure 1.3-1 Pinning diagram (PLCC 44)

1.3.2. CERDIL 40 package

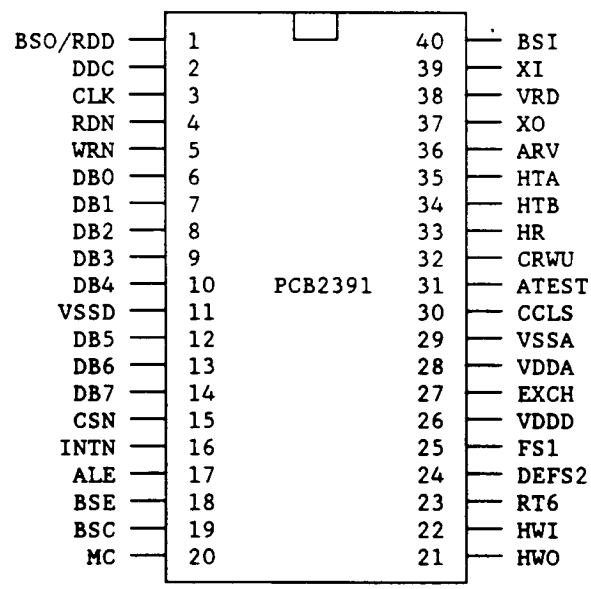


Figure 1.3-2 Pinning diagram (CERDIL 40)

The signals names which are illustrated in figure 1.3-1 and figure 1.3-2 are now described. The pin numbers refer to the PLCC 44 package (figure 1.3-1) and the pin numbers between brackets refer to the DIL 40 package (figure 1.3-2).

1	(1)	RDD/ BSO	Receiver D channel Data (RDD); Output direct D channel access; also used as Boundary Scan Output (BSO). When used as RDD, D-channel data is stable on the leading edge of DDC. When in the boundary scan mode, the data is stable on the leading edge of BSC.
2	(26)	VDDD	Digital power supply connection +5V.
3		DCC	Receiver D channel Clock; timing for RDD (16 kHz) The data on RDD is valid on the leading edge of DCC.
4	(3)	CLK	2.048 MHz master clock input/output. Clock output in subscriber mode. Clock input in exchange mode.
5	(4)	RDN	ReaD Not; signal used to read out the registers of the PCB2391. Active low. Data set on the microcontroller bus by the PCB2391 (when selected by CSN) when RDN is active.
6	(5)	WRN	WRite Not; signal used to write the data on the microcontroller bus into the internal registers of the PCB2391. Active low. Data is latched on the leading edge of WRN.
7	(6)	DB0	Data/Address bit 0.
8	(7)	DB1	Data/Address bit 1.
9	(8)	DB2	Data/Address bit 2.
10	(9)	DB3	Data/Address bit 3.
11	(10)	DB4	Data/Address bit 4.
12	(11)	VSSD	Digital ground.
13	(12)	DB5	Data/Address bit 5.
14	(13)	DB6	Data/Address bit 6.
15	(14)	DB7	Data/Address bit 7.
16	(15)	CSN	Chip Select (active low).
17		VDDD	Digital power supply connection +5V.
18	(16)	INTN	INTerrupt Not; interrupt output signal. Open drain, active low.
19	(17)	ALE	Address Latch Enable; the data available on DB0 and DB1 is

			latched in the internal address register on the trailing edge of the ALE signal.
20	(18)	BSE	Boundary Scan Enable; active high.
21	(19)	BSC	Boundary Scan Clock. In the boundary scan mode, input data on all inputs are latched in on the leading edge of BSC, while all outputs change on the trailing edge of BSC.
22	(20)	MC	Mode control. Together with BSE, MC determines the mode of the PCB2391.
23		VDDD	Digital power supply connection +5V.
24	(21)	HWO	HighWay Output. Output for the B-channel data which is placed in the 2.048 Mbit/s terminal highway timeslot(s) clocked by CLKFS1 and controlled by FS1 and DEFS2.
25	(22)	HWI	HighWay Input. Input for (2*) 64 kbit/s data in the 2.048 Mbit/s highway timeslot(s) (8 bits) timed by CLK (pin 4 (3)) and controlled by FS1 (pin 27 (25)) or DEFS2 (pin 26 (24)).
26	(24)	DEFS2	Data Enable input; Highway timing signal in exchange mode. Frame Select 2 output; Highway timing signal in subscriber mode.
27	(25)	FS1	Frame Select 1; Highway timing signal subscriber mode.
28	(23)	RT6	Synchronisation signal for switched mode power supply (152 kHz).
29		VDDD	Digital power supply connection +5V.
30	(27)	EXCH	Signal which selects the mode of operation of the circuit. EXCH = 0 selects subscriber mode, EXCH = 1 selects exchange mode.
31		VDDD	Digital power supply connection +5V.
32	(29)	VSSA	Analog ground.
33	(30)	CCLS	Capacitor Controlled Level Shifting. The external CLS integration capacitor should be connected to this point.
34	(31)	n.c.	Not connected. Should be left open.
35	(28)	VDDA	Analog power supply connection +5V.
36	(32)	CRWU	Capacitor Receiver Wake Up. The external RWU timing capacitor should be connected to this point.
37	(33)	HR	Hybrid Receiver; input for the receiver section, should be connected to the node of linetransformer and matching resistor

38	(34)	HTB	Hybrid Transmitter B wire; output of the line driver circuit, should be connected to the line transformer.
39	(35)	HTA	Hybrid Transmitter A wire; output of the line driver circuit, should be connected to the matching resistor.
40	(36)	ARV	Analog Reference Voltage 2.5 V; should be decoupled to ground, or connected to external current source.
41	(37)	XO	X-tal Output; connection for the external X-tal circuit (4.096 MHz). Only used in subscriber mode; should be pulled up in exchange mode.
42	(38)	VRD	Control voltage X-tal oscillator; output which should control the series capacitance of the X-tal circuit in subscriber mode; should be floating in exchange mode.
43	(39)	XI	X-tal Input; connection for the external X-tal circuit. Only used in subscriber mode; should be pulled up in exchange mode.
44	(40)	BSI	Boundary Scan Input; data input for boundary scan test.

2. Functional description

The PCB2391 biphase echo canceller is a CMOS IC forming an Integrated Services Digital Network (ISDN) transmission system. It is capable of transferring two 64 kbit/s B channels for encoded voice and/or data plus a 16 kbit/s D channel (for which the PCB2391 performs HDLC bit functions) for signalling and low speed data. These basic access data streams are transmitted in full duplex mode on two wire subscriber line using full echo canceller techniques.

The linecode used is biphase. It has a good timing content and it is insensitive to linear distorsion and reflections.

The PCB2391 can be used in two applications:

-Line termination, at the exchange end of the line.
-Network termination, at the subscribers end of the line.

In the block diagram 2.1-1 illustrating the PCB2391 three interfaces can be destinguished:

*The Terminal Highway (THW) is a PCM highway with a transmission rate of 2.048 Mbit/s consisting of thirty-two 64 kbit/s channels. The THW interface consists of two unidirectional data lines (HWI and HWO), a THW clock line (CLK) and two THW alignment signal lines (FS1 and DEFS2). The terminal highway is described in detail in section 2.4.

*The 8 bit microcontroller bus is a data/address multiplexed microcontroller bus. The microcontroller I/O port performs the interface for the control stages of the PCB2391. The microcontroller interface and the control of the PCB2391 is described in detail in section 2.5.

*The line interface is a two wire proprietary interface. This corresponds to the digital subscriber loop.

The PCB2391 is divided into a number of functional parts depicted in block diagram 2.1-1. A short description of these blocks is given below.

*The Digital Signalling Processor circuit (DSP): It takes care of the transmission and reception of data at bit level. Correction of the received signal for echos and intersymbol interference (ISI) is done with the aid of an adaptive mechanism without any training mechanism. Automatically the DSP adapts to various line characterisics including bridged taps.

This mechanism allows no correlation between transmit- and receive data; for this reason data (de)scramblers with different polynomials in up- and downstream direction are part of the DSP.

*Clock (re)generation (CLOCK): In exchange mode (see also section 2.2) this circuit derives all required clocks from a common, externally generated 2.048 MHz clock. In subscriber mode (see also section 2.2) the internal X-tal based VCXO of the CLOCK circuit generates the required 2.048 MHz clock; it is controlled by the phase detector of the DSP. The phase detector extracts the required control information from the received line signal; in this way the subscriber system is synchronized to the exchange system.

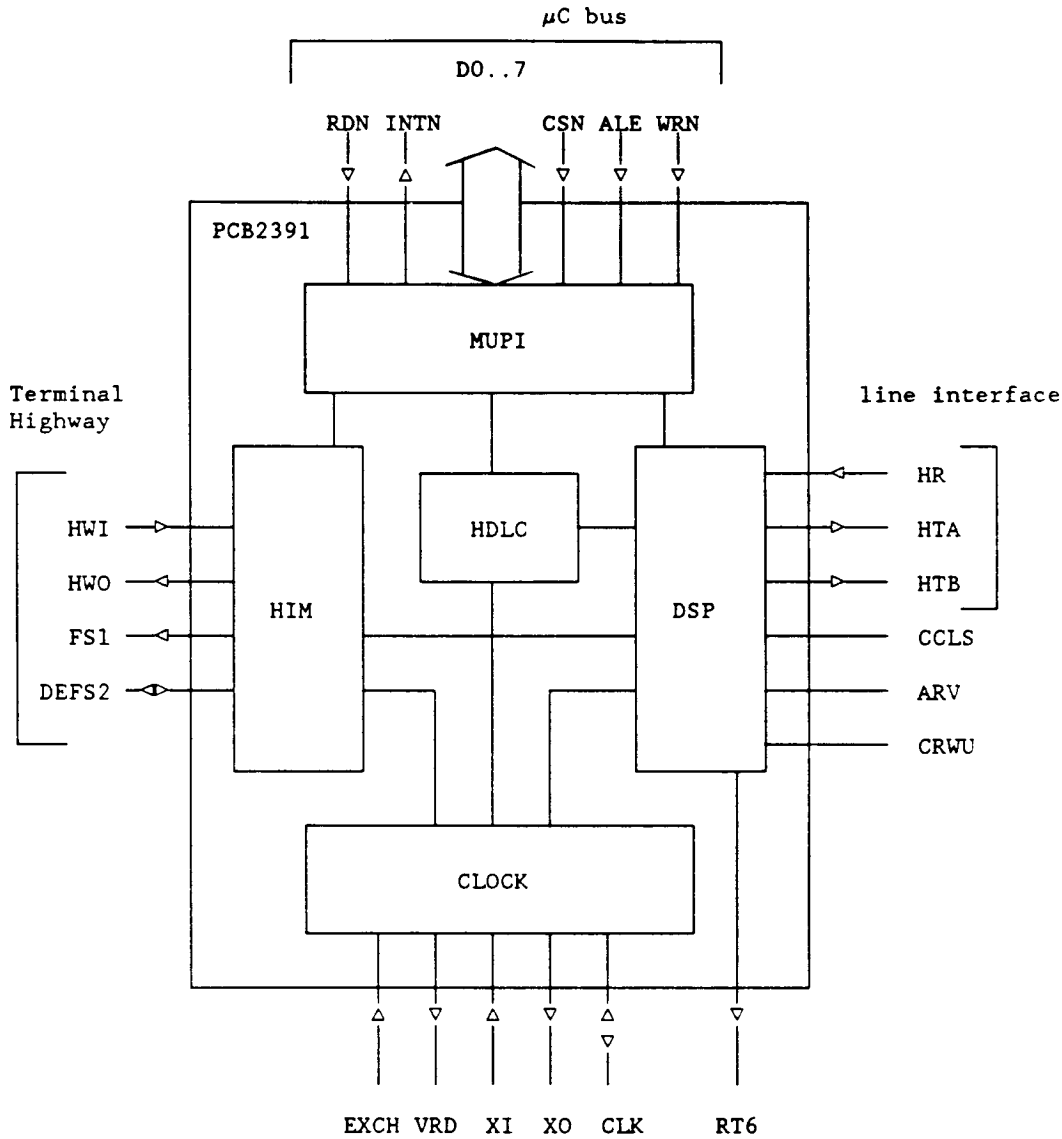


Figure 2.1-1 Block diagram of the PCB2391.

*The microcontroller interface (MUPI) is used for a number of functions:
- control of the transmission system
- status investigation of the transmission system
- access to the HDLC facilities of the D-channel
- control of the HDLC FIFOs
- control of testfacilities: boundary scan test

The design of the micro processor interface allows the use of the PCB2391 both in a 'polled' and an 'interrupt driven' environment.

*The HDLC controller takes care of the layer 2 bit functions (ECMA-40) such as flag generation/detection, zero insertion/deletion and CRC. An HDLC message contains a startflag (8 bit), addressfield (8 or 16 bit) and a controlfield (8 bit) followed by N*8 data bits and a 16 bit frame check sequence; it is terminated by an 8 bit endflag.

The PCB2391 handles the adress-, control- and data fields as transparent data, so they are all passed to the microcontroller. Main characteristics:

- byte oriented
- full duplex
- no restrictions on message length
- separate transmit and receive fifos of 32 bytes each (fifo levels can be guarded by microcontroller)

*The highway interface and maintenance circuit (HIM) performs all interface functions between DSP, MUPI and HDLC controller. The highway interface is also a part of HIM; a number of registers is used to buffer 125 μsec highway and 1 msec line frame structures. HIM uses the DSP circuit as a transparent full duplex data path. In transmit direction HIM assembles the data of B- and D-channels, some system control bits and the output of a frameword generator to data frames; these frames are passed to the DSP as a serial bitstream. The system control bits are part of a register implemented in MUPI; they are used for the remote loop- and activation procedures.

In receive direction HIM receives a serial bitstream from the DSP, takes care of frame alignment, detection of system control bits and demultiplexes the received data to separate B and D channels.

Other functions performed by the HIM are:
- activation/deactivation control and control of remote testloop
- interfacing the B channels to the user system
- transmission line polarity control
- determination of transmission quality by counting the number of frameword errors

2.1. Mode selection

With the mode control input signals MC and BSE the mode of the PCB2391 is set. Table 2.1-1 gives an overview of the modes of the PCB2391.

BSE	MC	mode
0	0	normal mode
0	1	not used
1	0	boundary scan test
1	1	digital outputs high-Z (floating)

Table 2.1-1 Operational modes of the PCB2391.

The boundary scan test is described in more detail in section 2.8.

When the normal mode is selected, the PCB2391 can be used in exchange or subscriber mode. By lead EXCH the exchange or subscriber mode can be selected. In table 2.1-2 an overview is given of the main functions in exchange and subscriber mode.

EXCH	0	1
application	subscriber	exchange
timing	master on U slave on THW	slave on U master on THW
U-interface		
transmit scrambler	$1 + X^{-4} + X^{-9}$	$1 + X^{-3} + X^{-10}$
receive scrambler	$1 + X^{-3} + X^{-10}$	$1 + X^{-4} + X^{-9}$

Table 2.1-2 Functional modes of the PCB2391.

2.2. Clock configuration

In exchange mode the PCB2391 derives all required clocks from a common, externally generated 2.048 MHz clock (the terminal highway clock CLK). The external clock input XI should be tied to Vdd (allowed series resistance 100E .. 10K).

The clock circuit used in the subscriber mode is depicted in figure 2.2-2. It is a voltage controlled crystal oscillator (VCXO) running at a nominal frequency of 4.096 MHz. The frequency of the VCXO controlled by the timing on the U reference point (line interface).

Parameter		
resonance frequency	t.b.f.	MHz
load capacitance (C_L)	t.b.f.	pF
temperature range	t.b.f.	^oC
frequency tolerance	t.b.f.	ppm
resonance resistance (R_r)	t.b.f.	Ω
motional capacitance (C_1)	t.b.f.	fF
static parallel capacitance (C_0)	t.b.f.	pF
inductance	t.b.f.	mH

Table 2.2-1 Quartz crystal parameters.

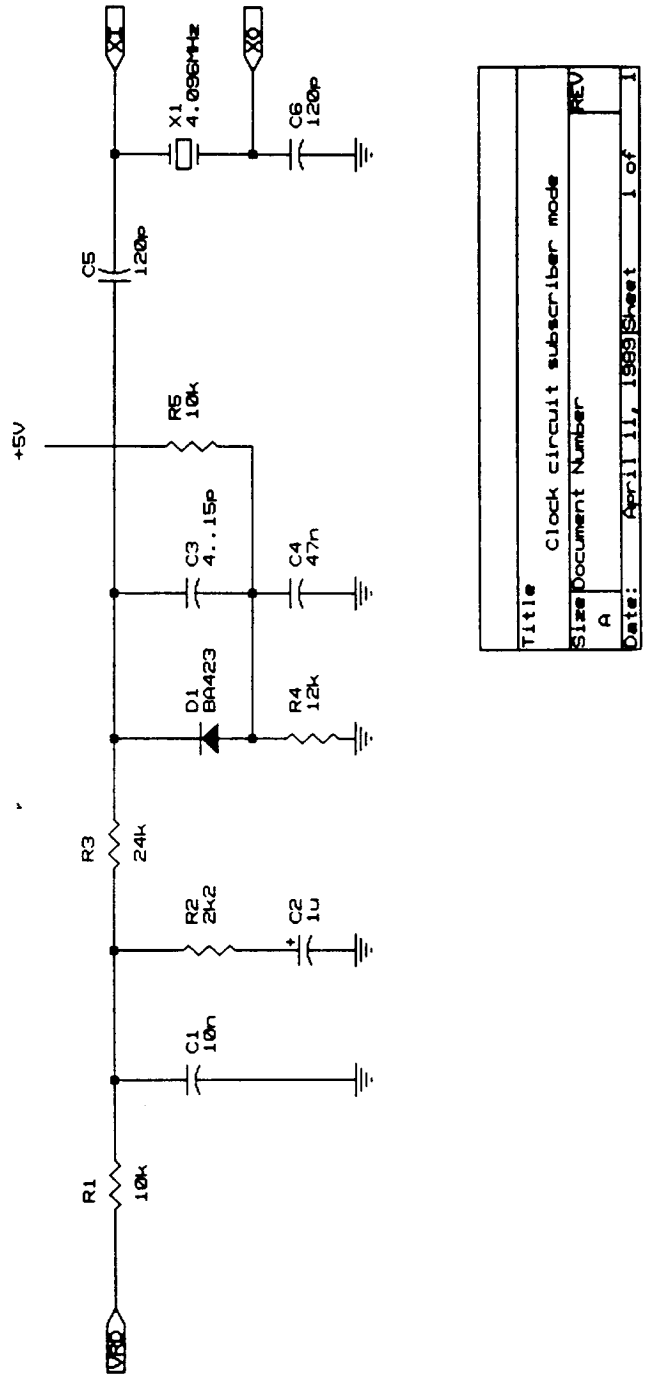


Figure 2.2-2 Clock configuration.

For synchronisation of a switched mode power supply in subscriber mode the RT6 signal is available (not available in DIL package). A bit interval (on the digital subscriber loop) is divided into 16 equal parts named LFR0 to LFRF (hex). The received data is sampled twice in each bit interval: the data is sampled at LFR1, the phase of the received signal is sampled between LFR5 and LFR6. The RT6 signal is in synchronisation with the internal LFR6 timing signal.

2.3. Line interface

The PCB2391 is coupled to the digital subscriber loop via the line interface. The main characteristics at the digital subscriber loop:

line code	: biphase
transmission	: full duplex on 2 wire
line rate	: 152 kbit/s
distance	: 1.8 km (0.4mm with 10dB/km at 100 kHz)
maximum allowed attenuation	: 18 dB at 100 kHz

2.3.1. Line frame format

The transparent data bit rate is 144 kbit/s. For synchronisation and transfer of control and status information an additional 8 kbit/s is added resulting in a line bit rate of 152 kbit/s. This additional capacity is handled by the frameword generator and decoder (within the HIM block).

The frame structure is illustrated in figure 2.3.1-1. It has a 2 msec multiframe structure. The multiframe is divided into an 'odd' and an 'even' 1 msec frame. Each 1 msec frame contains a frameword of 8 bits and 8*(8+8+2) bits of transparent data. The framewords are different for 'even' and 'odd' 1 msec frames. In the 'even' frame the frameword gives the status of the 'Remote Loop Request' bit (see section 2.5.1.1), followed by the sequence '1100100'. In the 'odd' frame the frameword gives the status of the 'Activation Request' bit (see section 2.5.1.1), followed by the sequence '0011011'. The used frameword and frame synchronisation procedure resembles CCITT G732.

To be able to detect an interchange of the A and B wire the 'Remote Loop Request bit in the upstream data should always be 'not active', thus making it impossible for the subscriber to ask for a remote testloop. In the downstream data the 'Remote Loop Request' bit may be 'active' if the 'Activation Request' bit is active. In this way the PCB2391 detects and corrects automatically data transmission/reception for interchanged A and B wires at the subscriber side.

Upstream frames (from subscriber to exchange) are scrambled using the polynomial:

$$X^{-9} + X^{-4} + 1$$

Downstream frames (from exchange to subscriber) are scrambled using the polynomial:

$$X^{-10} + X^{-3} + 1$$

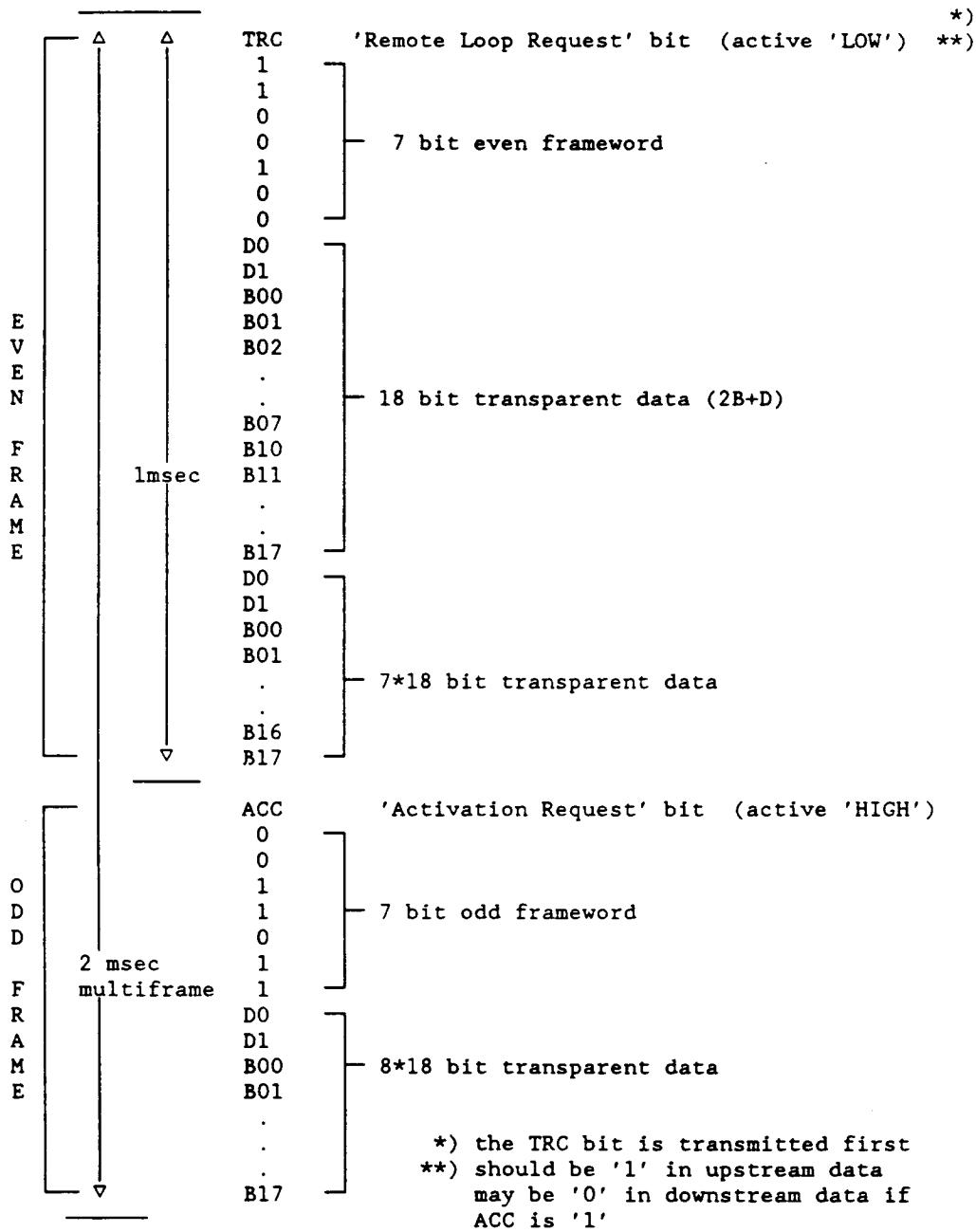


Figure 2.3.1-1 Line frame structure.

2.3.2. Frameword error counter

The frameword error counter can be used to monitor the quality of the transmission channel (received data path only). The 7 bit frameword of a 152 bit line frame always has a fixed contents. A 152 bit line frame takes 1 msec, so there is a 7 kbit/s data stream with known contents.

The frame error counter is an 3 bit counter (0..7) which saturates at 7. The counter is forced to 0 (reset) as long as bit FERCD of register W1 is set '1'. As soon as FERCD is made '0' the counter increments if a false frameword is detected. As soon as 7 is reached the status bit FERCO 'FER Counter Overflow' of register R4 is set. If enabled this will also generate an interrupt.

By measuring the time between start of count (FERCD->0) and counter full (FERCO->1) it is possible to derive an indication for the Bit Error Rate of the transmission channel.

A FER measurement is of no value if the framesynchronisation (SYNS of register R5) is lost during the measurement.

2.3.3. Electrical connection

The PCB2391 is coupled to the line via a transformer and some other passive components. This is illustrated in appendix A for the subscriber and exchange application.

A complete specification of the transformer used to couple the PCB2391 to the transmission line is specified in appendix C.

The signals placed on the line by the PCB2391 are specified in appendix D.

Whereby the following signals are significant:

HTA	Hybrid transmitter A wire; linedriver.
HTB	Hybrid transmitter B wire; linedriver.
HR	Hybrid receiver.

2.4. Terminal highway interface

The Terminal Highway (THW) is a 2.048 Mbit/s five-wire fully duplex PCM highway for 64 kbit/s circuit switched channels. It consists of:

In exchange mode (EXCH='1'):

HWI: Terminal Highway Input
HWO: Terminal Highway Output
CLK: Terminal Highway 2048 kHz clock input
FS1: Terminal Highway slot assignment input
DEFS2: Terminal Highway slot assignment input

In subscriber mode (EXCH='0'):

HWI: Terminal Highway Input
HWO: Terminal Highway Output
CLK: Terminal Highway 2048 kHz clock input
FS1: Terminal Highway slot assignment output
DEFS2: Terminal Highway slot assignment output

It is possible to select B+D or 2B+D operation with the aid of the controlbit 'BBD' of register W1 (see section 2.5.1.1). In B+D operation only one time slot of the terminal highway is used by the PCB2391 (instead of two in 2B+D operation).

2.4.1. Terminal highway desciption in exchange mode

HWO : Output for the 2B part of the 2B+D data link; data on HWO changes on the rising edge of the 2048 KHz clock 'CLK'. The DEFS2 signal aligns this output burst. The DEFS2 signal is also used to enable the tristate HWO output.

HWI : Input for the 2B part of the 2B+D data link; the input is sampled on the falling edge of 'CLK'. The DEFS2 signal should mask this input burst. If B+D is selected then all bits of the B1 channel of the 1·52 kbit/s datastream are made '0'.

DEFS2: Highway frame alignment signal; depends on the status of BBD: the pulse duration of DEFS2 is 8 CLK cycles when BBD = '1' or 16 cycles of CLK when BBD = '1'. The repetition rate of DEFS2 is 125 µsec.

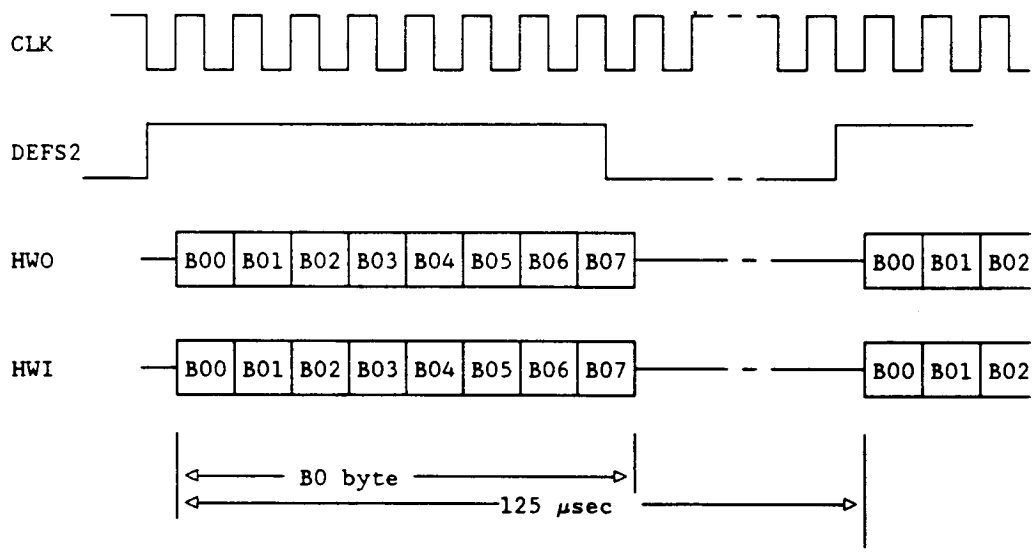


Figure 2.4.1-1 Functional timing THW B+D (BBD=0) exchange mode

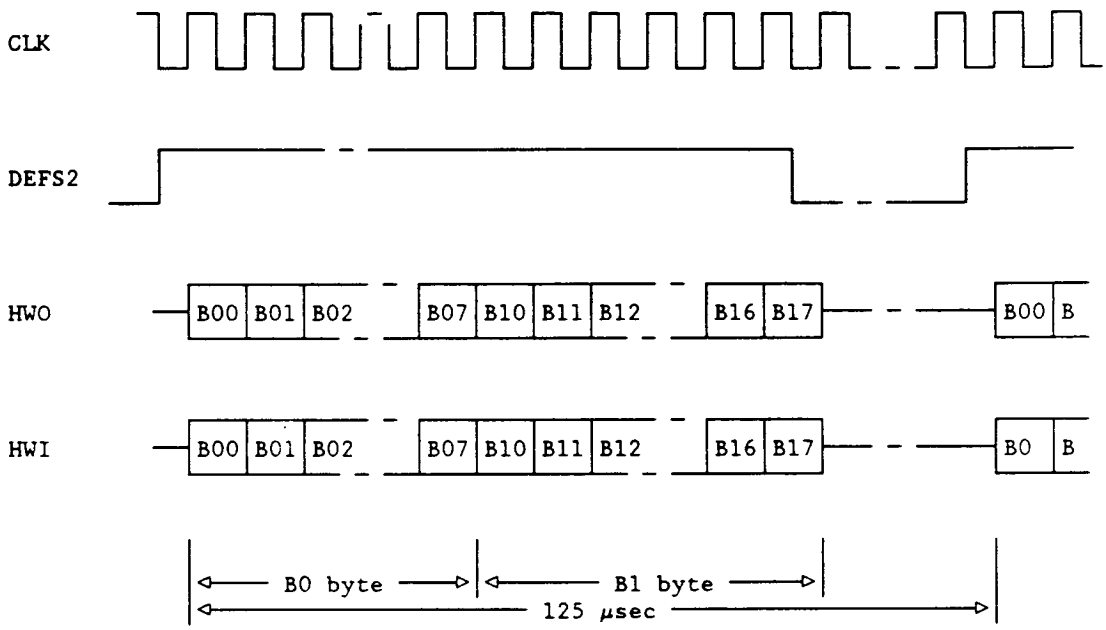


Figure 2.4.1-2 Functional timing THW 2B+D (BBD=1) exchange mode

2.4.2. Terminal highway desciption in subscriber mode

HWO: Output for the 2B part of the 2B+D data link; data on HWO changes on the rising edge of the 2048 kHz clock 'CLK'. The outputs FS1 and DEFS2 indicate the availability of the B0 resp. the B1 channel.

HWI: Input for the 2B part of the 2B+D data link; the input is sampled on the falling edge of the 2048 kHz clock. FS1 masks the B0 channel; DEFS2 masks the B1 channel.

FS1 and DEFS2 are frame alignment signals. Each signal has a duration of 8 periods of 'CLK' and a repetition rate of 125 µsec.

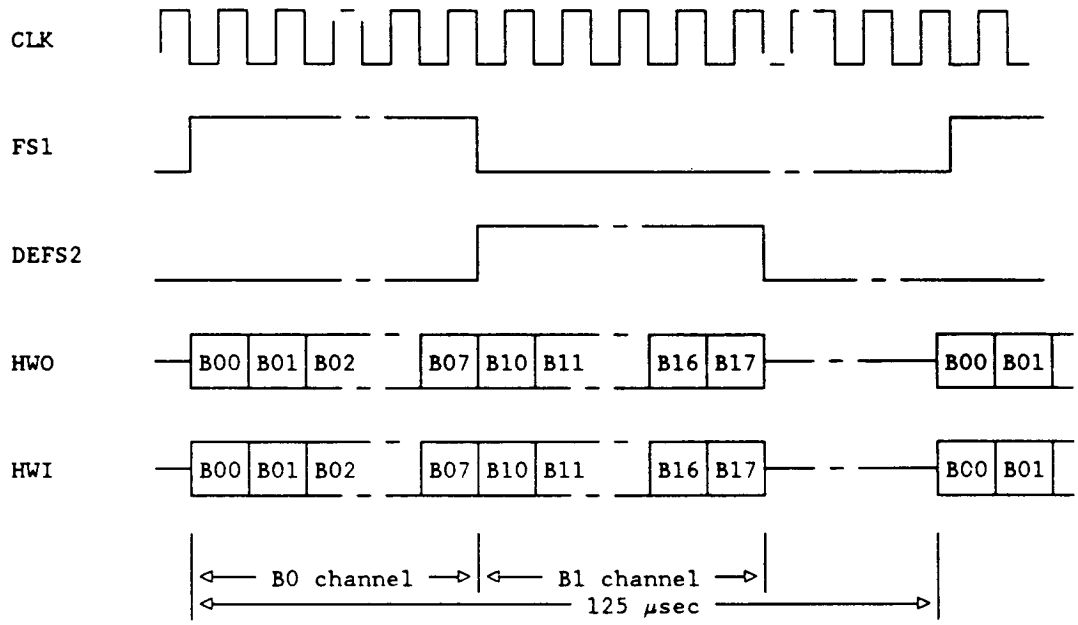


Figure 2.4.2-1 Functional timing THW interface subsc iber mode

2.5. Microcontroller interface

The PCB2391 is fully controllable via the 8-bit microcontroller bus. The bus consists of:

* 8 data/address multiplexed I/O lines (DB7 to DB0)
* A read enable input (RDN)
* A write enable input (WRN)
* An address latch enable input (ALE)
* A chip select input (CSN)
* An interrupt output (INTN)

On the trailing edge of ALE, data on the DB7-DB0 I/O port is latched into the address latch. One of the three write registers or one of the four read registers may be selected (see table 2.5-1). When RDN is LOW and CSN is LOW the PCB2391 writes the data-byte from the selected read register to the data-bus I/O port. On the leading edge of WRN (CSN is LOW), the data-byte from the data-bus I/O port is written into the addressed write register.

It is allowed to follow one ALE pulse by more then one read- or write cycle on the same internal PCB2391 address; this may be useful for writing or reading multiple data bytes to or from the HDLC FIFOs.

The PCB2391 has 3 write- (W1..W3) and 4 read- (R4..R7) registers. These registers are addressed with the data on DB0..DB2 on the trailing edge of ALE.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	address	write reg	read reg
X	X	X	X	X	0	0	1	1	W1	-
X	X	X	X	X	0	1	0	2	W2	-
X	X	X	X	X	0	1	1	3	W3	-
X	X	X	X	X	1	0	0	4	-	R4
X	X	X	X	X	1	0	1	5	-	R5
X	X	X	X	X	1	1	0	6	-	R6
X	X	X	X	X	1	1	1	7	-	R7

Table 2.5-1 Register addresses

2.5.1. Write registers

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W1	TRC	TL	ACC	BBD	FERCD	APOE	TRES	RRES
W2	TBEIE	TBAEIE	PHU	RIE	FERCOIE	SYNCIE	COVFLIE	TRRACIE
W3	D7	D6	D5	D4	D3	D2	D1	D0

Table 2.5.1-1 Bit assignment; register W0, W1, W2 and W3.

2.5.1.1. Register W1

bit TRC: Test Remote Command. The test remote command activates a testloop at the far-end PCB2391. When TRC='1' this testloop is activated. It is only allowed to activate the remote testloop (and thus make TRC '1') in the exchange mode (see also section 2.3.1) and the ACC bit should be always '1' if TRC='1'. It is also not possible to make a remote testloop if the subscriber or the exchange is in local testloop condition (so when TRC is '1', at the exchange and subscriber bit TL has to be '0').

The remote testloop is illustrated in figure 2.5.1.1-1.

Switching from normal operation to a remote testloop and back will cause a temporary loss of frame synchronisation at the initiator. During this switch-over procedure errors will occur on the terminal highway and

D-channel during max. 20 msec.

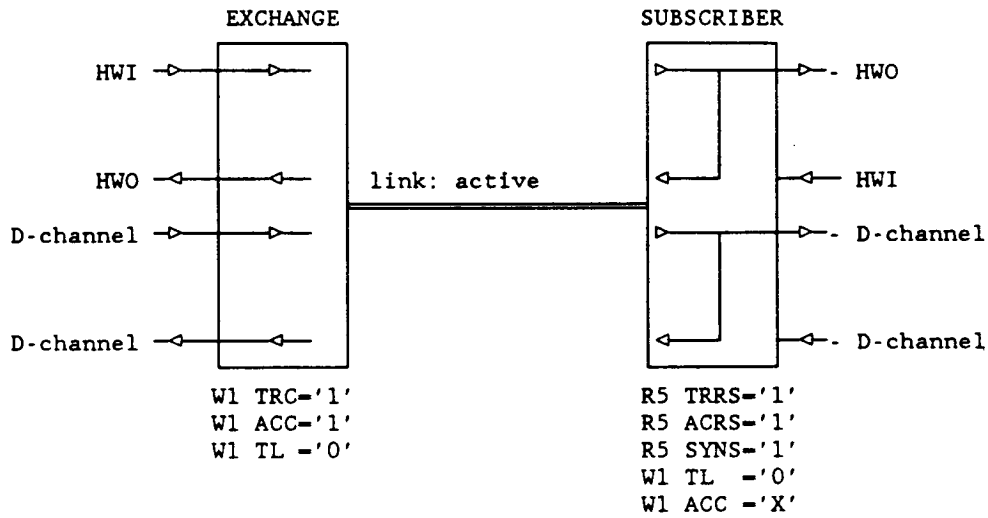


Figure 2.5.1.1-1 Remote testloop

bit TL: Test Local. It activates a local testloop as close to the line interface as possible. When TL= '1' the local testloop is activated. The local testloop is illustrated in figure 2.5.1.1-2.

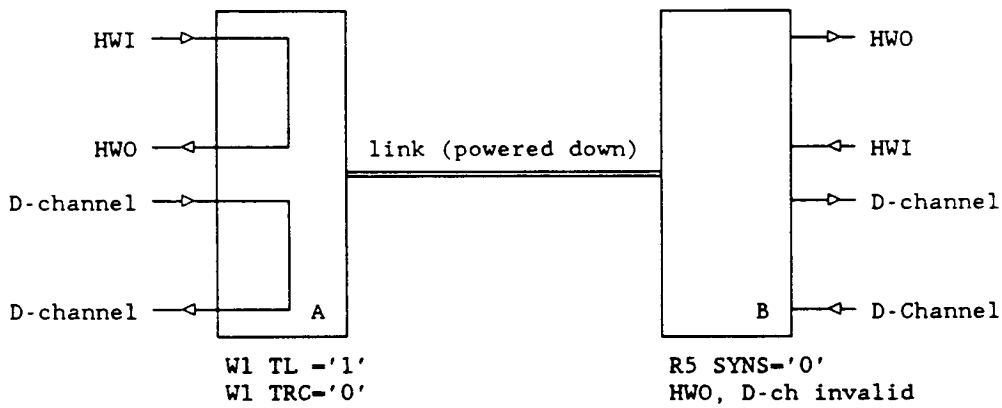


Figure 2.5.1.1-2 Local testloop.

The local testloop is activated if bit TL='1' and TRC='0' is written to register W1 (Local testloop condition inhibits a possible remote loop request from the far end). In this local test loop the PCB2391 makes an internal loop at 152 kbit/s frame level; this means that the B0, B1 and D-channels are looped back. The bits ACC and TRC of register W1 are looped back to status register R5 bits ACR and TRR.

Switching from normal operation to a local testloop will cause a temporary loss of frame synchronisation. During this switch-over procedure errors will occur on the terminal highway and D-channel during max. 20 msec. Changing from local loop to normal operation causes a temporary synchronisation loss of 20..500 msec. To prevent EC overflow (register R5 bit COVFL) interrupts during local loop it is advised do disable these interrupts.

The line driver is powered down during the Local Testloop.

Note: B-channel data can be disturbed if directly after power-up the local loop is initiated; this occurs only if the specified initialisation procedure described in appendix B is not used.

bit ACC: ACtivation Command. It is used for a activation/deactivation procedure (power down) (see section 2.7). If this procedure is not used then ACC should be set to '1'.

bit BBD: select 2B+D mode; BBD is used to select the number of active B-channels (64 kbit/s); only one B-channel (FS1 pulse = B0) is active if the BBD bit is 0. Both B channels are active if BBD=1; in subscriber mode BBD should be '1'.

bit FERCD: Frameword ERror Counter Disable. With this bit the Frameword ERror (FER) counter can be reset and disabled. The FER counter is disabled if FERCD = '1'. For a description of the frame error counter see section 2.3.2.

bit APOE: Automatic Power On Enable. Bit APOE is intended for the activation/deactivation procedure. It is in combination with the Receiver Wake Up (RWU) signal an enable for the Power Up signal. The RWU signal is generated by an internal line activity detector. The use of APOE and ACC is described at the activation/deactivation procedure in section 2.7.

If this procedure is not used then APOE should be set to '1'.

bit TRES: HDLC transmitter reset command. The reset command aborts a message during transmission, clears the HDLC transmit fifo and the HDLC transmitter transmits the idle/abort sequence. See also section 2.6 for a detailed description of the HDLC transmitter.

bit RRES: HDLC receiver reset command. The Receiver RESet command clears possible error conditions, clears the HDLC receiver fifo, resets R6, and changes the HDLC receiver status to hunt mode. In hunt mode the receiver waits for a startflag. If a Receiver RESet command is given after the receiver logic detected a startflag and before the corresponding endflag then that endflag will be interpreted as startflag; a '1111..' idle pattern causes a 'receiver abort sequence detected' error condition which requires a second RRES command.

2.5.1.2. Register W2

bit TBEIE: HDLC transmit buffer empty interrupt enable. When this bit is made '1' the PCB2391 generates an interrupt when bit TBE of register R4 is set to '1'.

bit TBAEIE: HDLC transmit buffer almost empty interrupt enable. When this bit is made '1', the PCB2391 generates an interrupt when bit TBAE of register R4 is set to '1'.

bit PHU: PHase detector Unlock. When this bit is '1' the phase detector of the DSP receiver is unlocked. This bit should be '0' in subscriber mode. In exchange mode it is not possible to adjust the master clock; for this reason it is necessary to enable the receiver phase detector to make discrete steps of 1/16 bit interval. This step mechanism is enabled as long as PHU (PHase detector Unlock) is '1'. The microcontroller should set PHU to '1' as soon as in register R5 SYNS=0 is detected. The microcontroller should write set PHU to '0' as soon as in register R5 ACRS=1 is detected.

bit RIE: HDLC receiver interrupts enable. When this bit is set to '1' an interrupt is generated by the PCB2391 when bit RMC, RE0 and/or RE1 (of register R4) becomes '1'.

bit FERCOIE: Frameword ERror Counter Overflow interrupt enable. When this bit is set to '1', an interrupt is generated by the PCB2391 when bit FERCO of register R4 becomes '1'.

bit SYNCIE: frame synchronisation indication interrupt enable. When bit SYNCIE is set to '1' an interrupt is generated when bit SYNA of register R5 becomes '1'.

bit COVFLIE: echo canceller overflow interrupt enable. When this bit is set to '1' the PCB2391 generates an interrupt when bit COA of register R5 becomes '1'.

bit TRRACIE: interrupt on remote loop command or activation request command. When this bit is set '1', the PCB2391 generates an interrupt when bit ACRS or TRRS of register R5 is set to '1'.

2.5.1.3. Register W3

Via this register, a character can be placed in the HDLC transmitter FIFO. The bit D0 of the character is transmitted first, bit D7 is transmitted last.

2.5.2. Read registers

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R4	IAR5	FERCO	RBAF	RE1	RE0	RMC	TBAE	TBE
R5	TRRA	ACRA	COA	SYNA	TRRS	ACRS	COS	SYNS
R6	-	RA	B5	B4	B3	B2	B1	B0
R7	D7	D6	D5	D4	D3	D2	D1	D0

Table 2.5.2-1 Bit assignments; register R4, R5, R6 and R7.

2.5.2.1. Register R4

bit IAR5: interrupt source in register R5. When this bit is set '1', the source of the interrupt can be found in register R5.

bit FERCO: frameword error counter overflow. The frameword error counter is an 8 counter (0..7) which blocks at count 7. The counter is forced to count 0 (reset) as long as FERCD='1' (see register W1). The counter increments if a false frameword is detected and FERCD='0'; as soon as count 7 is reached the bit FERCO is set. If enabled this will also generate an interrupt.

bit RBAF: HDLC Receiver buffer almost full. Bit RBAF is set '1' if the HDLC receiver buffer contains more than 15 data bytes.

bit RE0 and RE1: These bits contain coded error information if a HDLC message is received containing errors or if FIFO overflow occurs. After an error condition the receiver blocks. It can start receiving again after a receiver reset command is given.

RE1	RE0	HDLC Receiver Error
0	0	no error
0	1	HDLC Rec CRC error
1	0	HDLC Rec Fifo Overflow
1	1	HDLC Rec Abort Sequence Received

bit RMC: Receiver Message Complete. The receiver fifo contains a complete message with correct CRC, or the last part of a message with correct CRC. RMC changes to '0' as soon as the complete message is read from the fifo, or because of a Receiver RESet command (RRES).

TBAE: HDLC Transmit Buffer almost empty status bit. If this bit is '1' it indicates that the HDLC transmit buffer is almost empty. The transmit buffer contains between 1 and 16 data bytes.

TBE: status HDLC Transmit Buffer Empty. If this bit is '1' the HDLC transmit buffer is empty.

2.5.2.2. Register R5

Register R5 is used to reflect the status of the transmission system. The register is split up in status- and activity bits for the same functions. The status bits are used to indicate the actual status of a transmission system function. An activity bit is set if a status change of the concerning function occurs.

In Power Down mode the contents of this register is not valid. All activity bits are reset at the end of a register R5 read cycle.

bit TRRA: test remote request activity;

bit TRRS: test remote request status;

The TRR bit indicates the condition of the TRC bit of the received frameword. In local testloop the received frameword is identical to the own transmitted frameword.

The TRR = '1' condition is achieved as soon as 4 succeeding even framewords with the TRC bit is '0' are received (the even frameword repetition rate is 2 msec.). TRR is reset to '0' after 2 succeeding framewords with the TRC bit is '1' are received or if frame synchronisation is lost (bit SYNS = '0').

bit ACRA: activation request activity;
bit ACRS: activation request status;

The ACR bit indicates the condition of the ACC bit of the received frameword. In Local testloop the received frameword is identical to the own transmitted. The ACR = '1' condition is achieved as soon as 3 succeeding odd framewords with the ACC bit set to '1' are received (the odd frameword repetition rate is 2 msec.). ACR is reset to '0' after 3 succeeding framewords with the ACC bit is '0' are received or if framesync is lost (bit SYNS = '0').

bit COA: canceller overflow activity;
bit COS: canceller overflow status;

This bit indicates whether the EC , which is part of the DSP, is within its range. Normally EC overflow is only allowed during convergention or if no line is connected. Canceller overflow can be caused by extreme mismatches or if no line is connected.

bit SYNA: receiver frame synchronisation activity;
bit SYNS: receiver frame synchronisation status;

The SYNS bit indicates the condition of the frame synchronisation circuit. The circuit hunts for framewords in the received descrambled datastream.

The synchronisation condition is achieved as soon as 4 succeeding correct framewords are detected. Synchronisation is lost as soon as 4 succeeding faulty framewords are detected. The frameword repetition rate is 1 msec.

Frame synchronisation can only occur if the DSP is synchronised at bit level, so after convergence of the EC.

2.5.2.3. Register R6

bit RA: Receiver Activity. This bit is set to '1' when an activity is detected in the HDLC receiver. For the use of this bit is referred to appendix E.

Bit B0..B5: The bits indicate the number of bytes in HDLC receiver FIFO. The FIFO can contain between 0 (000000) and 32 (100000) bytes.

2.5.2.4. Register R7

Via this register, a character can be read out of the HDLC receiver FIFO.

2.6. HDLC controller

The HDLC controller handles the low layer 2 bit functions for the 16 kbit/s D-channel fully in accordance to ECMA-40. It is byte oriented, functions full duplex, has no restrictions on message length. Both transmitter and receiver have a 32 bytes fifo each.

A HDLC message contains an 8 bit startflag, a N*8 bit addressfield, and an 8 bit controlfield followed by M*8 data bits and a 16 bit frame check sequence (CRC polynome $X^{16} + X^{12} + X^5 + 1$), it is terminated by an 8 bit endflag.

The PCB2391 handles the adress-, control- and datafields as transparent data, so they are all passed to the microcontroller.

Note: The bitsequences of start- and endflag are exactly the same, so there is no difference between them. For clarity reasons the terms start- and endflag are used, but remember: the receiver logic sees no difference, the meaning of a flag is dictated by the state of the receiver control logic.

2.6.1. HDLC transmitter

The HDLC transmitter has a 32 byte transmit buffer (fifo). Microcontroller access to this fifo is possible via Register W3.

It is possible to reset this fifo with the Transmitter RESet commandbit (TRES) of register W1 (this command is volatile, so it is not necessary to reset TRES). The command is also used to abort a message during transmission. It is necessary to give this TRES command twice.

After a TRES command the transmitter changes directly to the mode which it generates the '1111...' idle pattern/abort sequence. This sequence is directly aborted and succeeded by a startflag '01111110' after a byte is written into the Tx fifo. For this reason it is advised to wait 3 msec after the TRES command before a data byte is written into register R3.

If the TRES command is given while the Tx fifo is not empty then the command will result in an Transmit Buffer Empty (TBE) interrupt (see register R4) if this interrupt is enabled. When this interrupt is disabled the TBE activity will be stored in an internal register (activity checker) which generates an TBE interrupt as soon as this interrupt is enabled, even if the interrupt cause has disappeared.

When the TRES command is given during the transmission of an endflag then that flag is changed to the abort sequence.

If a TRES command is given immediately after a TBE '0' to '1' status change then it can result in the abortion of the previously sent message if the CRC

and endflag of that message are not completely transmitted. If at that moment a next message was loaded into the fifo both messages will be cleared!

The micocontroller can read out the status of the transmitter buffer by bits 'TBAE' and 'TBE'of register R4. TBAE is '1' indicates that the transmit buffer is almost empty (contains 0 < bytes < 16). TBE is '1' indicates that the transmit buffer is empty.

TBAE is intended for usage with messages which do not fit in the Tx buffer; it is possible to write again 16 bytes of a message in the Tx buffer as soon as TBAE changes to '1'. TBAE changes to '0' as soon as the fifo is empty, or if the number of bytes in the fifo becomes more then 16.

Bit TBE changes to '1' as soon as the last byte is read from the transmit fifo. At that moment the transmitter starts with sending that last byte, followed by CRC and endflag. Total 4 bytes, so the transmitter is still busy during 2 msec.

It is allowed to write a new message in the Tx fifo as soon as the TBE bit has changed from '0' to '1'.

If one or more bytes are written in the fifo before the transmission of the previous endflag is completed then a single '1' is inserted between endflag and startflag; else the endflag is followed by the idle pattern '1111...'.

A '0' to '1' status change of TBE and/or TBAE generates an interrupt if enabled with the corresponding bits of interrupt enable register W2. This will also occur after a TRES command.

The INTN pin will remain low until register R4 is read by the micro-controller. The microcontroller does not change the status by reading the interrupt cause.

2.6.2. HDLC Receiver

The HDLC receiver has a 32 byte receive buffer (fifo). Microcontroller access to this buffer is possible via register R7. The number of bytes that are available in the receive fifo is given bit B0..B5 of register R6. The buffer can contain one single message, or a part of a message at a time.

The Receiver RESet command (bit RRES of register W1) clears possible error conditions, clears the receiver fifo, resets register R6 and changes the HDLC receiver status to hunt mode. In hunt mode the receiver waits for a startflag. The sequence '01111110....' is used as start- and endflag. The receiver can not handle shared start- and endflags.

If a receiver reset command is given after the receiver logic detected a startflag and before the corresponding endflag then that endflag will be interpreted as startflag; a '1111..' idle pattern (Both '1111.....' as '01111110....' are allowed as idle pattern) causes a 'receiver abort sequence detected' error condition which requires a second RRES command.

If a new startflag is recognised while the buffer is not empty (register R6

bit R0..R5>0) or if a not yet cleared receiver error condition exists then the new message is ignored.

It is not allowed to read all available bytes from the receive fifo (register R7). At least 1 byte should always remain in the fifo. Only after a 'RMC' condition (receiver message complete) it is allowed to read all bytes.

A '0' to '1' status change of the Receive buffer Almost Full (RBAF) bit (register R4) generates an interrupt if enabled with bit RBAFIE of interrupt enable register W2. If receiver interrupts are disabled the interrupt will occur as soon as these interrupts are enabled, even if the RRES command is given before the enabling of the receiver interrupts.

Under certain conditions interrupts will be generated without an in R4/R5 visible reason (In register R6 bit RA is set). These interrupts should be responded with an HDLC Receiver RESet command to prevent a HDLC receiver hangup (see also appendix E).

The HDLC receiver input is NOT gated with the lineframe synchronisation condition. This can cause a lot of interrupt conditions caused by imitated framewords and buffer overflow during loss of lineframe synchronisation. For this reason it is advised to disable all HDLC receiver interrupts while SYNS of register R5 is '0'. It is advised to reset the HDLC receiver and enable the interrupts as soon as bit ACRS of register R5 changes to '1'.

2.7. Activation/deactivation

The user procedures for the transmission system (activation, testloops) and the commands for the HDLC transmitter and receiver are described in this section.

In the PCB2391 power down facilities are implemented: in local testloop the linedriver is inhibited and if not in local testloop it is possible to inhibit the linedriver and the main part of the HDLC, HIM and DSP logic.

If not in local testloop the power down condition of the circuit is controlled with the aid of the activation/deactivation procedure. This procedure makes use of some hardware facilities of the PCB2391 and requires a microcontroller for mainly timing and control functions.

In section 2.7.1 and 2.7.2 the state diagrams of the activation/deactivation procedure at exchange and subscriber are depicted.

The activation procedure allows both exchange and subscriber as initiator, the deactivation procedure allows only the exchange as initiator. The subscriber should ask the exchange at a higher level for a deactivation if the subscriber desires to deactivate.

The next signals are used for the activation/deactivation procedures and power down control:

-The ACC bit of the maintenance channel (see section 2.3.1) is used to communicate with the far-end PCB2391 because the (de)activation procedure

affects both the far- and near-end PCB2391.

-ACC, ACtivation Command, enables the transmit driver and the logic of HIM and EC. ACC can be set/reset via the register W1. The status of the ACC bit is also sent via the maintenance channel field 'ACC' to the far-end PCB2391. The far-end PCB2391 places the received 'ACC' field in the 'ACRS' bit of register R5.

-APOE, Automatic Power On Enable, is logical ANDed with the Receiver Wake Up (RWU) signal and is used as a second enable for linedriver and the main logic of HDLC, HIM and EC. APOE can be set via the register W1.

-ACRS, ACtivation Request Status, reflects the status of the received 'ACC' field. The microcontroller can read this bit in register R5. One or more status changes of the ACRS bit between 2 read cycles set the ACRA, ACtivation Request Activity bit of register R5. This causes an interrupt if the TRRAC bit of register W2 is set.

-SYNS, SYNchronisation Status, reflects the status of the internal frame synchronisation circuit. The system should synchronise at lineframelevel after power up. The microcontroller can read this bit in register R5; one or more status changes of the SYNS bit between 2 readcycles set the SYNA, SYNchronisation Activity bit of register R5. This causes an interrupt if the SYNC bit of register W2 is set.

-RWU, Receiver Wake Up, is the output signal of the internal line activity detector; the line activity detector is activated if the received linesignal exceeds a certain level during a defined time. It also activates on the signal of the own linedriver. For this reason it is necessary to disable the linedriver with both ACC=0 and APOE=0 to let discharge the in the line activity detector used capacitor. The RWU signal is not available for the microcontroller.

-TRC, Test Remote command. With this bit the remote testloop can be initiated by the exchange. By making this bit '1' the TRC bit in the line frame is made active.

-TRRS, Test Remote Request Status. This bit indicates a request to switch the subscriber to the remote testloop. This bit reflects the status of the TRC bit in the received line frame.

It is preferred to have a microcontroller response time from event to action below 20 msec. If this time is occasionally exceeded it will cause a reduced performance on the time 'start activation proc - link available'. All timer functions should be performed by the microcontroller. The required accuracy of timers +10/-10 msec. Enlarged tolerances cause reduced performance.

During convergention of the EC (part of the DSP block) unexpected transitions can occur on ACR, TRR and SYNS; software integration of the status of these bits is advised.

Note: as soon as the system is switched to power down mode the internal clocks are frozen. As a result the contents of all read registers is also frozen. The same situation can occur after power-up, in that case the info of the read registers is invalid until the initalisation procedure described in appendix B is executed.

In table 2.7-1 the condition of outputs at power down, local loop and normal operation is depicted.

Pin	power down	local loop	normal	remarks
RDD	-	+	+	
DDC	-	+	+	
CLK	+	+	+	
INTN	+	+	+	
HWO	+	+	+	
DEFS2	+	+	+	subscriber mode
FS1	+	+	+	subscriber mode
RT6	-	+	+	
HTA	2.5 V	+	+	
HTB	2.5 V	+	+	
XO	+	+	+	

+ = active
- = not active (0, 1, or high-Z)

Table 2.7-1 State of the signals in the various modes.

The state diagrams of the activation/deactivation procedure are given in figure 2.7.1-1 and 2.7.2-2. The legend to the diagrams and the description of the states is given in sections 2.7.1 and 2.7.2.

The given state diagrams deal with the next cases:

- activation by exchange
- activation by subscriber
- simultaneous activation by exchange and subscriber
- illegal activation caused by line disturbance
- deactivation by exchange
- out of service, no line

2.7.1. Activation/deactivation at the exchange

The state diagrams of the activation/deactivation procedure at the exchange is illustrated in figure 2.7.1-1. The legend to the figure and the description of the states is given in this section.

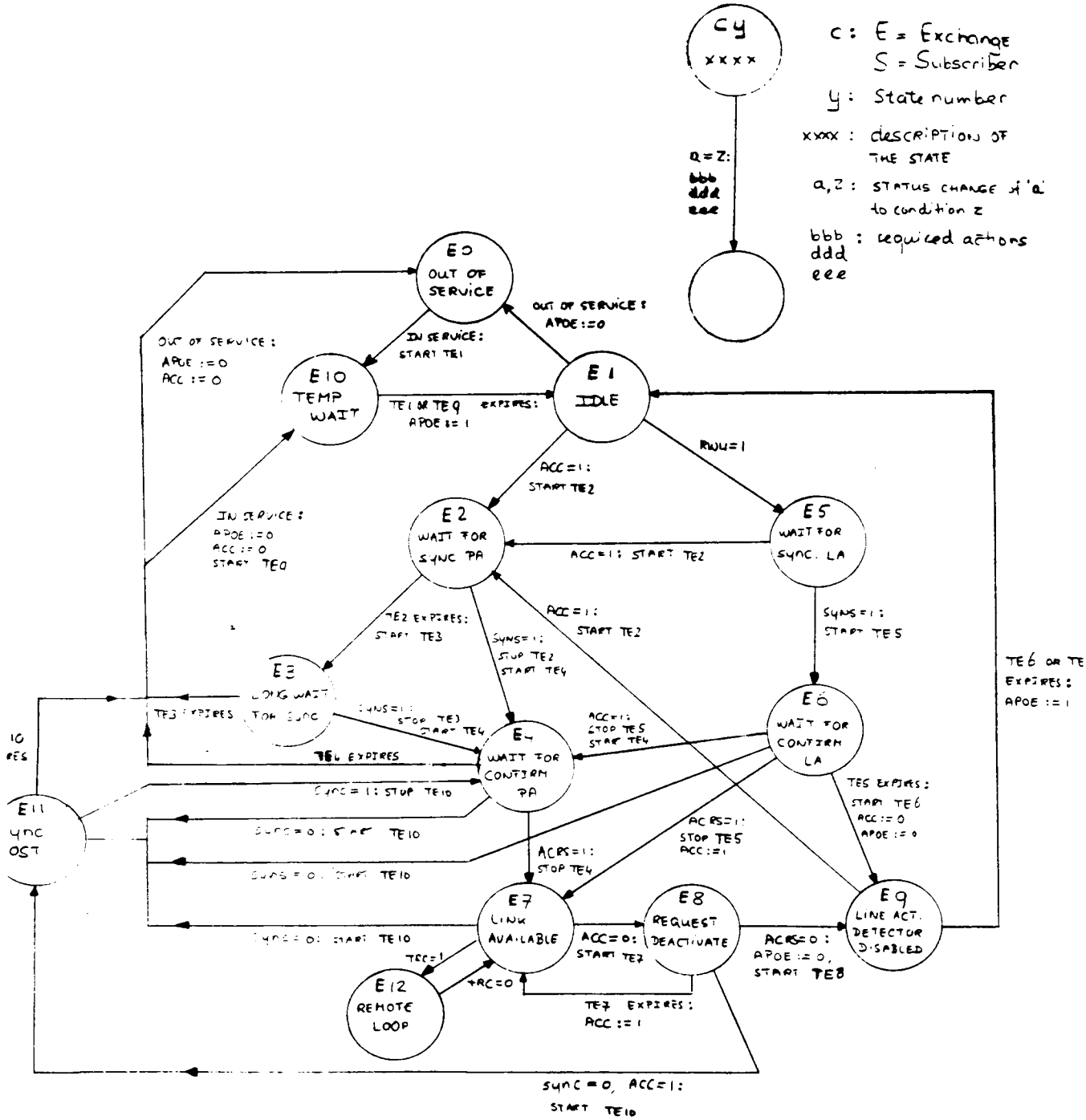


Figure 2.7.1-1 Activation/deactivation procedure at the exchange.

E0 OUT OF SERVICE

The channel is not available. This state is entered after power-up or if the PCB2391 is in local testloop.

E1 IDLE, POWER DOWN

The linedriver is disabled. In this state the circuit can be activated by the local microcontroller if it changes bit ACC of register W1 to '1' or by a received line signal which is generated by the far-end linedriver.

If the activation was caused by a received line signal the state changes to E5 but it should be noticed that the RWU signal is not available for the microcontroller, so the controller can not discriminate between state E1 and E5.

E2 WAIT FOR SYNCHRONISATION PA (processor activated)

The microcontroller has activated the local linedriver by setting bit ACC to '1'. This causes a linesignal on the far-end line activity detector which will initiate the far-end activation.

A timer (te2) is running to guard whether line synchronisation is achieved within the timelimit te2. If the timelimit expires the state changes to E3. Expiring of the timelimit can be caused by:

-initial convergention
-if the far-end is in state S9 caused by illegal activation or synchronisation loss
-other extreme conditions

E3 LONG WAIT FOR SYNCHRONISATION

Timer te3 is running to guard whether line synchronisation is achieved within timelimit te3. If no remote PCB2391 is connected (no line) or if it is in state S0 (out of service) the timer expires.

E4 WAIT FOR CONFIRMATION PA (processor activated)

Timer te4 is running to guard whether the far-end PCB2391 responds by setting the 'ACC' field of the lineframe in within timelimit te4.

E5 WAIT FOR SYNCHRONISATION LA (line activated)

The circuit was activated by the line activity detector when line RWU has become active.

The microcontroller does not know about this state; activation by making bit ACC of register W1 '1' is allowed. As soon as linesynchronisation is

achieved (bit SYNS=1) timer te5 must be started and the state changes to E6 (For the microcontroller it means a state E1 to E6 change if bit SYNS changes to '1').

E6 WAIT FOR CONFIRMATION LA (line activated)

Timer te5 is running to guard whether bit ACRS changes to 1 within time te5. If not the (illegal) activation was caused by a line disturbance. In that case the near-end linedriver and the activity detector are disabled for a time te6. (During state E6 an activation by the microcontroller is allowed.)

E7 LINK-AVAILABLE

The D- and B-channels are available for transmission in both directions. The exchange can ask for a deactivation by making the 'ACC' field '0'.

E8 REQUEST DEACTIVATION

The microcontroller made the 'ACC' field '0' by writing ACC='0' as deactivation request. The subscriber must response within time te7 on this deactivation request by making it's 'ACC' field '0' as an acknowledge.

E9 LINE ACTIVITY DETECTOR DISABLED

The linedriver and the line activity detector are disabled for a time te6 or te8. This time depends on the previous state.

E10 TEMPORARY WAIT AFTER ERROR

If an error condition occured this state is used to create a defined restart.

E11 SYNCHRONISATION LOST

In this state is waited for a period te10. If synchronisation is achieved within this period, state E4 is entered.

E12 REMOTE LOOP

The remote loop is requested by setting TRC to '1' by microcontroller. Back to E7 by setting TRC to '0'.

The timers used in the state diagram describing the activation/deactivation procedure at the exchange are listed in table 2.7.1-2.

TIMER	VALUE	COMMENT
te1	40 ms	recovery time capacitors (C ARV !)
te2	500 ms	waittime for line synchronisation: -RWU delay far-end -convergence time far-end -convergence time near-end -dead time caused by ts6,ts7 far-end
te3	3000 ms	waittime for line synchronisation at exceptional conditions (e.g. initial conditions)
te4	60 ms	waittime ACR=1 response on ACC=1 -10 msec recognition PCB2391 far-end -20 msec microcontroller response time far-end -10 msec recognition PCB2391 near-end -20 msec microcontroller response time near-end
te5	30 ms	waittime ACR=1 after SYNS=1 -10 msec recognition PCB2391 near-end -20 msec microcontroller response time near-end
te6	3500 ms	dead time Receiver Wake Up circuit after illegal activation caused by noise waittime disabling far-end line driver discharge time RWU capacitor
te7	70 ms	deactivation request
te8	200 ms	dead time Receiver Wake Up circuit waittime disabling far-end linedriver discharge time RWU capacitor
te9	3500 ms	dead time Receiver Wake Up circuit after error discharge time RWU capacitor
te10	1200 ms	

Table 2.7.1-2 Timers used in (de)activation procedure (exchange)

2.7.2. Activation/deactivation at the subscriber

The state diagrams of the activation/deactivation procedure at the subscriber is illustrated in figure 2.7.2-2. The legend to the figure and the description of the states is given in this section.

S0 OUT OF SERVICE

The channel is not available. This state is entered after power-up or if the PCB2391 is in local test loop.

S1 IDLE, POWER DOWN

The linedriver is enabled. In this state the circuit can be activated by the local microcontroller if bit ACC of register is changed to '1' or by a received line signal which is generated by the far-end linedriver.

If the activation was caused by a received line signal the state changes to S5 but it should be noticed that the RWU signal is not available for the microcontroller, so the microcontroller can not discriminate between state S1 and S5.

S2 WAIT FOR SYNCHRONISATION PA (processor activated)

The microcontroller has activated the local linedriver by writing ACC='1'. This causes a linesignal on the far-end line activity detector which will initiate the far-end activation.

Timer ts2 is running to guard whether line synchronisation is achieved within timelimit ts2. If the timelimit expires the state changes to S3. Expiring of the timelimit can be caused by:

-initial convergention
-if the far-end is in state E9 caused by illegal activation
-other extreme conditions

S3 LONG WAIT FOR SYNCHRONISATION

Timer ts3 is running to guard whether line synchronisation is achieved. If no remote PCB2391 is connected (no line) or if it is in state E0 (out of service) the timer expires.

S4 WAIT FOR CONFIRMATION PA (processor activated)

A timer ts4 is running to guard whether the far-end responds by setting the 'ACC' field of the lineframe in time.

S5 WAIT FOR SYNCHRONISATION LA (line activated)

The circuit was activated by the line activity detector which caused RWU to become active.

The microcontroller does not know about this state; activation by making bit ACC of register W1 '1' is allowed. As soon as linesynchronisation is achieved (bit SYNS='1') timer ts5 is started and the state changes to S6. For the microcontroller it means a state S1 to S6 change if bit SYNS changes to '1'.

S6 WAIT FOR CONFIRMATION LA (line activated)

Timer ts5 is running to guard whether bit ACRS changes to '1' within time. If not the (illegal) activation was caused by a line disturbance. In that case the near-end linedriver and the activity detector are disabled by a time out of ts6. (During state S6 an activation by the microcontroller is allowed.)

S7 LINK AVAILABLE

The D- and B-channels are available for transmission in both directions. The exchange can request to deactivate by making the 'ACC' field '0' which can be detected by bit ACRS = '0'.

S8 CONFIRMATION OF DEACTIVATION

As a response on bit ACRS changing to '0', the microcontroller should make the own 'ACC' field '0' during a time ts7. The microcontroller must make the ACC bit '0' as an acknowledge.

S9 LINE ACTIVITY DETECTOR DISABLED

The linedriver and the line activity detector are disabled for a time ts6 or ts11. This time depends on the previous state.

S10 TEMPORARY WAIT AFTER ERROR

If an error condition occured this state is used to create a defined restart.

S11 SYNCHRONISATION LOST

In this state is waited for a period tel0. If synchronisation is achieved within this period, state E4 is entered.

S12 REMOTE LOOP

The remote loop is requested when the TRRS bit is set to '1'. Back to E7 when TRRS is set to '0'.

The timers used in the state diagram describing the activation/deactivation procedure at the exchange are listed in table 2.7.2-1.

TIMER	VALUE	COMMENT
ts1	40 ms	recovery time capacitors (C ARV !)
ts2	500 ms	waittime for line synchronisation: -RWU delay far-end -convergence time far-end -convergence time near-end -dead time caused by ts6,ts7 far-end
ts3	3000 ms	waittime for line synchronisation at exceptional conditions (e.g. initial conditions)
ts4	60 ms	waittime ACR=1 response on ACC=1 -10 msec recognition PCB2391 far-end -20 msec microcontroller response time far-end -10 msec recognition PCB2391 near-end -20 msec microcontroller response time near-end
ts5	30 ms	waittime ACR=1 after SYNS=1 -10 msec recognition PCB2391 near-end -20 msec microcontroller response time near-end
ts6	3500 ms	dead time Receiver Wake Up circuit after illegal activation caused by noise waittime disabling far-end line driver discharge time RWU capacitor
ts7	40 ms	confirmation deactivation request of exchange -10 msec recognition PCB2391 far-end -20 msec μC response time near-end
ts8	200 ms	dead time Receiver Wake Up circuit waittime disabling far-end linedriver discharge time RWU capacitor
ts9	3500 ms	dead time Receiver Wake U_P circuit after error discharge time RWU capacitor
ts10	1200 ms	

Table 2.7.2-1 Timers used in (de)activation procedure (subscriber)

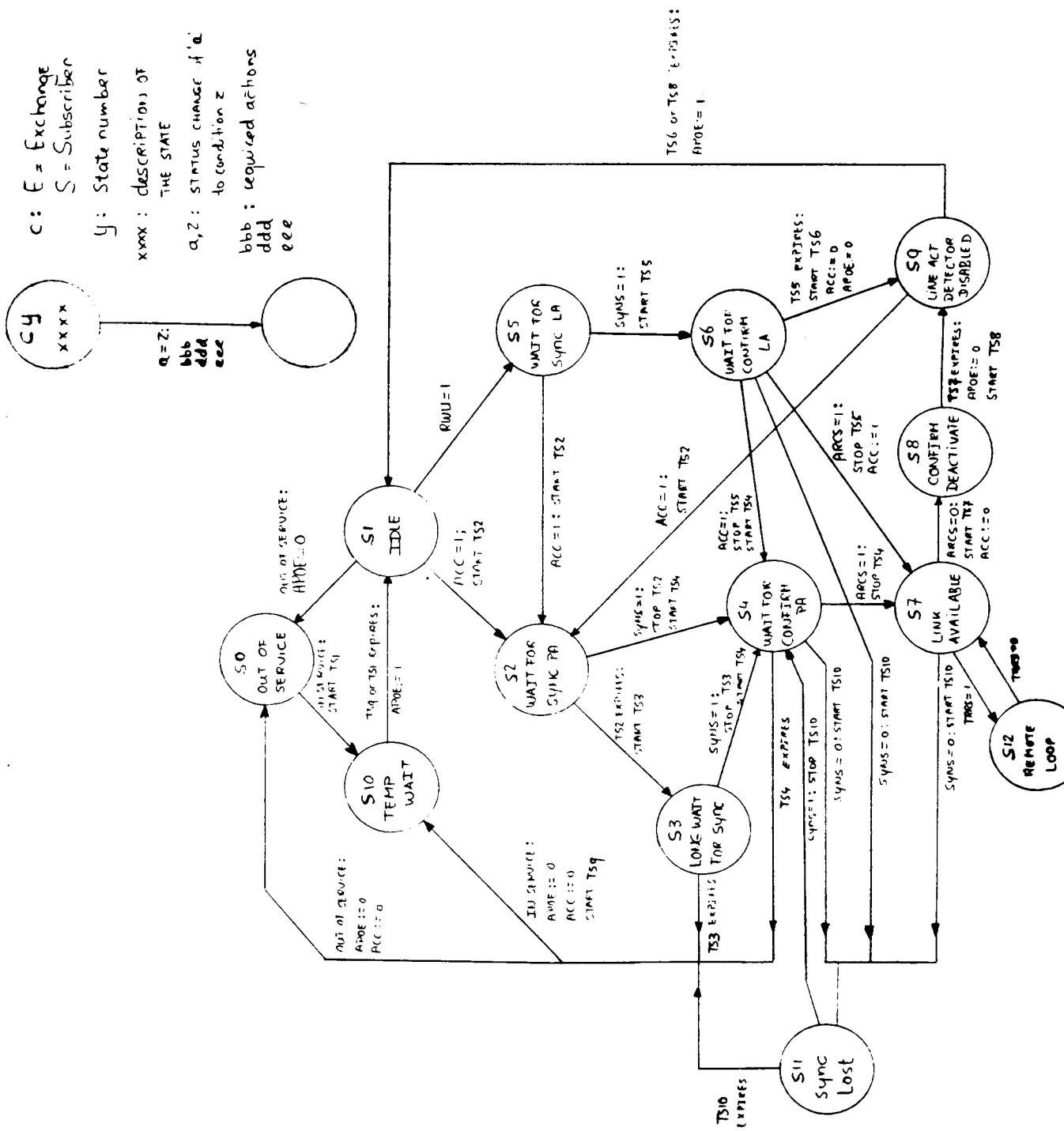


Figure 2.7.2-2 Activation/deactivation procedure at the subscriber.

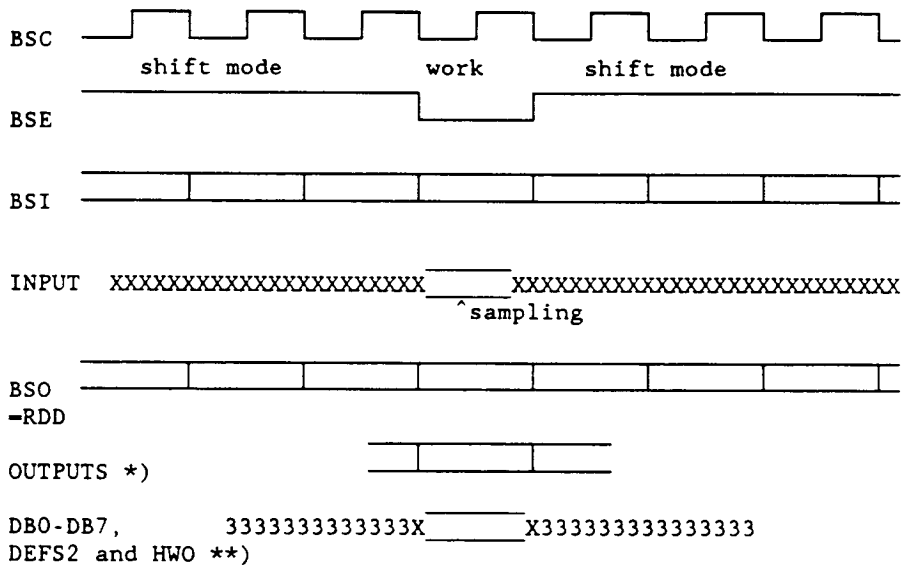
2.8. Boundary scan test

For board testing purposes a boundary scan chain is implemented. In section 2.1 is illustrated how the PCB2391 can be set in the boundary scan mode by signal MC and BSE.

The following signals are of interest:

BSI : boundary scan input.
BSO : boundary scan output.
BSC : boundary scan clock.

The timing relation relation between these signals in boundary scan mode is illustrated in figure 2.8-1.



*) except DB0 - DB7 and HWO
**) High-Z during shift, in workmode dependent of entry 10,16,23 see table

Figure 2.8-1 Timing relations between signals in boundary scan mode.

In the shift mode, BSE='1', the databus, the HWO and the DEFS2 pin are high-Z. In the work cycle, where the inputs are sampled in the boundary scan line, and outputs are forced, the direction of the I/Os DB0..7, DEFS2 and the mode of the HWO pin is determined by three boundary chain elements: entry 10, 16 and 23 which are depicted in figure 2.8-2.

flip-flop number	pin number	workcycle data in	workcycle data out	remarks
	44 (40)	BSI		chain input
1	16 (15)	CSN		
	18 (16)		INTN	
2	7 (6)	DB0	DB0	
3	8 (7)	DB1	DB1	
4	9 (8)	DB2	DB2	
5	10 (9)	DB3	DB3	
6	11 (10)	DB4	DB4	
7	13 (11)	DB5	DB5	
8	14 (12)	DB6	DB6	
9	15 (13)	DB7	DB7	
10	5 (4)	RDN		internal used to select direction of DB0..7 0=input 1=output
11	22 (20)	MC		if set to '1' the outputs change to high-Z mode
12	19 (17)	ALE		
13	6 (5)	WRN		
14	25 (22)	HWI		
	27 (25)		FS1	
15	26 (24)	DEFS2	DEFS2	
16	intern			internal used to select direction of DEFS2 1=input 0=output
17	-			t.b.f.
18	-			t.b.f.
19	-			t.b.f.
20	-			t.b.f.
21	30 (27)	EXCH		
	28 (23)		RT6	
22	24 (21)		HWO	
23	intern			internal used to select operation of HWO 0=high Z 1=output
	1 (1)		BSO/RDD	scan output

note: some boundary flipflops are used both to set outputs and to read inputs. In this case both names are coupled to a single ranknumber in boundary scan mode the following signals should have the specified state: CLK=1.

Figure 2.8-2 Chain order boundary scan (input pin BSI, output pin BSO)

3. DC characteristics

3.1. Ratings

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
DC supply voltage		V_{DD}	tbf	7.0	V
DC input diode current	V_I< -0.5 or V_I> Vdd+0.5	$\pm I_{IK}$	-	tbf	mA
DC output diode current	V_O< -0.5 or V_O> Vdd+0.5	$\pm I_{OK}$	-	tbf	mA
DC output sink current	-0.5 <V_O< Vdd + 0.5	$\pm I_O$	-	tbf	mA
DC output source current	-0.5 <VO< Vdd + 0.5	±IO	-	tbf	mA
DC V_{DD} current		$\pm I_{DD}$	-	tbf	mA
DC ground current		$\pm I_{GND}$	-	tbf	mA
Voltage on any pin		V_n	tbf	tbf	V
Storage temperature range		T_{stg}	tbf	tbf	^0C
Operating ambient temperature range		T_{amb}	-10	+75	^0C
Total power dissipation		P_{tot}	-	tbf	mW

3.2. DC characteristics

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Digital supply voltage	1)	$V_{DD}D$	4.5	5.5	V
Analog supply voltage	2)	VDDA	tbf	tbf	V
Inputs BSI, RDN,WRN,CSN, ALE,BSE,BSC, SCC,HWI,EXCH					
Threshold voltage positive-going	V_{DD} = 5V	V_{T+}	-	2.0	V
negative-going	V_{DD} = 5V	V_{T-}	0.8	-	V
Input leakage current	0 < V_I < VDD	I_{IL}	-	1.0	µA
Outputs RDD,FS1,RT6					
Output voltage LOW	V_{DD} = 5 V I_{OL} = 2.0 mA	V_{OL}	-	0.4	V
Output voltage HIGH	VDD = 5 V -IOH = 2.0 mA	V_{OH}	4.0	-	V
3-state OFF current	0 < V_O < V_{DD} I_O = 0	± I_{OZ}	-	10	µA
Output HWO					
Output voltage LOW	V_{DD} = 5 V I_{OL} = 4.0 mA	V_{OL}	-	0.4	V
Output voltage HIGH	VDD = 5 V -IOH = 4.0 mA	V_{OH}	4.0	-	V
3-state OFF current	0 < V_O < V_{DD} I_O = 0	± I_{OZ}	-	10	µA

1) Maximum difference between VDDD and VDDA: tbf.
2) Noise and ripple: tbf.

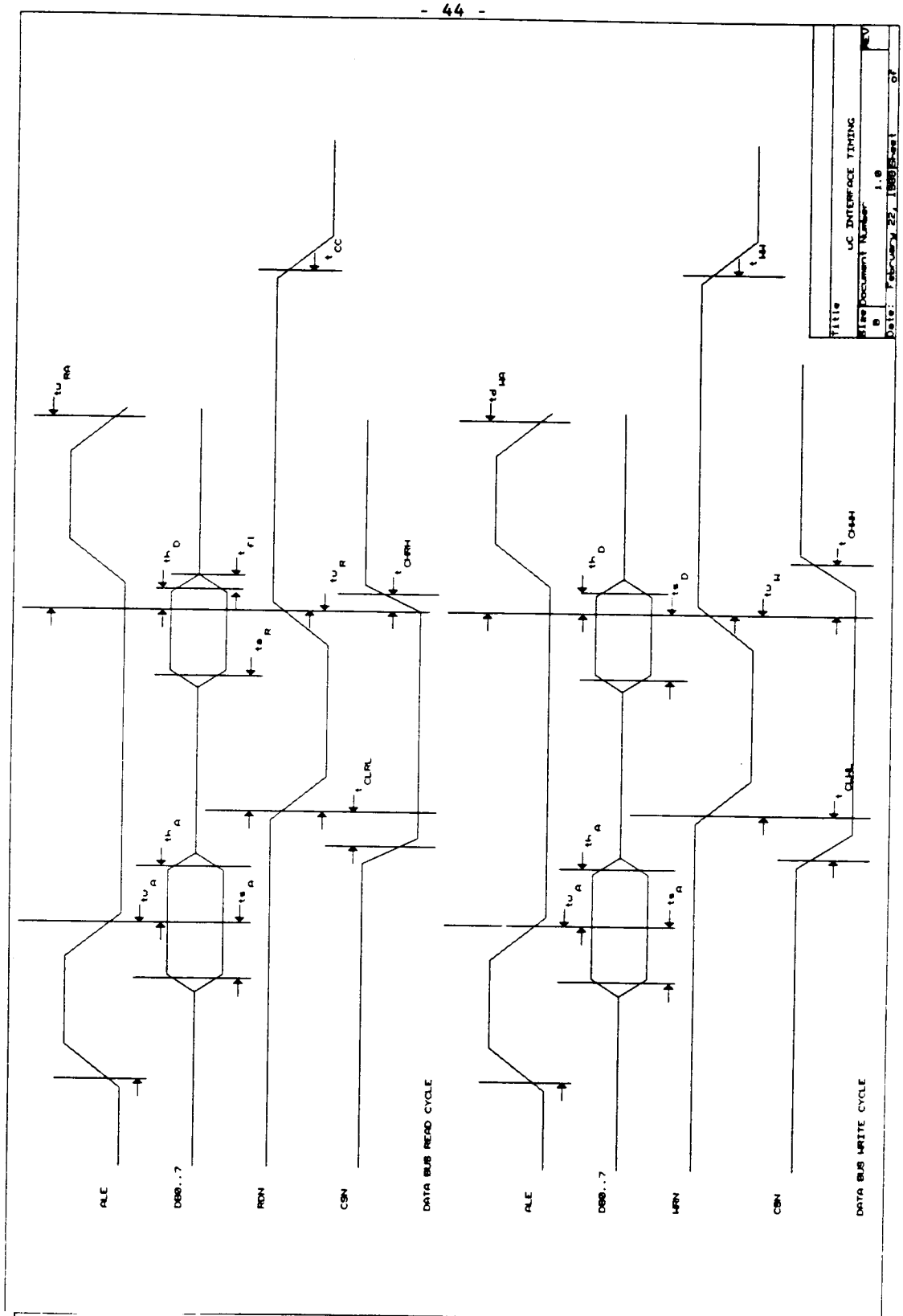
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
bi-directional buffers CLK, DB0..7, DEFS2					
Threshold voltage positive-going	V_{DD} = 5V	V_{T+}	-	2.0	V
negative-going	V_{DD} = 5V	V_{T-}	0.8	-	V
Input leakage current	0 < V_I < VDD	I_{IL}	-	10	µA
Output voltage LOW	V_{DD} = 5 V I_{OL} = 4.0 mA	V_{OL}	-	0.4	V
Output voltage HIGH	VDD = 5 V -IOH = 4.0 mA	V_{OH}	4.0	-	V
Open drain Output INTN					
Output voltage LOW	V_{DD} = 5 V I_{OL} = 4.0 mA	V_{OL}	-	0.4	V
Open drain Output DDC					
Output voltage LOW	V_{DD} = 5 V I_{OL} = 2.0 mA	V_{OL}	-	0.4	V

4. AC characteristics

Conditions: Vdd = 5 V, Tamb = -10..+75°C.
Timing measurements are specified at V_H=4V and V_L=1V unless otherwise stated.

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Microcontroller bus					
ALE pulse width		tw_A	100	-	ns
Data bus read cycle					
Address set up time		ts_A	50	-	ns
Address hold time		th_A	10	-	ns
RDN pulse width		tw_R	200	-	ns
Read access time	Cl = 200pF	ta_R	-	200	ns
Data hold time		th_D	10	-	ns
Time from RDN HIGH to ALE LOW		td_{RA}	2	-	μs
CSN LOW before RDN LOW		t_{CLRL}	tbs	-	ns
CSN HIGH after RDN HIGH		t_{CHRH}	10	-	ns
Bus floating after read		t_{fl}	-	110	ns
Time between two RDN		t_{RR}	2.6	-	μs

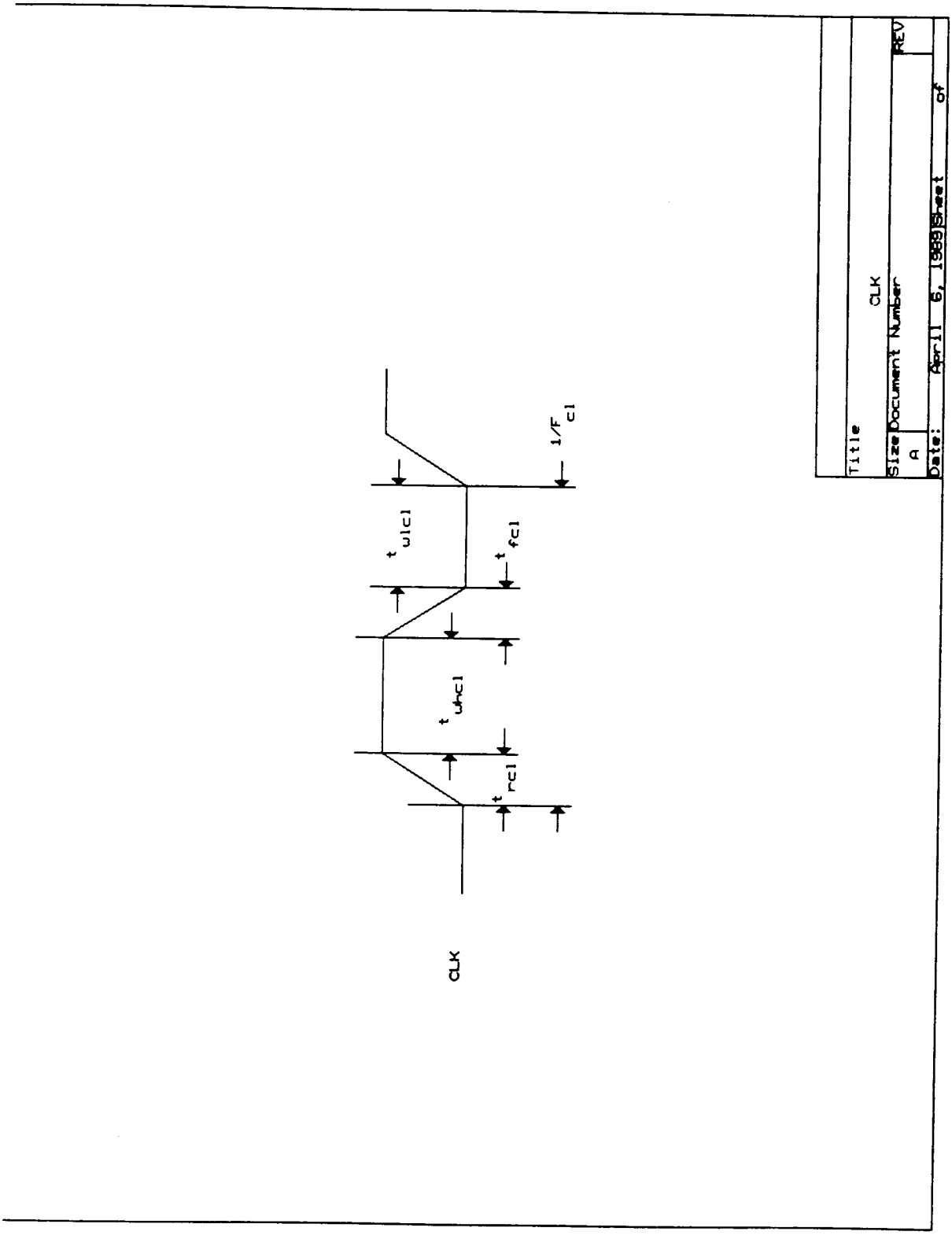
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Microcontroller bus					
ALE pulse width		tw_A	100	-	ns
Data bus write cycle					
Address set up time		ts_A	50	-	ns
Address hold time		th_A	10	-	ns
WRN pulse width		tw_W	100	-	ns
Data set up time		ts_D	100	-	ns
Data hold time		th_D	40	-	ns
Time from WRN HIGH to ALE LOW		td_{WA}	2	-	μs
CSN LOW before WRN LOW		t_{CLWL}	150	-	ns
CSN HIGH after WRN HIGH		t_{CHWH}	0	-	ns
Time between two WRN		t_{WW}	2.6	-	μs



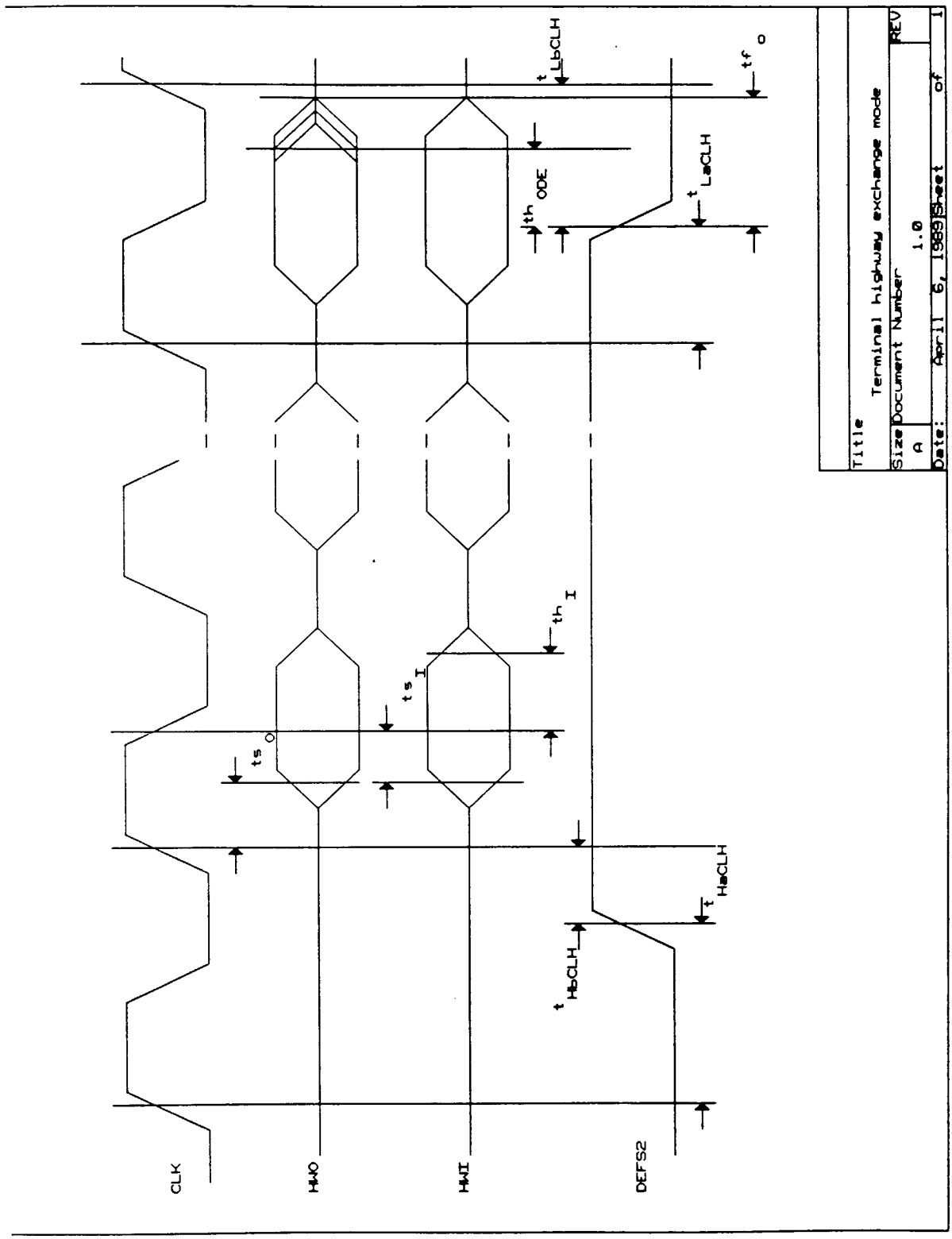
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Clock input:					
Clk frequency	nominal 2.048 MHz	F_{cl}	-50	+50	ppm.
CLK LOW time		t_{wlcl}	190	290	ns
CLK HIGH time		t_{whcl}	190	290	ns
CLK LOW to HIGH transition		t_{rcl}	15	40	ns
CLK HIGH to LOW transition		t_{fcl}	15	65	ns
output:					
CLK LOW time	Cl=150 pF	t_{wlcl}	220	260	ns
CLK HIGH time	Cl=150 pF	t_{whcl}	220	260	ns
CLK LOW to HIGH transition		t_{rcl}	-	40	ns
CLK HIGH to LOW transition		t_{fcl}	-	65	ns

Note: Maximum jitter on rising and falling edges of CLK:
- tbf ns in input mode
- tbf ns in output mode, if PCB2391 in synchronisation at line level

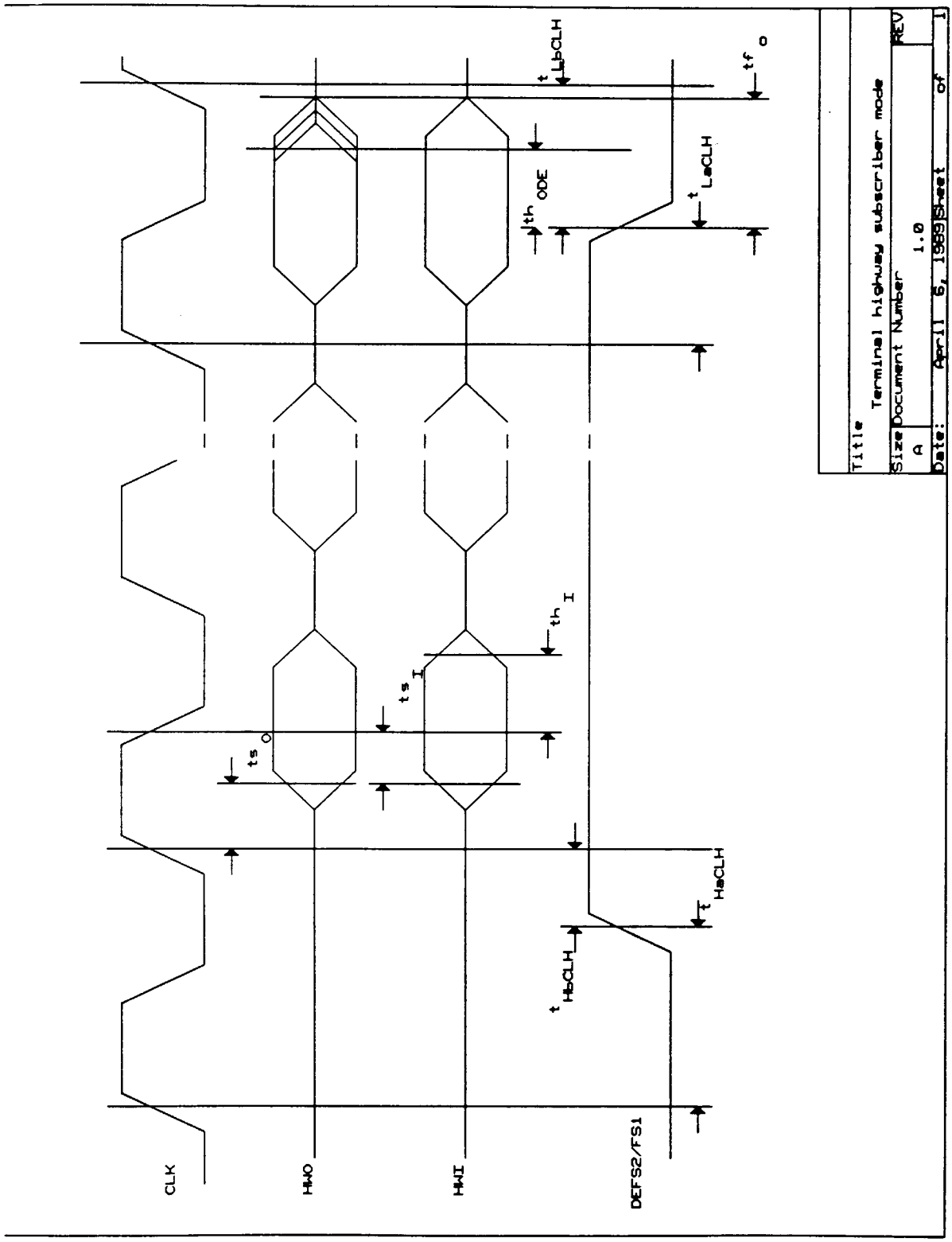
Maximum tolerance Fcl:
- 50 ppm in input mode
- 50 ppm in output mode, if in synchronisation at line level
- 1000 ppm in output mode, if not in synchronisation at line level



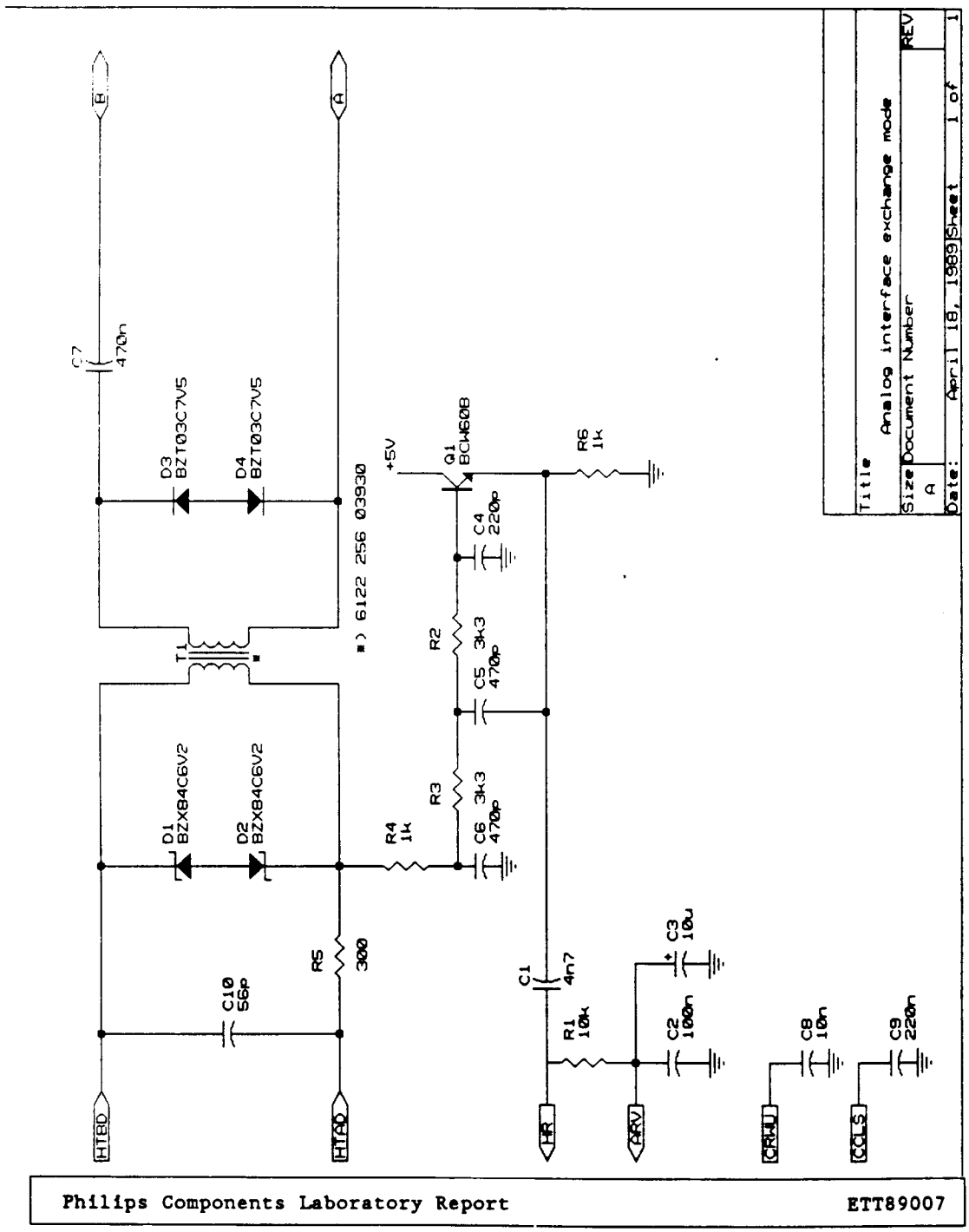
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Terminal Highway					
Exchange mode					
DEFS2					
HIGH after CLK HIGH		t_{HaCLH}	20	-	ns
HIGH before CLK HIGH		t_{HbCLH}	100	-	ns
LOW after CLK HIGH		t_{LaCLH}	20	-	ns
LOW before CLK HIGH		t_{LbCLH}	120	-	ns
HWI					
data set up time		ts_I	120	-	ns
data hold time		th_I	150	-	ns
HWO					
data set up time	C1=200pF	ts_O	0	220	ns
data hold time after DEFS2 LOW		th_{ODE}	0	-	ns
HWO floating after DEFS2 LOW		tf_O	-	120	ns

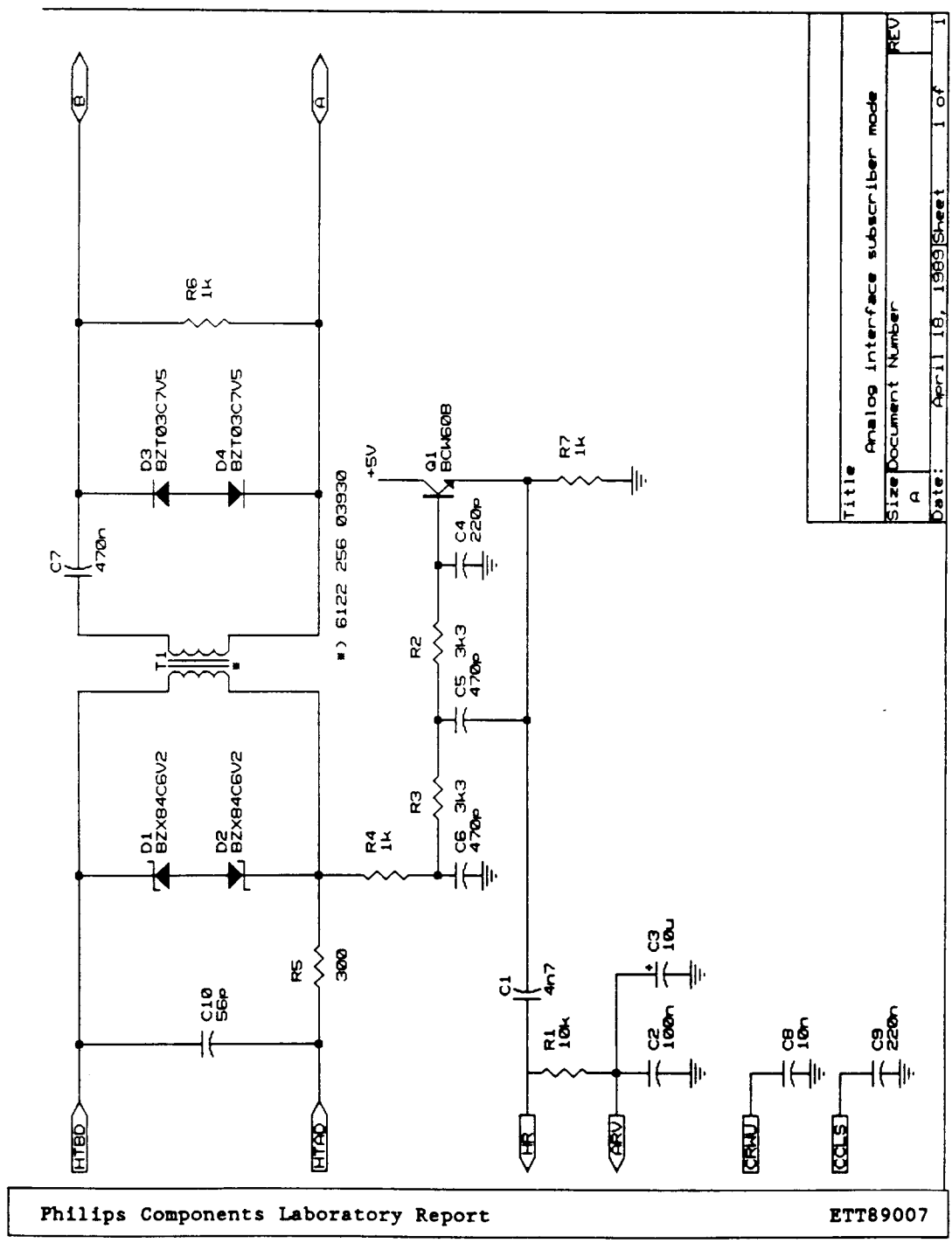


PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Terminal Highway					
subscriber mode					
FS1/DEFS2					
HIGH after CLK HIGH		t_{HaCLH}	20	-	ns
HIGH before CLK HIGH		t_{HbCLH}	100	-	ns
LOW after CLK HIGH		t_{LaCLH}	20	-	ns
LOW before CLK HIGH		t_{LbCLH}	120	-	ns
HWI					
data set up time		ts_I	120	-	ns
data hold time		th_I	150	-	ns
HWO					
data set up time	C1=200pF	ts_O	0	220	ns
data hold time after DEFS2/FS1 LOW		th_{ODE}	0	-	ns
HWO floating after DEFS2/FS1 LOW		tf_O	-	120	ns



APPENDIX A Application diagrams





APPENDIX B Initialisation procedure

To initialize the PCB2391 the following procedure must be used:

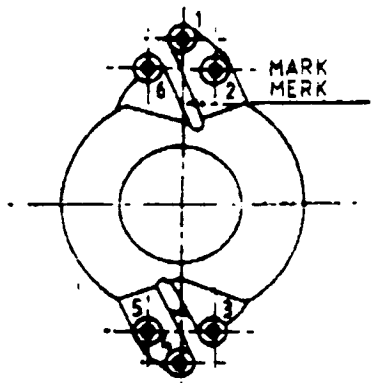
- disable all interrupts (register W2)
- enable internal clocks, to ensure correct R4 information (write '3F' to register W1)
- wait at least 12 μsec
- select operation mode (reg W1)
- 2X reset HDLC transmitter and receiver (register W1)
- reset possibly pending interrupts by reading the activity/status registers (register R4, R5)
- enable the desired interrupts (register W2)

Interrupts are disabled by writing HEX'00' to register W2.

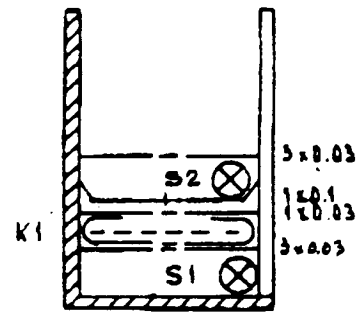
APPENDIX C Line transformer specification

Transformer specification for configuration without phantom power feed.

WIRING DIAGRAM/AANSLUITSCHEMA

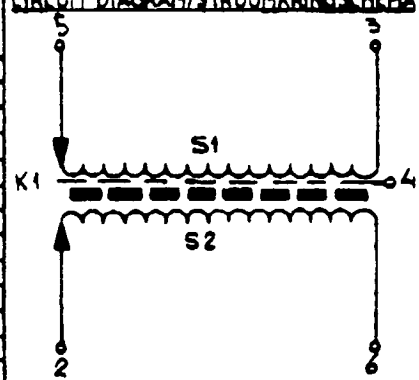


WINDING DIAGRAM/WIKKELSCHEMA



WIND WIKK	NUMBER OF/AANTAL TURNS WIND	LAYERS LAGEN	TURNS/LAYER WIND/LAAG	WIRE/DR ITEM POST	WINDING WIDTH WIKKELBREEDTE	REMARKS OPM
S1	69	ca 2	ca 35	1	CW-CW/FL-FL	
S2	49	ca 2	ca 35	1	CW-CW/FL-FL	

CIRCUIT DIAGRAM/STROOMKRINGSCHEMA



SPECIFICATION/SPECIFICATIE

MEAS. MET.	BETWEEN TUSSEN	INTERCONNECT DOORVERBINDEN	VALUE WAARDE	VOLT./FREQ. SPAN./FREQ.	REMARKS OPM.
L	2-6		≥ 10 mH	19 mV	
U	6-5/2-6		1.408 ± 1%		
S	2-6	3+5	≤ 9.5 µH		
R_o	2-6		1.55 Ω ± 15%		
R_o	5-5		1.85 Ω ± 15%		
	2-3	4+5		2000V-50Hz	10 SEC.
	4-5			500V-50Hz	
TEST VOLT PROP	2		AGAINST BRACKET TEGEN BEUGEL	500V-50Hz	
	1+4+6				
INSUL	AS ABOVE/ALS BOVEN		≥ 100MΩ		

REMARKS/OPMERKINGEN

1/02OKEBITE

AUXILIARY DATA/HULPGEGEVENS

TRANSFORMER
TRANSFORMATOR RM 6 - S/I/3E4

APPENDIX D Line signals

The coding method used on the two wire transmission line is the biphase method. Each information bit offered for transmission on the line is converted into two bits of unequal value. In case a '1' has to be transmitted, a '1' followed by a '0' is placed on the line. In case a '0' has to be transmitted a '0' followed by a '1' is placed on the line. The coding method is illustrated in figure D-1.

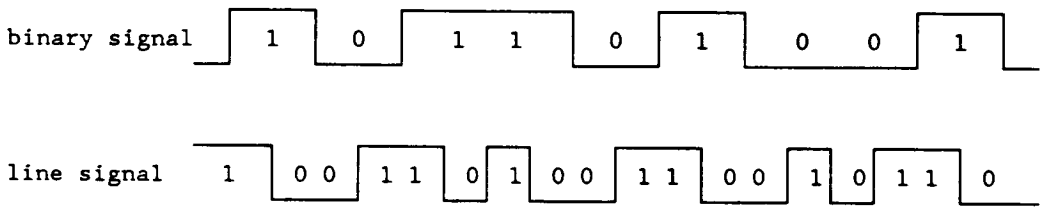


Figure D-1 Biphase coding

Specification the electrical connection at the line side of the line transformer:

Impedance:

characteristic impedance line	: 150 Ohm
allowed mismatch with performance degradation at a minimum receive level of tbf dB	:+/- 60 Ohm

Levels:

transmit line level into 150 Ohm (0 dB reference level) (no protection circuits added)	: tbf Vpp
tolerance on transmit level (design tol + Vdd tol)	: tbf dB
minimum receive level excl. echo and ISI	: tbf dB
maximum receive level incl. echo and ISI	: tbf dB
maximum receive level echo and ISI	: tbf dB
maximum level not compensated echo's and ISI with respect to the received signal exclusive echo and ISI	: tbf dB
minimum required line signal to activate Wake Up	: tbf dB
maximum allowed signal which does not activate Wake Up	: tbf dB

tbf

Figure D-2 Biphase coded 152 kbit/s line signal terminated with 150Ω

tbf

Figure D-3 Power spectrum of the biphase signal

APPENDIX E Interrupt handling on HDLC receiver interrupt

The interrupt handling procedure should contain the following statements:

```
Read register R6;
Read register R4;
IF register bit RMC='0' and bit RE0='0' and bit RE1='0' and register
R6 bit RA='1'
THEN reset HDLC receiver;
Handle possible other in register R4 indicated interrupts.
```

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