

DRAM MODULE

2 MEG x 64

16 MEGABYTE, 5V, FAST PAGE OR
EDO PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +5V $\pm 10\%$ power supply
- All device pins are TTL-compatible
- Low power, 8mW standby; 1,600mW active, typical
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR), HIDDEN
- All inputs are buffered except RAS
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles

OPTIONS

- Timing
60ns access
70ns access
- Packages
168-pin DIMM (gold)
- Access Cycle
FAST PAGE MODE
EDO PAGE MODE

MARKING

-6
-7

G

Blank
X

PART NUMBERS

PART NUMBER	DESCRIPTION
MT8D264G-xx	2 Meg x 64, FAST PAGE MODE
MT8D264G-xx X	2 Meg x 64, EDO

xx = speed

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	'RC	'RAC	'PC	'AA	'CAC	'CAS
-6	105ns	60ns	25ns	35ns	20ns	12ns
-7	125ns	70ns	30ns	40ns	25ns	12ns

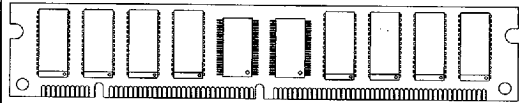
FPM Operating Mode

SPEED	'RC	'RAC	'PC	'AA	'CAC	'RP
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-15)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2	86	DQ32	128	RFU
3	DQ1	45	RAS2	87	DQ33	129	NC
4	DQ2	46	CAS4	88	DQ34	130	CAS5
5	DQ3	47	CAS6	89	DQ35	131	CAS7
6	Vcc	48	WE2	90	Vcc	132	PDE
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	Vcc	101	DQ44	143	Vcc
18	Vcc	60	DQ22	102	Vcc	144	DQ54
19	DQ13	61	RFU	103	DQ45	145	RFU
20	DQ14	62	RFU	104	DQ46	146	RFU
21	DQ15	63	RFU	105	DQ47	147	RFU
22	NC	64	RFU	106	NC	148	RFU
23	Vss	65	DQ23	107	Vss	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0	69	DQ25	111	RFU	153	DQ57
28	CAS0	70	DQ26	112	CAS1	154	DQ58
29	CAS2	71	DQ27	113	CAS3	155	DQ59
30	RAS0	72	DQ28	114	NC	156	DQ60
31	OE0	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ29	116	Vss	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

**NEW
DRAM DIMM**

GENERAL DESCRIPTION

The MT8D264(X) is a randomly accessed solid-state memory containing 2,097,152 words organized in a x64 configuration.

During READ or WRITE cycles, each bit is uniquely addressed through the 21 address bits. The address is entered first by $\overline{\text{RAS}}$ latching 11 bits and then $\overline{\text{CAS}}$ latching 10 bits. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.

READ and WRITE cycles are selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. An EARLY WRITE occurs when $\overline{\text{WE}}$ is taken LOW prior to $\overline{\text{CAS}}$ falling. A LATE WRITE or READ-MODIFY-WRITE occurs when $\overline{\text{WE}}$ falls after $\overline{\text{CAS}}$ was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of $\overline{\text{OE}}$. During LATE WRITE or READ-MODIFY-WRITE cycles, $\overline{\text{OE}}$ must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping $\overline{\text{OE}}$ LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{\text{RAS}}$ followed by a column-address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{\text{CAS}}$ goes back HIGH. EDO provides for $\overline{\text{CAS}}$ precharge time (t_{CP}) to occur without the output data going invalid. This elimination of $\overline{\text{CAS}}$ output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{\text{CAS}}$. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after $\overline{\text{CAS}}$ goes HIGH during READs, provided $\overline{\text{RAS}}$ and $\overline{\text{OE}}$ are held LOW. If $\overline{\text{OE}}$ is pulsed while $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{\text{OE}}$ is toggled or pulsed after $\overline{\text{CAS}}$ goes HIGH while $\overline{\text{RAS}}$ remains LOW, data will transition to and remain High-Z.

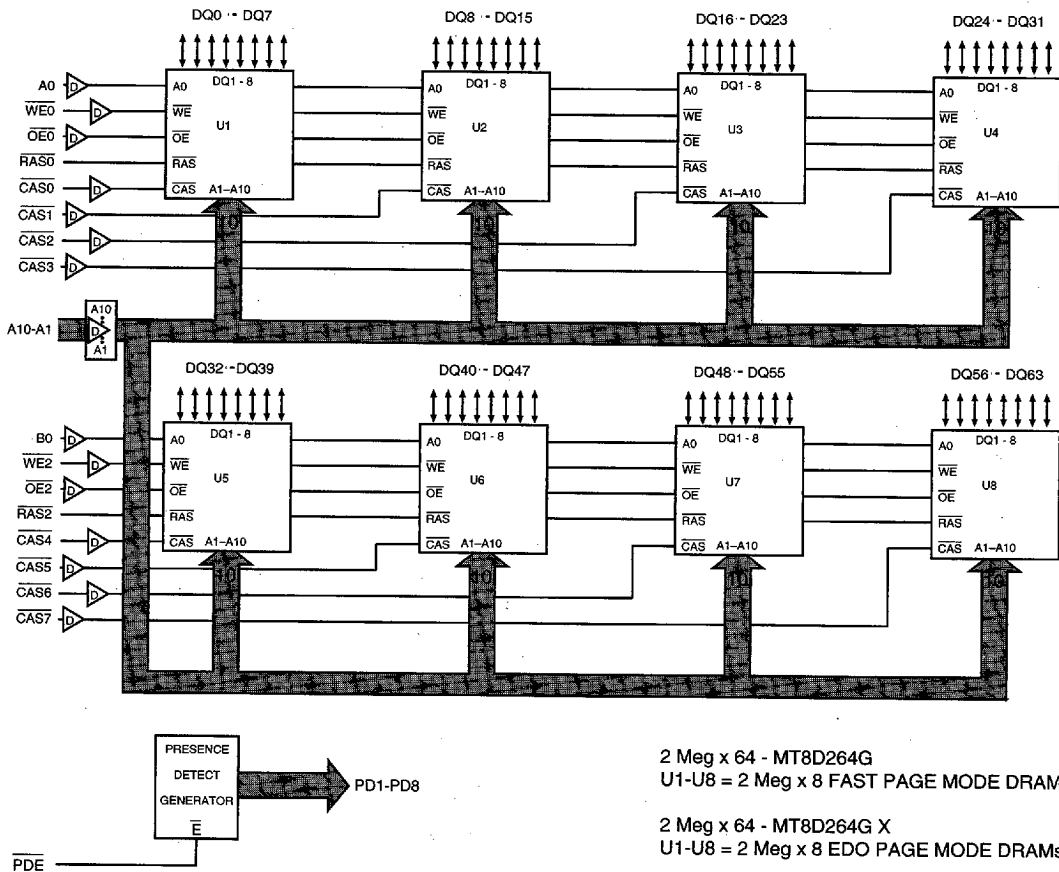
During an application, if the DQ outputs are wire OR'd, $\overline{\text{OE}}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{\text{WE}}$ to the idle banks during $\overline{\text{CAS}}$ HIGH time will also High-Z the outputs. Independent of $\overline{\text{OE}}$ control, the outputs will disable after 'OFF', which is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last (reference the MT4LC2M8E7 DRAM data sheet for additional information on EDO functionality).

REFRESH

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle, and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Correct memory cell data is preserved by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ ONLY, CBR or HIDDEN) so that all 2,048 combinations of $\overline{\text{RAS}}$ addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{\text{RAS}}$ addressing.

NEW
 DRAM DIMM

FUNCTIONAL BLOCK DIAGRAM



2 Meg x 64 - MT8D264G
U1-U8 = 2 Meg x 8 FAST PAGE MODE DRAMs

2 Meg x 64 - MT8D264G X
U1-U8 = 2 Meg x 8 EDO PAGE MODE DRAMs

NOTE: 1. All inputs with the exception of $\overline{\text{RAS}}$ are redriven.
2. D = line buffers.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Input	Row-Address Strobe: $\overline{\text{RAS}}$ is used to clock-in the 11 row-address bits. Two RAS inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	$\overline{\text{CAS0-7}}$	Buffered Input	Column-Address Strobe: $\overline{\text{CAS}}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight $\overline{\text{CAS}}$ inputs allow byte access control for any memory bank configuration.
27, 48	$\overline{\text{WE0}}, \overline{\text{WE2}}$	Buffered Input	Write Enable: $\overline{\text{WE}}$ is the READ/WRITE control for the DQ pins. $\overline{\text{WE0}}$ controls DQ0-DQ31. $\overline{\text{WE2}}$ controls DQ32-DQ63. If $\overline{\text{WE}}$ is LOW prior to $\overline{\text{CAS}}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{\text{WE}}$ is HIGH while $\overline{\text{CAS}}$ is LOW, the access is a READ cycle, provided $\overline{\text{OE}}$ is also LOW. If $\overline{\text{WE}}$ goes LOW after $\overline{\text{CAS}}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{\text{OE0}}, \overline{\text{OE2}}$	Buffered Input	Output Enable: $\overline{\text{OE}}$ is the input/output control for the DQ pins. $\overline{\text{OE0}}$ controls DQ0-DQ31. $\overline{\text{OE2}}$ controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.
2-5, 7-10, 13-17, 19-21, 52-53, 55-58, 60, 65, 67, 69-72, 74-76, 86-89, 91-94, 97-101, 103-105, 136-137, 139-142, 144, 149, 151, 153-156, 158-160	DQ0-DQ63	Input/Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITES may be performed by using the corresponding CAS select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
41-42, 61-64, 111, 115, 125, 128, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	Vcc	Supply	Power Supply: +5V $\pm$ 10%
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground

NEW
DRAM DIMM

■ 6111549 0013778 211 ■

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	PDE	Input	Presence-Detect Enable: PDE is the READ control for the buffered presence-detect pins.
11, 22, 24-25, 39, 50-51, 66, 77, 95, 106, 108-109, 114, 122-123, 129, 134-135, 150, 161	NC	—	No connect.

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	PDE	ADDRESSES		DATA-IN/OUT
							'R	'C	DQ0-63
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
	Any Cycle (X version)	L	L→H	H	L	X	n/a	n/a	Data-Out
EDO/FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
RAS-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
8MB	1 Meg x 64/72	10/9			1	1	0	0				
8MB	1 Meg x 64/72	10/10			0	0	1	0				
16MB	2 Meg x 64/72	10/10			1	0	1	0				
• 16MB	2 Meg x 64/72	11/10			1	0	0	1				
32MB	4 Meg x 64/72	11/10			0	1	0	1				
32MB	4 Meg x 64/72	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
Data Width		x64, No Parity	Vss									1
		x72 ECC	Vss									0

NOTE: Vss = ground; 0 = Vol; 1 = Voh.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting.

NEW
DRAM DIMM

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss -1V to +7V
 Operating Temperature, T_A (ambient) 0°C to +70°C
 Storage Temperature (plastic) -55°C to +125°C
 Power Dissipation 8W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{cc} = +5V ±10%)

PARAMETER/CONDITION	SYM	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V _{IH}	2.4	5.5	V	
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 5.5V (All other pins not under test = 0V)	CAS0 - CAS7 A0-A10, B0, PDE WE0,2, OE0,2	I _{I1}	-2	2	μA
	RAS0,2	I _{I2}	-8	8	μA
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	DQ0 - DQ63 PD1 - PD8	I _{OZ}	-10	10	μA
OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

NEW
DRAM DIMM

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-6	-7		
STANDBY CURRENT: (TTL) (RAS = CAS = V _{IH})	I _{CC1}	16MB	26	26	mA	26
STANDBY CURRENT: (CMOS) (RAS = CAS = V _{CC} - 0.2V)	I _{CC2}	16MB	14	14	mA	26
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, address cycling: ^t RC = ^t RC [MIN])	I _{CC3}	16MB	1,040	960	mA	3, 26, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _{IL} , CAS, address cycling: ^t PC = ^t PC [MIN])	I _{CC4}	16MB	720	640	mA	3, 26, 29
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current (RAS = V _{IL} , CAS, address cycling: ^t PC = ^t PC [MIN])	I _{CC5} (X only)	16MB	960	880	mA	3, 26, 29
REFRESH CURRENT: RAS ONLY Average power supply current (RAS cycling, CAS = V _{IH} : ^t RC = ^t RC [MIN])	I _{CC6}	16MB	1,040	960	mA	3, 26, 29
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, address cycling: ^t RC = ^t RC [MIN])	I _{CC7}	16MB	1,040	960	mA	3, 4, 26

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0, PDE	C _{I1}		9	pF	2
Input Capacitance: WE0, WE2, OE0, OE2	C _{I2}		9	pF	2
Input Capacitance: RAS0, RAS2	C _{I3}		40	pF	2
Input Capacitance: CAS0 - CAS7	C _{I4}		9	pF	2
Input/Output Capacitance: DQ0 - DQ63	C _{I0}		10	pF	2
Output Capacitance: PD1-PD8	C _O		10	pF	2

FAST PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Access time from column-address	t _{AA}		35		40	ns	23
Column-address hold time (referenced to RAS)	t _{AR}	48		53		ns	22
Column-address setup time	t _{ASC}	2		2		ns	21
Row-address setup time	t _{ASR}	5		5		ns	23
Column-address to WE delay time	t _{AWD}	57		62		ns	21, 28
Access time from CAS	t _{CAC}		20		25	ns	14, 23
Column-address hold time	t _{CAH}	15		20		ns	23
CAS pulse width	t _{CAS}	15	10,000	20	10,000	ns	
CAS hold time (CBR REFRESH)	t _{CHR}	13		13		ns	4, 22
CAS to output in Low-Z	t _{CLZ}	5		5		ns	21, 29
CAS precharge time	t _{CP}	10		10		ns	15
Access time from CAS precharge	t _{CPA}		40		45	ns	23
CAS to RAS precharge time	t _{CRP}	10		10		ns	23
CAS hold time	t _{CSH}	58		68		ns	22
CAS setup time (CBR REFRESH)	t _{CSR}	7		7		ns	4, 21
CAS to WE delay time	t _{CWD}	42		47		ns	21, 28
Write command to CAS lead time	t _{CWL}	15		20		ns	
Data-in hold time	t _{DH}	15		20		ns	23, 27
Data-in hold time (referenced to RAS)	t _{DHR}	45		55		ns	
Data-in setup time	t _{DS}	-2		-2		ns	22, 27
Output disable	t _{OD}	3	15	3	20	ns	30
Output enable	t _{OE}		15		20	ns	
OE hold time from WE during READ-MODIFY-WRITE cycle	t _{OEH}	13		13		ns	22
Output buffer turn-off delay	t _{OFF}	5	20	5	25	ns	19, 25, 33

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
OE setup prior to RAS during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	19
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	35		40		ns	
PDE to valid presence-detect data	t_{PD}		10		10	ns	32
PDE inactive to presence-detects inactive	t_{PDOFF}	2		2		ns	32
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	87		97		ns	21
Access time from RAS	t_{RAC}		60		70	ns	13
RAS to column-address delay time	t_{RAD}	13	25	13	30	ns	17, 24
Row-address hold time	t_{RAH}	8		8		ns	22
Column-address to RAS lead time	t_{RAL}	35		40		ns	23
RAS pulse width	t_{RAS}	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		130		ns	
RAS to CAS delay time	t_{RCD}	18	40	18	45	ns	16, 24
Read command hold time (referenced to CAS)	t_{RCH}	2		2		ns	18, 21
Read command setup time	t_{RCS}	2		2		ns	21
Refresh period (2,048 cycles)	t_{REF}		32		32	ms	
RAS precharge time	t_{RP}	40		50		ns	
RAS to CAS precharge time	t_{RPC}	0		0		ns	
Read command hold time (referenced to RAS)	t_{RRH}	0		0		ns	18
RAS hold time	t_{RSH}	20		25		ns	23
READ WRITE cycle time	t_{RWC}	155		185		ns	23
RAS to WE delay time	t_{RWD}	87		97		ns	21, 28
Write command to RAS lead time	t_{RWL}	20		25		ns	23
Transition time (rise or fall)	t_T	3	50	3	50	ns	
Write command hold time	t_{WCH}	15		20		ns	23
Write command hold time (referenced to RAS)	t_{WCR}	43		53		ns	22
WE command setup time	t_{WCS}	2		2		ns	21, 28
Write command pulse width	t_{WP}	10		15		ns	
WE hold time (CBR REFRESH)	t_{WRH}	8		8		ns	22
WE setup time (CBR REFRESH)	t_{WRP}	12		12		ns	21

NEW DRAM DIMM

EDO PAGE MODE**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Access time from column-address	t_{AA}		35		40	ns	23
Column-address setup to $\overline{CAS}$ precharge during writes	t_{ACH}	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	t_{AR}	43		48		ns	22
Column-address setup time	t_{ASC}	2		2		ns	21
Row-address setup time	t_{ASR}	5		5		ns	23
Column-address to $\overline{WE}$ delay time	t_{AWD}	57		62		ns	21, 28
Access time from $\overline{CAS}$	t_{CAC}		20		25	ns	14, 23
Column-address hold time	t_{CAH}	15		17		ns	23
$\overline{CAS}$ pulse width	t_{CAS}	12	10,000	12	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	t_{CHR}	8		10		ns	4, 22
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	2		2		ns	21
Data output hold after $\overline{CAS}$ LOW	t_{COH}	5		5		ns	21
$\overline{CAS}$ precharge time	t_{CP}	10		10		ns	15
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45	ns	23
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	23
$\overline{CAS}$ hold time	t_{CSH}	48		53		ns	22
$\overline{CAS}$ setup time (CBR REFRESH)	t_{CSR}	7		7		ns	4, 21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	37		42		ns	21, 28
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		ns	
Data-in hold time	t_{DH}	15		17		ns	23, 27
Data-in hold time (referenced to $\overline{RAS}$)	t_{DHR}	45		55		ns	
Data-in setup time	t_{DS}	-2		-2		ns	22, 27
Output disable	t_{OD}	0	15	0	15	ns	
Output enable	t_{OE}		15		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	t_{OEH}	10		10		ns	22
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	t_{OEHC}	10		10		ns	
$\overline{OE}$ HIGH pulse width	t_{OEP}	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	t_{OES}	5		5		ns	
Output buffer turn-off delay	t_{OFF}	5	20	5	20	ns	19, 25, 33
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	19
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	25		30		ns	
PDE to valid presence-detect data	t_{PD}		10		10	ns	32
PDE inactive to presence-detects inactive	$t_{PD OFF}$	2		2		ns	32
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	77		87		ns	21
Access time from $\overline{RAS}$	t_{RAC}		60		70	ns	13
$\overline{RAS}$ to column-address delay time	t_{RAD}	10	25	10	30	ns	17, 24
Row-address hold time	t_{RAH}	8		8		ns	22
Column-address to $\overline{RAS}$ lead time	t_{RAL}	35		40		ns	23
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	t_{RASP}	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	105		125		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	40	12	45	ns	16, 24
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	2		2		ns	18, 21

NEW
DRAM DIMM

6111549 0013784 515

EDO PAGE MODE**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Read command setup time	t_{RCS}	2		2		ns	21
Refresh period (2,048 cycles)	t_{REF}		32		32	ms	
RAS precharge time	t_{RP}	40		50		ns	
RAS to CAS precharge time	t_{RPC}	5		5		ns	
Read command hold time (referenced to RAS)	t_{RRH}	0		0		ns	18
RAS hold time	t_{RSH}	18		20		ns	23
READ WRITE cycle time	t_{RWC}	150		175		ns	23
RAS to WE delay time	t_{RWD}	82		92		ns	21, 28
Write command to RAS lead time	t_{RWL}	20		20		ns	23
Transition time (rise or fall)	t_T	2	50	2	50	ns	
Write command hold time	t_{WCH}	15		17		ns	23
Write command hold time (referenced to RAS)	t_{WCR}	43		53		ns	22
WE command setup time	t_{WCS}	2		2		ns	21, 28
Output disable delay from WE (CAS HIGH)	t_{WHZ}	2	18	2	20	ns	25
Write command pulse width	t_{WP}	10		12		ns	
WE pulse width for output disable when CAS HIGH	t_{WPZ}	10		12		ns	
WE hold time (CBR REFRESH)	t_{WRH}	8		8		ns	22
WE setup time (CBR REFRESH)	t_{WRP}	12		12		ns	21

NEW
DRAM DIMM

NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = +5V$; $f = 1\text{ MHz}$.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
6. An initial pause of $100\mu s$ is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the 'REF refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$ for FAST PAGE MODE and $2.5ns$ for EDO PAGE MODE.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
11. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and $100pF$ and $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
13. Assumes that $t_{RCD} < t_{RCD}(\text{MAX})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
14. Assumes that $t_{RCD} \geq t_{RCD}(\text{MAX})$.
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for t_{CPN} .
16. Operation within the $t_{RCD}(\text{MAX})$ limit ensures that $t_{RAC}(\text{MAX})$ can be met. $t_{RCD}(\text{MAX})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{MAX})$ limit, access time is controlled exclusively by t_{CAC} .
17. Operation within the $t_{RAD}(\text{MAX})$ limit ensures that $t_{RAC}(\text{MIN})$ can be met. $t_{RAD}(\text{MAX})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{MAX})$ limit, access time is controlled exclusively by t_{AA} .
18. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
19. $t_{OFF}(\text{MAX})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = \text{LOW}$ and $\overline{OE} = \text{HIGH}$.
21. A $+2ns$ timing skew from the DRAM to the module resulted from the addition of line drivers.
22. A $-2ns$ timing skew from the DRAM to the module resulted from the addition of line drivers.
23. A $+5ns$ timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A $-2ns$ (MIN) and a $-5ns$ (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A $+2ns$ (MIN) and a $+5ns$ (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
26. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by one-half when used in the x32 mode.
27. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
28. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS}(\text{MIN})$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{MIN})$, $t_{AWD} \geq t_{AWD}(\text{MIN})$ and $t_{CWD} \geq t_{CWD}(\text{MIN})$, the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$ -controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
29. Column-address changed once each cycle.

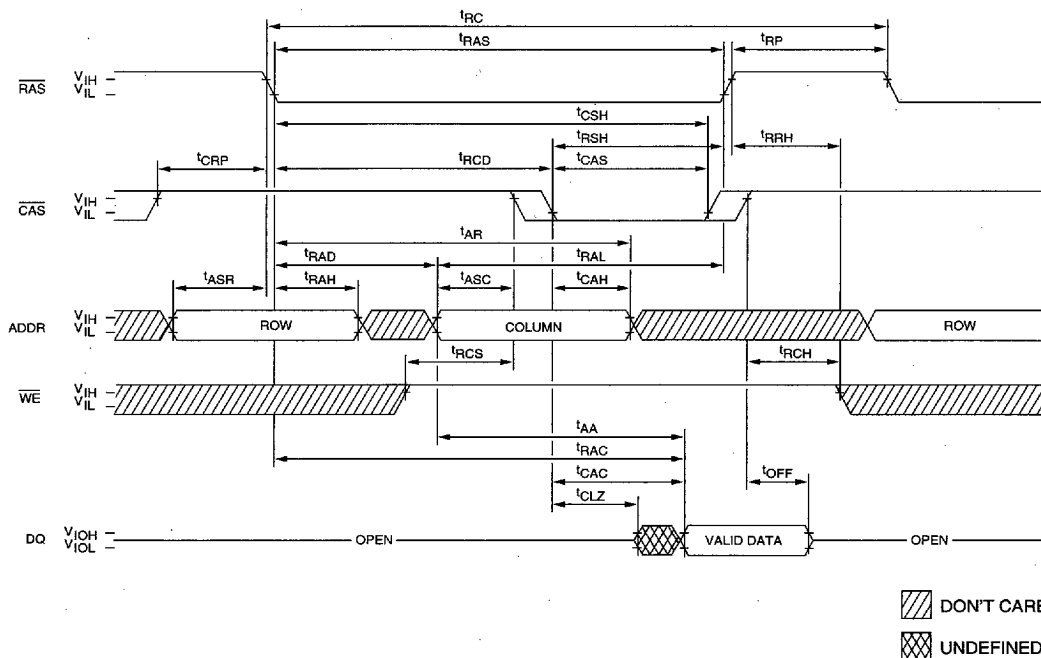
NEW
DRAM DIMM

NOTES (continued)

30. The 3ns minimum is a parameter guaranteed by design.
31. $t_{PD\text{OFF}} \text{ MAX}$ is determined by the pullup resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
32. Measured with the specified current load and 100pf.
33. For FAST PAGE MODE option, t_{OFF} is determined by the first $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ signal to transition HIGH. In comparison, t_{OFF} on an EDO option is determined by the latter of the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signal to transition HIGH.
34. Applies to both EDO and FAST PAGE MODE modules.

**NEW
DRAM DIMM**

READ CYCLE (FAST PAGE MODE Module)

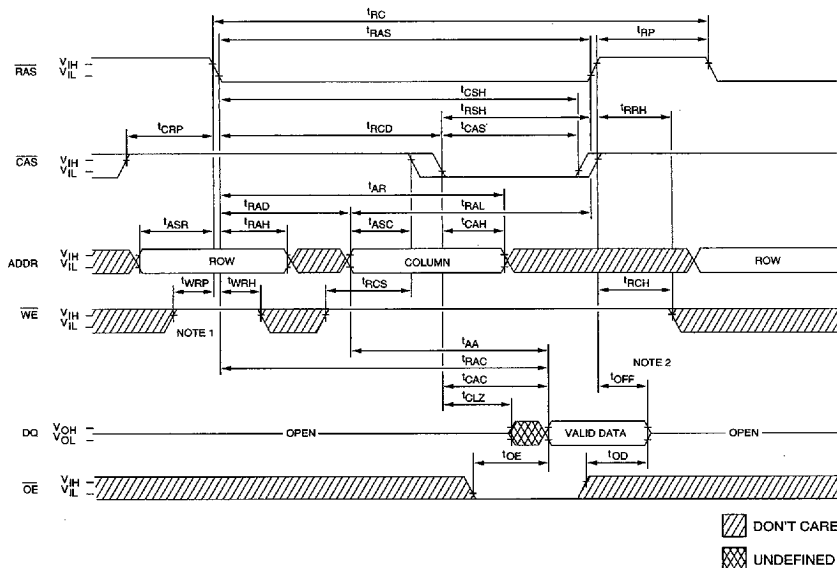


FAST PAGE MODE TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		35		40	ns
t_{AR}	48		53		ns
t_{ASC}	2		2		ns
t_{ASR}	5		5		ns
t_{CAC}		20		25	ns
t_{CAH}	15		20		ns
t_{CAS}	15	10,000	20	10,000	ns
t_{CLZ}	5		5		ns
t_{CRP}	10		10		ns
t_{CSH}	58		68		ns
t_{OD}	3	15	3	20	ns
t_{OE}		15		20	ns
t_{OFF}	5	20	5	25	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{RAC}		60		70	ns
t_{RAD}	13	25	13	30	ns
t_{RAH}	8		8		ns
t_{RAL}	35		40		ns
t_{RAS}	60	10,000	70	10,000	ns
t_{RC}	110		130		ns
t_{RCD}	18	40	18	45	ns
t_{RCH}	2		2		ns
t_{RCS}	2		2		ns
t_{RP}	40		50		ns
t_{RRH}	0		0		ns
t_{RSH}	20		25		ns

READ CYCLE (EDO PAGE MODE Module)

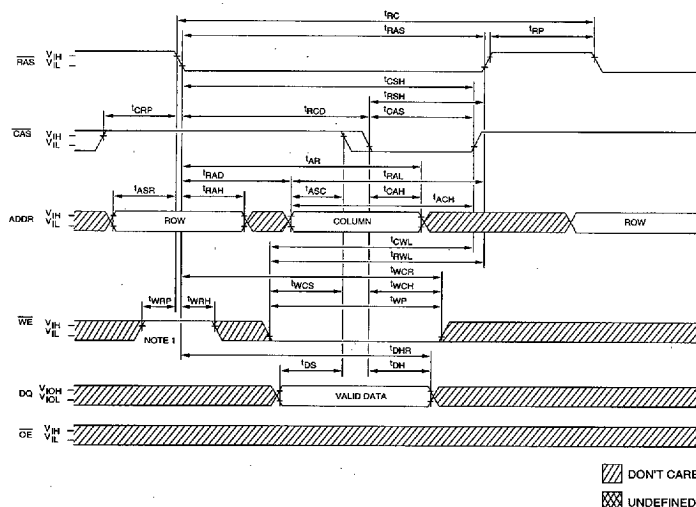


- NOTE:**
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for $\overline{WRP}$ and $\overline{WRH}$. This design implementation will facilitate compatibility with future EDO DRAMS.
 2. $\overline{OFF}$ is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ AA		35		40	ns
¹ AR	43		48		ns
¹ ASC	2		2		ns
¹ ASR	5		5		ns
¹ CAC		20		25	ns
¹ CAH	15		17		ns
¹ CAS	12	10,000	12	10,000	ns
¹ CLZ	2		2		ns
¹ CRP	10		10		ns
¹ CSH	48		53		ns
¹ OD	0	15	0	15	ns
¹ OE		15		20	ns
¹ OFF	5	20	5	20	ns
¹ RAC		60		70	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
1RAD	10	25	10	30	ns
1RAH	8		8		ns
1RAL	35		40		ns
1RAS	60	10,000	70	10,000	ns
1RC	105		125		ns
1RCD	12	40	12	45	ns
1RCH	2		2		ns
1RCS	2		2		ns
1RP	40		50		ns
1RRH	0		0		ns
1RSH	18		20		ns
1WRH	8		8		ns
1WRP	12		12		ns

EARLY WRITE CYCLE ³⁴


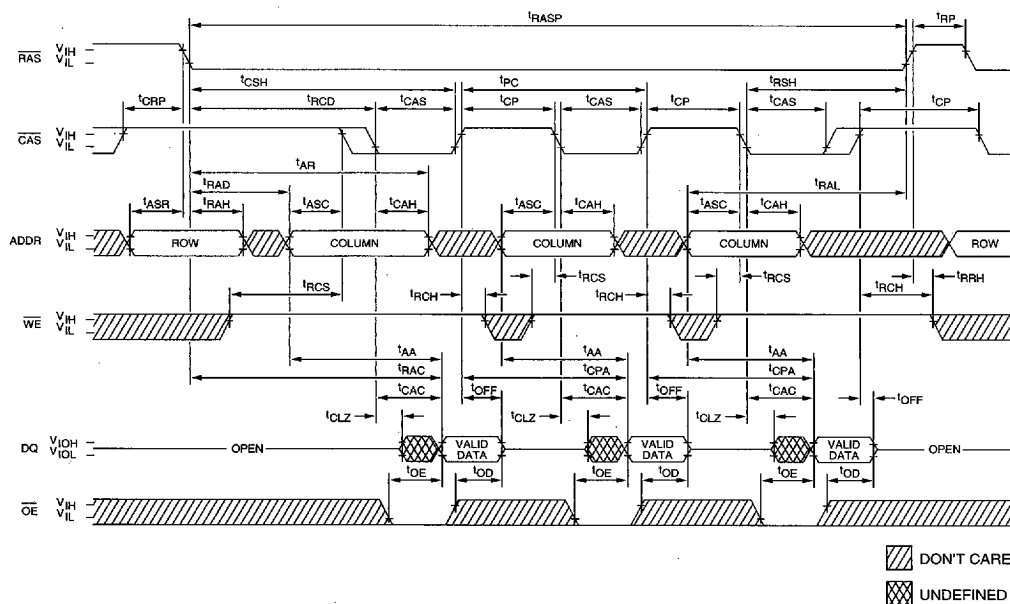
NOTE: 1. Although **WE** is a "don't care" at **RAS** time during an access cycle (READ or WRITE), the system designer should implement **WE** HIGH for **tWRP** and **tWRH**. This design implementation will facilitate compatibility with future EDO DRAMs.

**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{ACH} (EDO)	15		15		ns
t _{AR} (FPM)	48		53		ns
t _{AR} (EDO)	43		48		ns
t _{ASC}	2		2		ns
t _{ASR}	5		5		ns
t _{CAH} (FPM)	15		20		ns
t _{CAH} (EDO)	15		17		ns
t _{CAS} (FPM)	15	10,000	20	10,000	ns
t _{CAS} (EDO)	12	10,000	12	10,000	ns
t _{CRP}	10		10		ns
t _{CSH} (FPM)	58		68		ns
t _{CSH} (EDO)	48		53		ns
t _{CWL} (FPM)	15		20		ns
t _{CWL} (EDO)	15		15		ns
t _{DH} (FPM)	15		20		ns
t _{DH} (EDO)	15		17		ns
t _{DHR}	45		55		ns
t _{DS}	-2		-2		ns
t _{RAD} (FPM)	13	25	13	30	ns
t _{RAD} (EDO)	10	25	10	30	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{RAH}	8		8		ns
t _{RAL}	35		40		ns
t _{RAS}	60	10,000	70	10,000	ns
t _{RC} (FPM)	110		130		ns
t _{RC} (EDO)	105		125		ns
t _{RCD} (FPM)	18	40	18	45	ns
t _{RCD} (EDO)	12	40	12	45	ns
t _{RP}	40		50		ns
t _{RSH} (FPM)	20		25		ns
t _{RSH} (EDO)	18		20		ns
t _{RWL} (FPM)	20		25		ns
t _{RWL} (EDO)	20		20		ns
t _{WCH} (FPM)	15		20		ns
t _{WCH} (EDO)	15		17		ns
t _{WCR}	43		53		ns
t _{WCS}	2		2		ns
t _{WP} (FPM)	10		15		ns
t _{WP} (EDO)	10		12		ns
t _{WRH}	8		8		ns
t _{WRP}	12		12		ns

FAST-PAGE-MODE READ CYCLE



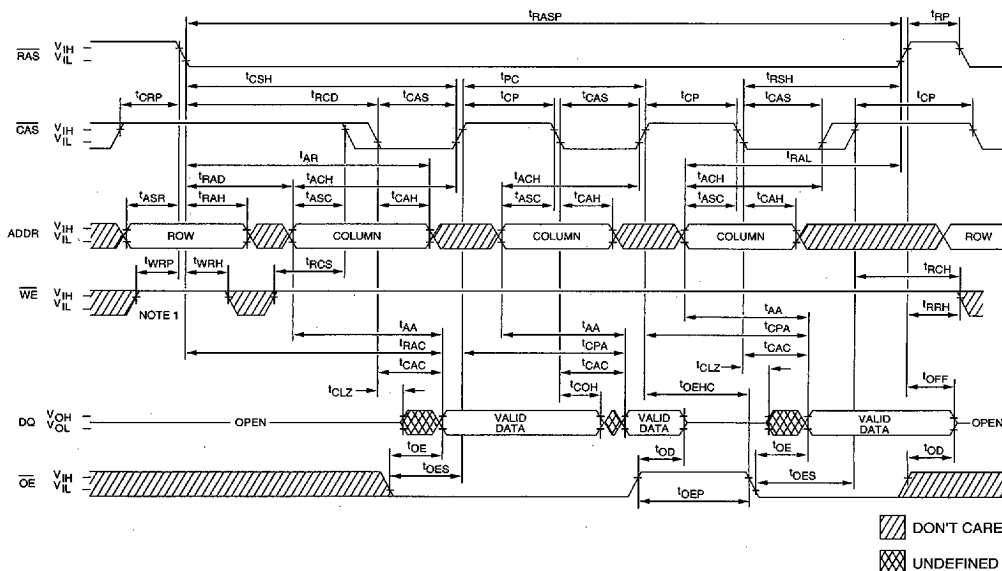
NEW ■ DRAM DIMM

FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
1AA		35		40	ns
1AR	48		53		ns
1ASC	2		2		ns
1ASR	5		5		ns
1CAC		20		25	ns
1CAH	15		20		ns
1CAS	15	10,000	20	10,000	ns
1CLZ	5		5		ns
1CP	10		10		ns
1CPA		40		45	ns
1CRP	10		10		ns
1CSH	58		68		ns
1OD	3	15	3	20	ns
1OE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
1OFF	5	20	5	25	ns
1PC	35		40		ns
1RAC		60		70	ns
1RAD	13	25	13	30	ns
1RAH	8		8		ns
1RAL	35		40		ns
1RASP	60	100,000	70	100,000	ns
1RCD	18	40	18	45	ns
1RCH	2		2		ns
1RCS	2		2		ns
1RP	40		50		ns
1RRH	0		0		ns
1RSH	20		25		ns

EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for 1WRP and 1WRH . This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

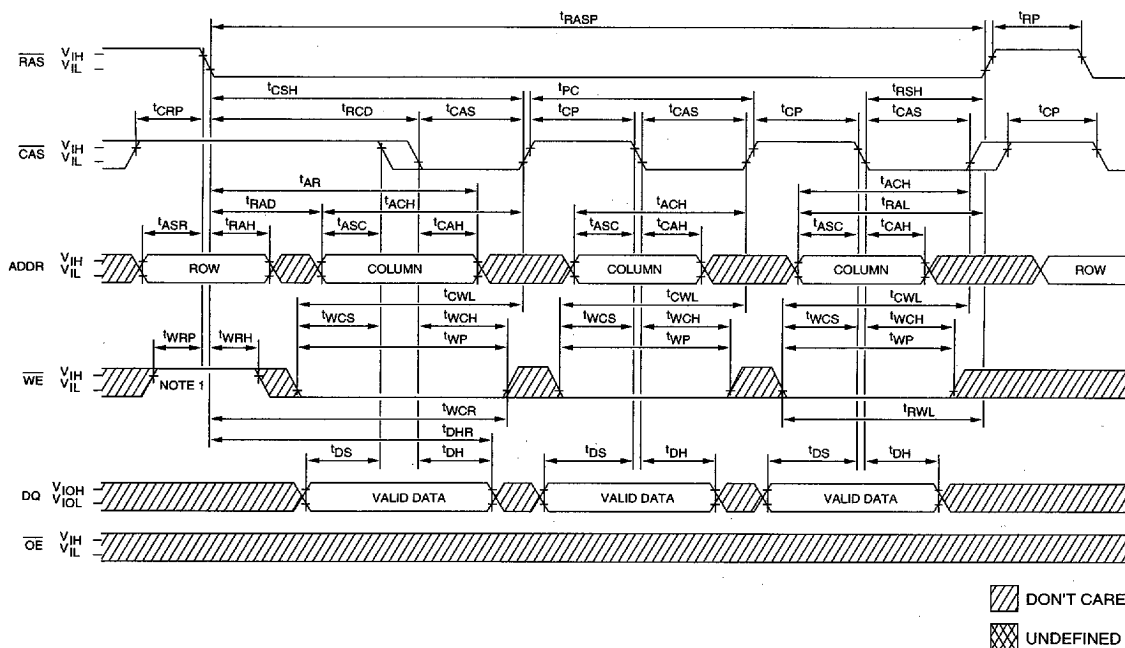
	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
'AA		35		40	ns
'ACH	15		15		ns
'AR	43		48		ns
'ASC	2		2		ns
'ASR	5		5		ns
'CAC		20		25	ns
'CAH	15		17		ns
'CAS	12	10,000	12	10,000	ns
'CLZ	2		2		ns
'COH	5		5		ns
'CP	10		10		ns
'CPA		40		45	ns
'CRP	10		10		ns
'CSH	48		53		ns
'OD	0	15	0	15	ns
'OE		15		20	ns
'OEHC	10		10		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
OE P	10		10		ns
OES	5		5		ns
OFF	5	20	5	20	ns
PC	25		30		ns
RAC		60		70	ns
RAD	10	25	10	30	ns
RAH	8		8		ns
RAL	35		40		ns
RASP	60	125,000	70	125,000	ns
RCD	12	40	12	45	ns
RCH	2		2		ns
RCS	2		2		ns
RP	40		50		ns
RRH	0		0		ns
RSH	18		20		ns
WRH	8		8		ns
WRP	12		12		ns

[illegible]

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
↑AR	48		53		ns
↑ASC	2		2		ns
↑ASR	5		5		ns
↑CAH	15		20		ns
↑CAS	15	10,000	20	10,000	ns
↑CP	10		10		ns
↑CRP	10		10		ns
↑CSH	58		68		ns
↑CWL	15		20		ns
↑DH	15		20		ns
↑DHR	45		55		ns
↑DS	-2		-2		ns
↑PC	35		40		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ RAD	13	25	13	30	ns
¹ RAH	8		8		ns
¹ RAL	35		40		ns
¹ RASP	60	100,000	70	100,000	ns
¹ RCD	18	40	18	45	ns
¹ RP	40		50		ns
¹ RSH	20		25		ns
¹ RWL	20		25		ns
¹ WCH	15		20		ns
¹ WCR	43		53		ns
¹ WCS	2		2		ns
¹ WP	10		15		ns

EDO-PAGE-MODE EARLY-WRITE CYCLE


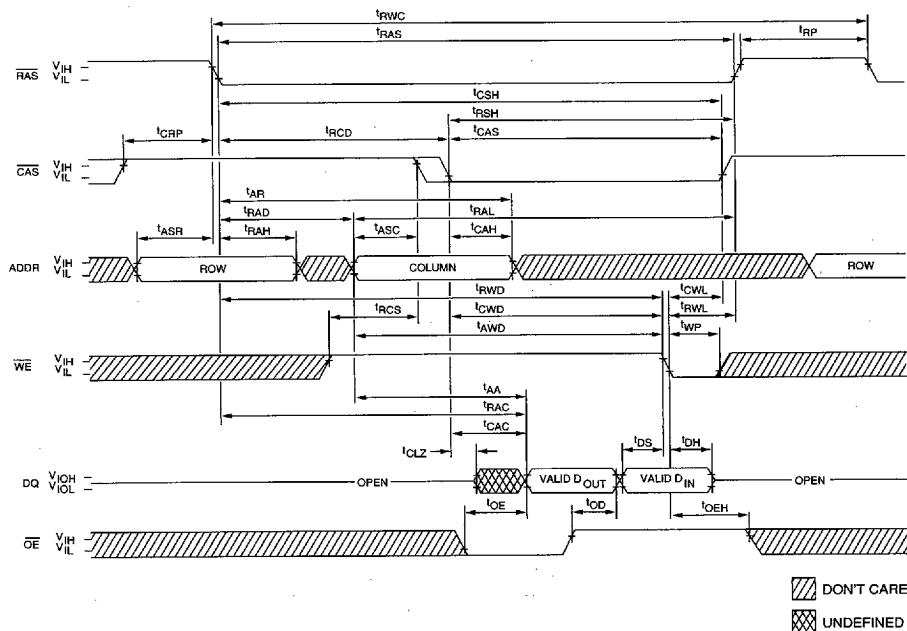
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{ACH}	15		15		ns
t_{AR}	43		48		ns
t_{ASC}	2		2		ns
t_{ASR}	5		5		ns
t_{CAH}	15		17		ns
t_{CAS}	12	10,000	12	10,000	ns
t_{CP}	10		10		ns
t_{CRP}	10		10		ns
t_{CSH}	48		53		ns
t_{CWL}	15		15		ns
t_{DH}	15		17		ns
t_{DHR}	45		55		ns
t_{DS}	-2		-2		ns
t_{PC}	25		30		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{RAD}	10	25	10	30	ns
t_{RAH}	8		8		ns
t_{RAL}	35		40		ns
t_{RASP}	60	125,000	70	125,000	ns
t_{RCD}	12	40	12	45	ns
t_{RP}	40		50		ns
t_{RSH}	18		20		ns
t_{RWL}	20		20		ns
t_{WCH}	15		17		ns
t_{WCR}	43		53		ns
t_{WCS}	2		2		ns
t_{WP}	10		12		ns
t_{WRH}	8		8		ns
t_{WRP}	12		12		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

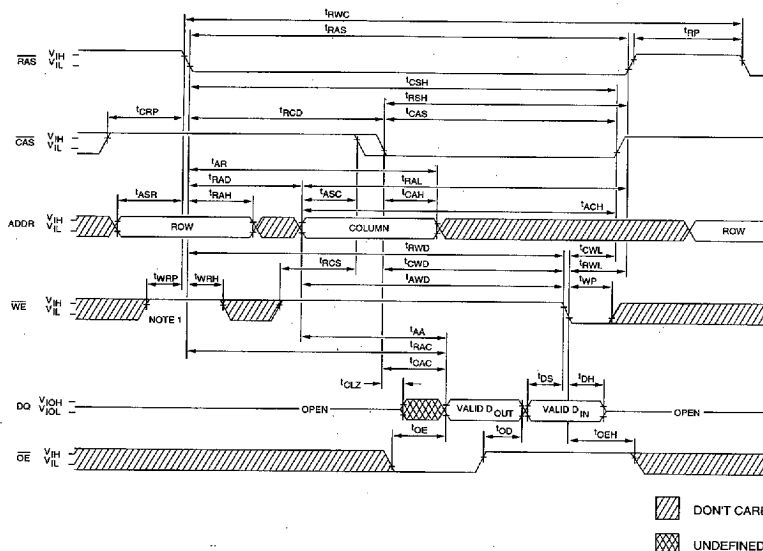


FAST PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tAA		35		40	ns
tAR	48		53		ns
tASC	2		2		ns
tASR	5		5		ns
tAWD	57		62		ns
tCAC		20		25	ns
tCAH	15		20		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	5		5		ns
tCRP	10		10		ns
tCSH	58		68		ns
tCWD	42		47		ns
tCWL	15		20		ns
tDH	15		20		ns
tDS	-2		-2		ns
tOD	3	15	3	20	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tOE		15		20	ns
tOEH	13		13		ns
tRAC		60		70	ns
tRAD	13	25	13	30	ns
tRAH	8		8		ns
tRAL	35		40		ns
tRAS	60	10,000	70	10,000	ns
tRCD	18	40	18	45	ns
tRCS	2		2		ns
tRP	40		50		ns
tRSH	20		25		ns
tRWC	155		185		ns
tRWD	87		97		ns
tRWL	20		25		ns
tWP	10		15		ns

READ WRITE CYCLE **(LATE WRITE and READ-MODIFY-WRITE cycles)**



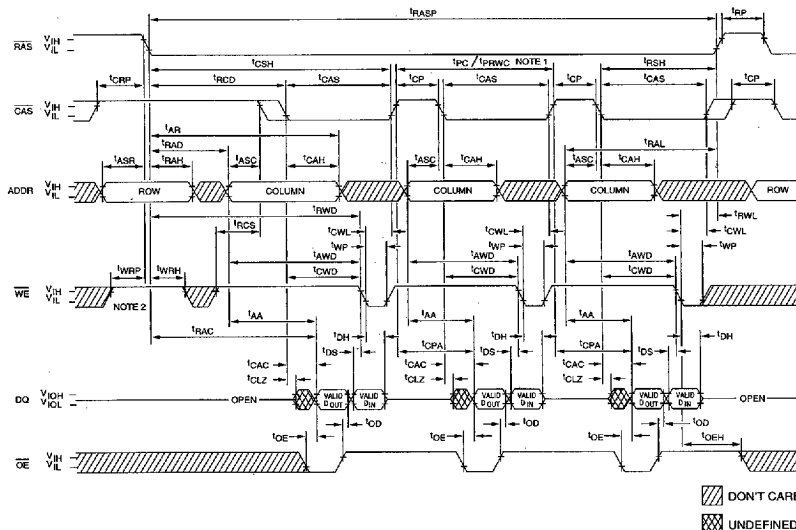
NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE **TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tAA		35		40	ns
tACH	15		15		ns
tAR	43		48		ns
tASC	2		2		ns
tASR	5		5		ns
tAWD	57		62		ns
tCAC		20		25	ns
tCAH	15		17		ns
tCAS	12	10,000	12	10,000	ns
tCLZ	2		2		ns
tCRP	10		10		ns
tCSH	48		53		ns
tCWD	37		42		ns
tCWL	15		15		ns
tDH	15		17		ns
tDS	-2		-2		ns
tOD	0	15	0	15	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tOE		15		20	ns
tOEH	10		10		ns
tRAC		60		70	ns
tRAD	10	25	10	30	ns
tRAH	8		8		ns
tRAL	35		40		ns
tRAS	60	10,000	70	10,000	ns
tRCD	12	40	12	45	ns
tRCS	2		2		ns
tRP	40		50		ns
tRSH	18		20		ns
tRWC	150		175		ns
tRWD	82		92		ns
tRWL	20		20		ns
tWP	10		12		ns
tWRH	8		8		ns
tWRP	12		12		ns

FAST-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



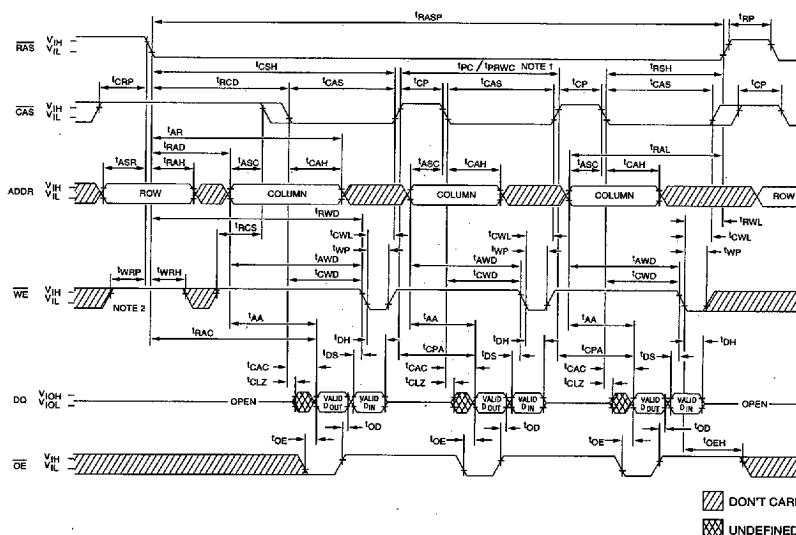
- NOTE:**
1. $\overline{\text{PC}}$ is for LATE WRITE cycles only.
 2. Although $\overline{\text{WE}}$ is a "don't care" at $\overline{\text{RAS}}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{\text{WE}}$ HIGH for $\overline{\text{WRP}}$ and $\overline{\text{WRH}}$. This design implementation will facilitate compatibility with future EDO DRAMS.

FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
1AA		35		40	ns
1AR	48		53		ns
1ASC	2		2		ns
1ASR	5		5		ns
1AWD	57		62		ns
1CAC		20		25	ns
1CAH	15		20		ns
1CAS	15	10,000	20	10,000	ns
1CLZ	5		5		ns
1CP	10		10		ns
1CPA		40		45	ns
1CRP	10		10		ns
1CSH	58		68		ns
1CWD	42		47		ns
1CWL	15		20		ns
1DH	15		20		ns
1DS	-2		-2		ns
1OD	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ OE		15		20	ns
¹ OEH	13		13		ns
¹ PC	35		40		ns
¹ PRWC	87		97		ns
¹ RAC		60		70	ns
¹ RAD	13	25	13	30	ns
¹ RAH	8		8		ns
¹ RAL	35		40		ns
¹ RASP	60	100,000	70	100,000	ns
¹ RCD	18	40	18	45	ns
¹ RCS	2		2		ns
¹ RP	40		50		ns
¹ RSH	20		25		ns
¹ RWD	87		97		ns
¹ RWL	20		25		ns
¹ WP	10		15		ns
¹ WRH	8		8		ns
¹ WRP	12		12		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



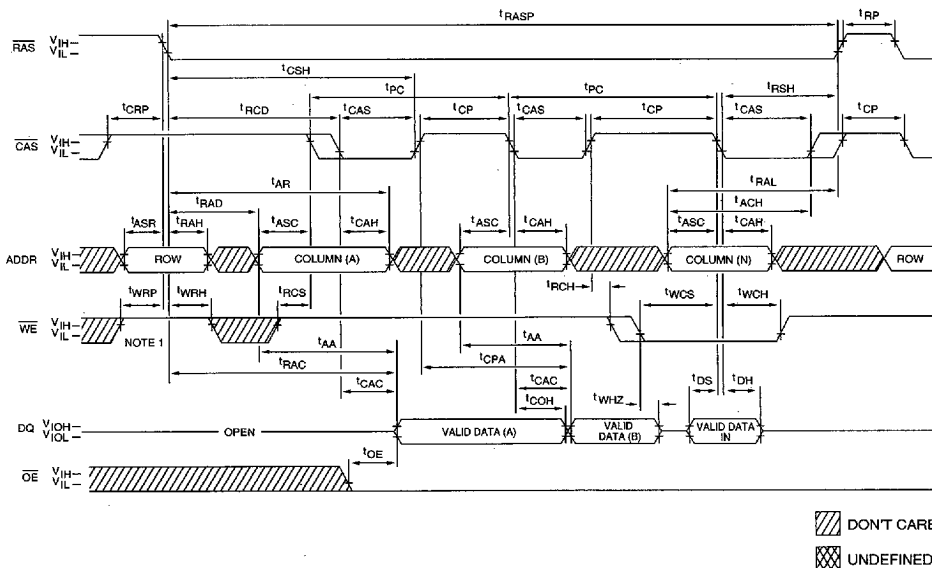
- NOTE:**
1. t_{PC} is for LATE WRITE cycles only.
 2. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

**EDO PAGE MODE
TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		35		40	ns
t_{AR}	43		48		ns
t_{ASC}	2		2		ns
t_{ASR}	5		5		ns
t_{AWD}	57		62		ns
t_{CAC}		20		25	ns
t_{CAH}	15		17		ns
t_{CAS}	12	10,000	12	10,000	ns
t_{CLZ}	2		2		ns
t_{CP}	10		10		ns
t_{CPA}		40		45	ns
t_{CRP}	10		10		ns
t_{CSH}	48		53		ns
t_{CWD}	37		42		ns
t_{CWL}	15		15		ns
t_{DH}	15		17		ns
t_{DS}	-2		-2		ns
t_{OD}	0	15	0	15	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{OE}		15		20	ns
t_{OEH}	10		10		ns
t_{PC}	25		30		ns
t_{PRWC}	77		87		ns
t_{RAC}		60		70	ns
t_{RAD}	10	25	10	30	ns
t_{RAH}	8		8		ns
t_{RAL}	35		40		ns
t_{RASP}	60	125,000	70	125,000	ns
t_{RCD}	12	40	12	45	ns
t_{RCS}	2		2		ns
t_{RP}	40		50		ns
t_{RSH}	18		20		ns
t_{RWD}	82		92		ns
t_{RWL}	20		20		ns
t_{WP}	10		12		ns
t_{WRH}	8		8		ns
t_{WRP}	12		12		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY-WRITE)

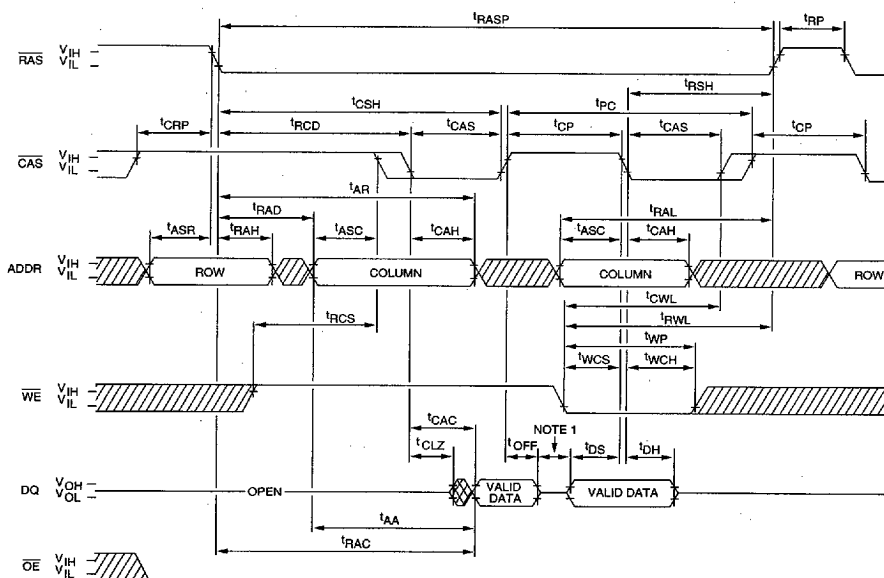


NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
AA		35		40	ns
ACH	15		15		ns
AR	43		48		ns
ASC	2		2		ns
ASR	5		5		ns
CAC		20		25	ns
CAH	15		17		ns
CAS	12	10,000	12	10,000	ns
COH	5		5		ns
CP	10		10		ns
CFA		40		45	ns
CRP	10		10		ns
CSH	48		53		ns
DH	15		17		ns
DS	-2		-2		ns
OE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^t PC	25		30		ns
^t RAC		60		70	ns
^t RAD	10	25	10	30	ns
^t RAH	8		8		ns
^t RAL	35		40		ns
^t RASP	60	125,000	70	125,000	ns
^t RCD	12	40	12	45	ns
^t RCH	2		2		ns
^t RCS	2		2		ns
^t RP	40		50		ns
^t RSR	18		20		ns
^t WCH	15		17		ns
^t WCS	2		2		ns
^t WHZ	2	18	2	20	ns
^t WRH	8		8		ns
^t WRP	12		12		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)


DON'T CARE
 UNDEFINED

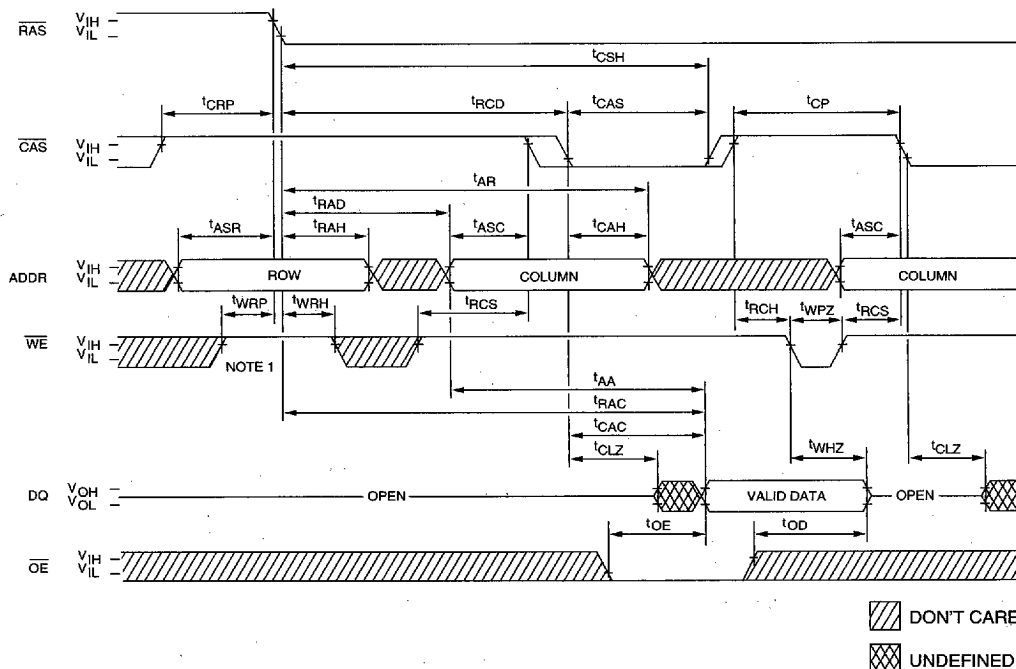
NOTE: 1. Do not drive data prior to tristate.

FAST PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		35		40	ns
t _{AR}	48		53		ns
t _{ASC}	2		2		ns
t _{ASR}	5		5		ns
t _{CAC}		20		25	ns
t _{CAH}	15		20		ns
t _{CAS}	15	10,000	20	10,000	ns
t _{CLZ}	5		5		ns
t _{CP}	10		10		ns
t _{CRP}	10		10		ns
t _{CSH}	58		68		ns
t _{CWL}	15		20		ns
t _{DH}	15		20		ns
t _{DS}	-2		-2		ns
t _{OFF}	5	20	5	25	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{PC}	35		40		ns
t _{RAC}		60		70	ns
t _{RAD}	13	25	13	30	ns
t _{RAH}	8		8		ns
t _{RAL}	35		40		ns
t _{RASP}	60	100,000	70	100,000	ns
t _{RCD}	18	40	18	45	ns
t _{RCS}	2		2		ns
t _{RP}	40		50		ns
t _{RSH}	20		25		ns
t _{RWL}	20		25		ns
t _{WCH}	15		20		ns
t _{WCS}	2		2		ns
t _{WP}	10		15		ns

EDO READ CYCLE
(with $\overline{WE}$ -controlled disable)



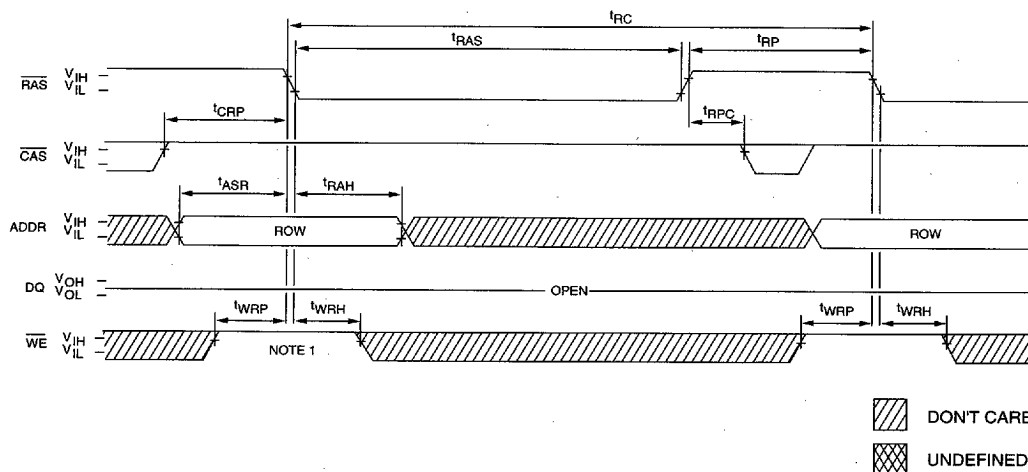
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE
TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{AA}		35		40	ns
t_{AR}	43		48		ns
t_{ASC}	2		2		ns
t_{ASR}	5		5		ns
t_{CAC}		20		25	ns
t_{CAH}	15		17		ns
t_{CAS}	12	10,000	12	10,000	ns
t_{CLZ}	2		2		ns
t_{CP}	10		10		ns
t_{CRP}	10		10		ns
t_{CSH}	48		53		ns
t_{OD}	0	15	0	15	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{OE}		15		20	ns
t_{RAC}		60		70	ns
t_{RAD}	10	25	10	30	ns
t_{RAH}	8		8		ns
t_{RCD}	12	40	12	45	ns
t_{RCH}	2		2		ns
t_{RCS}	2		2		ns
t_{WHZ}	2	18	2	20	ns
t_{WPZ}	10		12		ns
t_{WRH}	8		8		ns
t_{WRP}	12		12		ns

RAS-ONLY REFRESH CYCLE



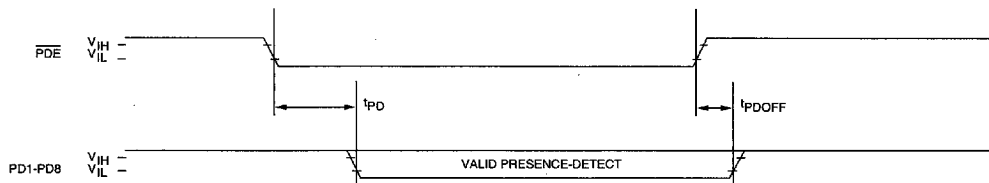
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH}. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

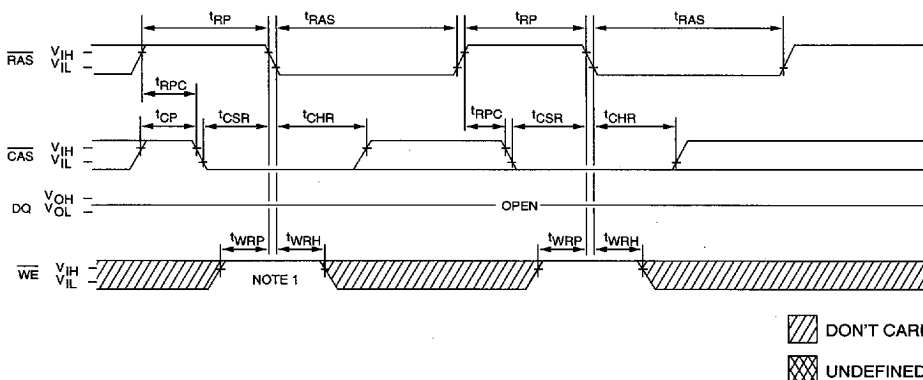
SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	5		5		ns
t _{CRP}	10		10		ns
t _{RAH}	8		8		ns
t _{RAS}	60	10,000	70	10,000	ns
t _{RC} (FPM)	110		130		ns
t _{RC} (EDO)	105		125		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{RP}	40		50		ns
t _{RPC} (FPM)	0		0		ns
t _{RPC} (EDO)	5		5		ns
t _{WRH}	8		8		ns
t _{WRP}	12		12		ns

PRESENCE-DETECT READ CYCLE ³⁴



CBR REFRESH CYCLE ³⁴
(Addresses, $\overline{OE}$ = DON'T CARE)



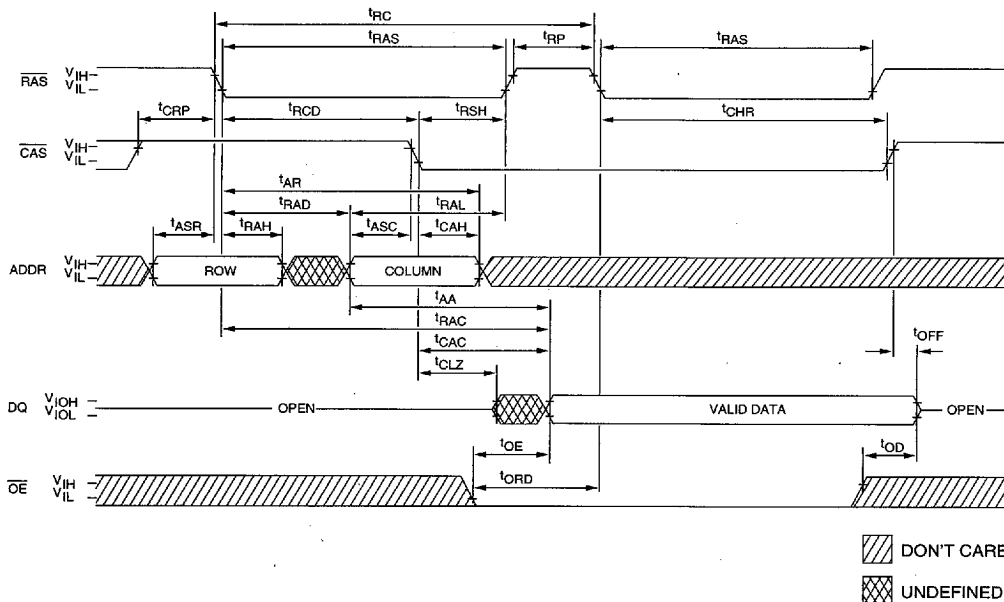
NOTE:

1. t_{WRP} and t_{WRH} are for system design reference only. The $\overline{WE}$ signal is actually a "don't care" at t_{RAS} time during a CBR REFRESH. However, $\overline{WE}$ should be held HIGH at t_{RAS} time during a CBR REFRESH to ensure compatibility with other DRAMs which require $\overline{WE}$ HIGH at t_{RAS} time during a CBR REFRESH.
2. PD pins must be pulled HIGH at next level.

FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{CHR} (FPM)	13		13		ns
t_{CHR} (EDO)	8		10		ns
t_{CP}	10		10		ns
t_{CSR}	7		7		ns
t_{PD}		10		10	ns
t_{PDOff}	2		2		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t_{RAS}	60	10,000	70	10,000	ns
t_{RP}	40		50		ns
t_{RPC} (FPM)	0		0		ns
t_{RPC} (EDO)	5		5		ns
t_{WRH}	8		8		ns
t_{WRP}	12		12		ns

HIDDEN REFRESH CYCLE^{20, 34}
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t _{AA}		35		40	ns
t _{AR} (FPM)	48		53		ns
t _{AR} (EDO)	43		48		ns
t _{ASC}	2		2		ns
t _{ASR}	5		5		ns
t _{CAC}		20		25	ns
t _{CAH} (FPM)	15		20		ns
t _{CAH} (EDO)	15		17		ns
CHR (FPM)	13		13		ns
t _{CHR} (EDO)	8		10		ns
t _{CLZ} (FPM)	5		5		ns
t _{CLZ} (EDO)	2		2		ns
t _{CRP}	10		10		ns
t _{OD} (FPM)	3	15	3	20	ns
t _{OD} (EDO)	0	15	0	15	ns
t _{OE}		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t _{OFF} (FPM)	5	20	5	25	ns
t _{OFF} (EDO)	5	20	5	20	ns
t _{ORD}	0		0		ns
t _{RAC}		60		70	ns
t _{RAD} (FPM)	13	25	13	30	ns
t _{RAD} (EDO)	10	25	10	30	ns
t _{RAH}	8		8		ns
t _{RAL}	35		40		ns
t _{RAS}	60	10,000	70	10,000	ns
t _{RC} (FPM)	110		130		ns
t _{RC} (EDO)	105		125		ns
t _{RCD} (FPM)	18	40	18	45	ns
t _{RCD} (EDO)	12	40	12	45	ns
t _{RP}	40		50		ns
t _{RSH} (FPM)	20		25		ns
t _{RSH} (EDO)	18		20		ns