

# MSC1215-xx

## 17 × 2 Duplex Driver with Dimming, Keyscan and A/D Converter Function

### GENERAL DESCRIPTION

The MSC1215-xx is a 1/2-duty vacuum fluorescent display tube driver implemented in Bi-CMOS technology. This LSI consists of a 37-bit shift register, 34 latches, an analog dimming circuit, (a PWM conversion circuit), a 3×4 keyscan circuit, a 6ch-6-bit A/D converter and 17 segment drivers, and 2-grid pre-drivers.

The MSC1215-xx has capabilities of displaying audio system frequencies and various informations on a VFD tube for the automobile application and also interfacing with keyboard inputs and on an analog volume input.

For automobile audio systems, the front panel functions (such as a frequency display, keyboard input and analog voltage input from a volume) can be accomplished by this IC.

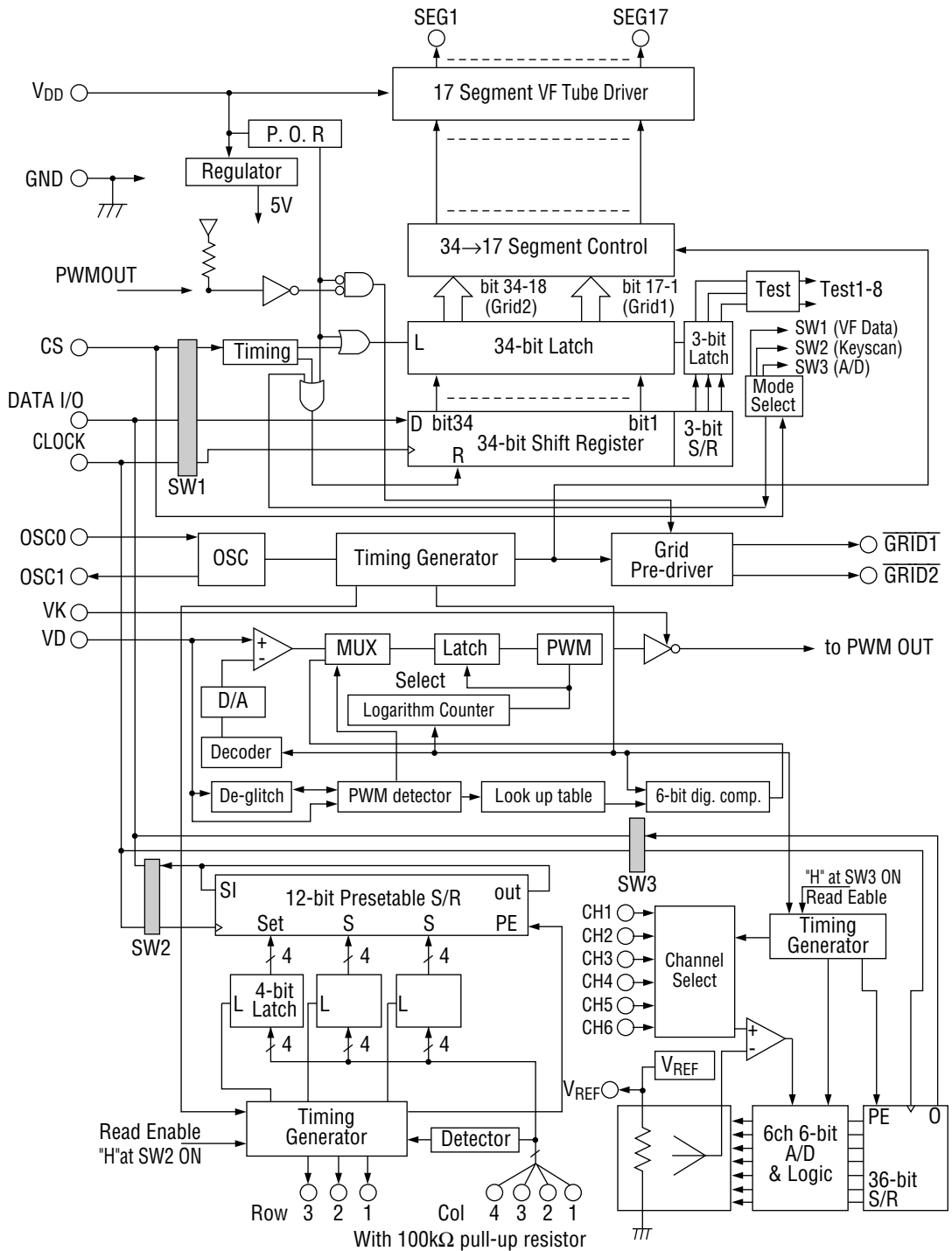
The analog dimming/PWM conversion modes can be selected automatically for the brightness control, so this IC is applicable to any type of automobile without any change of the specifications.

The interface with a MCU can be done only with 3 wires (CS, DATA I/O and CLOCK signals). Also, DATA I/O and CLOCK signal lines can be shared with other peripherals because of chip select function by CS signal.

### FEATURES

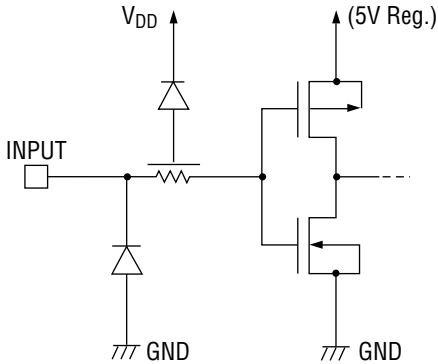
- Power supply voltage :  $V_{DD}=8$  to 18 V
- Operating temperature range :  $T_a=-40$  to  $+85^{\circ}\text{C}$
- 17-segment driver outputs ( $I_{OH}=-5\text{mA}$  at  $V_{OH}=V_{DD}-0.8\text{V}$ )
- Built-in analog dimming circuit (6-bit resolution, user-programmable)
- Built-in PWM conversion circuit (Lamp PWM signal to vacuum fluorescent display PWM signal)
- Built-in automatic-selection circuit for analog dimming/PWM conversion function
- Built-in 6ch 6-bit A/D converter
- Built-in 3 × 4 Keyscan circuit
- Built-in oscillation circuit (external R and C,  $f_{OSC}=3.3\text{MHz}$ )
- Built-in Power-On-Reset circuit
- Package:
  - 42-pin plastic DIP (DIP 42-P-600-2.54) (Product name: MSM1215-xxRS)
  - xx indicates the code number.

**BLOCK DIAGRAM**

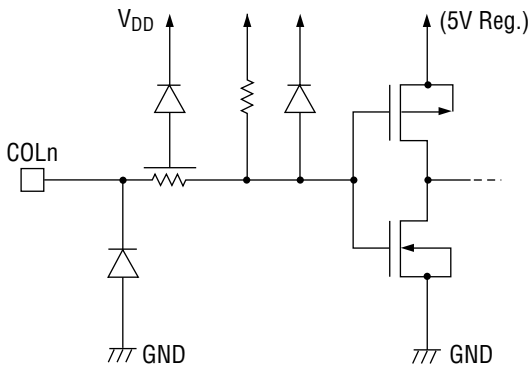


### INPUT AND OUTPUT CONFIGURATION

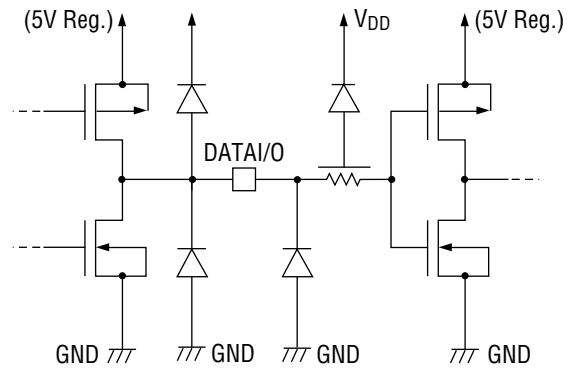
- Schematic Diagrams of Logic Portion Input Circuit 1



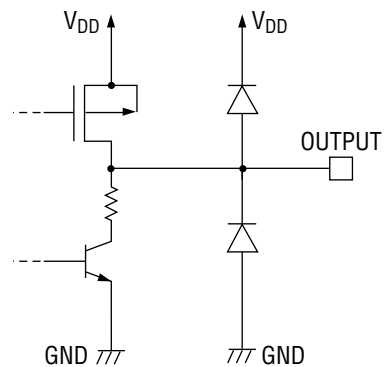
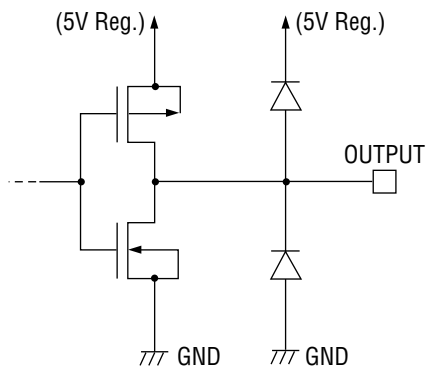
- Schematic Diagrams of Logic Portion Input Circuit 2



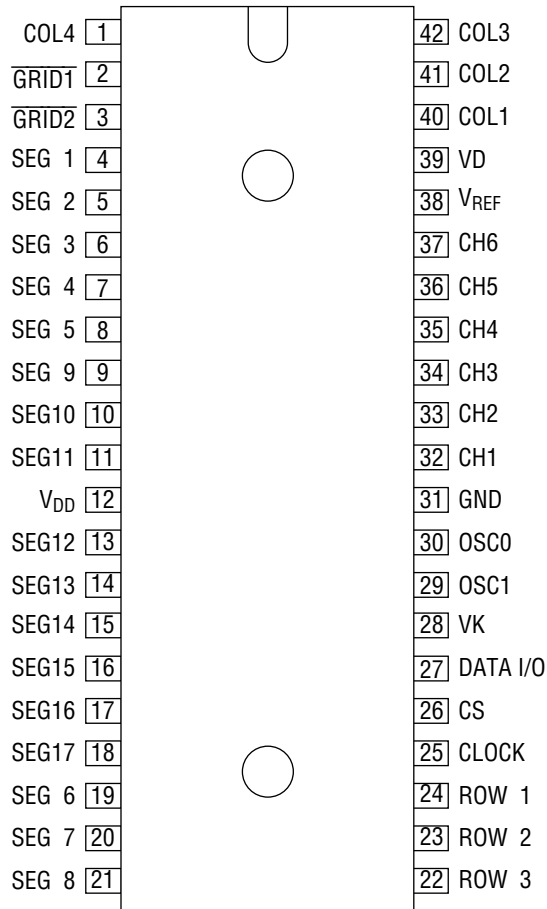
- Schematic Diagrams of Logic Portion Input/Output Circuit



- Schematic Diagrams of Logic Portion Output Circuit
- Schematic Diagrams of Driver Output Circuit



**PIN CONFIGURATION (TOP VIEW)**



**42-Pin Plastic DIP**

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	$V_{DD}$	—	-0.3 to +20	V
Input Voltage (1)	$V_{IN1}$	All inputs except VK	-0.3 to +6	V
Input Voltage (2)	$V_{IN2}$	VK	-0.3 to + $V_{DD}$	V
Power Dissipation	$P_D$	$T_a=85^{\circ}\text{C}$	400	mW
Storage Temperature	$T_{STG}$	—	-55 to +150	$^{\circ}\text{C}$

**RECOMMENDED OPERATING CONDITION**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{DD}$	—	8	—	18	V
Operating Temperature	$T_{OP}$	—	-40	—	85	$^{\circ}\text{C}$
High Level Input Voltage (1)	$V_{IH1}$	All inputs except VK	3.8	—	5.5	V
High Level Input Voltage (2)	$V_{IH2}$	VK	3.8	—	$V_{DD}$	V
Low Level Input Voltage	$V_{IL}$	All inputs	0	—	0.8	V
Clock Frequency	$f_c$	—	—	—	250	kHz
OSC Frequency	$f_{osc}$	$R=4.7\text{ k}\Omega, C=10\text{ pF}$	—	3.33	—	MHz
Frame Frequency	$f_{FR}$	—	—	200	—	Hz

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

(Ta=-40 to +85°C, V<sub>DD</sub>=8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit
"H" Input Voltage	V <sub>IH</sub>	All inputs except VD	3.8	—	V
"L" Input Voltage	V <sub>IL</sub>	All inputs except VD	—	0.8	V
"H" Input Current (1)	I <sub>IH1</sub>	All inputs except COL1-4 V <sub>IN</sub> =4.4 V	-5	5	μA
"H" Input Current (2)	I <sub>IH2</sub>	COL1-4, V <sub>IN</sub> =3.8 V	-70	-5	μA
"L" Input Current (1)	I <sub>IL1</sub>	All inputs except COL1-4 V <sub>IN</sub> =0 V	-5	5	μA
"L" Input Current (2)	I <sub>IL2</sub>	COL1-4, V <sub>IN</sub> =0 V	-160	-10	μA
"H" Output Voltage (1)	V <sub>OH1</sub>	SEG, GRID I <sub>OH1</sub> =-5 mA, V <sub>DD</sub> =9.5 V	V <sub>DD</sub> -0.8	—	V
"H" Output Voltage (2)	V <sub>OH2</sub>	DATA I/O, V <sub>DD</sub> =9.5 V I <sub>OH2</sub> =-200 μA Output open	4 4.5	—	V V
"L" Output Voltage (1)	V <sub>OL1</sub>	SEG, GRID, V <sub>DD</sub> =9.5 V I <sub>OL1</sub> =500 μA I <sub>OL1</sub> =200 μA I <sub>OL1</sub> =2 μA	— — —	2 1 0.3	V V V
"L" Output Voltage (2)	V <sub>OL2</sub>	DATA I/O, ROW1-3 V <sub>DD</sub> =9.5 V, I <sub>OL2</sub> =200 μA	—	0.8	V
Current Consumption	I <sub>DD</sub>	f <sub>osc</sub> =3.3 MHz, no load	—	20	mA

**Switching Characteristics**

(Ta=-40 to +85°C, VDD=8 to 18 V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillation Frequency	$f_{osc}$	—	2	4.5	MHz
Clock Frequency	$f_c$	—	—	250	kHz
Clock Pulse Width	$t_{cw}$	—	1.3	—	$\mu$ s
Data Set-up Time	$t_{DS}$	—	1	—	$\mu$ s
Data Hold Time	$t_{DH}$	—	200	—	ns
CS Pulse Width	$t_{CSW}$	Except reset mode	8	—	$\mu$ s
CS Off Time	$t_{CSL}$	Except reset mode	32	—	$\mu$ s
CS Pulse Width	$t_{RCSW}$	Reset mode	4	—	$\mu$ s
CS Off Time	$t_{RCSL}$	Reset mode	4	—	$\mu$ s
CS Set-up Time CS-clock Time	$t_{CSS}$	—	2	—	$\mu$ s
CS Hold Time Clock-CS Time	$t_{CSH}$	—	2	—	$\mu$ s
DATA Output Delay CLCOK-DATA Out Time	$t_{PD}$	—	—	1	$\mu$ s
SEG & GRID Outputs Delay Time from CS	$t_{ODS}$	$C_L=100$ pF	—	8	$\mu$ s
Slew Rate (All Drivers)	$t_R$	$C_L=100$ pF $t=20\%$ to $80\%$ or $80\%$ to $20\%$ of $V_{DD}$	—	5	$\mu$ s
Power on Timing	$t_{PCS}$	—	300	—	$\mu$ s

**Analog Dimming Characteristics**

(Ta=-40 to +85°C, V<sub>DD</sub>=8 to 18V)

Parameter	Condition	Min.	Typ.	Max.	Unit
D/A Output Voltage Error	—	—	—	±3	%
Reference Voltage Accuracy *1	—	—	—	±6	%

\*1 Reference voltage is 6.6 V typical.

**A/D Converter Characteristics**

(Ta=-40 to +85°C, V<sub>DD</sub>=8 to 18 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
A/D Conversion Accuracy	—	—	—	±1	LSB
Reference Voltage (V <sub>REF</sub> )	*2	4.5	5	5.5	V
Output Current	—	—	—	4	mA
Input Voltage Range	—	GND	—	V <sub>REF</sub>	V
Conversion Time/Channel	f <sub>OSC</sub> =3.3MHz	384	543	896	μs

\*2 When six loads of 10 kΩ are connected in parallel.

**Keyscan Characteristics**

(Ta=-40 to +85°C, V<sub>DD</sub>=8 to 18 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Keyscan Cycle Time	f <sub>OSC</sub> =3.3MHz	220	312	512	μs
Keyscan Pulse Width	f <sub>OSC</sub> =3.3MHz	55	78	128	μs

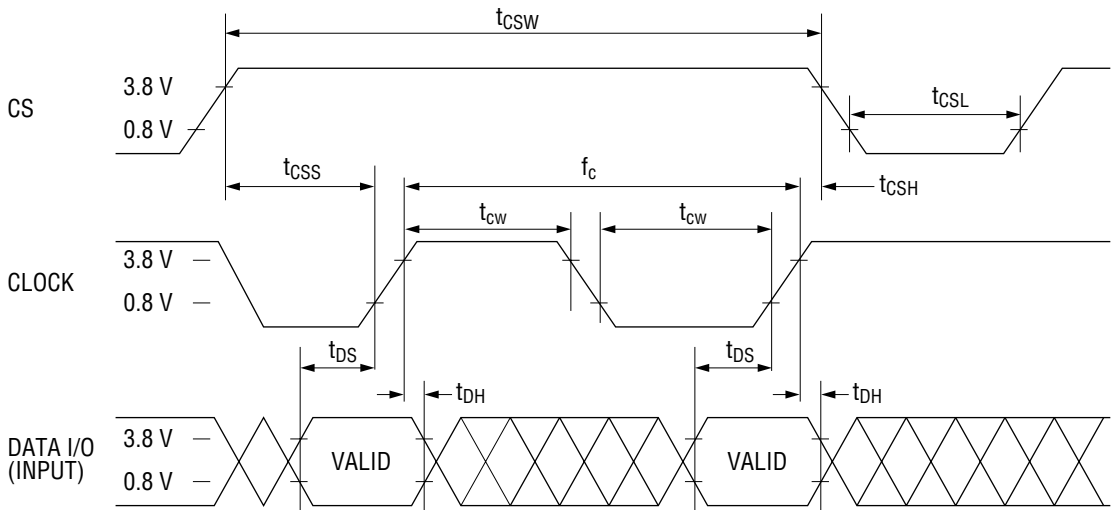
**PWM Conversion Characteristics**

(Ta=-40 to +85°C, V<sub>DD</sub>=8 to 18 V)

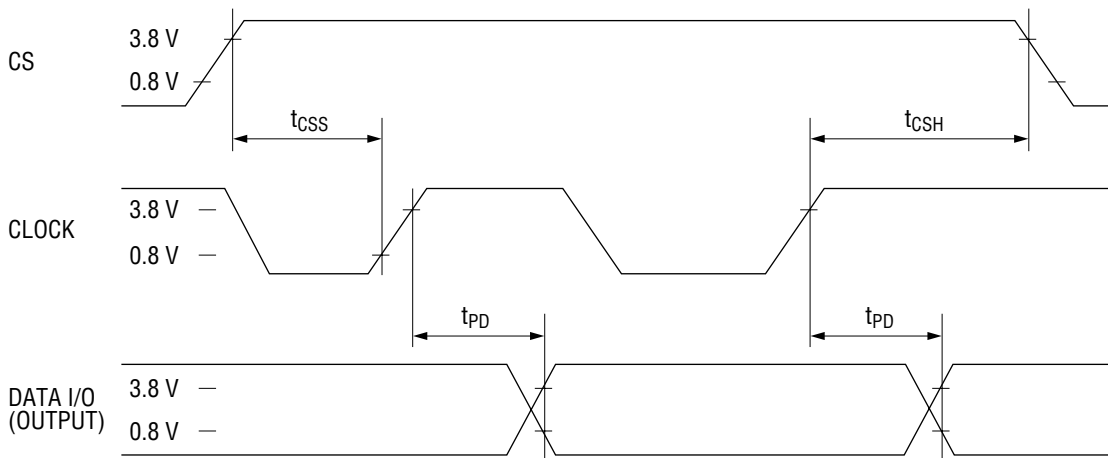
Parameter	Condition	Min.	Typ.	Max.	Unit
PWM Input Frequency	—	112	122	132	Hz
Rise/Fall Time	t <sub>r</sub> =10%→90%, t <sub>f</sub> =90%→10%	100	300	800	μs
PWM Pulse Width	t=50%→50%	125	—	—	μs
Input Duty Cycle	VD pin	1.65	—	98.3	%
"H" Input Threshold voltage	VD pin	0.26V <sub>DD</sub>	0.28V <sub>DD</sub>	0.30V <sub>DD</sub>	V
"L" Input Threshold voltage	VD pin	0.20V <sub>DD</sub>	0.22V <sub>DD</sub>	0.24V <sub>DD</sub>	V
Hysteresis Width	VD pin	0.02V <sub>DD</sub>	0.06V <sub>DD</sub>	0.10V <sub>DD</sub>	V



**TIMING DIAGRAM**



**Figure 1. DATA Input Timing**



**Figure 2. DATA Output Timing**

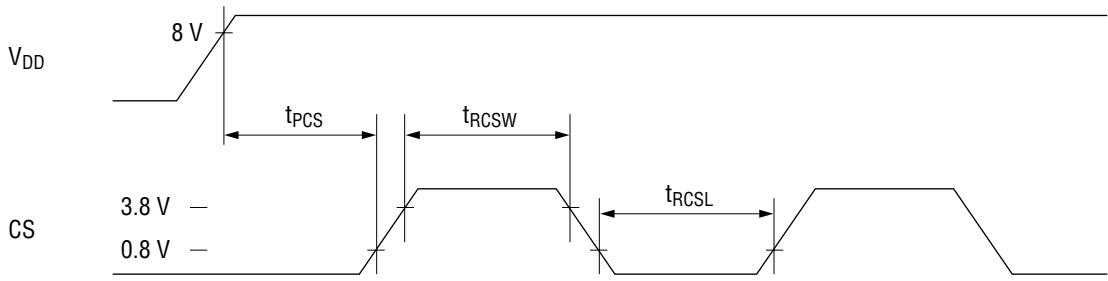


Figure 3. Power-on-Reset Timing

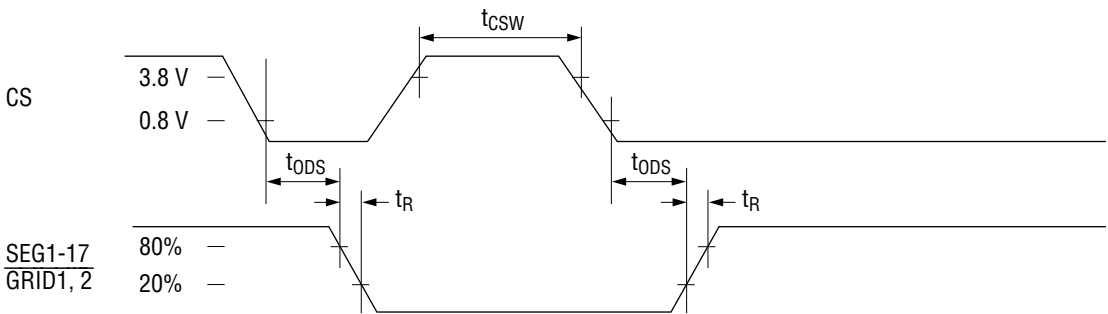


Figure 4. SEG and GRID Output Timing

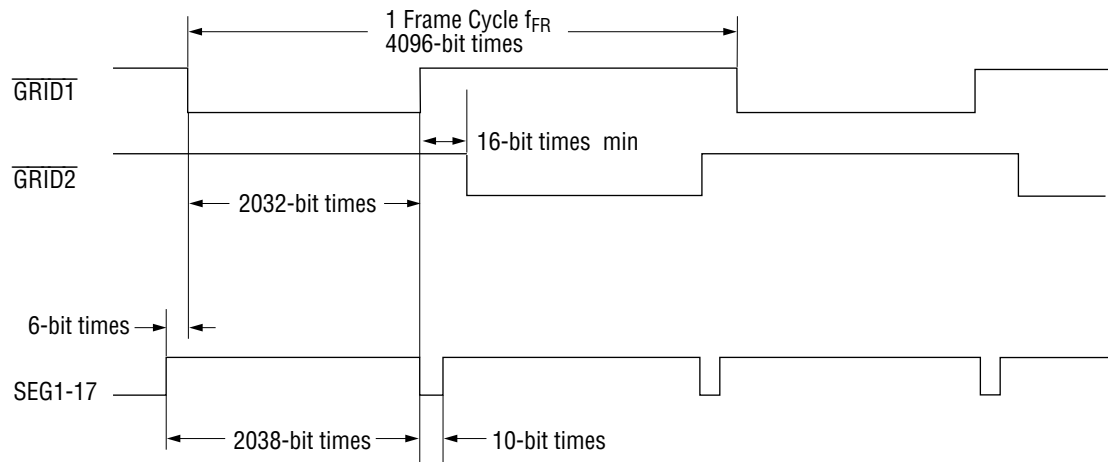
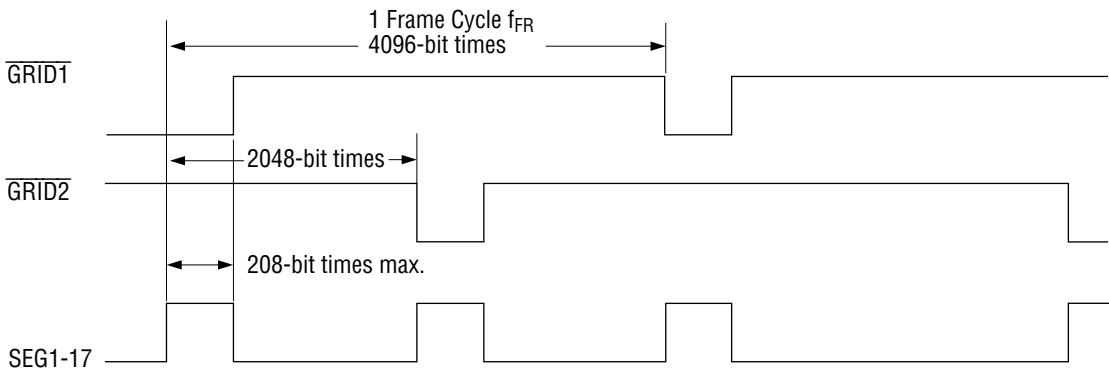


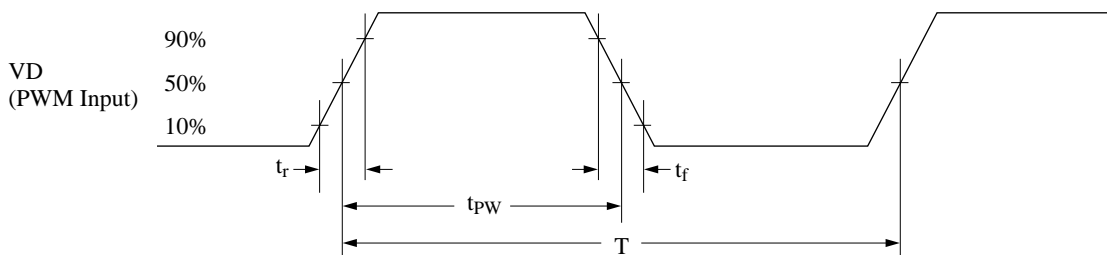
Figure 5. SEG-GRID output Timing (Daylight Mode)

Note: 1. Timing shown for analog dimming with a duty cycle of 2032/2048 at VK="L".  
 2. 1-bit time=T<sub>OSC</sub> (=4/f<sub>OSC</sub>)=1.2 μs typical.

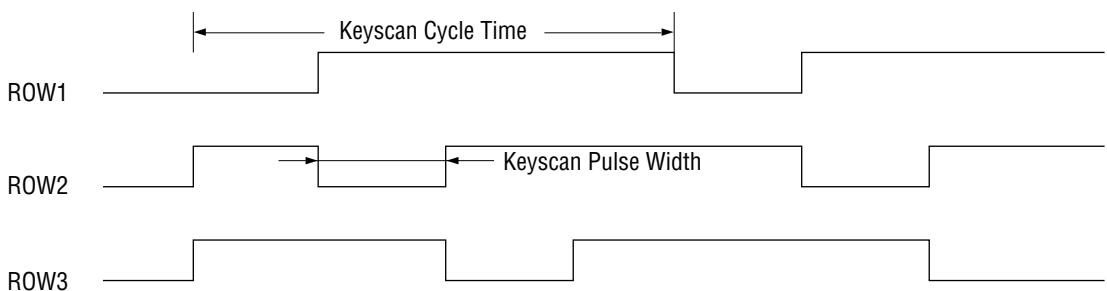


**Figure 6. SEG- $\overline{\text{GRID}}$  output Timing (Dark Mode)**

- Note: 1. Timing shown for analog dimming with a duty cycle of 208/2048 at VK="H".  
 2. 1-bit time= $T_{OSC}$  ( $=4/f_{OSC}$ )=1.2  $\mu\text{s}$  typical.

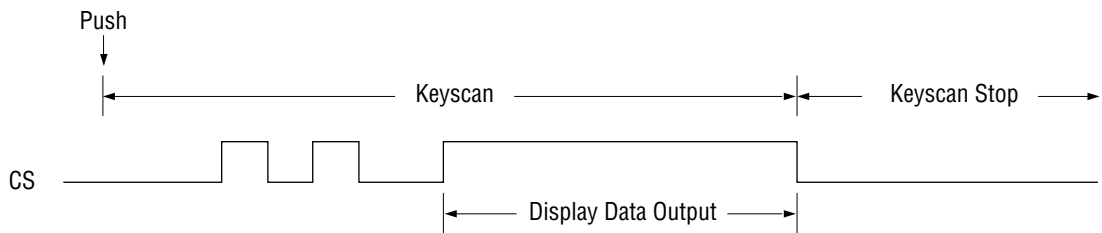


**Figure 7. PWM Waveform**



**Figure 8. Keyscan Timing**

- Note: 1. Key scanning from ROW1 to ROW3 is started when any key is pushed down or released. Scanning will stop when CS turns to "L" from "H", after 2 times of CS pulses and the transfer of display data.



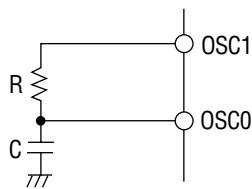
**Figure 9. Keyscan Stop Timing**

## FUNCTIONAL DESCRIPTION

### Pin Functional Description

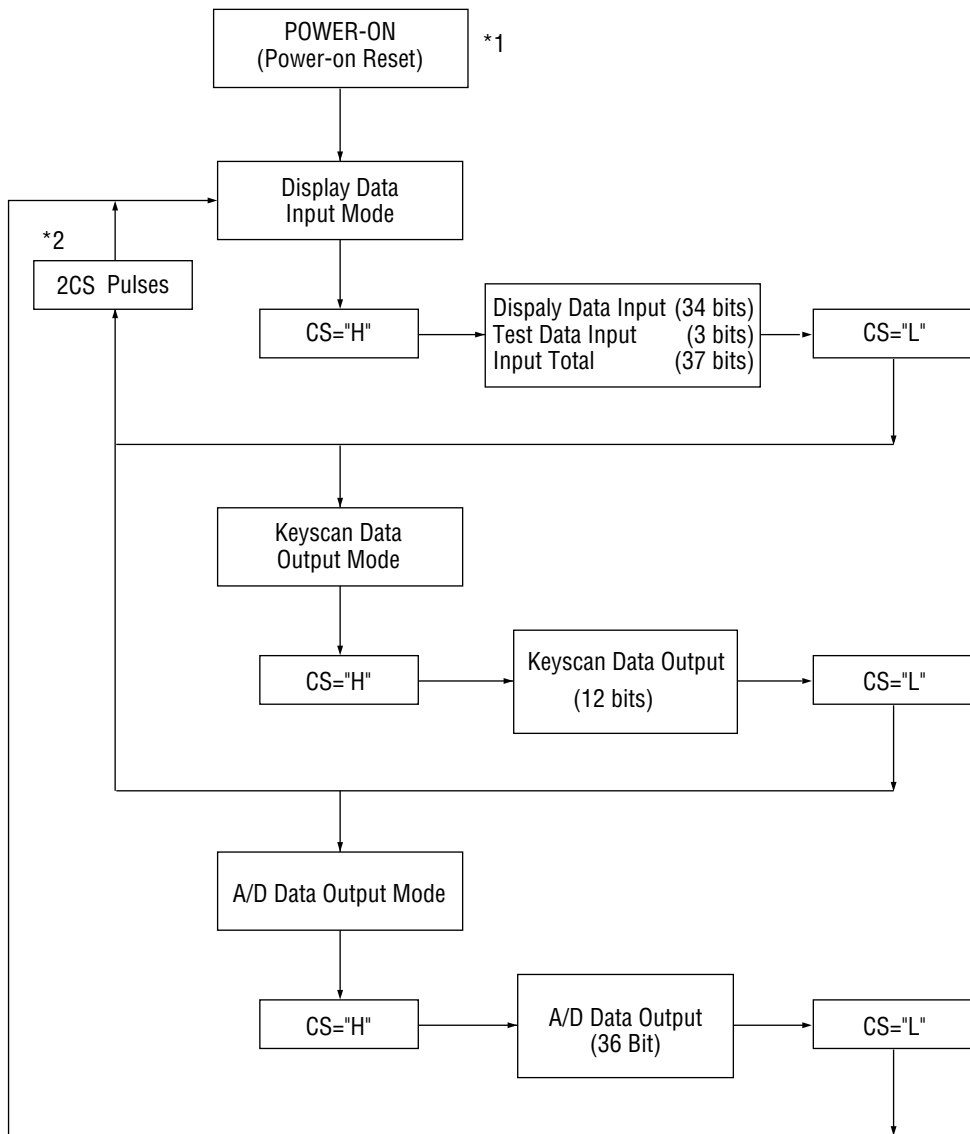
- $V_{DD}$   
Power supply input pin  
Connected to a 12V power supply
- GND  
Ground Pin  
This pin is 0V level.
- CLOCK  
Serial clock input pin
- CS  
Chip select input pin  
When "H" is input to this pin, interfacing with a MCU is available through the CLOCK and the DATA pins.  
Therefore, 2 signal lines of the CLOCK and the DATA can be shared with other peripherals.
- DATA I/O (Input-output)  
Serial data input-output pin  
This pin inputs display data and outputs keyscan and A/D conversion data.
- VK  
Daylight/dark mode selection input pin  
When "H" is input, the dark mode is selected and an output duty cycle is determined by analog or PWM data input into the VD pin.  
When "L" is input, the daylight mode is selected and the output duty cycle becomes about 100%.
- VD  
Analog/PWM dimming data input pin  
Analog/PWM dimming mode selection will be done by an internal detection circuit automatically.
- $V_{REF}$   
Reference voltage output pin for the A/D converter

- CH1-6  
Analog voltage input pin for the A/D converter
- COL1-4  
Key matrix input pins  
These pins are active "Low" and pulled up to "H" through built-in resistors except when "L" is input by a pushed down key.
- ROW1-3  
Key matrix scanning output  
Normally ROW1-3 output "L", by detecting the key switch to be pushed down or released, a key scan starts, sending CS pulses two times and VF data, after above turning the CS pin to "L" from "H". After scan stops, all the ROW outputs turn to "L".
- OSC0, 1  
RC oscillation input pins  
A resistor and a capacitor are connected to these pins. (See figure below)



- SEG1-17  
Segment output pins
- $\overline{\text{GRID}}1, 2$   
Grid output pins  
Output an inverted signal of a grid signal.  
These pins are connected to inputs of external drivers (such as a PNP transistor).

Functional Flowchart



- Note:
1. When power supply turns on, the internal circuits are initialized as follows by the built-in power-on reset circuit.
    - Display data input mode is selected
    - All segment outputs are in OFF state ("L")
    - All internal registers and latches are set to "0" level
  2. The status of the internal circuit after serial 2 CS pulses were applied, are as follows.
    - Display data input mode is selected
    - The other status are the same as before the serial 2CS pulses were applied.

### Display Data Input

Data input is available only when "H" is applied to the "CS" pin. Input data is shifted into shift registers through the "DATA I/O" pin at the rising edge of the clock. The data is automatically loaded to latches at the falling edge of "CS" signal.

[Data Format]

Bit	37	36	35	-----	6	5	4	3	2	1	→ First in		
Data	34	33	32	-----	3	2	1	T3	T2	T1			
								← Display Data			← Test Data		
											*1		

Note: Three bits (T1 to T3) for the test data are used for shipping inspection. For the normal operation mode, all these bits should be set to "0" level.

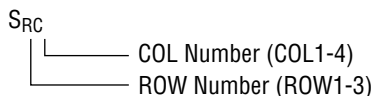
### Keyscan Data Output

Data output is available only when "H" is applied to the "CS" pin. When keyscan data output mode is selected, "DATA I/O" pin is changed to an output mode. Then, 12 bits of keyscan data come out from "DATA I/O" pin synchronizing with the rising edge of the clock. This output mode is changed to A/D data output mode at the falling edge of the CS input signal. To select directly the display input mode from this output mode, serial 2CS pulses should be input to the CS pin.

[Data Format]

Bit	12	11	10	9	8	7	6	5	4	3	2	1	→ First out
Data	S34	S33	S32	S31	S24	S23	S22	S21	S14	S13	S12	S11	
													*2

Note: Symbols of the keyscan data are as follows.



### A/D Data Output

A/D data output is available only when "H" is input to the CS pin. When the A/D data output mode is selected, DATA I/O pin is changed to an output mode. Then 36 bits of A/D data come out from DATA I/O pin synchronizing with the rising edge of the shift clock. This output mode is changed to the display input mode at the falling edge of the CS input signal.

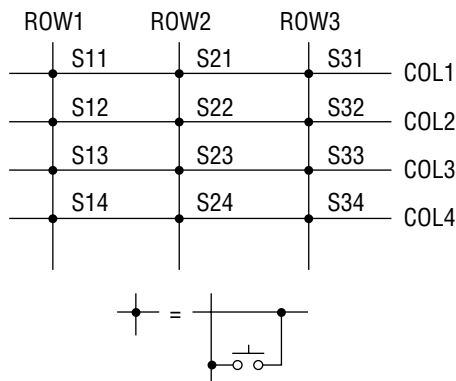
[Data Format]

Bit	36-31	30-25	24-19	18-13	12-7	6-1	→ First out
Data	MSB-LSB CH6	MSB-LSB CH5	MSB-LSB CH4	MSB-LSB CH3	MSB-LSB CH2	MSB-LSB CH1	

**Keyscan**

To keep a scanning noise to a minimum, a scanning of the key switch starts only when a key is pushed down or released. The scanning stops when CS input turns to "L" from "H" after sending CS pulses two times and display data.

[Key Matrix of COL Input and ROW Output]

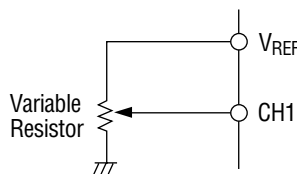


**A/D Conversion**

The IC has a built-in 6-ch × 6-bit A/D converter.

As shown in the circuit below, the  $V_{REF}$  output pin is connected to a variable resistor forming a voltage divider and the divided analog voltage is used to input into the CH1 to CH6 pins.

[Circuit Example]



**PWM Dimming**

Lamp PWM signal is input to the VD pin and converted to VF display PWM signal by the PWM conversion circuit.

The conversion table is mark-programmable.

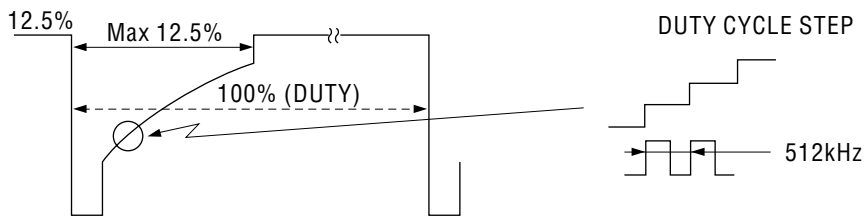
Note: The duty cycle of the lamp PWM signal is measured with a reference point of the threshold voltage of the VD input pin. The threshold voltage changes due to process parameter deviation. Therefore, the PWM conversion error increases as the rise/fall time of the lamp PWM increases.



### Analog Dimming

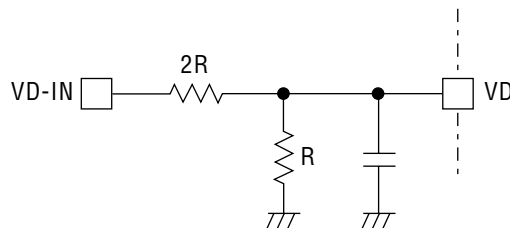
The PWM duty cycle is controlled by analog voltage which is the output of the brightness control volume on a dashboard. The dimming curve is mask-programmable with the following limitations;

1. Maximum duty cycle is 12.5%.



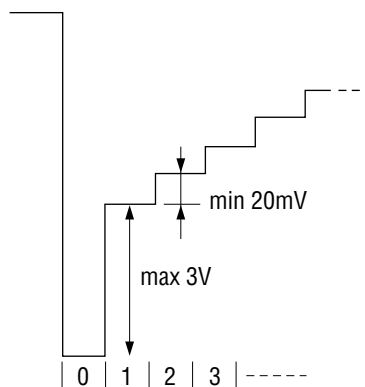
2. Number of pulse steps is max. 52.
3. Input Voltage to "VD"

The input voltage to "VD" needs to use a voltage divider as shown below.



Note: The maximum voltage to the VD is 5V.

4. Maximum Threshold Voltage  
The maximum threshold voltage is 5.0V.
5. Minimum & Maximum VDIM Input Voltage  
The minimum threshold voltage step is 20mV.  
Only for the first step, the threshold voltage can be any value between 20mV and 3V.



**PWM Conversion Table**

STEP No.	LAMP PWM DUTY CYCLE	VFD PWM DUTY CYCLE	STEP No.	LAMP PWM DUTY CYCLE	VFD PWM DUTY CYCLE
0	100.00%	12.50%	33	58.75%	
1	98.75%		34	57.50%	
2	97.50%		35	56.25%	
3	96.25%		36	55.00%	
4	95.00%		37	53.75%	
5	93.75%		38	52.50%	
6	92.50%		39	51.25%	
7	91.25%		40	50.00%	
8	90.00%		41	48.75%	
9	88.75%		42	47.50%	
10	87.50%		43	46.25%	
11	86.25%		44	45.00%	
12	85.00%		45	43.75%	
13	83.75%		46	42.50%	
14	82.50%		47	41.25%	
15	81.25%		48	40.00%	
16	80.00%		49	38.75%	
17	78.75%		50	37.50%	
18	77.50%		51	36.25%	
19	76.25%		52	35.00%	
20	75.00%		53	33.75%	
21	73.75%		54	32.50%	
22	72.50%		55	31.25%	
23	71.25%		56	30.00%	
24	70.00%		57	28.75%	
25	68.75%		58	27.50%	
26	67.50%		59	26.25%	
27	66.25%		60	25.00%	
28	65.00%		61	23.75%	
29	63.75%		62	22.50%	
30	62.50%		63	21.25%	
31	61.25%		64	20.00%	
32	60.00%				

**Dimming Voltage-Pulse width Correspondence Table**

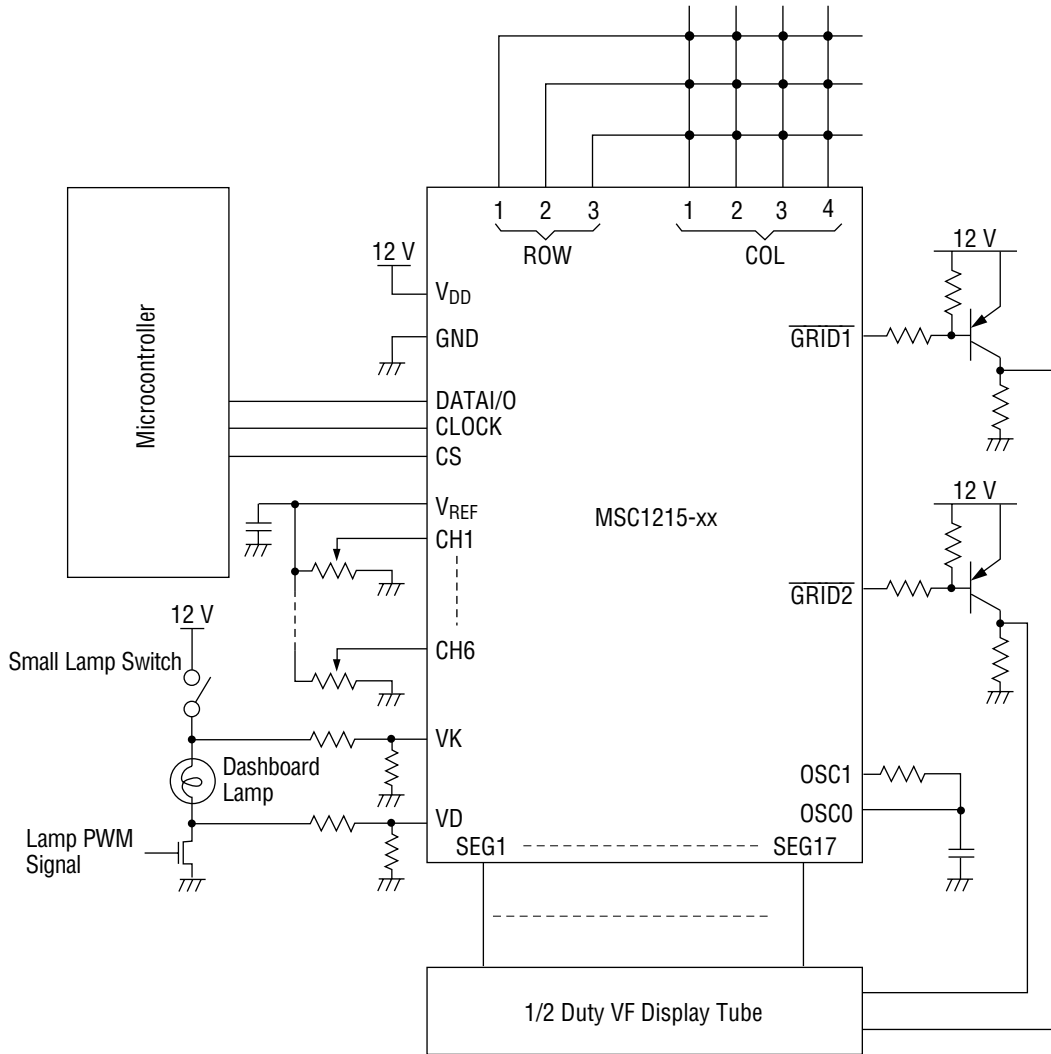
VDI Threshold dimming voltage vs. PWM duty cycle (Typical Value)  
 12.5% PWM maximum table

(@V<sub>DD</sub>=2.8 V)

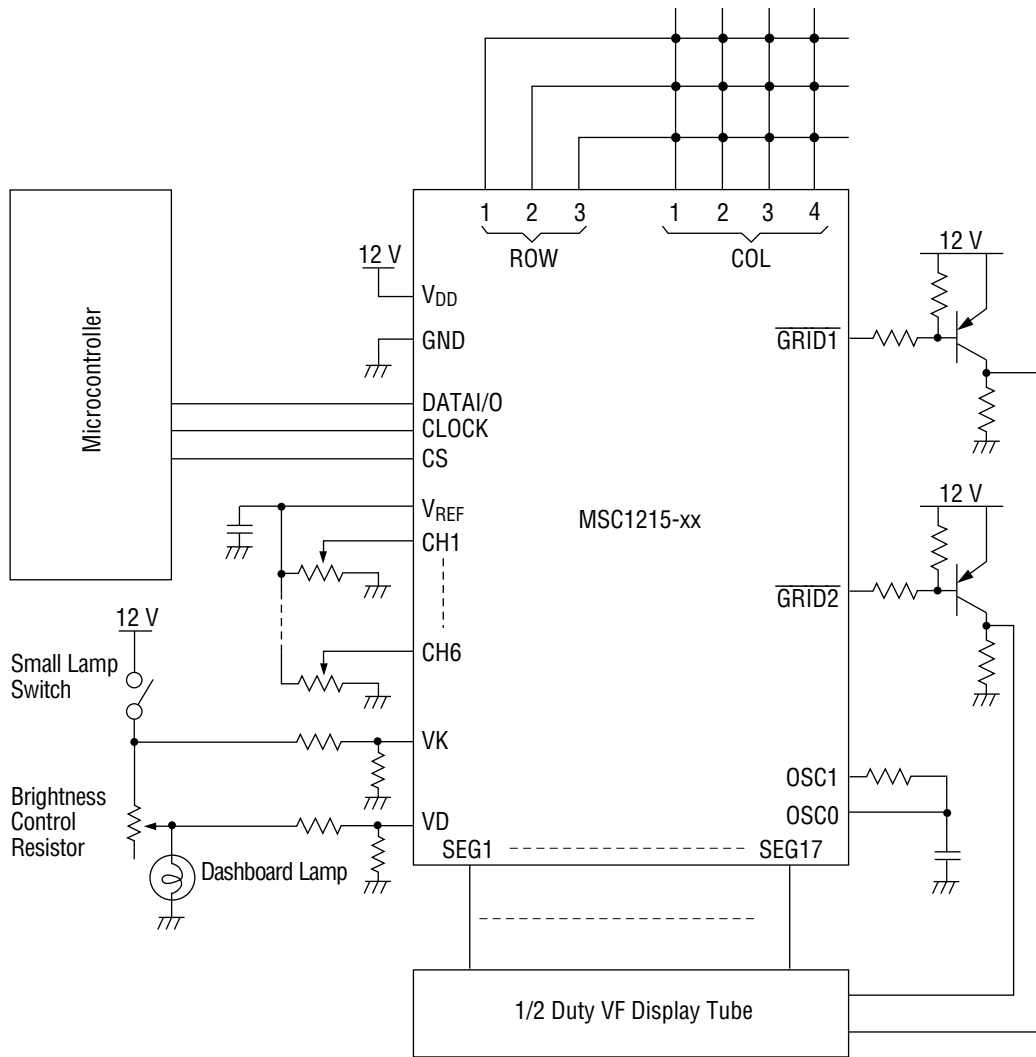
Pulse Step Number	PWM Duty Cycle		Threshold Voltage	Pulse Step Number	PWM Duty Cycle		Threshold Voltage
	Pulse Count	%			Pulse Count	%	
52	256/2048	12.5		26	56/2048	2.73	
51	240/2048	11.7		25	52/2048	2.54	
50	224/2048	10.9		24	48/2048	2.34	
49	208/2048	10.2		23	46/2048	2.25	
48	192/2048	9.38		22	44/2048	2.15	
47	184/2048	8.98		21	42/2048	2.05	
46	176/2048	8.59		20	40/2048	1.95	
45	168/2048	8.20		19	38/2048	1.86	
44	160/2048	7.81		18	36/2048	1.76	
43	152/2048	7.42		17	34/2048	1.66	
42	144/2048	7.03		16	32/2048	1.56	
41	136/2048	6.64		15	30/2048	1.46	
40	128/2048	6.25		14	28/2048	1.37	
39	120/2048	5.86		13	26/2048	1.27	
38	112/2048	5.47		12	24/2048	1.17	
37	104/2048	5.08		11	23/2048	1.12	
36	96/2048	4.69		10	22/2048	1.07	
35	92/2048	4.49		9	21/2048	1.03	
34	88/2048	4.30		8	20/2048	0.98	
33	84/2048	4.10		7	19/2048	0.93	
32	80/2048	3.91		6	18/2048	0.88	
31	76/2048	3.71		5	17/2048	0.83	
30	72/2048	3.52		4	16/2048	0.78	
29	68/2048	3.32		3	15/2048	0.73	
28	64/2048	3.13		2	14/2048	0.68	
27	60/2048	2.93		1	13/2048	0.63	
							0.000

APPLICATION CIRCUITS

Dimming Mode

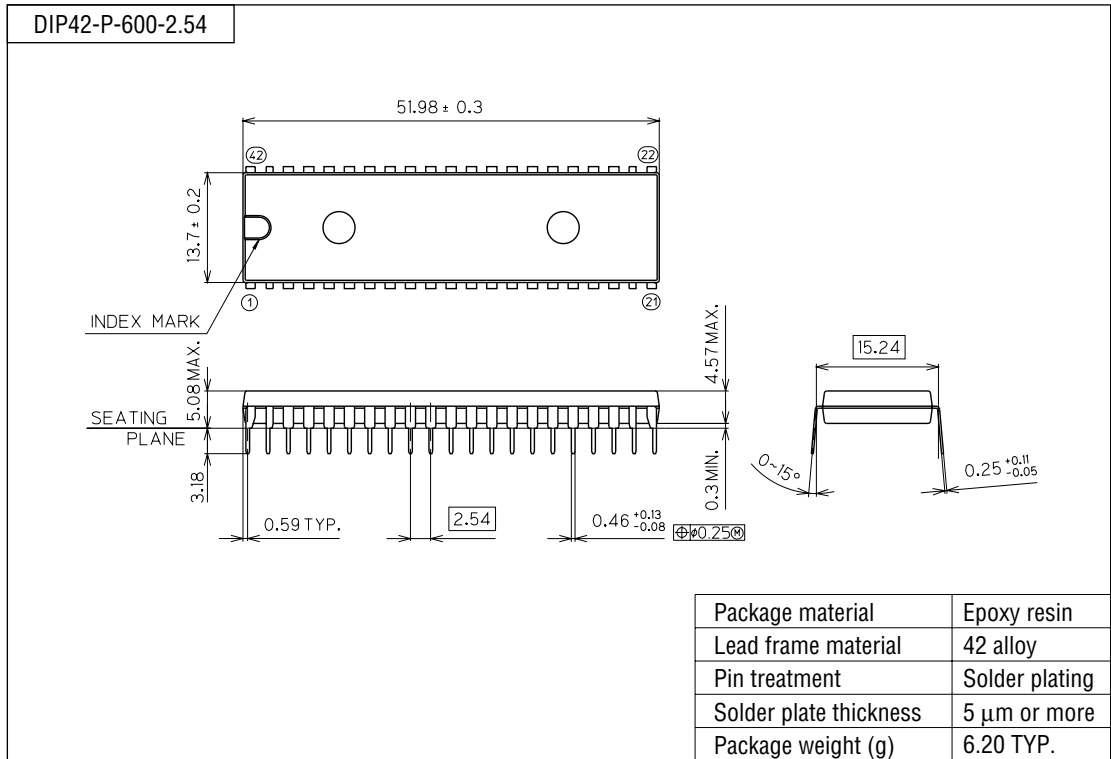


Analog Dimming Mode



**PACKAGE DIMENSIONS**

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).