

256Kx4 CMOS Dynamic RAM

Page Mode, Commercial and Industrial Temperature Range

The MCM514256A is a 1.0 μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514256A requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line package (ZIP).

- Two Temperature Ranges: Commercial — 0°C to 70°C
Industrial — -40°C to +85°C
- Three-State Data Output
- Fast Page Mode
- TTL-Compatible Inputs and Output
- $\overline{\text{RAS}}$ Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
 - MCM514256A = 8 ms
 - MCM51L4256A = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
 - MCM514256A-70 and MCM51L4256A-70 = 70 ns (Max)
 - MCM514256A-80 and MCM51L4256A-80 = 80 ns (Max)
 - MCM514256A-10 and MCM51L4256A-10 = 100 ns (Max)
- Low Active Power Dissipation:
 - MCM514256A-70 and MCM51L4256A-70 = 440 mW (Max)
 - MCM514256A-80 and MCM51L4256A-80 = 385 mW (Max)
 - MCM514256A-10 and MCM51L4256A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
 - MCM514256A and MCM51L4256A = 11 mW (Max), TTL Levels
 - MCM514256A = 5.5 mW (Max), CMOS Levels
 - MCM51L4256A = 1.1 mW (Max), CMOS Levels

MCM514256A

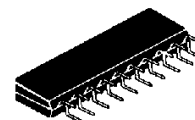
MCM51L4256A



P PACKAGE
300 MIL PLASTIC
CASE 738A



J PACKAGE
300 MIL SOJ
CASE 822



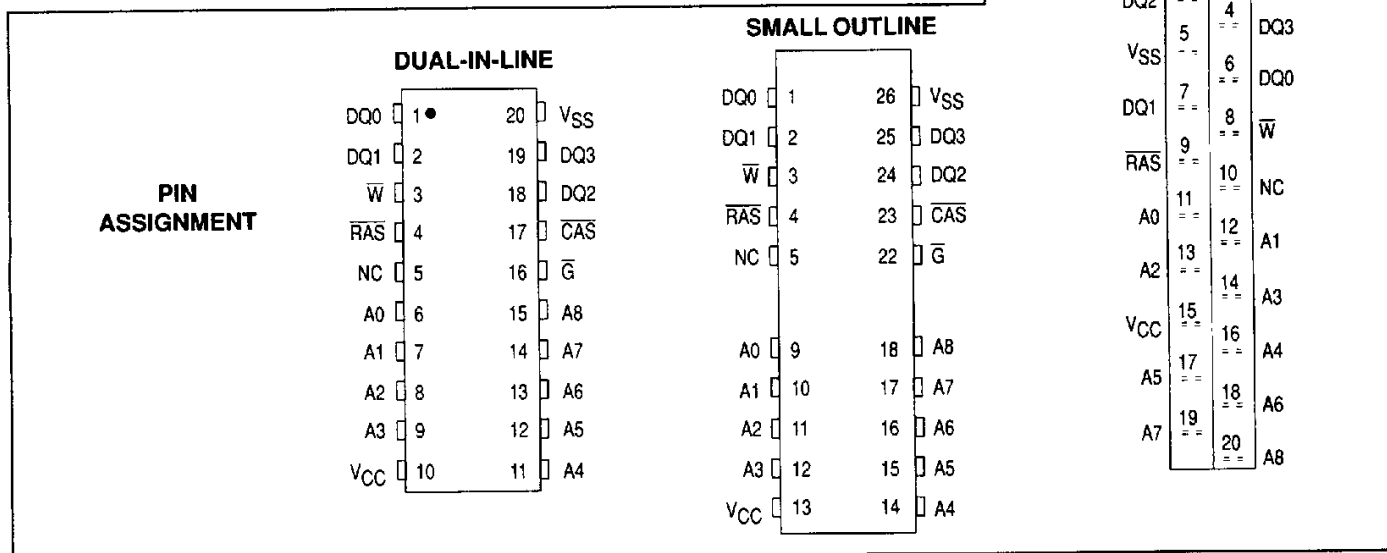
Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

PIN NAMES

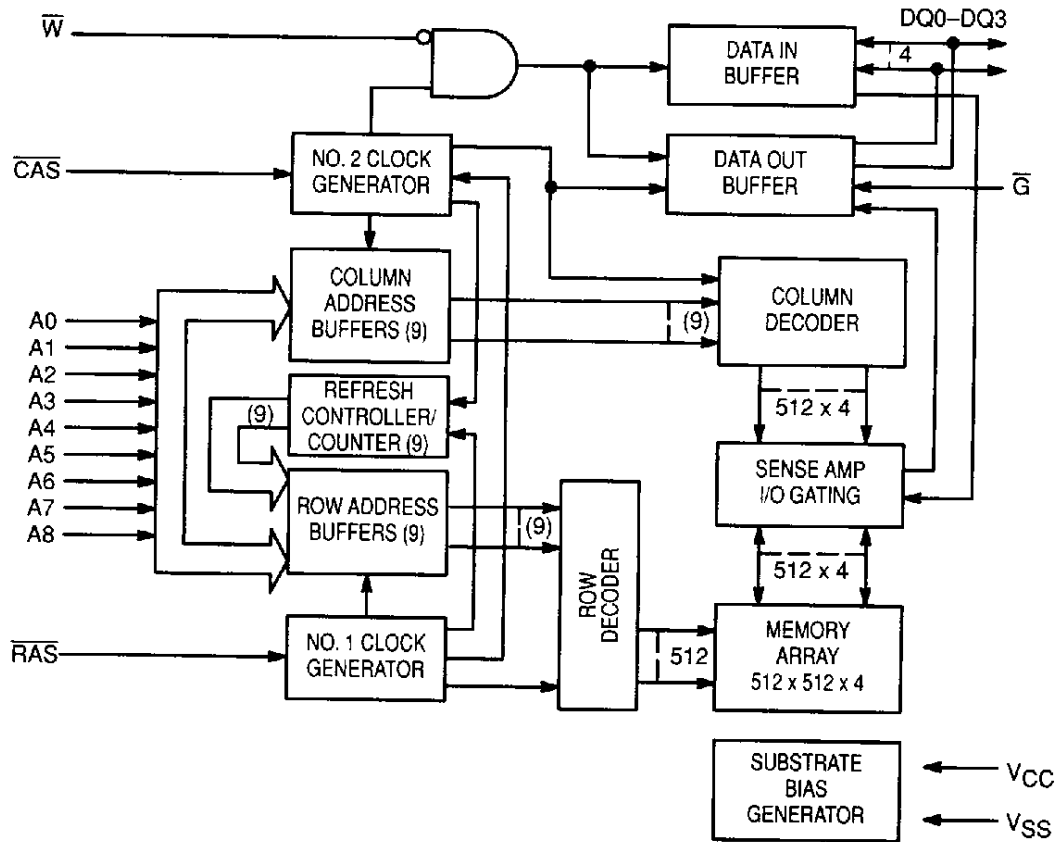
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
VCC	Power Supply (+5 V)
VSS	Ground
NC	No Connection

ZIG-ZAG IN-LINE

$\overline{\text{G}}$	1	2	$\overline{\text{CAS}}$
DQ2	3	4	
VSS	5	6	DQ3
DQ1	7	8	DQ0
$\overline{\text{RAS}}$	9	10	$\overline{\text{W}}$
A0	11	12	NC
A2	13	14	A1
VCC	15	16	A3
A5	17	18	A4
A7	19	20	A6
			A8



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	-1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Commercial Industrial		-40 to +85	
Storage Temperature Range	T_{stg}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } 70^\circ\text{C}$ and $-40 \text{ to } +85^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	-1.0	—	0.8	V	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM514256A-70 and MCM51L4256A-70, $t_{RC} = 130$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-80 and MCM51L4256A-80, $t_{RC} = 150$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-10 and MCM51L4256A-10, $t_{RC} = 180$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-C70 and MCM51L4256A-C70, $t_{RC} = 130$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C80 and MCM51L4256A-C80, $t_{RC} = 150$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C10 and MCM51L4256A-C10, $t_{RC} = 180$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CC1}	—	80 70 60 85 75 65	mA	3
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CAS}=V_{IH}$) MCM514256A- and MCM51L4256A-, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-C and MCM51L4256A-C, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CC2}	—	2 3	mA	
V_{CC} Power Supply Current During \overline{RAS} Only Refresh Cycles ($\overline{CAS}=V_{IH}$) MCM514256A-70 and MCM51L4256A-70, $t_{RC} = 130$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-80 and MCM51L4256A-80, $t_{RC} = 150$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-10 and MCM51L4256A-10, $t_{RC} = 180$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-C70 and MCM51L4256A-C70, $t_{RC} = 130$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C80 and MCM51L4256A-C80, $t_{RC} = 150$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C10 and MCM51L4256A-C10, $t_{RC} = 180$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CC3}	—	80 70 60 85 75 65	mA	3
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS} = V_{IL}$) MCM514256A-70 and MCM51L4256A-70, $t_{PC} = 40$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-80 and MCM51L4256A-80, $t_{PC} = 45$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-10 and MCM51L4256A-10, $t_{PC} = 55$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-C70 and MCM51L4256A-C70, $t_{PC} = 40$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C80 and MCM51L4256A-C80, $t_{PC} = 45$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C10 and MCM51L4256A-C10, $t_{PC} = 55$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CC4}	—	60 50 40 65 55 45	mA	3, 4
V_{CC} Power Supply Current (Standby) ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2$ V) MCM514256A-, $T_A = 0^\circ\text{C}$ to 70°C and MCM514256A-C, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM51L4256A-, $T_A = 0^\circ\text{C}$ to 70°C MCM51L4256A-C, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CC5}	—	1.0 200 400	mA μA μA	
V_{CC} Power Supply Current During \overline{CAS} Before \overline{RAS} Refresh Cycle MCM514256A-70 and MCM51L4256A-70, $t_{RC} = 130$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-80 and MCM51L4256A-80, $t_{RC} = 150$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-10 and MCM51L4256A-10, $t_{RC} = 180$ ns, $T_A = 0^\circ\text{C}$ to 70°C MCM514256A-C70 and MCM51L4256A-C70, $t_{RC} = 130$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C80 and MCM51L4256A-C80, $t_{RC} = 150$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ MCM514256A-C10 and MCM51L4256A-C10, $t_{RC} = 180$ ns, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CC6}	—	80 70 60 85 75 65	mA	3
V_{CC} Power Supply Current, Battery Backup Mode ($t_{RC} = 125$ μs , $t_{RAS} = 1$ μs , $\overline{CAS}=\overline{CAS}$ Before \overline{RAS} Cycle or 0.2 V, A0–A9, \overline{W} , D = $V_{CC} - 0.2$ V or 0.2 V) MCM51L4256A-, $T_A = 0^\circ\text{C}$ to 70°C MCM51L4256A-C, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	I_{CC5}	—	300 500	μA	3
Input Leakage Current (0 V $\leq V_{in} \leq 6.5$ V)	$I_{lkg(I)}$	-10	10	μA	
Output Leakage Current ($\overline{CAS} = V_{IH}$, 0 V $\leq V_{out} \leq 5.5$ V, Output Disable)	$I_{lkg(O)}$	-10	10	μA	
Output High Voltage ($I_{OH} = -5$ mA)	V_{OH}	2.4	—	V	
Output Low Voltage ($I_{OL} = 4.2$ mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, $T_A = 25^\circ\text{C}$, $V_{CC} = 5$ V, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit	Notes
Input Capacitance	A0–A8 \overline{G} , \overline{RAS} , \overline{CAS} , \overline{W}	5	pF	4
		7		
I/O Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	DQ0–DQ3	7	pF	4

NOTES:

- All voltages referenced to V_{SS} .
- Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
- Measured with one address transition per page mode cycle.
- Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

 $(V_{CC} = 5.0 V \pm 10\%, T_A = 0 \text{ to } 70^\circ\text{C} \text{ and } -40 \text{ to } +85^\circ\text{C}, \text{ Unless Otherwise Noted})$

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80		MCM514256A-10 MCM51L4256A-10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RELREL}	t _{RC}	130	—	150	—	180	—	ns	5
Read-Write Cycle Time	t _{RELREL}	t _{RMW}	185	—	205	—	245	—	ns	5
Fast Page Mode Cycle Time	t _{CELCEL}	t _{PC}	40	—	45	—	55	—	ns	
Fast Page Mode Read-Write Cycle Time	t _{CELCEL}	t _{PRMW}	95	—	100	—	115	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RELVQ}	t _{RAC}	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t _{CELVQ}	t _{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t _{AVQV}	t _{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CEHVQ}	t _{CPA}	—	35	—	40	—	50	ns	6
$\overline{\text{CAS}}$ to Output in Low-Z	t _{CELVQ}	t _{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t _{CEHVQ}	t _{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t _T	t _T	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{REHREL}	t _{RP}	50	—	60	—	70	—	ns	
RAS Pulse Width	t _{RELREH}	t _{RAS}	70	10,000	80	10,000	100	10,000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RELREH}	t _{RASP}	70	100,000	80	100,000	100	100,000	ns	
RAS Hold Time	t _{CELREH}	t _{RSH}	20	—	20	—	25	—	ns	
RAS Hold Time from $\overline{\text{CAS}}$ Precharge (Page Mode Cycle Only)	t _{CELREH}	t _{RHCP}	35	—	40	—	50	—	ns	
CAS Hold Time	t _{RELCEH}	t _{CSH}	70	—	80	—	100	—	ns	
CAS Pulse Width	t _{CELCEH}	t _{CAS}	20	10,000	20	10,000	25	10,000	ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t _{RELCEL}	t _{RCD}	20	50	20	60	25	75	ns	11
RAS to Column Address Delay Time	t _{RELAV}	t _{RAD}	15	35	15	40	20	50	ns	12
CAS to RAS Precharge Time	t _{CEHREL}	t _{CRP}	5	—	5	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t _{CEHCEL}	t _{CPN}	10	—	10	—	15	—	ns	
CAS Precharge Time (Page Mode Cycle Only)	t _{CEHCEL}	t _{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t _{AVREL}	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RELAX}	t _{RAH}	10	—	10	—	15	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
2. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0$ ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ and -40 to $+85^\circ\text{C}$) is assured.
6. Measured with a current load equivalent to 2 TTL ($-200 \mu\text{A}$, $+4 \text{ mA}$) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0 \text{ V}$ and $V_{OL} = 0.8 \text{ V}$.
7. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$.
8. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
9. Assumes that $t_{RAD} \geq t_{RAD}(\text{max})$.
10. $t_{OFF}(\text{max})$ and/or $t_{GZ}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
12. Operation within the $t_{RAD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .

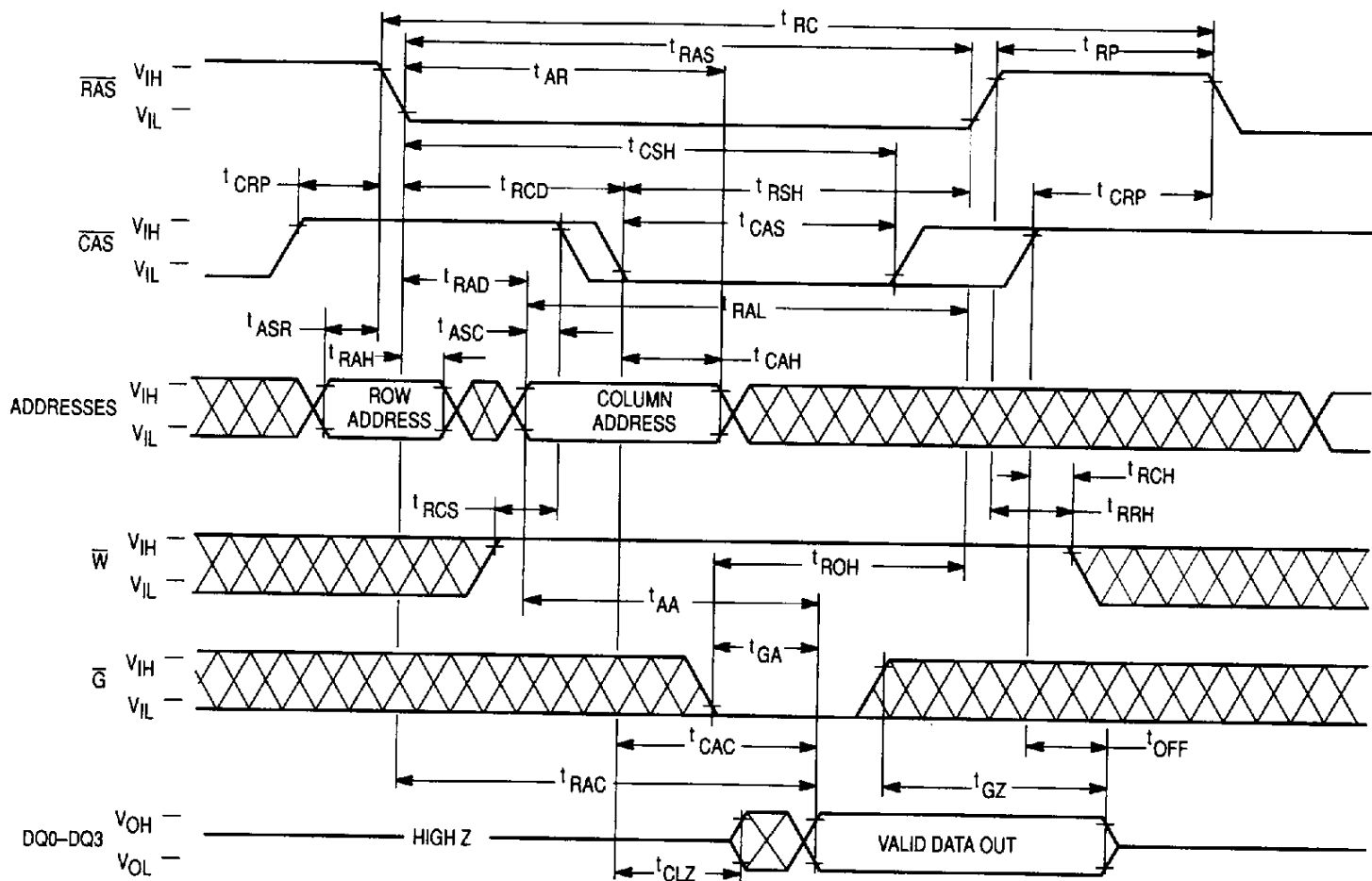
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80		MCM514256A-10 MCM51L4256A-10		Unit	Notes	
	Std	Alt	Min	Max	Min	Max	Min	Max			
Column Address Setup Time	t _{AVCEL}	t _{ASC}	0	—	0	—	0	—	ns		
Column Address Hold Time	t _{CELAX}	t _{CAH}	15	—	15	—	20	—	ns		
Column Address Hold Time Referenced to RAS	t _{RELAX}	t _{AR}	55	—	60	—	75	—	ns		
Column Address to RAS Lead Time	t _{AVREH}	t _{RAL}	35	—	40	—	50	—	ns		
Read Command Setup Time	t _{WHCEL}	t _{RCS}	0	—	0	—	0	—	ns		
Read Command Hold Time	t _{CEHWX}	t _{RCH}	0	—	0	—	0	—	ns	13	
Read Command Hold Time Referenced to RAS	t _{REHWX}	t _{RRH}	0	—	0	—	0	—	ns	13	
Write Command Hold Time Referenced to CAS	t _{CELWH}	t _{WCH}	15	—	15	—	20	—	ns		
Write Command Hold Time Referenced to RAS	t _{RELWH}	t _{WCR}	55	—	60	—	75	—	ns		
Write Command Pulse Width	t _{WLWH}	t _{WP}	15	—	15	—	20	—	ns		
Write Command to RAS Lead Time	t _{WLREH}	t _{RWL}	20	—	20	—	25	—	ns		
Write Command to CAS Lead Time	t _{WLCEH}	t _{CWL}	20	—	20	—	25	—	ns		
Data in Setup Time	t _{DVCEL}	t _{DS}	0	—	0	—	0	—	ns	14	
Data in Hold Time	t _{CELDX}	t _{DH}	15	—	15	—	20	—	ns	14	
Data in Hold Time Referenced to RAS	t _{RELDX}	t _{DHR}	55	—	60	—	75	—	ns		
Refresh Period	MCM514256A MCM51L4256A	t _{RVRV}	t _{RFSH}	—	8 64	—	8 64	—	8 64	ms	
Write Command Setup Time	t _{WLCEL}	t _{WCS}	0	—	0	—	0	—	ns	15	
CAS to Write Delay	t _{CELWL}	t _{CWD}	50	—	50	—	60	—	ns	15	
RAS to Write Delay	t _{RELWL}	t _{RWD}	100	—	110	—	135	—	ns	15	
Column Address to Write Delay Time	t _{AVWL}	t _{AWD}	65	—	70	—	85	—	ns	15	
CAS Precharge to Write Delay	t _{CEHWL}	t _{CPWD}	65	—	70	—	85	—	ns	15	
CAS Setup Time for CAS Before RAS Refresh	t _{RELCEL}	t _{CSR}	5	—	5	—	5	—	ns		
CAS Hold Time for CAS Before RAS Refresh	t _{RELCEH}	t _{CHR}	15	—	15	—	20	—	ns		
RAS Precharge to CAS Active Time	t _{REHCEL}	t _{RPC}	0	—	0	—	0	—	ns		
CAS Precharge Time for CAS Before RAS Counter Test	t _{CEHCEL}	t _{CPT}	40	—	40	—	50	—	ns		
RAS Hold Time Referenced to G	t _{GLREH}	t _{ROH}	10	—	10	—	20	—	ns		
G Access Time	t _{GLQV}	t _{GA}	—	20	—	20	—	25	ns		
G to Data Delay	t _{GLHDX}	t _{GD}	20	—	20	—	25	—	ns		
Output Buffer Turn-Off Delay Time from G	t _{GHQZ}	t _{GZ}	0	20	0	20	0	25	ns	10	
G Command Hold Time	t _{WLGL}	t _{GH}	20	—	20	—	25	—	ns		

NOTES:

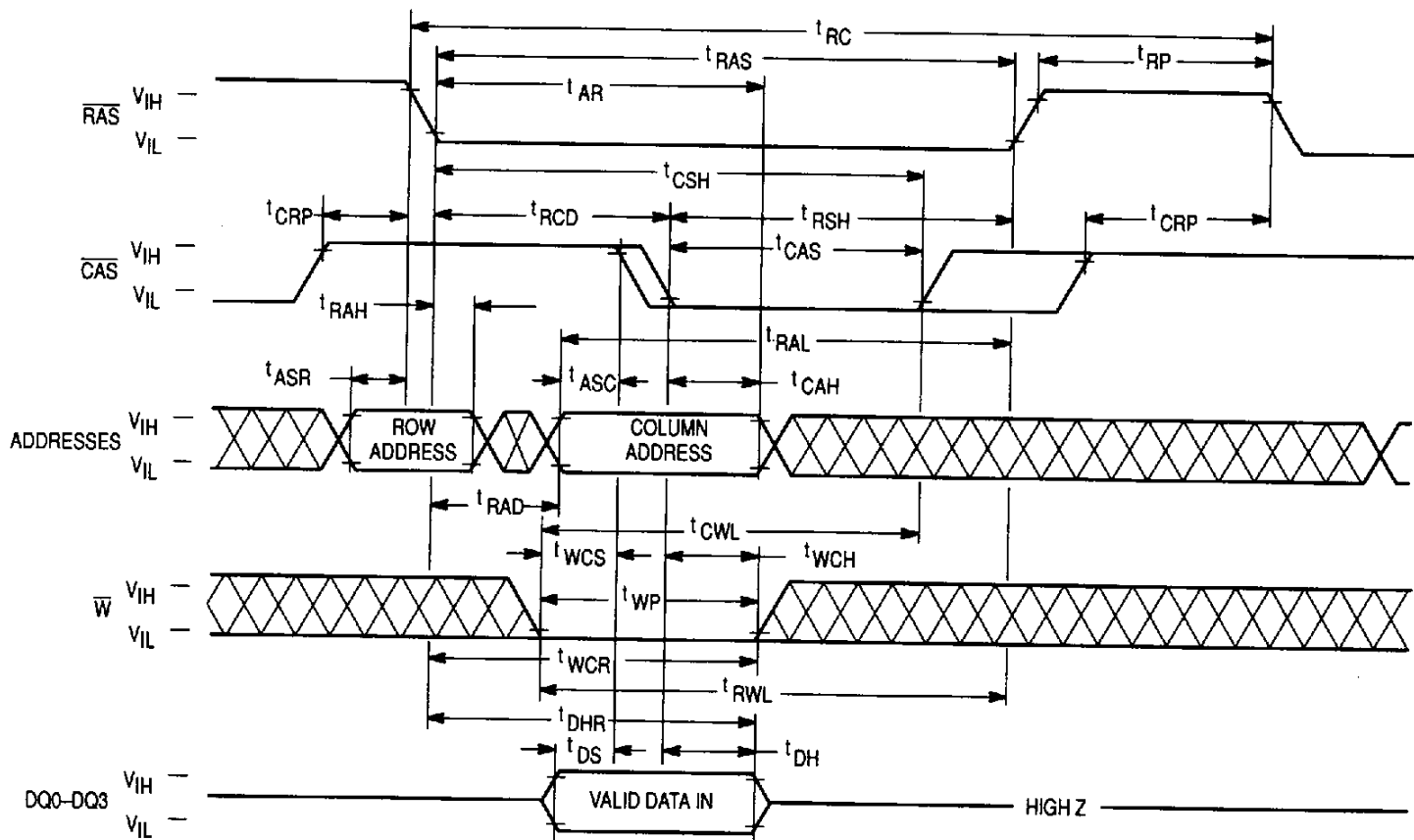
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in delayed write or read-write cycles.
- t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} ≥ t_{CWD} (min), t_{RWD} ≥ t_{RWD} (min), t_{CPWD} ≥ t_{CPWD} (min), and t_{AWD} ≥ t_{AWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE

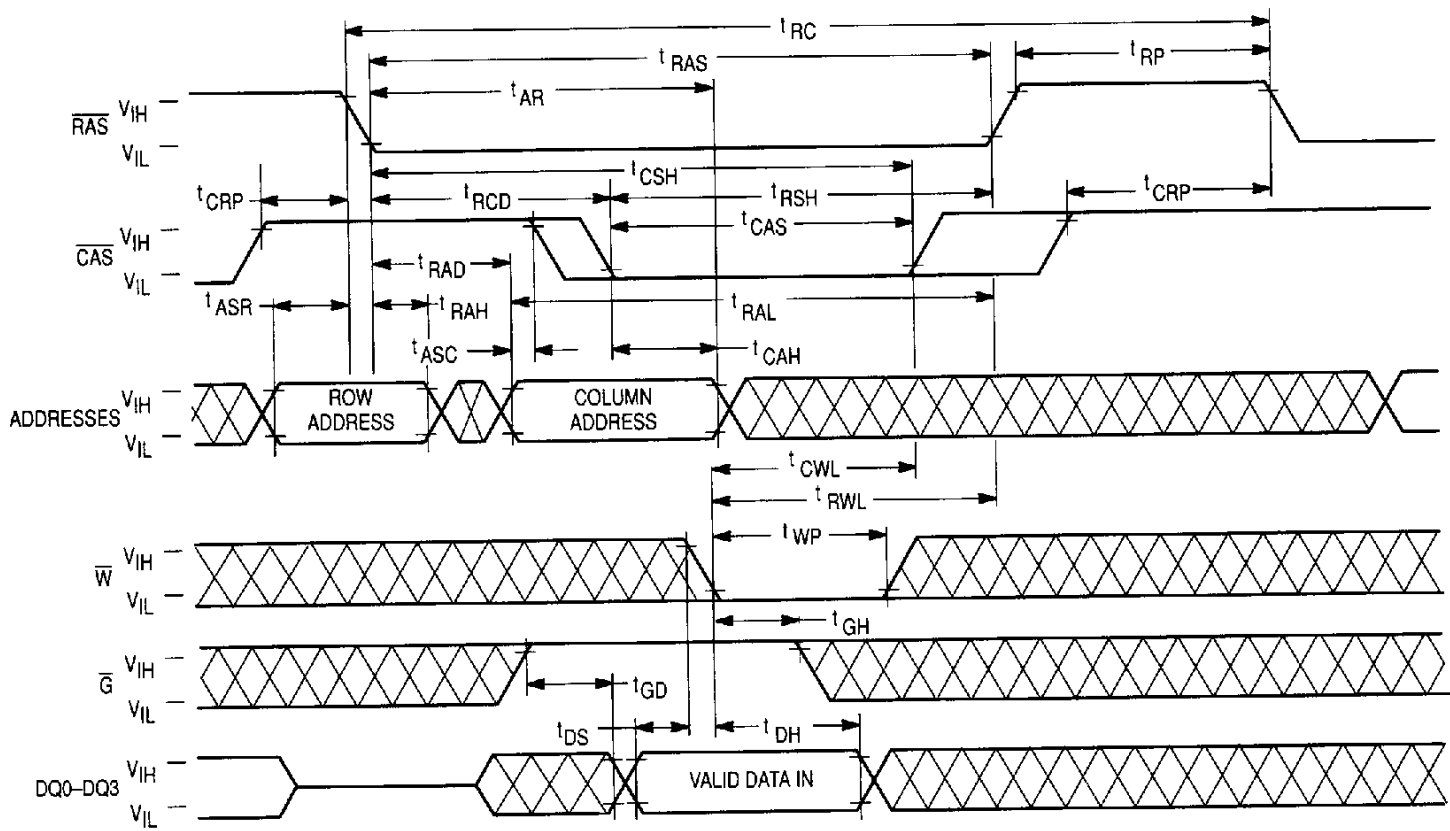


www.DataSheet4U.com

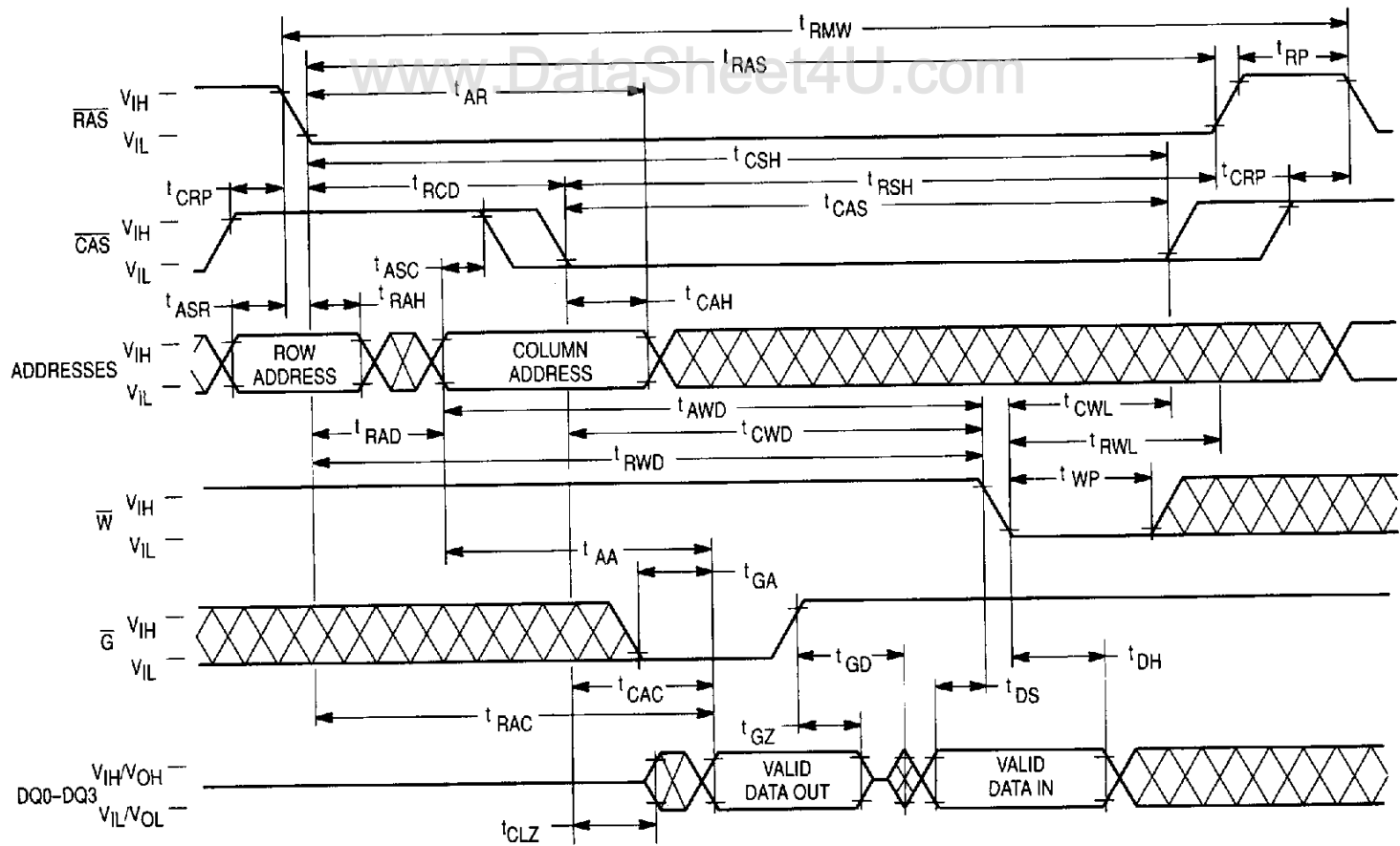
EARLY WRITE CYCLE



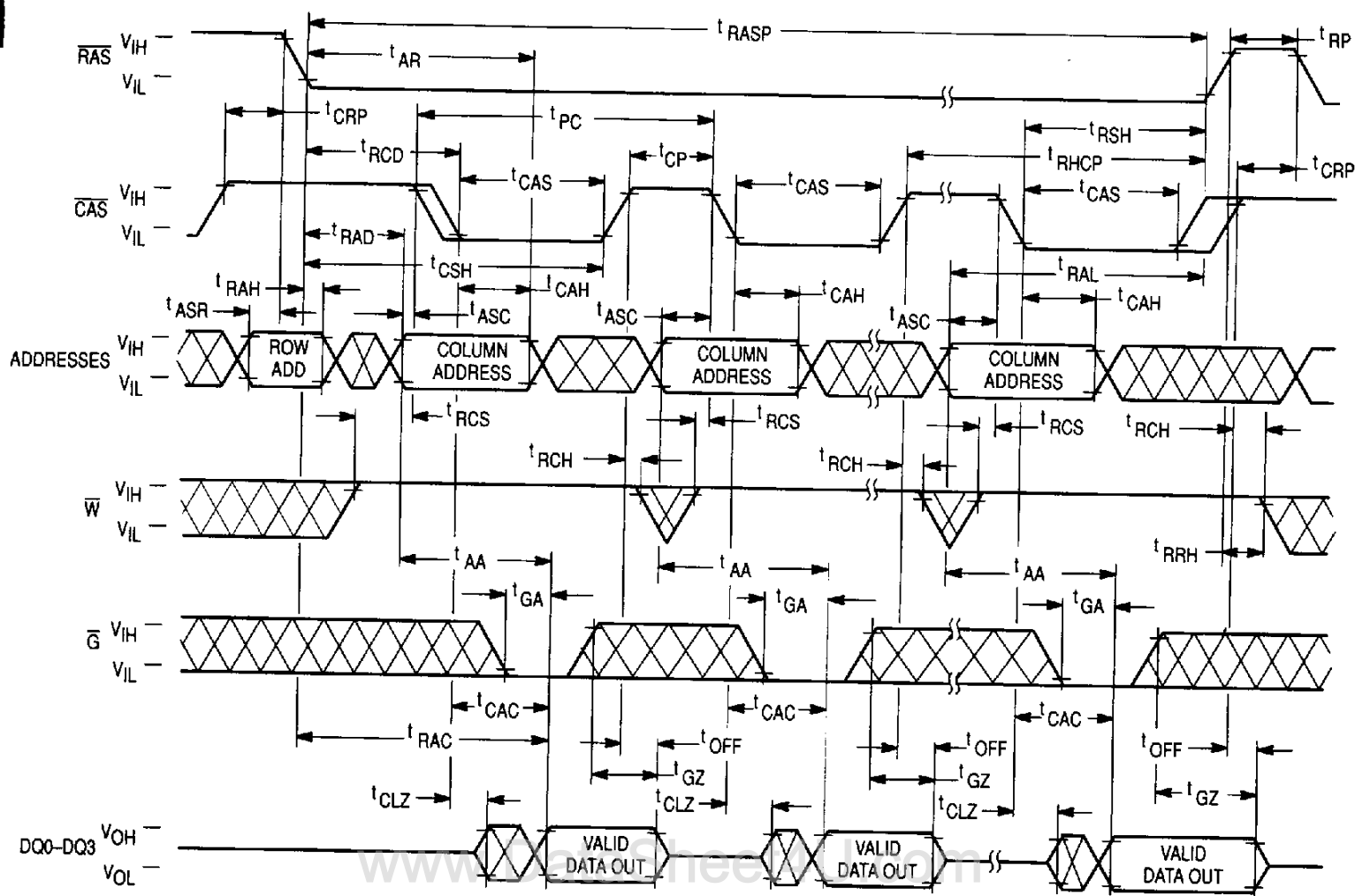
\bar{G} CONTROLLED LATE WRITE CYCLE



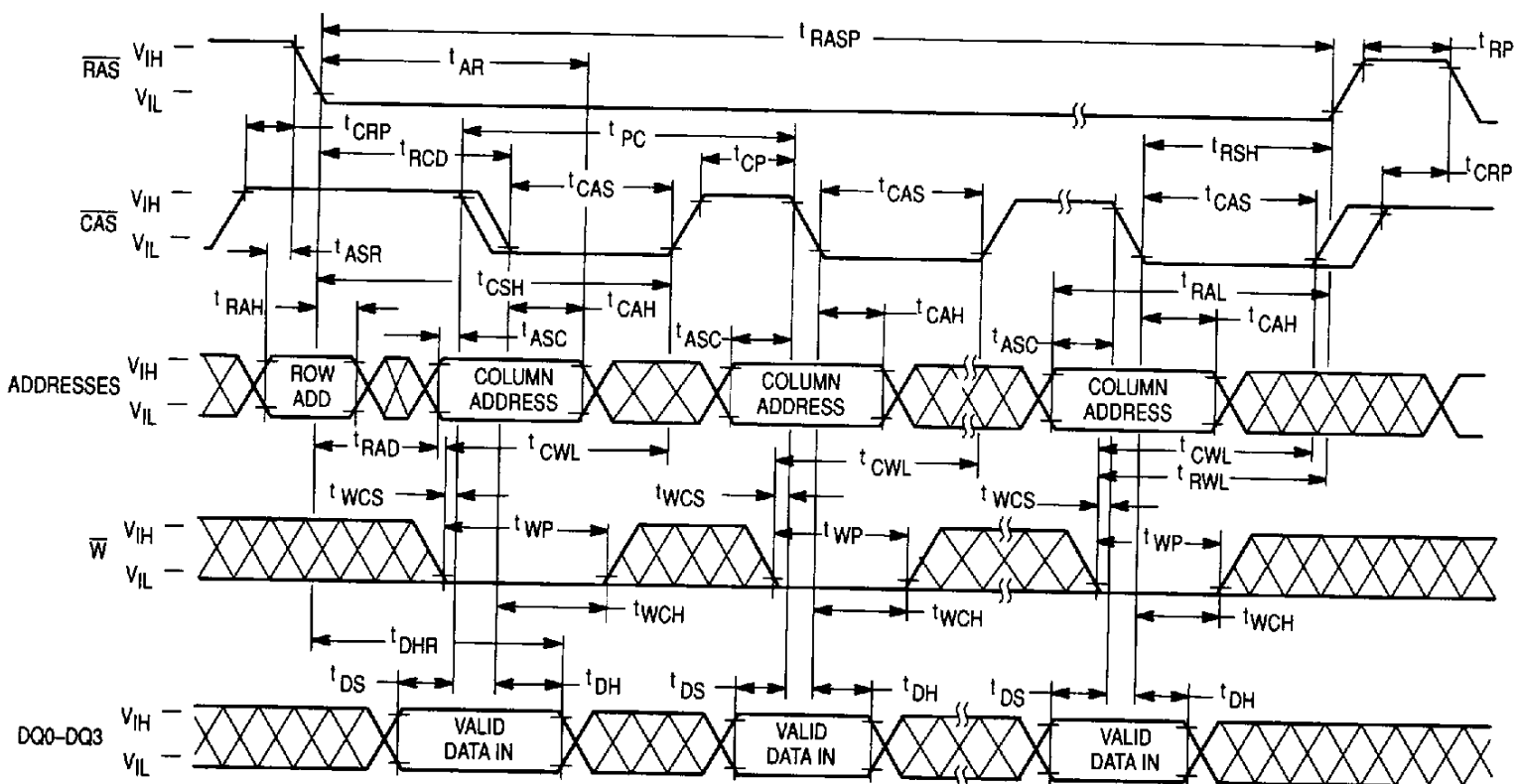
READ-WRITE CYCLE



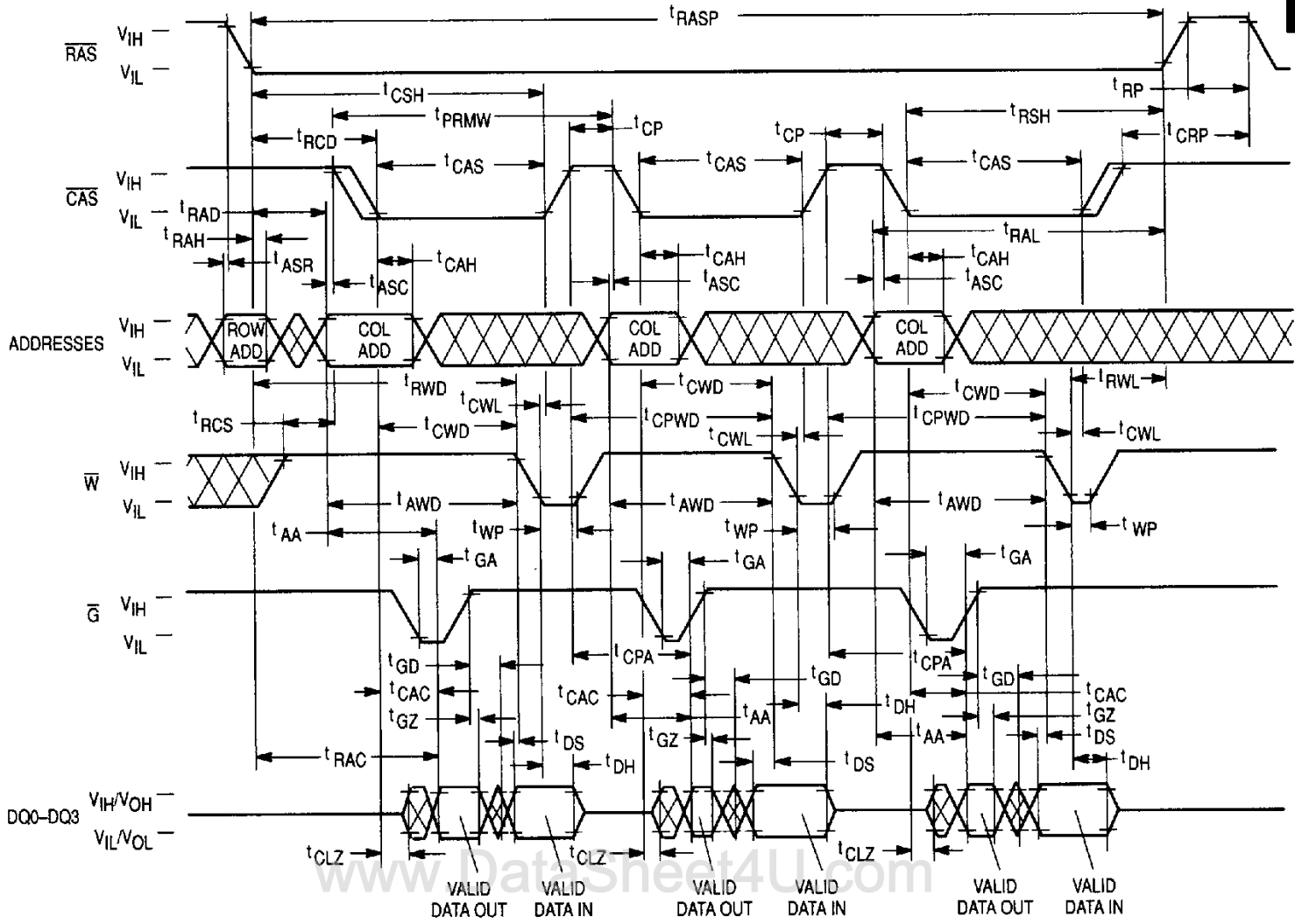
FAST PAGE MODE READ CYCLE



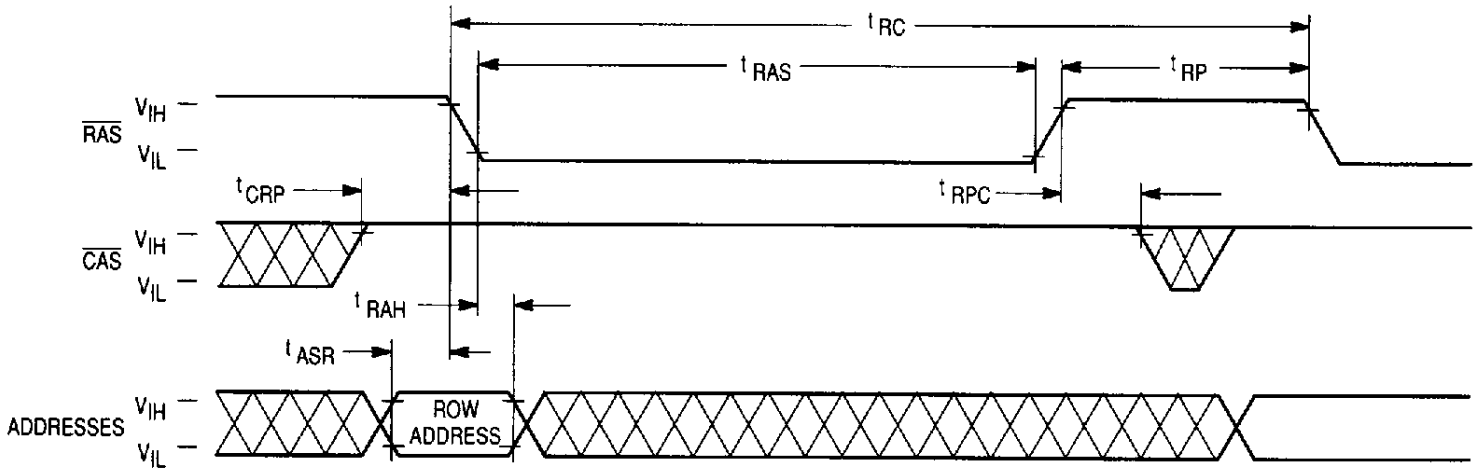
FAST PAGE MODE EARLY WRITE CYCLE



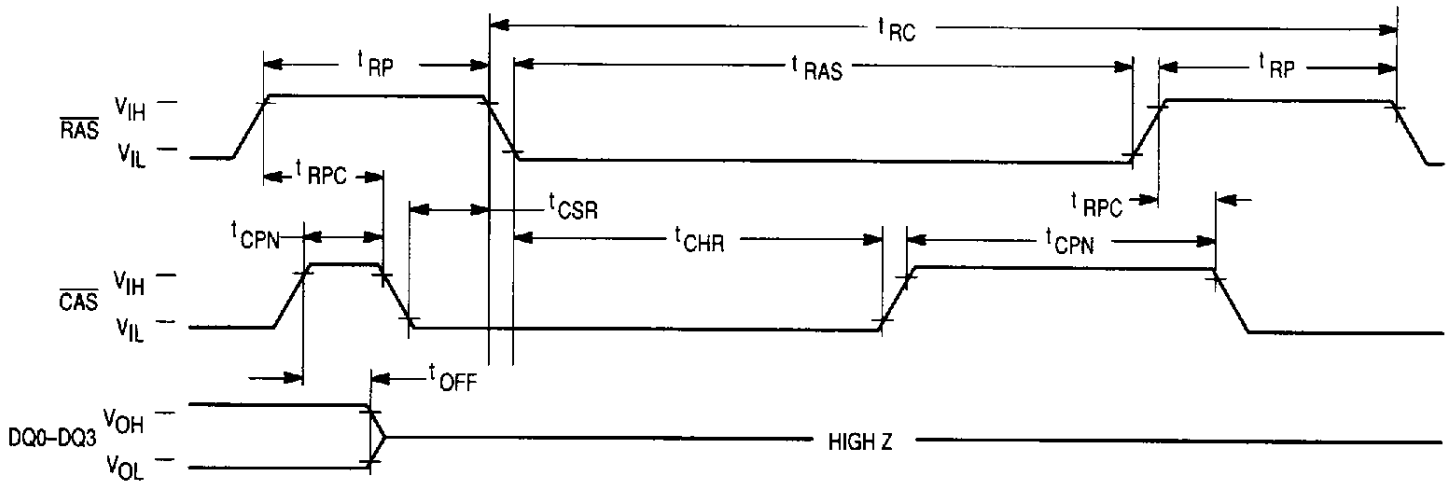
FAST PAGE MODE READ-WRITE CYCLE



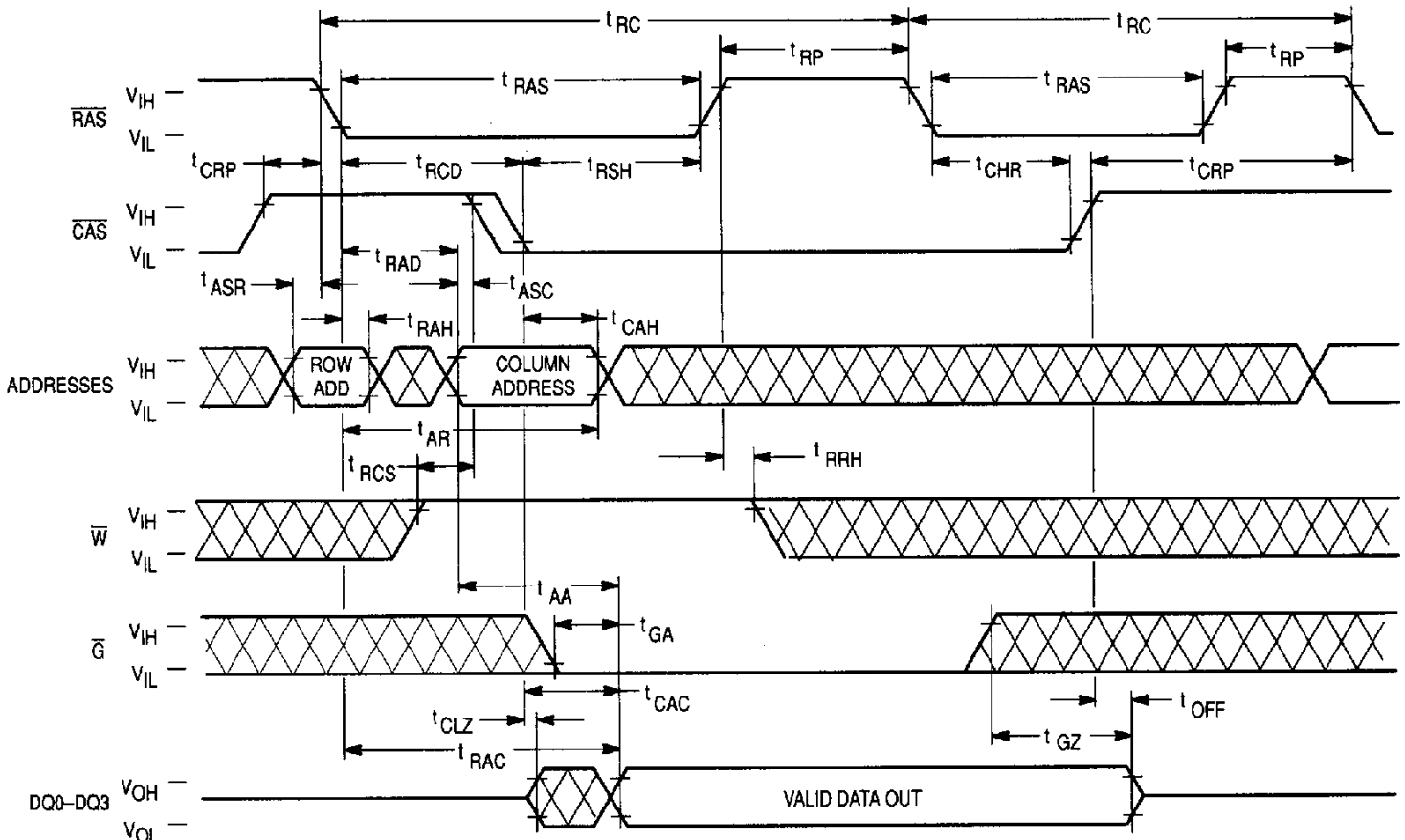
RAS ONLY REFRESH CYCLE
(\overline{W} and \overline{G} are Don't Care)



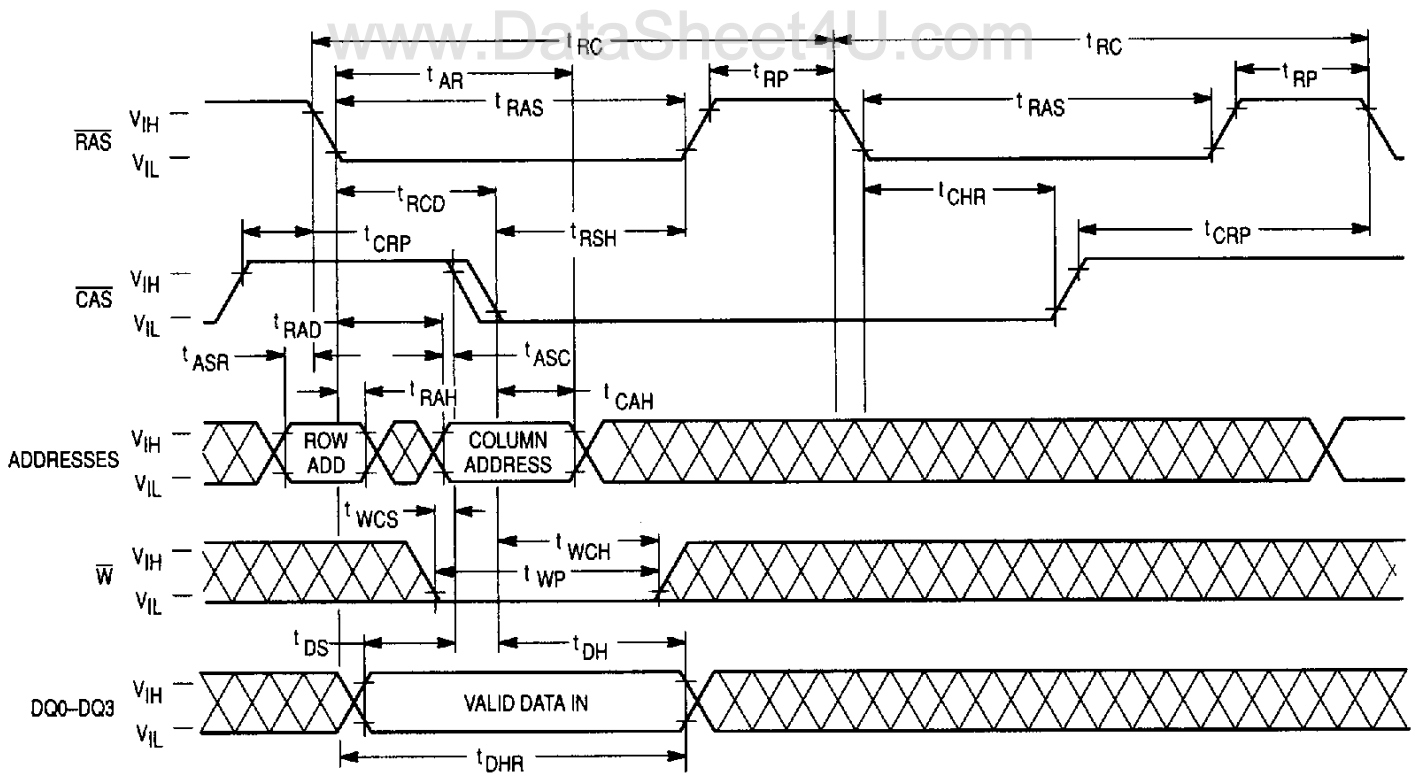
CAS BEFORE RAS REFRESH CYCLE
(\overline{W} , \overline{G} , and A0-A8 are Don't Care)



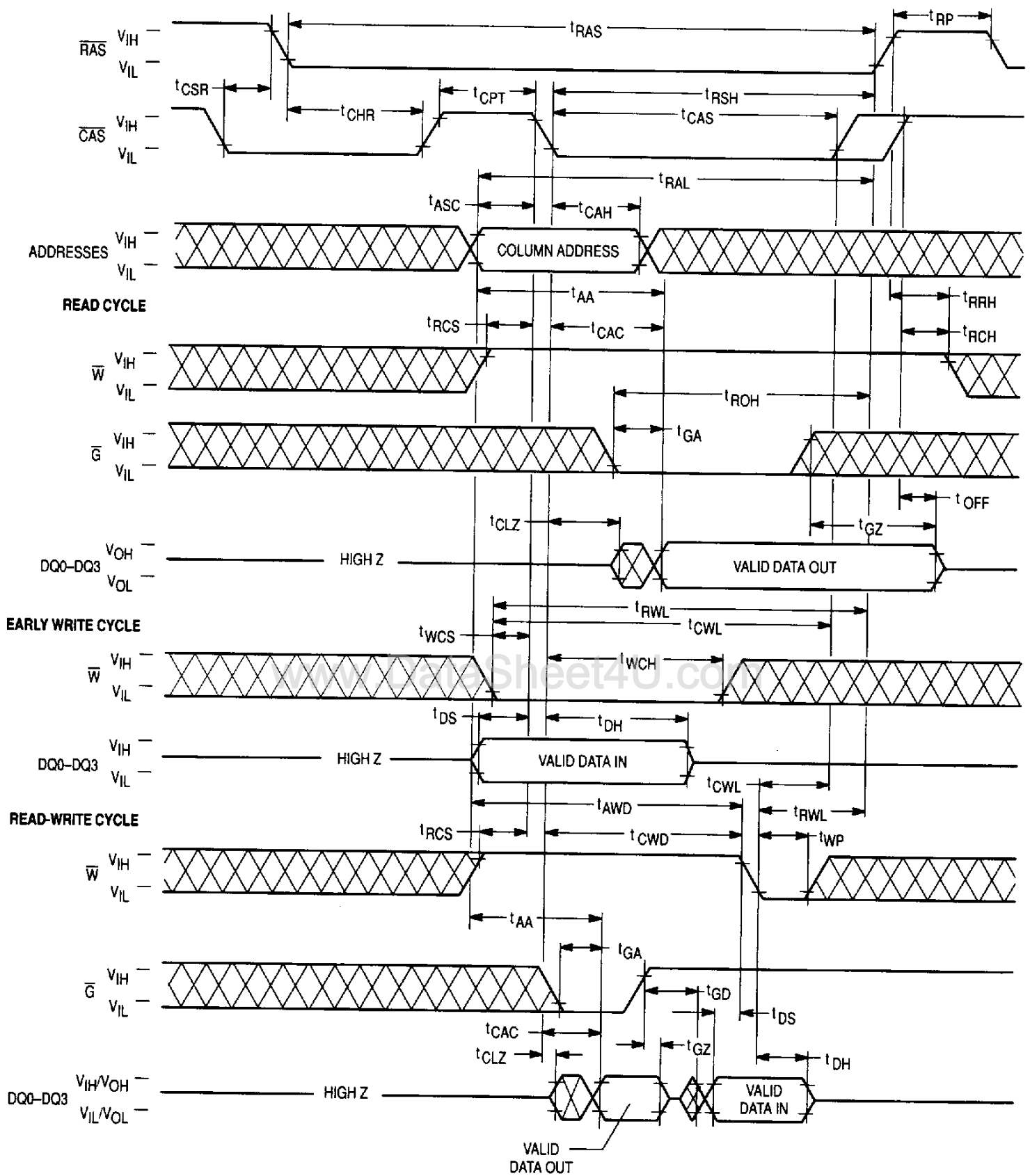
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = V_{IL} , t_{RCD} minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This gate feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are two other variations in addressing the 256K \times 4 RAM: **RAS only refresh cycle** and **CAS before RAS refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{G}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at t_{RCD} maximum and $\overline{\text{G}}$ must be active $t_{\text{RAC}} - t_{\text{GA}}$ (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{\text{RAS}}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{\text{G}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active

cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{G}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{G}}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time t_{RAS} and t_{CAS} , and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time t_{WCS} before $\overline{\text{CAS}}$ active transition. Data In (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for t_{RWL} and t_{CWL} , respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data out buffers disabled, effectively disabling $\overline{\text{G}}$.

A late write cycle (referred to as $\overline{\text{G}}$ controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{\text{RCD}} + t_{\text{CWD}} + t_{\text{RWL}} + t_{\text{T}} \leq t_{\text{RAS}}$, if timing minimums (t_{RCD} , t_{RWL} , and t_{T}) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but Q may be indeterminate—see note 15 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for t_{CWD} minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the 256K \times 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access time, t_{RAC} . Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between V_{IH} and V_{IL} . The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum t_{CP} , while $\overline{\text{RAS}}$ remains low (V_{IL}). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASp} . Page mode operation is ended when $\overline{\text{RAS}}$

transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the MCM514256A require refresh every 8 milliseconds while refresh time for the MCM51L4256A is 64 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM514256A and 124.8 microseconds for the MCM51L4256A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds on the MCM514256A and 64 milliseconds on the MCM51L4256A.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **RAS-only refresh**, **CAS before RAS refresh**, and **Hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1).

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle timing diagram**.

The test can be performed after a minimum of **eight CAS before RAS** initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **CAS before RAS refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

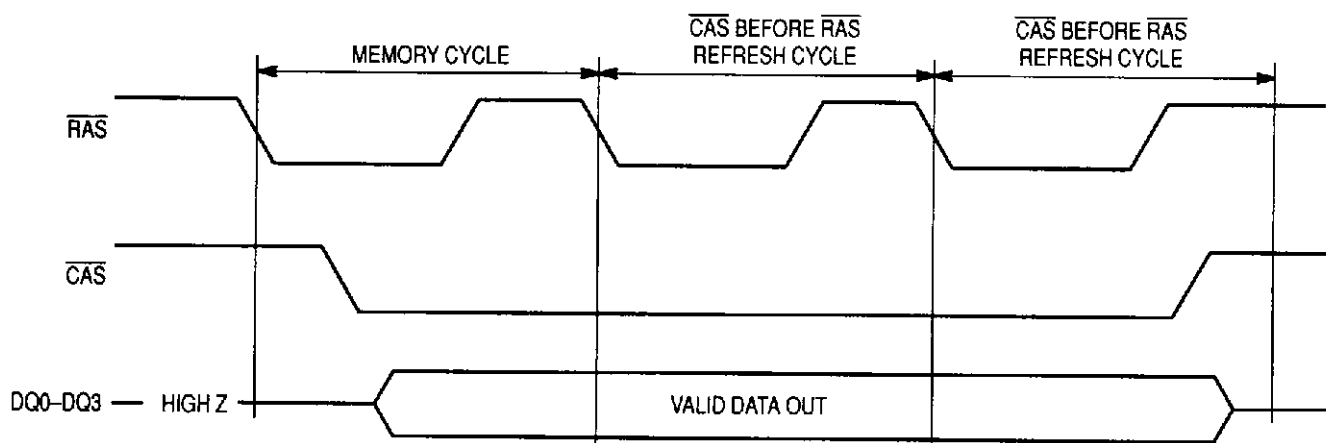
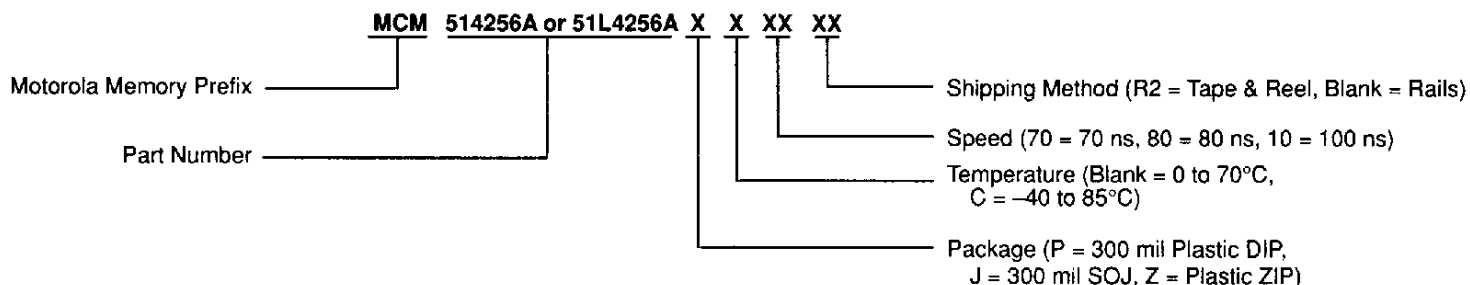


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION (Order by Full Part Number)



Commercial Temperature Range 0 to 70°C

Full Part Numbers—	MCM514256AP70	MCM514256AJ70	MCM514256AJ70R2	MCM514256AZ70
	MCM514256AP80	MCM514256AJ80	MCM514256AJ80R2	MCM514256AZ80
	MCM514256AP10	MCM514256AJ10	MCM514256AJ10R2	MCM514256AZ10
	MCM51L4256AP70	MCM51L4256AJ70	MCM51L4256AJ70R2	MCM51L4256AZ70
	MCM51L4256AP80	MCM51L4256AJ80	MCM51L4256AJ80R2	MCM51L4256AZ80
	MCM51L4256AP10	MCM51L4256AJ10	MCM51L4256AJ10R2	MCM51L4256AZ10

Industrial Temperature Range -40 to +85°C

MCM514256APC70	MCM514256AJC70	MCM514256AJC70R2	MCM514256AZC70
MCM514256APC80	MCM514256AJC80	MCM514256AJC80R2	MCM514256AZC80
MCM514256APC10	MCM514256AJC10	MCM514256AJC10R2	MCM514256AZC10
MCM51L4256APC70	MCM51L426AJC70	MCM51L426AJC70R2	MCM51L4256AZC70
MCM51L4256APC80	MCM51L426AJC80	MCM51L426AJC80R2	MCM51L4256AZC80
MCM51L4256APC10	MCM51L426AJC10	MCM51L426AJC10R2	MCM51L4256AZC10

NOTE: Low Power Industrial Temperature SOJ device part numbers are one character shorter than corresponding PDIP or ZIP part numbers.

www.DataSheet4U.com