I-Cube®

IQ Family Data Sheet

FEATURES

- SRAM-based, in-system programmable
- Switch Matrix
  - — Non-Blocking
  - — Identical and predictable delays
  - — One-to-one, one-to-many and many-to-one connections
- RapidConnect™ parallel interface for fast, incremental configuration of Switch Matrix and I/O Port attributes
  - — 100% JTAG compliant
  - — Pin compatible with the IQX family of devices
- Clocked, Latched and Flow-through Dataflow Modes
  - — As low as 7 ns pin-to-pin delay in flow-through mode and 150 MHz clock rate in registered mode
- I/O Ports
  - — Individually programmable as input, output or bidirectional
  - — For each I/O Port, clock, clock enable, input enable and output enable can be selected independently from a large pool of common control signals
  - — 12 mA current drive
  - — Separated I/O power pins for easy interfacing between 5V and 3.3V signals

DESCRIPTION

The IQ family of SRAM-based bit-oriented switching devices is manufactured using 0.6µm CMOS processes. These devices offer clock speeds of up to 150 MHz and pin-to-pin delay as low as 7 ns.

The IQ devices are used in applications requiring dynamic switching and flexible routing /interconnection of signals. These applications include communication switches, network systems, image processing engines, file/video servers, testers and emulators.

At the heart of IQ devices is a non-blocking Switch Matrix. A line in the Switch Matrix can be connected to one or more other lines. The Switch Matrix lines are connected to I/O Ports with programmable functional attributes.

The Switch Matrix connections are programmed and the I/O Port attributes are configured by storing data in the internal SRAM cells. The IQ devices use a JTAG-based serial mode for configuration. For dynamic switching, the RapidConnect interface allows fast connection changes.

The IQ devices support the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The same interface is also used for serially downloading the configuration bit stream into the devices.

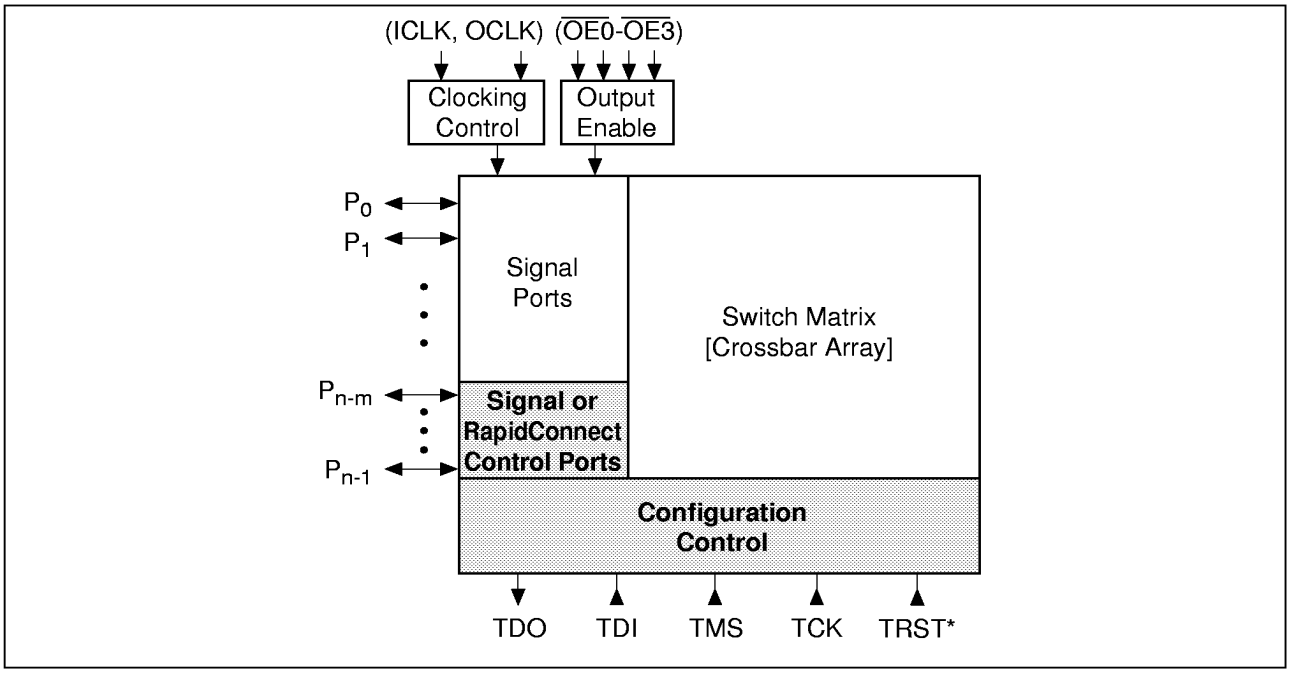
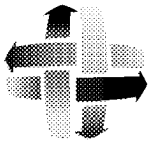
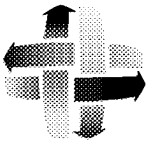


Figure 1. IQ Functional Block Diagram

Contents



Figures



Tables

1.0 ARCHITECTURE

The IQ devices are designed using 0.6 µm CMOS technology and are configured by storing appropriate data into the internal SRAM cells and registers. The main functional blocks of the device are the Switch Matrix (Crossbar Array), I/O Ports, and Configuration Controller (see Figure 1).

External signals enter and exit each device through its I/O Ports. The Switch Matrix is used to internally connect these I/O Ports to one another.

The JTAG-based Configuration Controller decodes the incoming configuration bitstream and stores the data into the Switch Matrix SRAM cells and I/O Port configuration registers. Additionally, by enabling the RapidConnect mode, the SRAM cells can be accessed directly, allowing incremental changes (make or break) to the Switch Matrix connections in a single cycle.

1.1 Switch Matrix

Figure 2 shows a small section of the Switch Matrix.

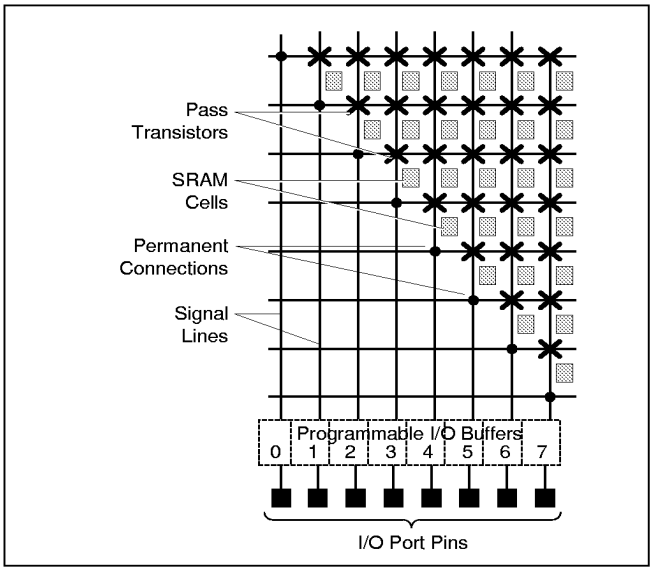


Figure 2. Switch Matrix (Crossbar Array) Structure

The Switch Matrix consists of a number of signal lines, one per I/O Port, and an array of pass transistor switches, each programmable with an SRAM cell. Each switch, when programmed to be in the ON state, connects a unique pair of signal lines in the Switch Matrix. The external signals are connected to the Switch Matrix signal lines through I/O Ports.

A connection between two I/O Ports is made by turning ON the transistor switch at the intersection of the corresponding signal lines. The Switch Matrix is globally connected, and therefore a connection can always be made between any two I/O Ports. Moreover, only one transistor switch needs to be turned ON in order to make a connection between two I/O Ports. This arrangement provides a fully non-blocking architecture offering 100% utilization, guaranteed connections, and uniform and predictable delays.

This Switch Matrix architecture supports connecting more than two I/O Ports together for multicasting/broadcasting operation. A new connection can be made or an existing connection can be broken without affecting other connections, allowing incremental reconfiguration of the Switch Matrix.

The contents of the SRAM cells controlling the pass transistor switches are unchanged when the device is reset. The SRAM cells must be explicitly cleared during initialization to eliminate any residual connections.

1.2 Programmable I/O Ports

The I/O Port structure is shown in Figure 3.

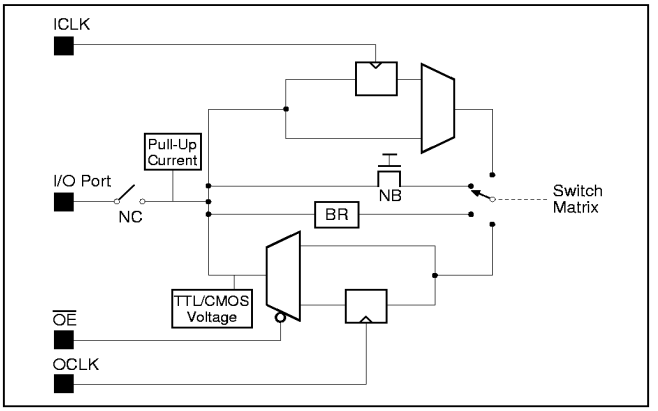


Figure 3. Programmable I/O Buffer

The attributes of each I/O Port are individually programmable. The attributes include its I/O function, output voltage level and pull-up current. Each I/O Port is buffered to provide high input impedance, low input capacitance, low output impedance and high current drive.

The IQ devices, with the exception of IQ48 and IQ32B, have four Output Enable signals, each controlling an equal number of I/O Ports; 80 each in the case of IQ320, 60 each for IQ240B and so on. The IQ48 and IQ32B have a single Output Enable signal that controls all I/O Ports. All IQ devices have two global clock signals, ICLK and OCLK.

1.3 I/O Buffer Functions

Table 1 shows the various I/O Port functions that can be programmed and are described below.

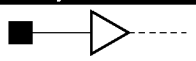
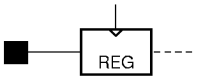
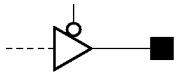
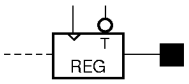
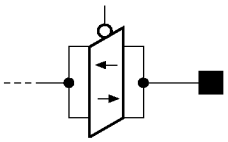
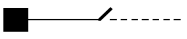
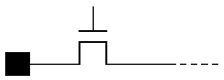
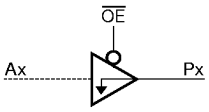
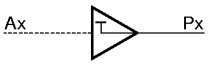
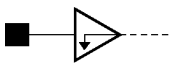
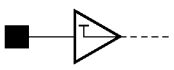
Symbol	I/O Port Function	Mnemonic
	**Input** - The external signal at the I/O Port pin is connected to the corresponding Switch Matrix line through a buffer.	IN
	**Registered Input** - The external signal at the I/O Port pin is connected to the input of a flip-flop and the output of the flip-flop is connected to the corresponding Switch Matrix line. The clock input of the flip-flop is driven by the external clock signal, ICLK. The state of the flip-flop is not affected by device reset. When an I/O Port is configured as an Input (IN) or Registered Input (RI), V_{IH} and V_{IL} are at TTL levels.	RI
	**Output** - The corresponding Switch Matrix line is connected to the I/O Port pin through a buffer.	OP †
	**Registered Output** - The corresponding Switch Matrix line is connected to the input of a flip-flop, and the output of the flip-flop is connected to the I/O Port pin. The clock input of the flip-flop is driven by the external clock signal, OCLK. The state of the flip-flop is not affected by device reset.	RO †
	**Bus Repeater** - In the Bus Repeater mode, the I/O Port and the corresponding Switch Matrix line behave as if they were connected by a wire (with a non-zero propagation delay), allowing bidirectional signal flow. The Bus Repeater (patented by I-Cube) incorporates a self-sensing circuit to determine signal direction. When multiple I/O Ports configured as Bus Repeater are connected together through the Switch Matrix to form a single internal node, a signal appearing at any one of the I/O Ports is repeated to the remaining I/O Ports that are a part of that node. The Bus Repeater mode requires an external or internal (see the section on "Programmable Pull-up Current") pull-up current source to operate properly. For more details, refer to the Technical Note: "The Bus Repeater Mode."	BR †
	**No Connect** - The I/O Port pin is isolated from the Switch Matrix line. Upon reset all I/O Ports are automatically configured as No Connect (NC).	NC
	**Non-Buffer** - The I/O buffer is bypassed and the I/O Port pin is connected to the corresponding Switch Matrix line through a pass transistor. This mode can be used to pass analog signals if certain conditions are met. Contact I-Cube for more details.	NB
	**Pin Side Force 0** - The I/O Port pin is forced low (logic 0) by the internal buffer, regardless of the signal on the corresponding Switch Matrix line.	F0 †
	**Pin Side Force 1** - The I/O Port pin is forced high (logic 1) by the internal buffer, regardless of the signal on the corresponding Switch Matrix line.	F1†
	**Array Side Force 0** - The Switch Matrix line is forced low (logic 0), regardless of the signal on the corresponding I/O Port.	A0
	**Array Side Force 1** - The Switch Matrix line is forced high (logic 1), regardless of the signal on the corresponding I/O Port.	A1

Table 1. IQ Family I/O Buffer Attributes

† In these modes, the Output Enable signal control the active and Hi-Z state. The buffers are driving the pin when the corresponding Output Enable signal (see Table 7) is low, and Hi-Z when it is high.

I/O Buffer Function	Data Flow	Tristate Function	Mnemonic Used by I-Cube Software
Input	Flow–through	No	IN
	Registered	No	RI
Output	Flow–through	Yes	OP
	Registered	Yes	RO
Bidirectional (Bus Repeater)	Flow–through	Yes	BR
Pin Side Force 0 or 1	N/A	Yes	F0, F1
Array Side Force 0 or 1	N/A	No	A0, A1
Non Buffered	Flow–through	No	NB
No Connect	N/A	N/A	NC

Table 2. Summary of Programmable I/O Attributes for IQ Devices

1.4 Output Voltage Level

When an I/O Port is configured in the "output" modes - Output (OP), Registered Output (RO), and Output Force 1 - the output high voltage can be programmed as TTL high or CMOS high. In the Bus Repeater (BR) mode, the output high level is always CMOS high.

1.5 Programmable Pull-up Current

As shown in figure 4, the I/O buffer contains several pull-up devices. The normal pull–up current (I_{OH})is supplied by an n or p channel device for TTL and CMOS output levels respectively. The devices supplying the normal pull–up are controlled by internally generated control signals.

An additional pull–up current (I_{PU-WK}) or (I_{PU-SG}) can be programmed at each I/O Port. This additional current is primarily used for the Bus Repeater (BR) mode, but its use is not restricted to that mode alone. P channel devices, controlled by programming cells are used to supply the additional pull–up current; therefore, when this feature is used with one of the "output" modes - Output (OP), Registered Output (RO), Bus Repeater (BR), and Output Force 1 (F1) - the outputs high voltage levels become CMOS levels.

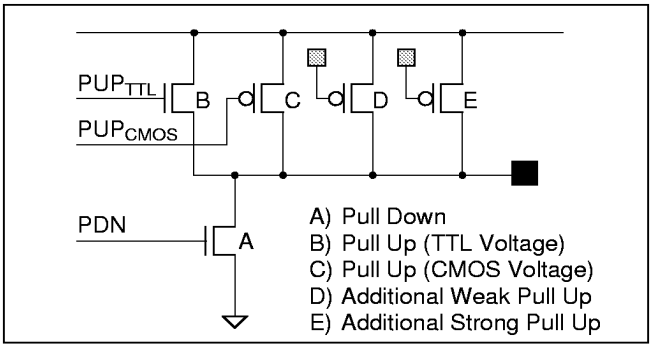


Figure 4. IQ Output Driver and Pull-Up Current

2.0 Configuration Controller

The configuration of IQ devices involves initializing internal Mode/Control register, configuring the I/O Ports and establishing connections among the Switch Matrix lines. The IQ devices are ready for configuration as soon as they come out of reset.

The JTAG (IEEE 1149.1) interface, described below is used as the primary configuration mechanism for configuring IQ devices. In addition, the RapidConnect parallel mode is available for changing connections in the Switch Matrix.

2.1 JTAG Interface

The JTAG interface is a serial interface and uses four pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select (TMS). TCK is used to clock data in and out of TDI and TDO. TMS, in conjunction with TDI implements the state machine that controls the various operations of the JTAG protocol. In addition, the device reset signal (TRST*) is used to reset the JTAG controller.

2.2 I/O Port Configuration

I/O Port configuration is accomplished by loading the appropriate bitstream into the programming registers present at each I/O Port. Only the JTAG interface can be used to load these programming registers.

2.3 Switch Matrix Configuration

The contents of the SRAM cells controlling the Switch Matrix connections can be modified using either the JTAG interface or the RapidConnect interface.

The JTAG serial interface is used to load the data, one word at a time into the SRAM cells in the Switch Matrix. The RapidConnect parallel interface, on the other hand, provides direct write access to individual SRAM cells in the Switch Matrix.

The RapidConnect mode is used in applications which require fast switching. In this mode, a designated number of I/O pins are reassigned as RapidConnect pins. These pins form the address (RA, CA), instruction (C0, C1) and control ($\overline{WE}$, $\overline{STROBE}$) buses. These buses directly address the internal Switch Matrix SRAM cells allowing their contents to be altered very quickly, resulting in fast connection changes. For more details refer to the section on "RapidConnect Hardware Interface."

3.0 MISCELLANEOUS DETAILS

3.1 Device Reset

To ensure proper operation, the device reset pin, TRST* must be held low during power up. The recommended reset circuitry is shown in Figure 5. The reset pulse must be at least 200ns long.

IQ devices can be reset either by pulsing TRST* low or by applying five JTAG clocks (TCK pin) while holding TMS high.

When the IQ device is reset, the I/O buffers return to the No Connect (NC) state, Turbo mode (see next section) is set to its default state, and the RapidConnect mode is disabled.

When the IQ device is reset, the Switch Matrix SRAM cells are NOT cleared. The SRAM cells must be cleared explicitly by loading the initialization bitstream sequence, which is generated either by the user or by I-Cube supplied software.

The IQ devices are ready for configuration as soon as they come out of reset.

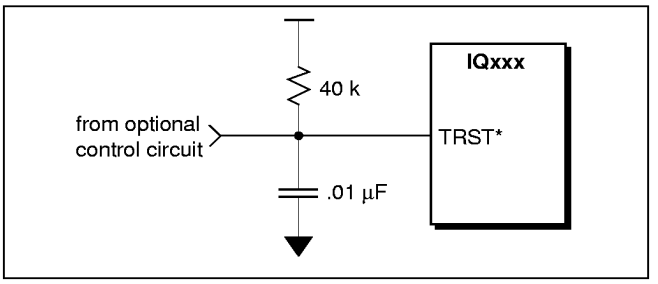


Figure 5. Reset Circuit

3.2 Turbo Mode

The Turbo mode reduces the propagation delay "t_{PLH}" and "t_{PHL}" through the IQ devices. This is achieved by detecting low-to-high and high-to-low transitions earlier than the standard mid-voltage threshold. In this mode, the low-to-high transition point is set at a voltage lower that the mid-point $V_{DD}/_2$, while the high-to-low transition point is set at a voltage higher than $V_{DD}/_2$.

To permit high frequency NRZ data streams to pass through the IQ devices, the Turbo mode can be disabled by changing the appropriate bit in the Mode/Control Register. For further information refer to the Technical Note: "The Turbo Mode."

The Turbo mode is disabled upon reset for all IQ devices except IQ48 and IQ32B, and can be enabled or disabled through JTAG. The initialization sequence generated by the I-Cube software enables the Turbo Mode unless instructed to do otherwise.

In this data sheet, all AC parameters except the NRZ data rate (R_{DATA}) are specified with the Turbo Mode enabled.

3.3 Clock and Output Enable Pins

The IQ devices have two global clock pins, ICLK and OCLK. These pins are used as clocks for the I/O Ports configured as Registered Input (RI) and Registered Output (RO) respectively. When unused, these pins should be tied to V_{SS}.

The Output Enable pins are used to control the active and hi-Z states of the I/O Ports configured as Output (OP), Registered Output (RO), Bus Repeater (BR), Pin Side Force 0 (F0) and Pin Side Force 1 (F1). Table 7 lists the I/O Ports controlled by the different Output Enable pins. In these modes, the I/O Port buffers are driving when the corresponding Output Enable signal is low, and hi-Z when it is high. The Output Enable signals have no effect on the I/O Ports configured in any modes other than the ones listed above. In most applications the Output Enable pins will be tied to V_{SS}.

3.4 Mode/Control Register

The IQ devices contain a 16-bit register that is used to store the RapidConnect Enable and Turbo Mode Enable bits. The remaining bits are used for internal testing purposes. For more information see the "IQ Family Register Programming Users Reference".

4.0 CONFIGURING IQ DEVICES

The IQ devices are typically configured as follows:

- The device is reset by external circuitry (TRST*=0).
- A bitstream is downloaded through the JTAG interface to initialize the JTAG configuration controller, clear and/or configure the Switch Matrix SRAM cells, configure the I/O Ports and lastly set the Mode/Control register to enable RapidConnect mode and/or disable Turbo Mode if necessary.
- Switch connections are changed with JTAG or RapidConnect (if enabled).

4.1 Bitstream Generation

A bitstream can be generated off-line or in-system by an embedded CPU using one of the following methods:

- By using I-Cube Development System Software products IDS100 or IDS200.
- Generated by the user with the help of the "IQ Family Register Programming User's Reference" manual. I-Cube software is not required when using this method.

If the bitstream is generated off-line then, depending on the application, it is either stored in non-volatile memory or directly downloaded from a host processor.

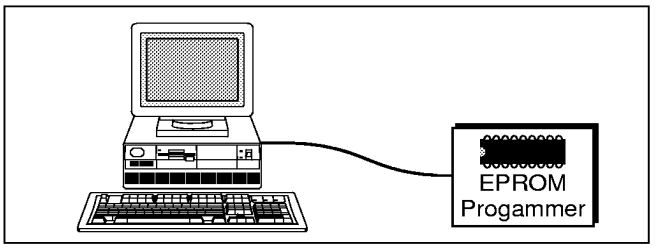


Figure 6. Off -line Bitstream Generation

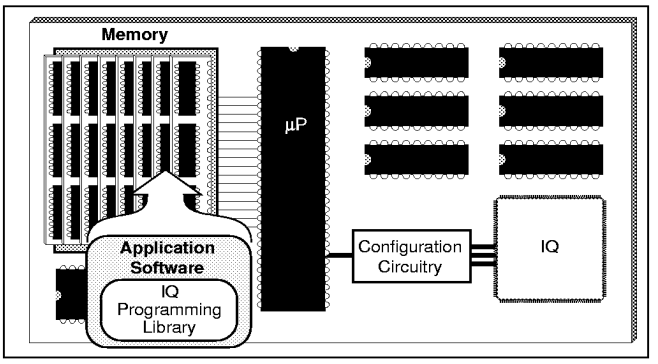


Figure 7. Embedded Bitstream Generation

4.2 JTAG Hardware Interface

JTAG-based configuration allows a single IQ device or multiple IQ devices connected in a chain to be programmed in a single operation. For multiple IQ configuration the TCK, TMS and TRST* signals are bused to all devices. The TDI and TDO signals are daisy chained as shown in Figure 8.

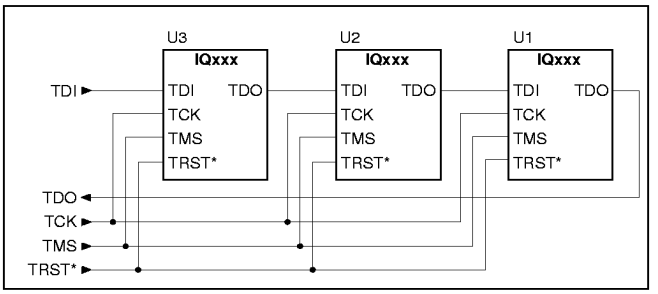


Figure 8. Configuring Multiple IQ Devices

During the initial configuration sequence, the JTAG controllers on all IQ devices are first brought to their default state by either using the TRST* reset pin or by applying a sequence of five 1s ("11111") on the TMS pins (the JTAG reset sequence). This is followed by the actual configuration bitstream, which is downloaded into the IQ devices over the TDI and TMS pins. The JTAG cycle count, configuration times and bitstream size are shown in Table 3.

Operation	IQ96	IQ64B	IQ48	IQ32B
Make /Break a single connection using JTAG	122 cycles	122 cycles	74 cycles	74 cycles
Configuration Time (µs)	4.88	4.88	2.96	2.96
Configure all I/O Ports	410 cycles	410 cycles	218 cycles	218 cycles
Configuration Time (µs)	16.4	16.4	8.72	8.72
Complete Configuration [Configure all I/O Ports and Switch Matrix connections]	10,000 cycles	8,000 cycles	3,000 cycles	2,500 cycles
Configuration Time (ms)	0.4	0.32	0.15	0.125
Bitstream size (Bytes)	2,500	2,000	750	625

Table 3. Number of JTAG Cycles and Configuration Time (using a 20 MHz JTAG Clock)

4.3 RapidConnect Hardware Interface

RapidConnect mode allows direct access to the Switch Matrix SRAM cells allowing fast connection changes. By using RapidConnect, a single connection can be changed (made or broken) in one SRAM write cycle. This feature is very useful for real-time switching applications. Figure 9 shows a typical interface for real-time configuration of the IQ devices. Table 4 shows the number of I/O Ports used by the RapidConnect interface.

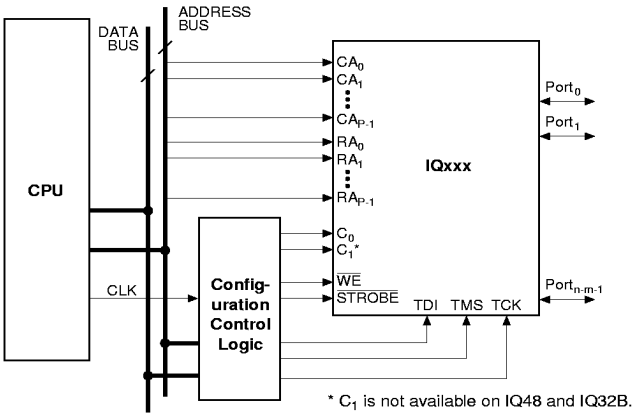


Figure 9. Target System Interface in RapidConnect Mode

	IQ96	IQ64B	IQ48	IQ32B
Total number of signal I/O Ports on the device (n)	96	64	48	32
I/O Ports used for RapidConnect interface (m)	18	16	15	13
Number of I/O Ports used for Row and Column Address each (p)	7	6	6	5
Number of signal I/O Ports that can be switched using RapidConnect interface (n-m)	78	48	33	19

Table 4. Number of Pins Used for RapidConnect Interface

4.4 RapidConnect Commands and Initialization

Upon reset, the RapidConnect mode is disabled and must be enabled by setting the RapidConnect Enable bit in the on-chip Mode/Control Register. In addition, the RapidConnect interface pins must be configured as inputs (IN). These two operations are performed by loading the appropriate bitstream through the JTAG configuration interface.

Pins used for RapidConnect form three buses - address, control and instruction. As shown in Figure 2, the Switch Matrix SRAM cells form a two dimensional array and each SRAM cell is uniquely identified by its Row Address, RA_0 - RA_{P-1}, and Column Address, CA_0 - CA_{P-1}. The control bus is composed of a write enable (chip select) signal, $\overline{WE}$, and write strobe signal, $\overline{STROBE}$. C0 and C1 comprise the command bus. Table 5 describes various combinations of commands.

C1	C0	RapidConnect Action
0	0	Write "0" to the selected SRAM cell, breaking the connection. Clear all other SRAM cells in the row selected by Row Address, thereby breaking the corresponding connections.
0	1	Write "1" to the selected SRAM cell, making the connection. Clear all other SRAM cells in the row selected by Row Address, thereby breaking the corresponding connections.
1	0	Write "0" to the selected SRAM cell, breaking the connection. No other connections are affected.
1	1	Write "1" to the selected SRAM cell, making the connection. No other connections are affected.

Table 5. RapidConnect Operations

The making or breaking of a connection takes place on the falling edge of $\overline{STROBE}$, when $\overline{WE}$ is active (low).

When RapidConnect is enabled, the JTAG interface can be used to change the I/O Port attributes but cannot be used to change Switch Matrix connections. The RapidConnect mode must first be disabled (through the JTAG interface) before the Switch Matrix connections can be changed using the JTAG interface.

The number of I/O Ports that can be addressed (switched) using the RapidConnect interface is shown in Table 4.

For more application details on the RapidConnect interface, refer to the related Technical Notes.

5.0 PIN SUMMARY

The pin summary for the members of the IQ family is given in Tables 6 and 7.

Pin Name				I/O/B	Description
IQ96	IQ64B	IQ48	IQ32B		
P00 - P77	P00 - P47	P00 - P32	P00 - P18	I/O/B	I/O port pins
P78 - P84/ CA0 - CA6	P48 - P53/ CA0 - CA5	P33 - P38/ CA0 - CA5	P19 - P23/ CA0 - CA4	I/O/B	I/O port pins in JTAG serial configuration mode and crossbar column address pins in RapidConnect mode
P85 - P91/ RA0 - RA6	P54 - P59/ RA0 - RA5	P39 - P44/ RA0 - RA5	P24 - P28/ RA0 - RA4	I/O/B	I/O port pins in JTAG serial configuration mode and crossbar row address pins in RapidConnect mode
P92/C0	P60/C0	P45/C0	P29/C0	I/O/B	I/O port or RapidConnect control bit 0
P93/C1	P61/C1	-	-	I/O/B	I/O port or RapidConnect control bit 1
P94/$\overline{WE}$	P62/$\overline{WE}$	P46/$\overline{WE}$	P30/$\overline{WE}$	I/O/B	I/O port or RapidConnect write enable, Active low
P95/$\overline{STROBE}$	P63/$\overline{STROBE}$	P47/$\overline{STROBE}$	P31/$\overline{STROBE}$	I/O/B	I/O port or RapidConnect strobe, Active low
$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$-$\overline{OE3}$	$\overline{OE0}$	$\overline{OE0}$	I	Dedicated output enable control pins. Active low. Each pin controls an equal number of I/O pins. See next table.
ICLK	ICLK	ICLK	ICLK	I	Clock for input registers
OCLK	OCLK	OCLK	OCLK	I	Clock for output registers
TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	I I O	JTAG pins
TRST*	TRST*	TRST*	TRST*	I	Chip Reset, Active low
V_{DD}.PAD	V_{DD}.PAD	V_{DD}.PAD	V_{DD}.PAD	P	Power Pins for I/O Buffer Drivers Only
V_{DD}	V_{DD}	V_{DD}	V_{DD}	P	Power Pins for on-chip circuitry other than I/O Buffer Drivers
V_{SS}.PAD	V_{SS}.PAD	V_{SS}.PAD	V_{SS}.PAD	P	Ground Pins for I/O Buffer Drivers Only
V_{SS}	V_{SS}	V_{SS}	V_{SS}	P	Ground Pins for on-chip circuitry other than I/O Buffer Drivers

Table 6. Pin Summary

	IQ96	IQ64B	IQ48	IQ32B
$\overline{OE0}$	0-23	0-15	0-47	0-31
$\overline{OE1}$	24-47	16-31	-	-
$\overline{OE2}$	48-71	32-47	-	-
$\overline{OE3}$	72-95	48-63	-	-

Table 7. Output Enable Pin Summary

6.0 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings (1)

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	-0.3 to +7.0	V
V_{DD}.PAD	Supply Voltage for I/O Buffer Driver (IQ96, IQ64B, IQ48 and IQ32B only)	$-0.3 \le V_{DD}.PAD \le V_{DD} + 0.3$	V
V_{IN}(2)	Input Voltage (IQ96, IQ64B, IQ48 and IQ32B)	-0.3 to V_{DD}.PAD+0.3	V
T_J	Junction Temperature (PQFP, TQFP and PLCC)	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{SINK}	Sink Current per Pin	150	mA

Table 8. Absolute Maximum Ratings

6.2 Recommended Operating Conditions (2)

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	+4.75 to +5.25	V
V_{DD}.PAD	I/O Buffer Driver Pad Voltage to Ground (IQ96, IQ64B, IQ48 and IQ32B only)	+4.75 to +5.25 or +2.97 to +3.62	V
T_A	Operating Temperature	0 to +70	°C

Table 9. Recommended Operating Conditions

6.3 Capacitance (3)

Symbol	Parameter	IQ96, IQ64B		IQ48, IQ32B		Units
		Min	Max	Min	Max	
C_{JTAG}	TDI, TMS, TCK and TRST* Pins	-	5	-	5	pF
C_{PORT}	I/O Port Pins	-	10	-	10	pF
C_{IN}	OE, ICLK, OCLK Pins	-	8	-	8	pF

Table 10. Capacitance

Notes:
(1) Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A maximum overshoot and undershoot of 2V for a maximum duration of 20 ns is acceptable.
(3) Capacitance measured at 25°C. Sample-tested only.

6.4 DC Electrical Specifications

(T_A = 0°C to 70°C, V_{DD} = 5V±5%; V_{DD}.PAD = 5V±5%, or V_{DD}.PAD = 3.3V±10%)

Symbol	Parameter	Conditions	IQ96, IQ64B		IQ48, IQ32B		Units
			Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	V_{DD}.PAD +0.3	2.0	V_{DD}.PAD +0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	0.8	-0.3	0.8	V
V_{OH}	High-Level Output Voltage (1)	V_{DD} = Min, V_{DD}.PAD = 4.75V I_{OH} = -8 mA	2.4	-	2.4	-	V
	High-Level Output Voltage (2)	V_{DD} = Min, V_{DD}.PAD = 2.97V I_{OH} = -4 mA	2.4	-	2.4	-	V
V_{OL}	Low-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 4.75V I_{OL} = 12 mA	-	0.4	-	0.4	V
	Low-Level Output Voltage(3)	V_{DD} = Min, V_{DD}.PAD = 2.97V I_{OL} = 12 mA	-	0.4	-	0.4	V
$\|I_{IH}\|$, $\|I_{IL}\|$	Input Leakage Current for I/O Ports (4)	V_{DD} = Max $0 \le V_{IN} \le V_{DD}$ .PAD $\le V_{DD}$	-	5	-	5	µA
$\|I_{IH}\|$, $\|I_{IL}\|$	Input Leakage Current for Inputs other than I/O Ports (5)	V_{DD} = Max $0 \le V_{IN} \le V_{DD}$	5	20	5	20	µA
$\|I_{OZ}\|$	Tristate Output Off-State Current	V_{DD} = Max $0 \le V_{IN} \le V_{DD}$	-	5	-	5	µA
I_{PU-WK}	Programmed-Weak Additional Pull-Up Current	V_{DD} = V_{DD}.PAD = 4.75V V_O = GND	2.5	4.5	2.5	4.5	mA
I_{PU-SG}	Programmed-Strong Additional Pull-Up Current	V_{DD} = V_{DD}.PAD = 4.75V V_O = GND	10	15	10	15	mA
I_{OS}	Short Circuit Current (1, 3, 6)	V_{DD} = Max, V_{DD}.PAD = 5.25V V_O = GND	-60	-	-60	-	mA
I_{DDQ_CORE}	Quiescent Core Power Supply Current	V_{DD}.PAD = 5.25V, All I/O's = NC V_{DD} = Max, V_O = GND	-	3.0	-	1.5	mA
I_{DDQ_PAD}	Quiescent Pad Power Supply Current	V_{DD}.PAD = 5.25V, All I/O's = NC V_{DD} = Max, V_O = GND	-	80	-	80	µA
Q_{DDD}	Total Dynamic Power Supply Current per Input (3)	V_{DD}.PAD = 5.25V, No Load, @ 1.0 MHz clock input, connect one output per input	-	0.1	-	0.1	mA/ MHz

Table 11. DC Electrical Specifications

Notes:

(1)Programmable Output Voltage-level set to TTL.
(2)Programmable Output Voltage-level set to CMOS and no additional pull-up current.
(3)These parameters are guaranteed but not tested in production.
(4)Transient currents of 250 µA are required to pull I/O Ports from logic high to logic low.
(5)Transient currents of 650 µA are required to pull input pins from logic high to logic low.
(6)No more than one output should be tested at a time and the duration of the test should be less than one second.
(7) Not Applicable.

6.5 AC Electrical Specifications IQ96, IQ64B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%, V_{DD}.PAD=5V±5% or V_{DD}.PAD =3.3V±10%. Assume two I/O Ports connected through the Switch Matrix with 35 pF loading.)

Speed Grade		-10			
Symbol	Parameter	Min	Max	Units	Ref. Figure
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay	-	10	ns	
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	0.25	ns	
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0	ns	11
$t_{\Delta CMOS}$	Additional Delay when Output Voltage Level is CMOS	-	0.5	ns	
t_{SK}	Skew Between Output Ports (1)	-	1.0	ns	
R_{DATA}	NRZ Data Rate (1)	-	160	Mbs	
t_{W+}	Positive Input Signal Pulse Width	7	-	ns	
t_{W-}	Negative Input Signal Pulse Width	5.5	-	ns	
t_{PZL}, t_{PZH}	Output Enable to Data Valid	-	12	ns	12
t_{PLZ}, t_{PHZ}	Output Enable to Output at High Z (1)	-	12	ns	
f_{RI}	Register Input Clock Frequency (1)	-	100	MHz	
t_{W-RI}	Register Input Clock Pulse Width, Low or High	4.5	-	ns	
t_{S-RI}	Register Input Setup Time	1	-	ns	13
t_{H-RI}	Register Input Hold Time	1	-	ns	
t_{P-RI}	Register Input Clock to Output Data Valid	-	14	ns	
f_{RO}	Register Output Clock Frequency (1)	-	100	MHz	
t_{W-RO}	Register Output Clock Pulse Width, Low or High	4.5	-	ns	
t_{S-RO}	Register Output Setup Time	5	-	ns	14
t_{H-RO}	Register Output Hold Time	0	-	ns	
t_{P-RO}	Register Output Clock to Output Data Valid	-	11.5	ns	
f_{RIO}	Register Input/Output Clock Frequency (1)	-	100	MHz	
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	4.5	-	ns	
t_{S-RIO}	Register Input/Output Setup Time	1	-	ns	
t_{H-RIO}	Register Input/Output Hold Time	1	-	ns	15
t_{P-RIO}	Register Input/Output Clock to Output Data Valid	-	11.5	ns	
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)	8	-	ns	
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)	-	3	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency	-	25	MHz	
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20	-	ns	
t_{S-JTAG}	JTAG Setup Time	15	-	ns	16
t_{H-JTAG}	JTAG Hold Time	15	-	ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15	-	ns	
T_{RC}	RapidConnect Strobe Period	30	-	ns	
t_{W-RC}	RapidConnect Strobe Pulse Width	12	-	ns	
t_{S-RC}	RapidConnect Address and Data Setup Time	8	-	ns	17
t_{H-RC}	RapidConnect Address and Data Hold Time	0	-	ns	
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection	20	-	ns	

Table 12. AC Electrical Specifications IQ96, IQ64B

6.6 AC Electrical Specifications IQ48, IQ32B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%, V_{DD}.PAD = 5V±5% or V_{DD}.PAD = 3.3V±10%. Assume two I/O Ports connected through the Switch Matrix with 35 pF loading.)

Speed Grade		-7			
Symbol	Parameter	Min	Max	Units	Ref. Figure
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay	-	7	ns	11
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	0.25	ns	
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0	ns	
$t_{\Delta CMOS}$	Additional Delay when Output Voltage Level is CMOS	-	0.5	ns	
t_{SK}	Skew Between Output Ports (1)	-	1.5	ns	
R_{DATA}	NRZ Data Rate (1)	-	250	Mbs	
t_{W+}	Positive Input Signal Pulse Width	5.5	-	ns	
t_{W-}	Negative Input Signal Pulse Width	3	-	ns	
t_{PZL}, t_{PZH}	Output Enable to Data Valid	-	7	ns	12
t_{PLZ}, t_{PHZ}	Output Enable to Output at High Z (1)	-	7	ns	
f_{RI}	Register Input Clock Frequency (1)	-	150	MHz	13
t_{W-RI}	Register Input Clock Pulse Width, Low or High	3	-	ns	
t_{S-RI}	Register Input Setup Time	1	-	ns	
t_{H-RI}	Register Input Hold Time	1	-	ns	
t_{P-RI}	Register Input Clock to Output Data Valid	-	10	ns	
f_{RO}	Register Output Clock Frequency (1)	-	150	MHz	14
t_{W-RO}	Register Output Clock Pulse Width, Low or High	3.5	-	ns	
t_{S-RO}	Register Output Setup Time	3.5	-	ns	
t_{H-RO}	Register Output Hold Time	0	-	ns	
t_{P-RO}	Register Output Clock to Output Data Valid	-	6	ns	
f_{RIO}	Register Input/Output Clock Frequency (1)	-	150	MHz	15
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	3.5	-	ns	
t_{S-RIO}	Register Input/Output Setup Time	1	-	ns	
t_{H-RIO}	Register Input/Output Hold Time	1	-	ns	
t_{P-RIO}	Register Input/Output Clock to Output Data Valid	-	6	ns	
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)	5	-	ns	
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)	-	3	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency	-	25	MHz	16
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20	-	ns	
t_{S-JTAG}	JTAG Setup Time	15	-	ns	
t_{H-JTAG}	JTAG Hold Time	15	-	ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15	-	ns	
T_{RC}	RapidConnect Strobe Period	20	-	ns	17
t_{W-RC}	RapidConnect Strobe Pulse Width	8	-	ns	
t_{S-RC}	RapidConnect Address and Data Setup Time	5	-	ns	
t_{H-RC}	RapidConnect Address and Data Hold Time	0	-	ns	
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection	16	-	ns	

Table 13. AC Electrical Specifications IQ48, IQ32B

Notes:
(1)These parameters are guaranteed but not tested in production.

6.7 Test Circuit and Timing Diagrams

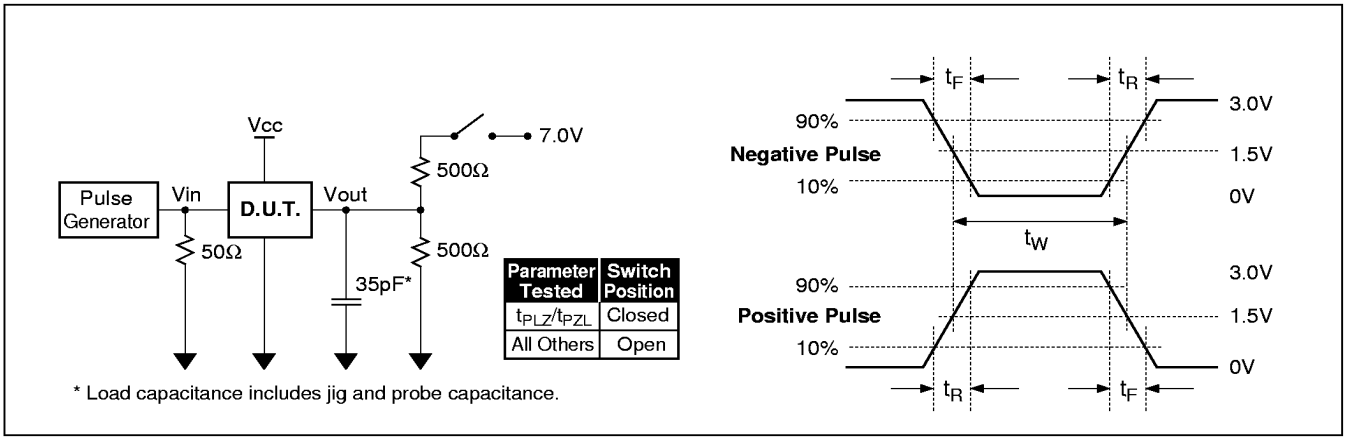


Figure 10. Test Circuit and Waveform Definition

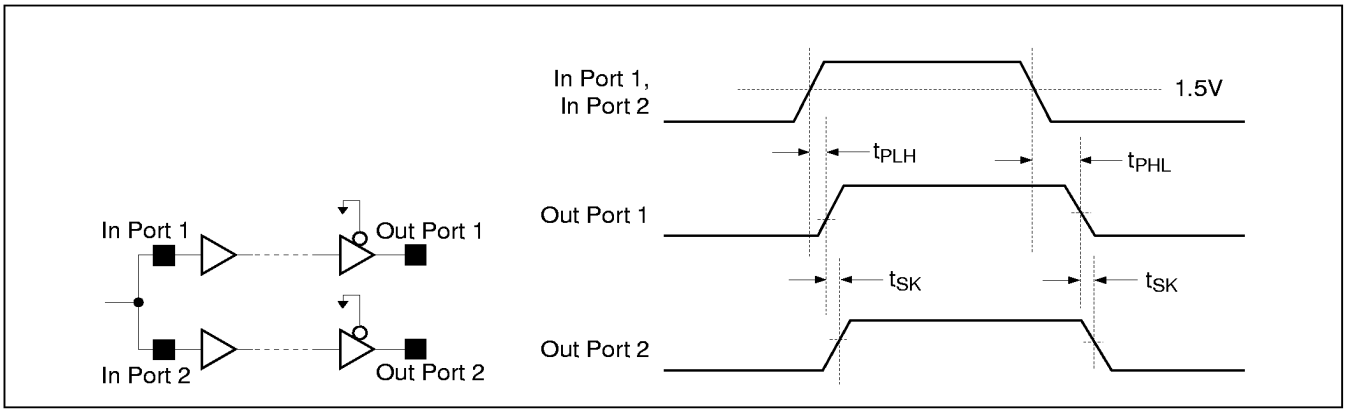


Figure 11. I/O Port Timing (Flow-through Mode)

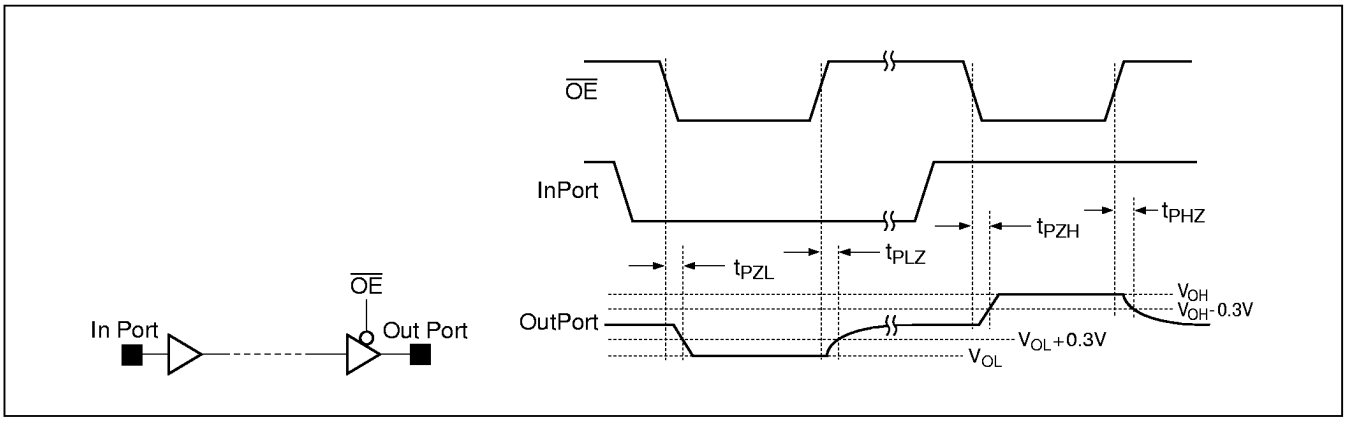


Figure 12. Output Enable Timing (Flow-through Mode)

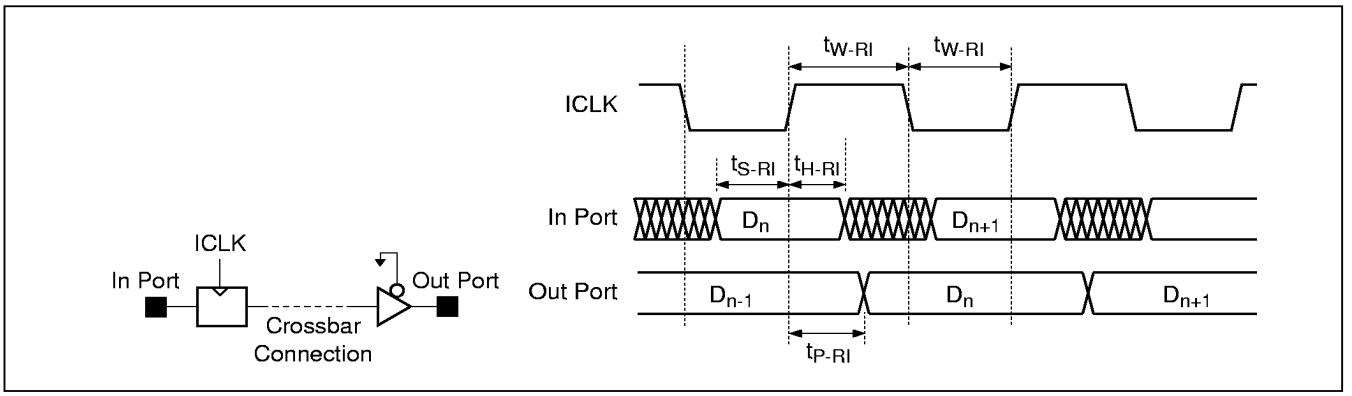


Figure 13. Clocked Input to Unclocked Output

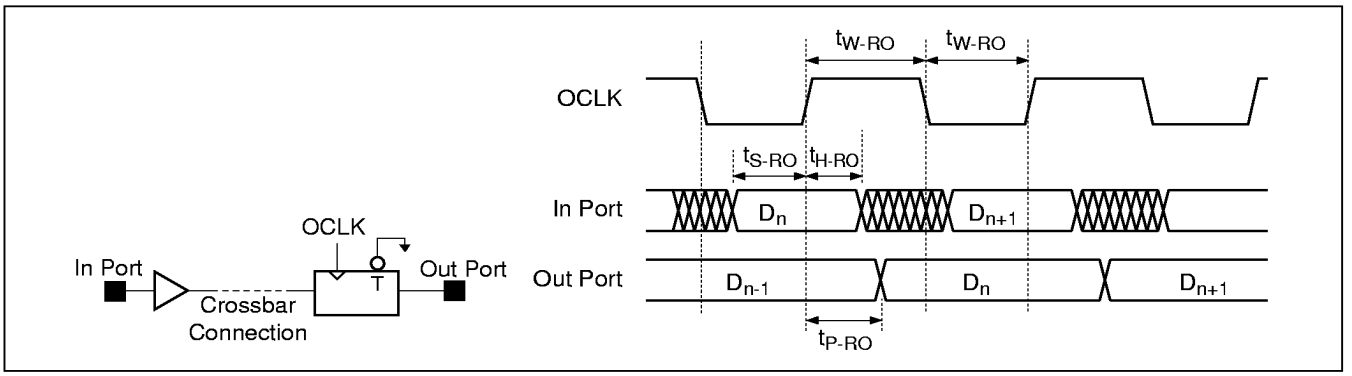


Figure 14. Unclocked Input to Clocked Output

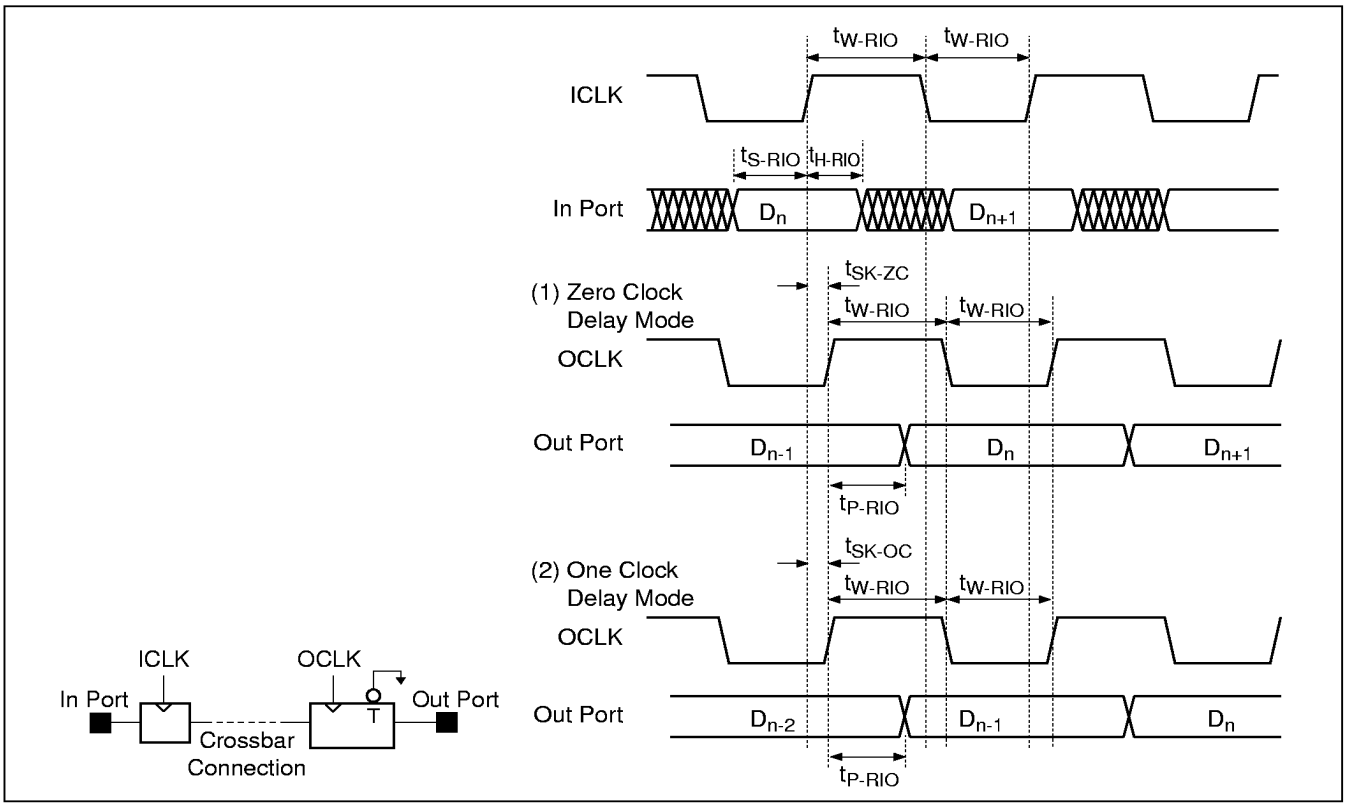


Figure 15. Clocked Input to Clocked Output (ICLK and OCLK are Synchronized)

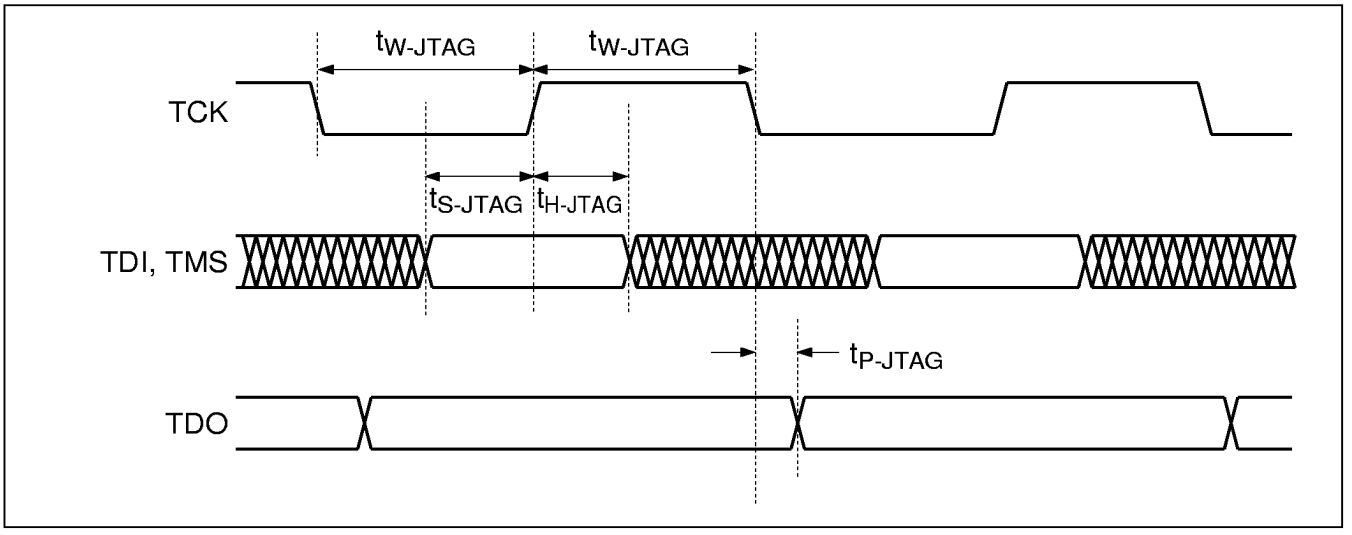


Figure 16. JTAG Timing

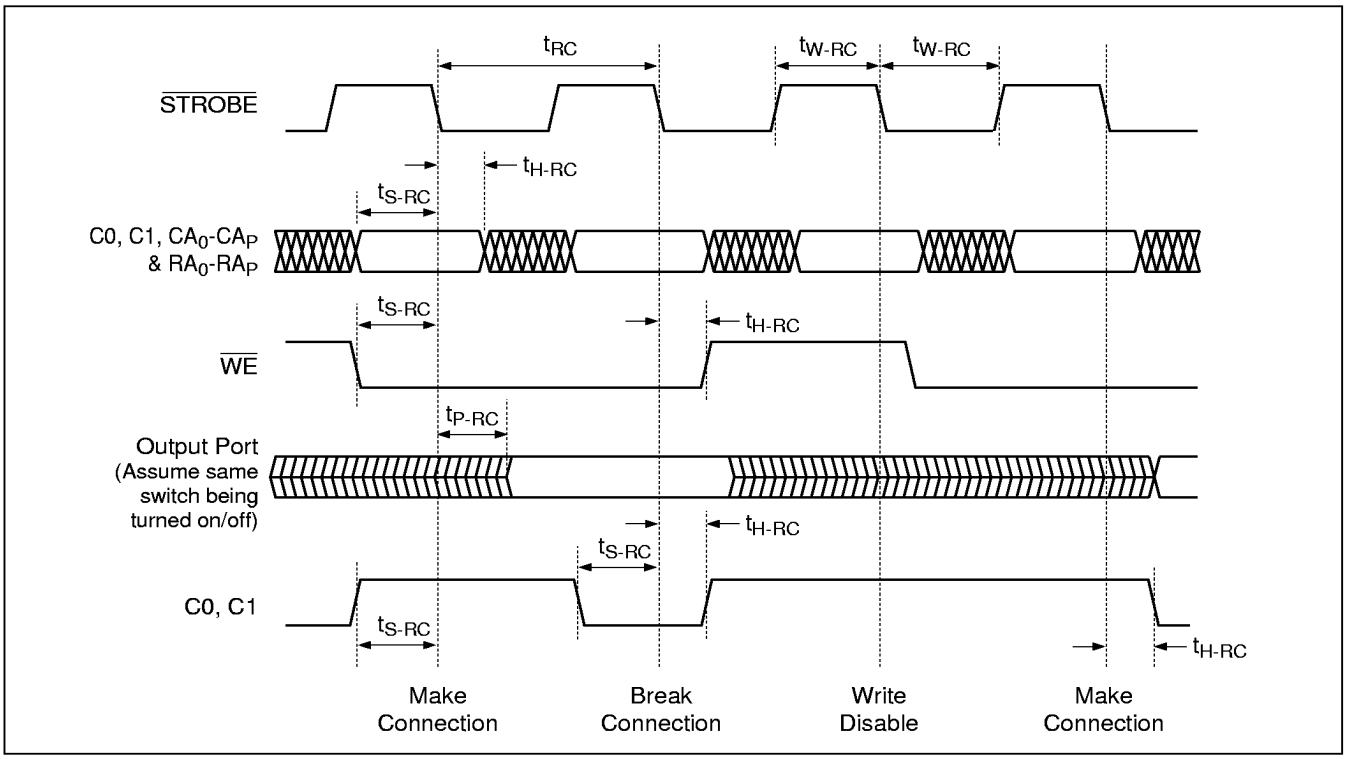
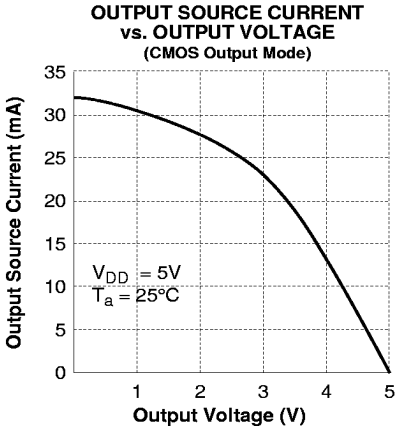
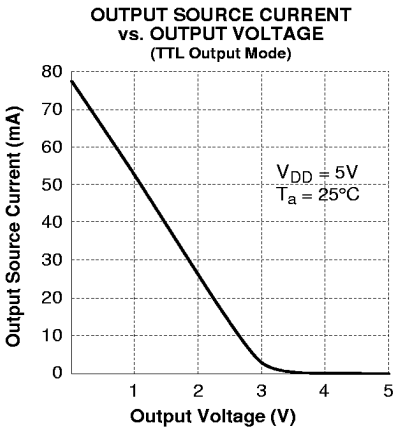
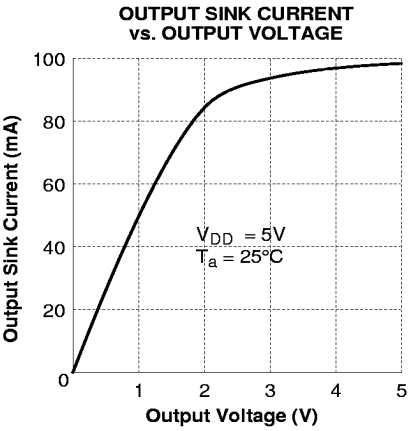


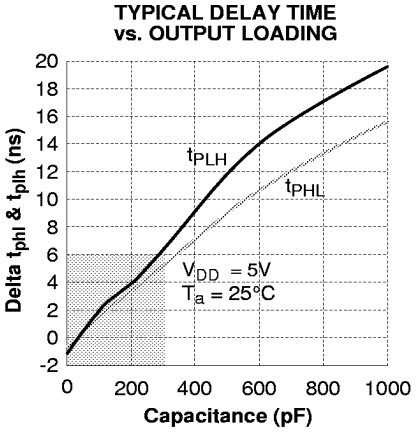
Figure 17. RapidConnect Timing

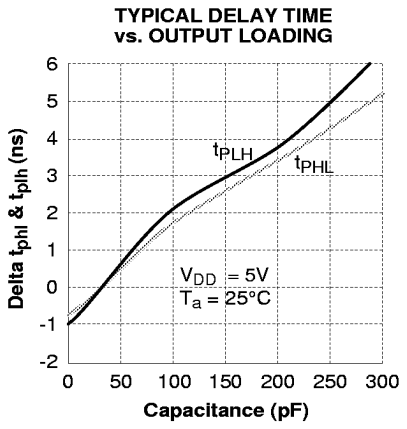
6.8 Typical AC and DC Characteristics (Measured for IQ96 and IQ64B)

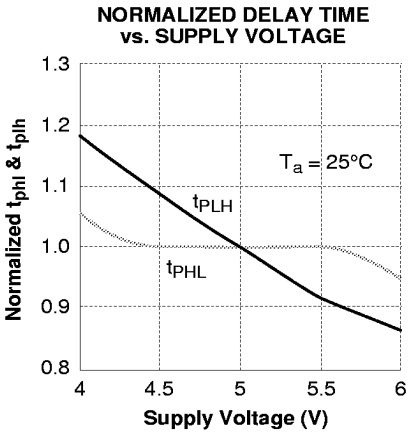


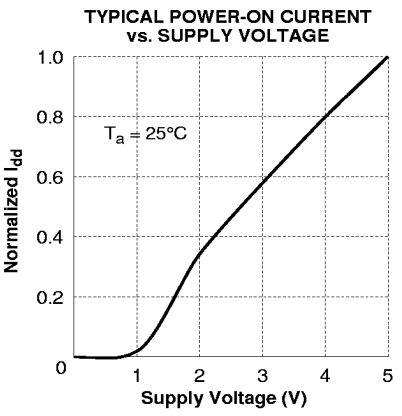


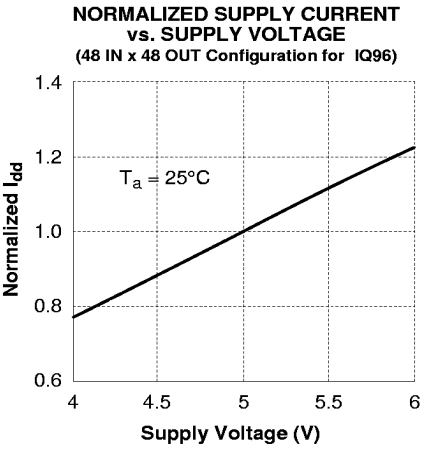


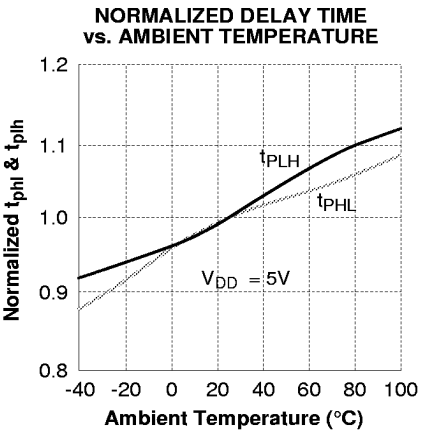




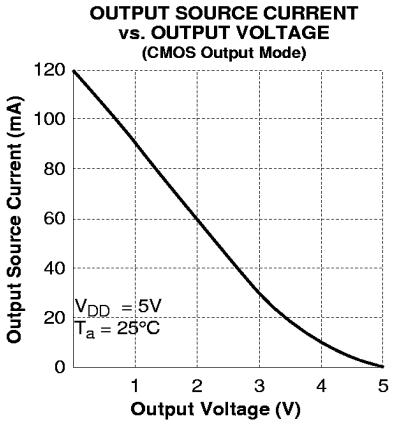


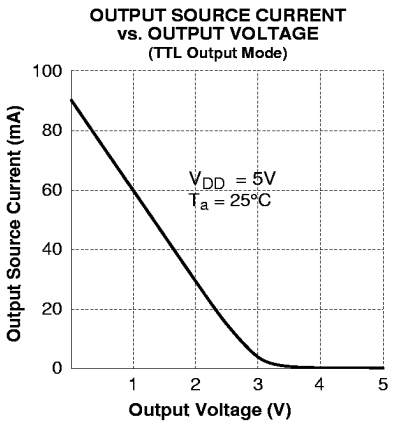


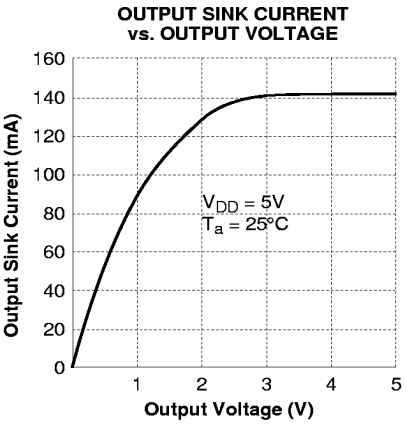


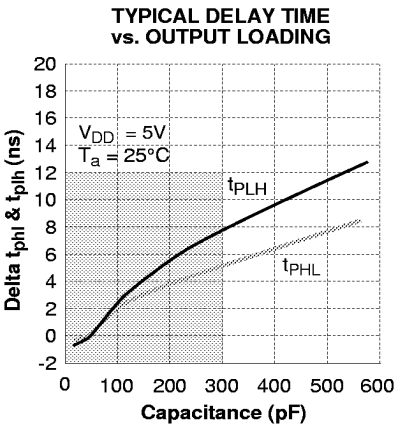


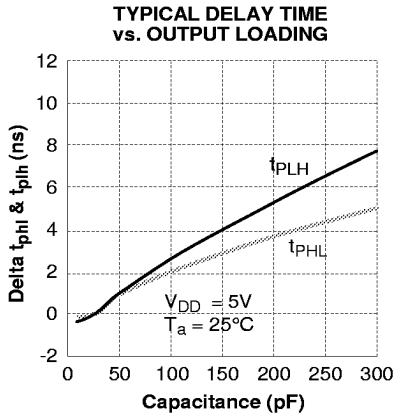
6.9 Typical AC and DC Characteristics (Measured for IQ48 and 32B)

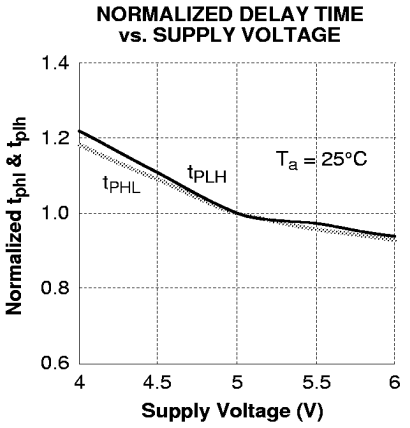


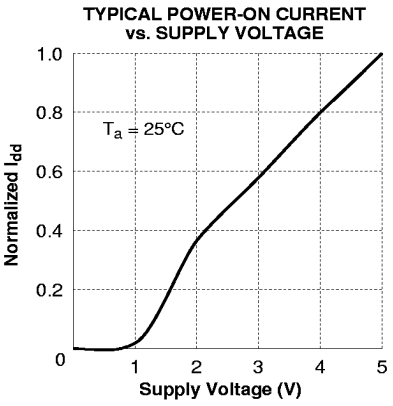


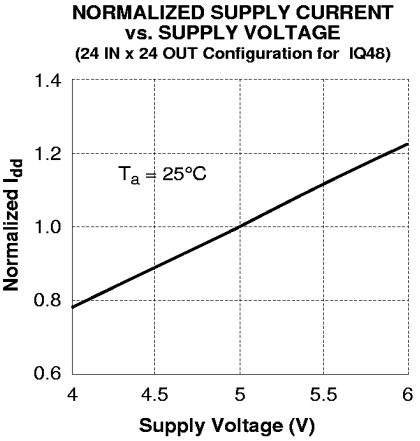


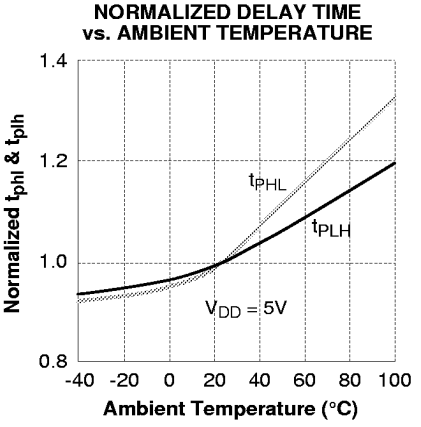


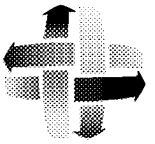












7.0 PINOUT

7.1 IQ96 [TQFP and PQFP/144L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TDI	37	$\overline{OE2}$	73	P047	109	$\overline{OE0}$
2	P095/$\overline{STROBE}$	38	P073	74	P046	110	P021
3	P094/$\overline{WE}$	39	P072	75	V_{SS}	111	P020
4	P093/C1	40	P071	76	P045	112	V_{SS}
5	P092/C0	41	P070	77	P044	113	V_{DD}.PAD
6	V_{SS}.PAD	42	V_{SS}	78	P043	114	P019
7	OCLK	43	V_{DD}.PAD	79	P042	115	P018
8	V_{DD}.PAD	44	P069	80	V_{SS}.PAD	116	P017
9	V_{SS}.PAD	45	P068	81	V_{DD}.PAD	117	P016
10	ICLK	46	P067	82	P041	118	V_{SS}.PAD
11	P091/RA6	47	P066	83	P040	119	P015
12	P090/RA5	48	V_{SS}.PAD	84	P039	120	P014
13	P089/RA4	49	P065	85	P038	121	P013
14	P088/RA3	50	P064	86	V_{SS}.PAD	122	P012
15	P087/RA2	51	P063	87	P037	123	V_{SS}.PAD
16	P086/RA1	52	P062	88	P036	124	P011
17	V_{SS}.PAD	53	V_{SS}.PAD	89	P035	125	P010
18	P085/RA0	54	P061	90	P034	126	P009
19	P084/CA6	55	P060	91	V_{DD}.PAD	127	P008
20	P083/CA5	56	V_{DD}.PAD	92	V_{SS}.PAD	128	V_{SS}.PAD
21	V_{SS}.PAD	57	P059	93	P033	129	V_{DD}.PAD
22	P082/CA4	58	P058	94	P032	130	P007
23	P081/CA3	59	V_{SS}.PAD	95	P031	131	P006
24	P080/CA2	60	P057	96	P030	132	P005
25	P079/CA1	61	P056	97	V_{SS}.PAD	133	P004
26	P078/CA0	62	P055	98	P029	134	V_{SS}.PAD
27	V_{DD}.PAD	63	P054	99	P028	135	P003
28	V_{SS}	64	V_{SS}.PAD	100	P027	136	P002
29	P077	65	P053	101	P026	137	P001
30	V_{SS}.PAD	66	P052	102	V_{DD}	138	P000
31	P076	67	P051	103	V_{SS}.PAD	139	V_{SS}.PAD
32	P075	68	P050	104	P025	140	TRST*
33	V_{DD}	69	V_{SS}.PAD	105	P024	141	V_{DD}
34	V_{SS}.PAD	70	V_{DD}	106	P023	142	TCK
35	P074	71	P049	107	P022	143	TDO
36	$\overline{OE3}$	72	P048	108	$\overline{OE1}$	144	TMS

Table 14. IQ96 [TQFP and PQFP/144L Package] Pinout

7.2 IQ96 [TQFP and PQFP/144L Package] Pinout

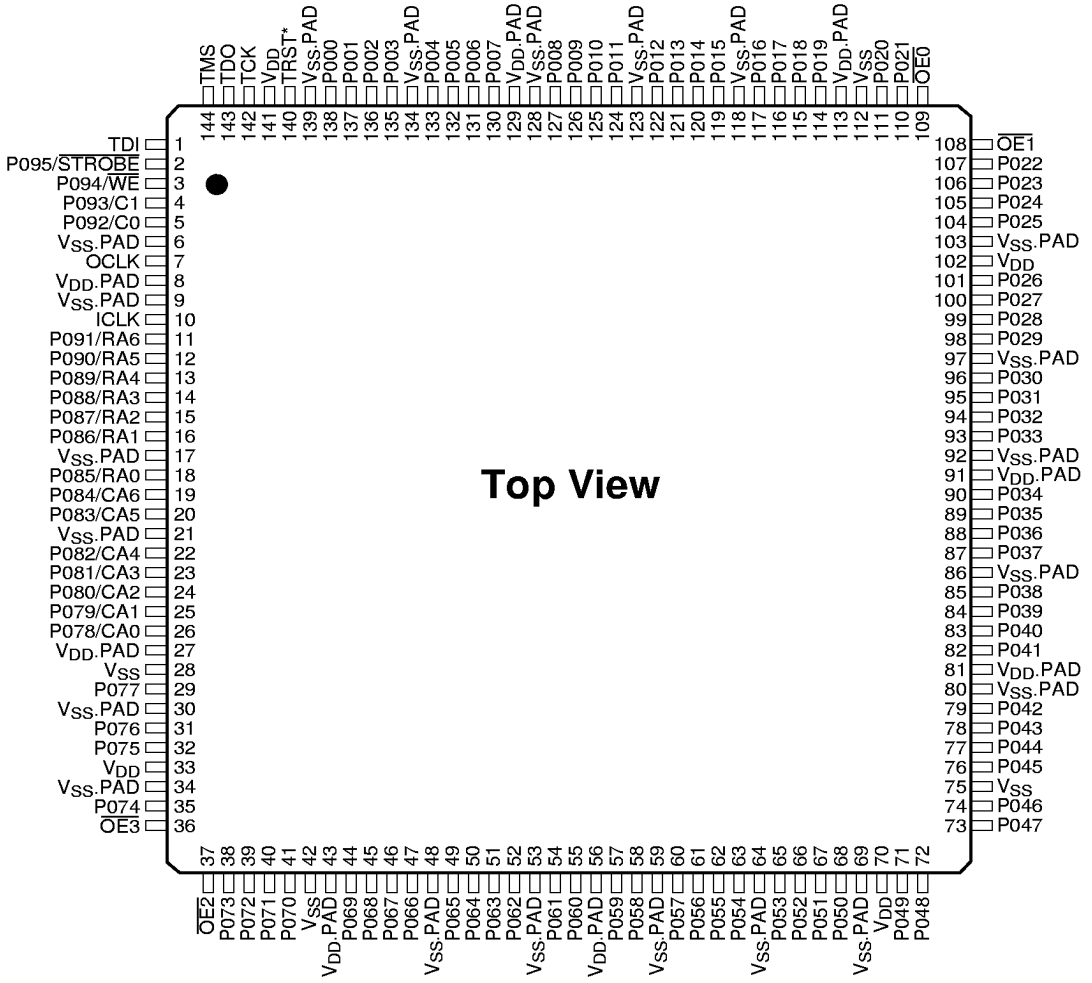


Figure 18. IQ96 [TQFP and PQFP/144L Package] Pinout

7.3 IQ64B [TQFP/100L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TDI	26	$\overline{OE3}$	51	P030	76	P013
2	P063/$\overline{STROBE}$	27	$\overline{OE2}$	52	V_{SS}	77	P012
3	P062/$\overline{WE}$	28	V_{SS}	53	P029	78	V_{SS}
4	P061/C1	29	V_{DD}.PAD	54	P028	79	P011
5	P060/C0	30	V_{SS}.PAD	55	P027	80	P010
6	OCLK	31	P047	56	P026	81	P009
7	V_{DD}.PAD	32	P046	57	V_{SS}.PAD	82	P008
8	V_{SS}.PAD	33	V_{SS}.PAD	58	P025	83	V_{SS}.PAD
9	ICLK	34	P045	59	P024	84	P007
10	P059/RA5	35	P044	60	P023	85	P006
11	P058/RA4	36	P043	61	P022	86	P005
12	P057/RA3	37	P042	62	V_{SS}.PAD	87	P004
13	P056/RA2	38	V_{SS}.PAD	63	P021	88	V_{SS}.PAD
14	P055/RA1	39	P041	64	P020	89	V_{DD}.PAD
15	V_{SS}.PAD	40	P040	65	P019	90	P003
16	P054/RA0	41	P039	66	P018	91	P002
17	P053/CA5	42	P038	67	V_{DD}.PAD	92	V_{SS}.PAD
18	V_{SS}.PAD	43	V_{SS}.PAD	68	V_{SS}.PAD	93	P001
19	P052/CA4	44	P037	69	P017	94	P000
20	P051/CA3	45	P036	70	P016	95	V_{SS}.PAD
21	P050/CA2	46	P035	71	V_{SS}.PAD	96	TRST*
22	P049/CA1	47	P034	72	P015	97	V_{DD}
23	P048/CA0	48	P033	73	P014	98	TCK
24	V_{SS}	49	P032	74	$\overline{OE1}$	99	TDO
25	V_{DD}	50	P031	75	$\overline{OE0}$	100	TMS

Table 15. IQ64B [TQFP/100L Package] Pinout

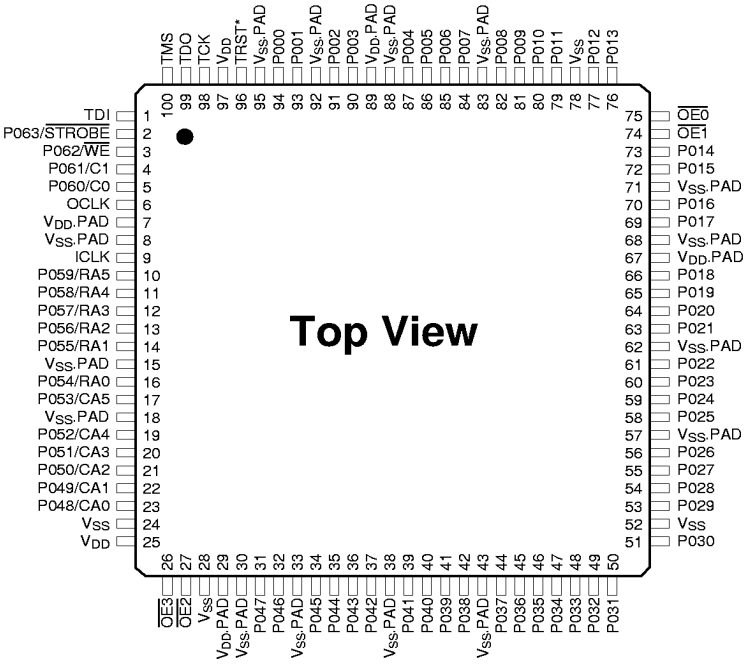


Figure 19. IQ64B [TQFP/100L Package] Pinout

7.4 IQ64B [PLCC/84L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P005	22	P056/RA2	43	V_{SS}	64	P021
2	P004	23	P055/RA1	44	P041	65	P020
3	V_{SS}	24	V_{SS}	45	P040	66	P019
4	P003	25	P054/RA0	46	P039	67	P018
5	P002	26	P053/CA5	47	P038	68	V_{SS}
6	P001	27	P052/CA4	48	P037	69	P017
7	P000	28	P051/CA3	49	P036	70	P016
8	TRST*	29	P050/CA2	50	P035	71	V_{SS}
9	TCK	30	P049/CA1	51	P034	72	P015
10	TDO	31	P048/CA0	52	P033	73	P014
11	TMS	32	V_{DD}	53	P032	74	$\overline{OE1}$
12	TDI	33	$\overline{OE3}$	54	P031	75	$\overline{OE0}$
13	P063/$\overline{STROBE}$	34	$\overline{OE2}$	55	P030	76	P013
14	P062/$\overline{WE}$	35	V_{SS}	56	P029	77	P012
15	P061/C1	36	V_{DD}	57	P028	78	V_{DD}
16	P060/C0	37	P047	58	P027	79	P011
17	OCLK	38	P046	59	P026	80	P010
18	ICLK	39	P045	60	P025	81	P009
19	P059/RA5	40	P044	61	P024	82	P008
20	P058/RA4	41	P043	62	P023	83	P007
21	P057/RA3	42	P042	63	P022	84	P006

Table 16. IQ64B [PLCC/84L Package] Pinout

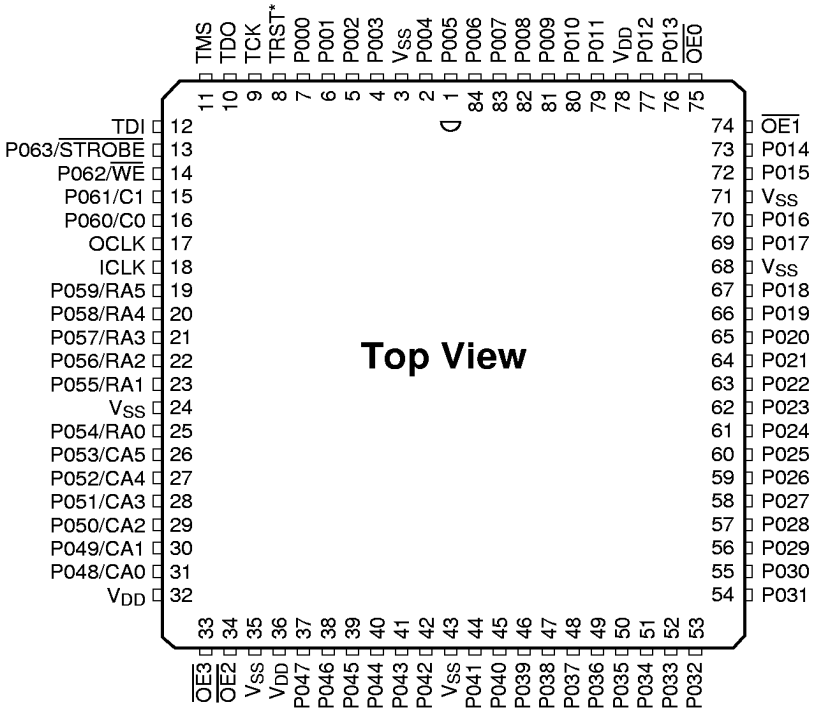


Figure 20. IQ64B [PLCC/84L Package] Pinout

7.5 IQ48 [PQFP/80L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	NC	21	NC	41	NC	61	NC
2	V_{SS}	22	TDO	42	V_{SS}	62	$\overline{OE0}$
3	P047/$\overline{STROBE}$	23	P035/CA2	43	P023	63	P011
4	P046/$\overline{WE}$	24	P034/CA1	44	P022	64	P010
5	P045/C0	25	P033/CA0	45	P021	65	P009
6	V_{SS}.PAD	26	V_{SS}.PAD	46	V_{SS}.PAD	66	V_{SS}.PAD
7	P044/RA5	27	P032	47	P020	67	P008
8	P043/RA4	28	P031	48	P019	68	P007
9	P042/RA3	29	P030	49	P018	69	P006
10	V_{DD}	30	V_{DD}.PAD	50	V_{DD}	70	V_{DD}.PAD
11	V_{DD}.PAD	31	P029	51	V_{DD}.PAD	71	P005
12	P041/RA2	32	P028	52	P017	72	P004
13	P040/RA1	33	P027	53	P016	73	P003
14	P039/RA0	34	V_{SS}.PAD	54	P015	74	V_{SS}.PAD
15	V_{SS}.PAD	35	P026	55	V_{SS}.PAD	75	P002
16	P038/CA5	36	P025	56	P014	76	P001
17	P037/CA4	37	P024	57	P013	77	P000
18	P036/CA3	38	ICLK	58	P012	78	TRST*
19	TDI	39	OCLK	59	TMS	79	TCK
20	NC	40	NC	60	NC	80	NC

Table 17. IQ48 [PQFP/80L Package] Pinout

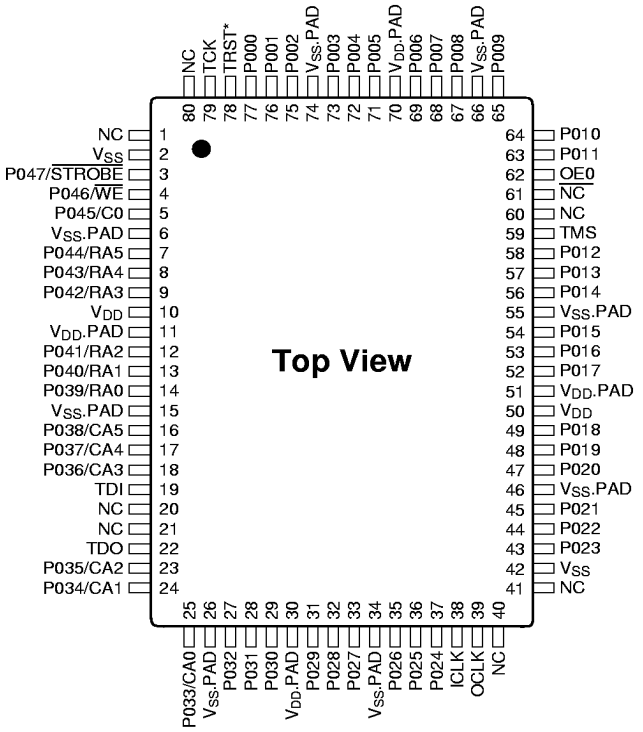


Figure 21. IQ48 [PQFP/80L Package] Pinout

7.6 IQ32B [TQFP/52L Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P031/$\overline{\text{STROBE}}$	14	TDI	27	VSS	40	$\overline{\text{OE0}}$
2	P030/$\overline{\text{WE}}$	15	TDO	28	P014	41	P006
3	P029/C0	16	P021/CA2	29	P013	42	P005
4	VSS.PAD	17	P020/CA1	30	P012	43	P004
5	P028/RA4	18	P019/CA0	31	VSS.PAD	44	VSS.PAD
6	P027/RA3	19	VSS.PAD	32	P011	45	P003
7	VDD	20	P018	33	VDD	46	P002
8	VDD.PAD	21	P017	34	VDD.PAD	47	VSS.PAD
9	P026/RA2	22	VSS.PAD	35	P010	48	P001
10	P025/RA1	23	P016	36	P009	49	P000
11	P024/RA0	24	P015	37	P008	50	TRST*
12	P023/CA4	25	ICLK	38	P007	51	TCK
13	P022/CA3	26	OCLK	39	TMS	52	VSS

Table 18. IQ32B [TQFP/52L Package] Pinout

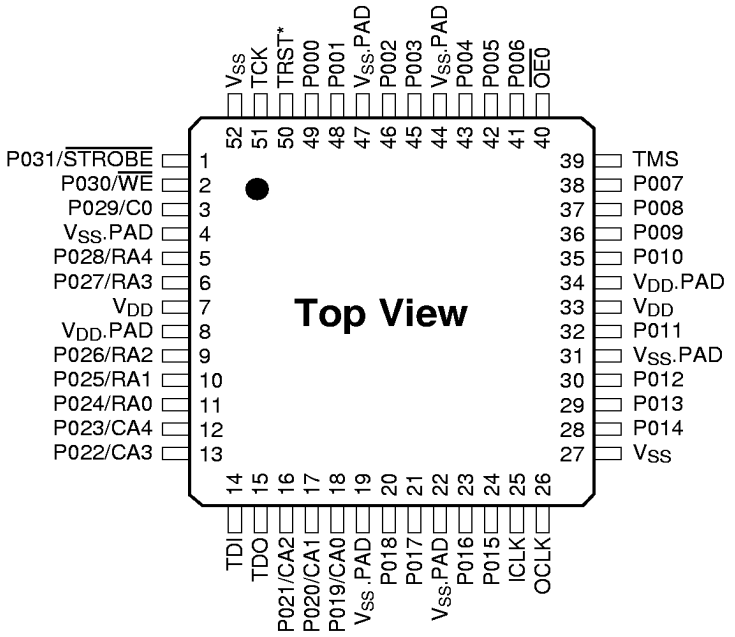


Figure 22. IQ32B [TQFP/52L Package] Pinout

8.0 MECHANICAL SPECIFICATION

8.1 PQFP Package Dimensions (1,2)

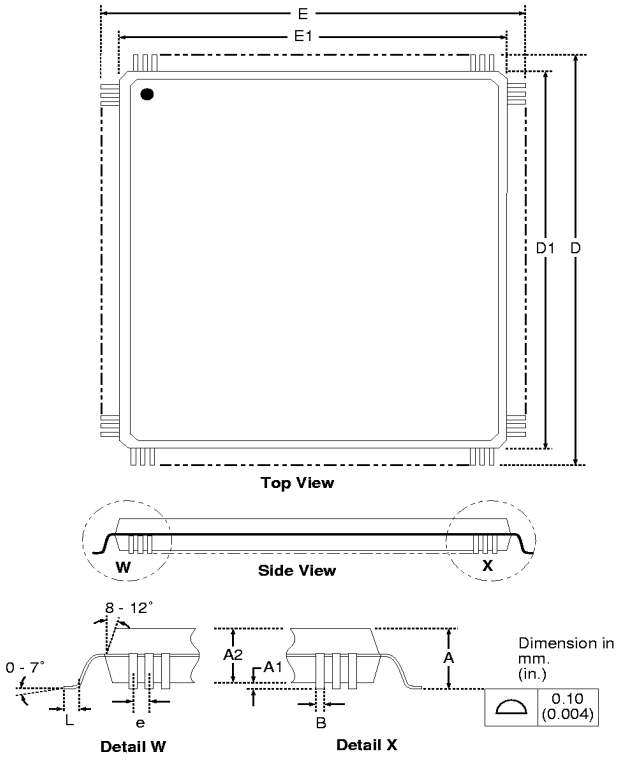


Figure 23. PQFP Package Dimensions

Package Dimension Table		PQFP/144L		PQFP/80L	
		inch	mm	inch	mm
A	max	.157	3.99	.127	3.23
A1	min	.010	0.25	.012	0.30
	max	.017	0.43	.017	0.43
A2	min	.135	3.43	.102	2.60
	max	.140	3.56	.110	2.80
D	min	1.219	31.01	.904	22.95
	max	1.238	31.49	.923	23.45
D1	min	1.098	27.93	.783	19.90
	max	1.106	28.14	.791	20.10
E	min	1.219	31.01	.667	16.95
	max	1.238	31.49	.687	17.45
E1	min	1.098	27.93	.547	13.90
	max	1.106	28.14	.555	14.10
L	min	.029	0.74	.029	0.73
	max	.041	1.04	.041	1.03
B	min	.009	0.23	.012	0.30
	max	.014	0.36	.018	0.45
e	BSC.	.0256	0.65	.0315	0.80

Table 19. PQFP Package Dimensions

8.2 TQFP Package Dimension (1,2)

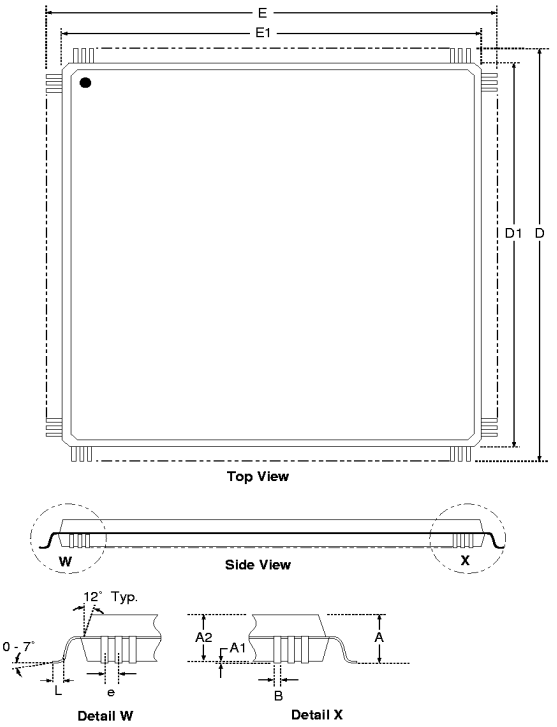


Figure 24. TQFP Package Dimension

Package Dimension Table		TQFP/144L		TQFP/100L		TQFP/52L	
		inch	mm	inch	mm	inch	mm
A	max	.063	1.60	.063	1.60	.063	1.60
A1	min	.002	0.05	.002	0.05	.002	0.05
	max	.006	0.15	.006	0.15	.006	0.15
A2	min	.053	1.35	.053	1.35	.053	1.35
	max	.057	1.45	.057	1.45	.057	1.45
D	min	.858	21.80	.622	15.80	.465	11.80
	max	.874	22.20	.638	16.20	.480	12.20
D1	min	.783	19.90	.547	13.90	.390	9.90
	max	.791	20.10	.555	14.10	.398	10.10
E	min	.858	21.80	.622	15.80	.465	11.80
	max	.874	22.20	.638	16.20	.480	12.20
E1	min	.783	19.90	.547	13.90	.390	9.90
	max	.791	20.10	.555	14.10	.398	10.10
L	min	.018	0.45	.012	0.30	.018	0.45
	max	.030	0.75	.028	0.70	.030	0.75
B	min	.007	0.17	0.007	0.17	.009	0.22
	max	.011	0.2 7	0.111	0.27	.015	0.38
e	BSC.	.0197	0.50	.0197	0.50	.0256	0.65

Table 20. TQFP Package Dimension

Notes:

(1) Use "mm" as the controlling dimension

(2) PQFP - Plastic Quad Flat Package

8.3 PLCC Package Dimensions (1, 2)

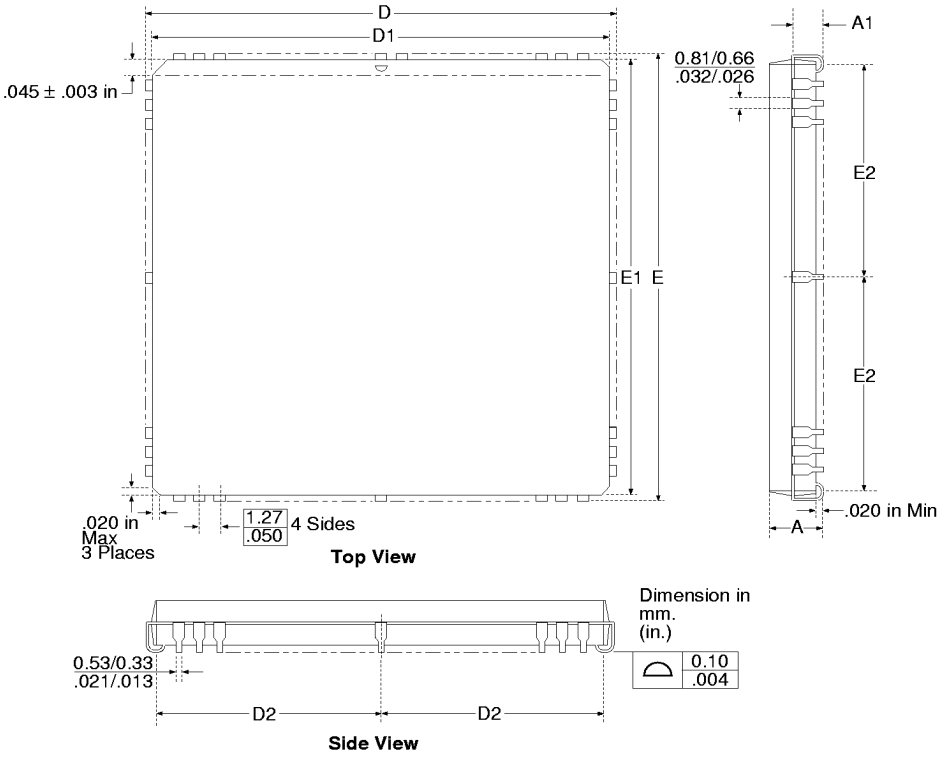


Figure 25. PLCC Package Dimensions

Package Dimension Table		PLCC/84L	
		inch	mm
A	max	.200	5.08
A1	min	.090	2.28
	max	.130	3.30
D	min	1.185	30.09
	max	1.195	30.35
D1	min	1.150	29.21
	max	1.158	29.41
D2	min	.545	13.84
	max	.565	14.35
E	min	1.185	30.09
	max	1.195	30.35
E1	min	1.150	29.21
	max	1.158	29.41
E2	min	.545	13.84
	max	.565	14.35

Table 21. PLCC Package Dimensions

Notes:
(1) Use inch as the controlling dimension
(2) PLCC- Plastic Leaded Chip Carrier

9.0 Component Availability and Ordering Information

The following table lists the IQ devices and the different package options, and speed grades that are currently available.

Package	Pins	52	80	84	100	144	
	Type	TQFP	PQFP	PLCC	TQFP	PQFP	TQFP
	Code	TQ52	PQ80	J84	TQ100	PQ144	TQ144
IQ96	-10					X	X
IQ64B	-10			X	X		
IQ48	-7		X				
IQ32B	-7	X					

Table 22. Component Availability

Device	Speed	Package*	Ordering#
IQ96	-10	PQ 144C	IQ96-PQ144
	-10	TQ 144C	IQ96-TQ144
IQ64B	-10	TQ 100C	IQ64B-TQ100
	-10	J 84C	IQ64B-J84
IQ48	-7	PQ 80C	IQ48-PQ80
IQ32B	-7	TQ 52C	IQ32B-TQ52

Table 23. Ordering Information

* J=PLCC, PQ=Plastic Quad Flat Pack, TQ=Thin Plastic Quad Pack

10.0 IQ Family at a Glance

Device	IQ96	IQ64B	IQ48	IQ32B
Number of Usable I/O	96	64	48	32
Switch Matrix Size	96	64	48	32
Pin-to-Pin Delay (ns)	10	10	7	7
NRZ Data Rate (Mbs)	200	200	250	250
Clock Frequency (MHz)	125	125	150	150
I/O Current Drive (mA)	12	12	12	12
Process (um)	0.6	0.6	0.6	0.6
Core Voltage (V)	5	5	5	5
I/O Voltage (V)	3.3 and/or 5 (1)	3.3 and/or 5 (1)	3.3 and/or 5 (1)	3.3 and/or 5 (1)
Package(s) J=PLCC, PQ=PQFP, TQ=TQFP	144PQ 144TQ	100TQ 84J	80PQ	52TQ

Table 24. IQ Family Summary

(1) Device has separate supply voltage for core and I/O buffers