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SD(HC)-memory card and MMC interface conditioning

Rev. 01 — 29 April 2010　　　　　　　　　**Application note**

Revision history

Rev	Date	Description
01	20100429	Initial version

Contact information

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1. Introduction

The SD-memory card and MMC are the most popular memory cards in today's communication, computer and consumer appliances. They are designed to support state-of-the-art security and capacity requirements demanded by today's audio and video applications in consumer and communication products.

SD-memory cards support content protection, prevention of illegal use of content and security systems based on e.g. ISO-7816. The MMC is available as an embedded version eMMC according the JESD84-A43. It offers up to an 8-bit wide interface and can basically be operated in SD-memory card compatible hardware interfaces.

While the SD-memory card adds an advanced memory/data storage function to an application, there is a more general Secure Digital Input Output (SDIO) card.

The SDIO card specification is a separately specified interface to different I/O units providing various functions to an SD host, including memory storage that is supposed to be compatible with the SD-memory card specification. Even if an SD host is not SDIO compatible, i.e. just supporting SD-memory cards – no physical damage or disruption of operation shall occur.

A typical SD-memory card communication is based on an advanced 8/9-pin interface (clock, command, 1- or 4-bit data and 2/3 x power/GND) designed to operate at a maximum operating frequency of 50 MHz.

The MMC works with an up to 52 MHz clock but supports in its latest versions up to 8 data bits in a 13-pin interface (clock, command, 1-, 4- or 8-bit data, 3x power/GND).

While the SD-memory card is supposed to contain some ESD protection (please refer to chapter 8.1.3. of Ref. 1 "SD specifications, part 1, Physical Layer Specification version 2.00, May 9, 2006"), SD host interfaces require an additional high-level ESD protection according the IEC61000-4-2 standard in addition to the host-interface integrated ESD protection which is typically very weak.

Further more, strict EMI regulations and system requirements as specified in GSM mobile phones strongly request filters that reduce the radiated/conducted EMI but still comply with the electrical requirements of the interface specification.

In addition, the continuing trend of miniaturization of portable appliances implies that interface devices offering ESD protection and EMI filtering should also, where possible, integrate biasing circuits/resistors into a single small-sized package.

The NXP Semiconductors SD-memory card interface conditioning devices explained in this document fully support this continuing trend and offer interface conditioning functions such as:

- High-level ESD protection according the IEC61000-4-2 standard, often exceeding the highest specified level 4
- EMI filtering, suppressing unwanted Radio Frequencies (RF), in combination with SD interface compliant physical signaling
- Integrated biasing resistor networks to reduce the component count and to free up additional space on the Printed-Circuit Board (PCB) surface
- A regulated power supply to supply SD-memory cards directly from e.g. a battery

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- Voltage level translation to enable the use of low-voltage host processors to communicate with 2.7 V to 3.6 V compliant SD-memory card devices

2. SD-memory card electrical interface

Today, most appliances use the (2.7 V to 3.6 V) operating mode. This enables the use of a fixed voltage interface and power supply to reduce cost and complexity of the control circuitry.

All further descriptions are related to this "high-voltage range" 2.7 V to 3.6 V supply voltage operated interfaces.

A list of SD-memory card threshold levels for the high-voltage range is listed in Table 1.

2.1 Bus operation conditions

The minimum output level of the driving device and the receiving device input level are specified in Table 1 (taken from Ref. 1).

To decouple the SD-memory card interface specification from the signal-conditioning device (EMI filter, ESD protection, etc.), an intermediate signal threshold is specified in Table 2. This "EMI filter, card interface side" leveling is taken as a minimum requirement for an SD-memory card compliant interface conditioning device.

As ESD protection and EMI filter devices should be placed as close as possible to the contacts of the protected interface and integrate a major portion of the total bus capacitance C_{BUS}, they are expected to be responsible, as any other filter device would be, for the majority of the voltage drop.

Subsequently, the high-level and the low-level output voltages of the filter or conditioning device can be reduced (refer to V_{OH}, V_{OL} in Table 2) compared to the output threshold levels specified in Ref. 1 and still exceed the input voltage level requirements (refer to Table 1 for values specified in Ref. 1) (see also Table note 1 and 2 on page 5).

A detailed graphical overview of the different threshold levels at different positions of the signal path is depicted in Figure 1, starting with the driver output on the left side and ending with the receiving side on the right side of the drawing.

The three different threshold levels are shown in relation to each other in Figure 2, comparing the SD-memory card output, the NXP signal-conditioning device output and the SD-memory card input threshold levels.

Table 1.   SD-memory card threshold level for high-voltage range
Values taken from Ref. 1

Symbol	Parameter	Condition	Min	Max	Unit
V_{SD}	SD-memory card supply voltage		2.7	3.6	V
V_{OH}	high-level output voltage	$I_{OH} = -100\ \mu A$; $V_{SD} = 2.7\ V$	$0.75 * V_{SD}$	-	V
V_{OL}	low-level output voltage	$I_{OL} = 100\ \mu A$; $V_{SD} = 2.7\ V$	-	$0.125 * V_{SD}$	V

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Table 1.   SD-memory card threshold level for high-voltage range …*continued*
Values taken from Ref. 1

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	high-level input voltage		$0.625*V_{SD}$	-	V
V_{IL}	low-level input voltage		-	$0.25*V_{SD}$	V
t_{Pup}	power up time	$0\ V \leq V_{SD} \leq 2.7\ V$	-	250	ms

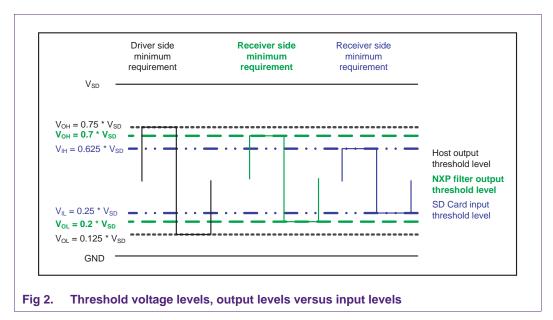**Table 2.   SD-memory card operating conditions**

Symbol	Parameter		Min	Max	Unit
V_{SD}	SD-memory card supply voltage		2.7	3.6	V
I_{DD}	supply current in high-speed mode		-	200	mA
V_{OH}	high-level output voltage	[1][3]	$0.7*V_{SD}$	-	V
V_{OL}	low-level output voltage	[2][3]	-	$0.2*V_{SD}$	V
C_L	load capacitance		-	40	pF
C_{CARD}	SD- memory card signal line capacitance		-	10	pF
$C_{HOST + BUS}$	capacitance of host interface and signal bus		-	30	pF
$R_{CMD};\ R_{DAT}$	external pull-up resistor value (except dat3/CD) to prevent bus floating		10	100	kΩ
R_{DAT3}	SD-memory card internal pull-up resistor value Dat3/CD pin only		10	90	kΩ
L_{ch}	single line inductance		-	16	nH

[1]   SD-memory card specification is: V_{OH} minimum is $0.75*V_{SD}$ and V_{IH} minimum is $0.625*V_{SD}$ in Ref. 1;
       NXP V_{OH} minimum is $0.7*V_{SD}$.

[2]   SD-memory card specification is: V_{OL} maximum is $0.125*V_{SD}$ and V_{IL} maximum is $0.25*V_{SD}$ in Ref. 1;
       NXP V_{OL} minimum is $0.2*V_{SD}$.

[3]   The 20 % to 70 % limits are chosen to cover also the MMC specification more easily.

Fig 1.   Threshold voltage levels along the signals path

Fig 2. **Threshold voltage levels, output levels versus input levels**

All further considerations are based on a chosen 20 % and 70 % threshold respectively (related to the SD-memory card supply voltage V_{SD}) as specified in Table 2, unless otherwise indicated. These relative voltage levels also simplify an alignment with the MMC specification.

2.2 SD-memory card bus timing conditions

The SD-memory card interface has different timing requirements for its default mode and the high-speed mode up to 50 MHz clock frequency.

Special attention should be paid to the clock signal rise time and fall time requirements (3 ns maximum).

As all NXP devices support the high-speed mode that supersedes the default mode requirements, only these requirements are taken into account here.

However, the devices explained in this document support both, the default mode and the high-speed mode.

Table 3. **SD-memory card timing conditions (high-speed mode)[1]**

Symbol	Parameter	Condition		Min	Max	Unit
f_{PP}	operating clock frequency			0	50	MHz
t_r	rise time	20 % to 70 % of V_{DD}	[2] -		3	ns
t_f	fall time	70 % to 20 % of V_{DD}	[2] -		3	ns

[1] Other timing parameters such as hold time, set-up time, high-level and low-level are dependent on the host / SD-memory card interface and not significantly influenced by the NXP interface conditioning devices.

[2] Values refer to V_{OH}, V_{OL} specified for the EMI filter output.

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2.3 Capacitive load at the interface conditioning device output

In the NXP data sheets of devices such as IP4853CX24/LF, IP4352CX24/LF etc. rise time and fall time requirements are specified similarly to the data shown in Table 4 (taken from the IP4853CX24/LF data sheet).

Table 4.   Extract from the IP4853CX24/LF data sheet
$T_{amb} = 25$ °C, $V_{CC} = 1.8$ V, $V_{BAT} = 3.5$ V, $V_{SD} = 2.9$ V. High-ref = 70 %*V_{SD}, low-ref = 20 %*V_{SD}

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_r, t_f	rise time, fall time	Z_{load} = 20 pF || 100 kΩ	-	1.5	2.5	ns
t_r, t_f	rise time, fall time	Z_{load} = 40 pF || 100 kΩ	-	2.7	3.6	ns

The following abbreviations are used:

- Z_{load}: Capacitive load representing $C_{PCB2} + C_{HOLD} + C_{CARD}$ in the NXP data sheets
- C_{PCBx}: PCB trace capacitance
- C_{HOLD}: Card holder capacitance
- C_{BUS}: Total (single) bus channel capacitance excluding the SD-memory card
- C_L: Total (single) bus channel capacitance including the SD-memory card

(For further details, please refer to Figure 3.)

In this specification, Z_{load} represents C_{CARD} and a part of C_{BUS}.

Figure 3 depicts the various basic capacitances of the signal path summing up to:

$$C_{BUS} = C_{PCB1} + C_{CH/2} + C_{CH/2} + C_{PCB2} + C_{HOLD} \leq 30 \text{ pF}$$

Please note that a significant portion (NXP assumption 20 % to 30 %) of the SD-memory cards available on the market today, have a card capacitance (C_{CARD}) of more than 10 pF.

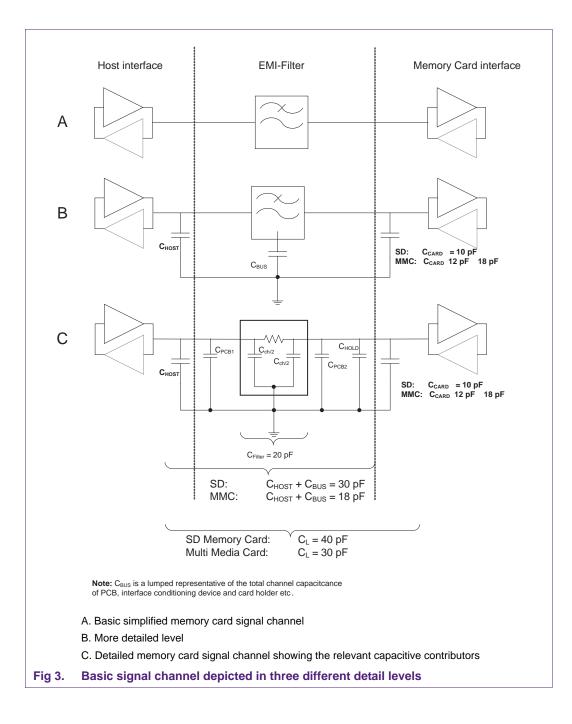According the SD-memory card specification, the total channel capacitance C_L is defined as:

$$C_L = C_{BUS} + C_{CARD} \leq 40 \text{ pF}$$

Assuming that state-of-the-art host interfaces show a capacitance of $C_{HOST} \leq 4$ pF and the NXP interface-conditioning devices add a capacitance in the range of $C_{CH} = 2 \times C_{CH/2} \leq 20$ pF, a capacitance of $C_{PCB1} + C_{PCB2} + C_{HOLD} \leq 6$ pF is left for the routing on the PCB and the card holder, which can already amount to 3 pF to 5 pF.

Due to Z_{load} representing a lumped capacitance of 20 pF in addition to the filter channel capacitance, it is obvious that the rise time and fall time requirement of 3 ns can be easily fulfilled.

Note: C_{BUS} is a lumped representative of the total channel capacitcance of PCB, interface conditioning device and card holder etc.

A. Basic simplified memory card signal channel

B. More detailed level

C. Detailed memory card signal channel showing the relevant capacitive contributors

Fig 3. **Basic signal channel depicted in three different detail levels**

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2.4 SD-memory card detect mechanism

To detect an SD-memory card, two different mechanisms can be used.

The preferred detection mechanism uses a mechanical switch in the card holder. The other mechanism is based on the pull-up resistor integrated into the SD-memory card. This resistor is connected to the DAT3/CD pin (CD = Card Detect). A detailed schematic showing both detection mechanisms is depicted in Figure 5.

If MMC and SD-memory card shall be used in the same holder, only the mechanical switch-based card detection can be used.

In contrast to the SD-memory card specification, the MMC specification does not specify any internal pull-up resistors for an electrical card detection mechanism.

Additionally, the SD-memory card specification gives clear priority to the mechanical switch detection method.

3. MMC electrical interface

Advanced appliances optimized for low-power consumption can operate MMC's at two different supply voltages with the slight disadvantage of the increased control effort and a selectable supply voltage. A number of MMC threshold levels for the high-voltage range are listed in Table 5.

3.1 Bus operating conditions

The minimum output level of the driving device, together with the receiving device input level is specified in Table 5 (taken from Ref. 2 "Multi Media Card System Specification version 4.3, JESD84-A43, November 2007").

Similar considerations as shown in Section 2.2 "SD-memory card bus timing conditions" have to be applied for the MMC, too.

For high-voltage operation mode, the threshold conditions are identical to the SD-memory card conditions, so that both can be operated if connected to the same physical interface as long as the electrical card detection mechanism is not used.

Table 5.   MMC threshold levels
(values taken from Ref. 2)

Symbol	Parameter	Condition	Min	Max	Unit
V_{MMC}	MMC supply voltage				
	high-voltage range		2.7	3.6	V
	low-voltage range	[1]	1.7	1.95	V
Push-pull mode bus signal level for high-voltage MMC					
V_{OH}	high-level output voltage	$I_{OH} = -100 \mu A$; V_{MMCmin}	$0.75*V_{MMC}$	-	V
V_{OL}	low-level output voltage	$I_{OL} = 100 \mu A$; V_{MMCmin}	-	$0.125*V_{MMC}$	V
V_{IH}	high-level input voltage		$0.625*V_{MMC}$	$V_{MMC}+0.3$	V
V_{IL}	low-level input voltage		$V_{SS}-0.3$	$0.25*V_{MMC}$	V

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Table 5. **MMC threshold levels** *…continued*
(values taken from Ref. 2)

Symbol	Parameter	Condition	Min	Max	Unit
Push-pull mode bus signal level for the dual voltage MMC in 1.70 V to 1.95 V mode, for high-voltage specified above for high-voltage MMC					
V_{OH}	high-level output voltage	$I_{OH} = -100$ μA; V_{MMCmin}	$V_{MMC}-0.2$	-	V
V_{OL}	low-level output voltage	$I_{OL} = 100$ μA; V_{MMCmin}	-	0.2	V
V_{IH}	high-level input voltage		$0.7*V_{MMC}$	$V_{MMC}+0.3$	V
V_{IL}	low-level input voltage		$V_{SS}-0.3$	$0.3*V_{MMC}$	V

[1] Low-voltage levels are part of the dual voltage range card specification including also the high-voltage range. The voltage range from 1.95 V to 2.7 V is undefined.

Compared to the SD-memory card, the MMC bus is limited to a maximum of only 30 pF (SD-memory card is 40 pF maximum).

The eMMC contains pull-up resistors at the pins Data0 to Data7 to prevent floating of unconnected data lines. All other MMCs do not contain any pull-up resistors to prevent bus floating.

Two basic differences are the minimum resistor value of R_{CMD} which is less than half the specified minimum of the SD-memory card specification, and the Data0 to Data7 pull-up resistor values, starting at 50 kΩ instead of 10 kΩ in the SD-memory card specification (see Table 2 for details).

Table 6. **MMC operating conditions**

Symbol	Parameter	Min	Max	Unit
C_L	total bus capacitance for each signal line	-	30	pF
C_{CARD}	single card signal line capacitance			
	C_{MICRO}	-	12	pF
	C_{MOBILE}	-	18	pF
	C_{BGA}	-	12	pF
R_{CMD}	CMD pull-up resistor value	4.7	100	kΩ
R_{DAT7-0}	external Data7 to Data0 pull-up resistor value (except eMMC)	50	100	kΩ
R_{intDAT}	eMMC internal Data7 to Data0 pull-up resistor value	50	150	kΩ
L_{ch}	maximum signal line capacitance	-	16	nH

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3.2 Bus timing conditions

The MMC interface has different timing requirements for its default mode and the high-speed mode running up to 52 MHz. Special attention should be paid to the clock signal rise time/fall time requirement (3 ns maximum) which is similar to the high-voltage range cards and the SD-memory card timing conditions (see Table 3).

Also, a reduced clock speed of up to 26 MHz can be used with these cards to save power in appliances that do not require high data rates.

As all NXP devices support the high-speed mode that supersedes the default-mode requirements, only these requirements are taken into account here. However, the devices explained in this document support both, the default-mode and the high-speed mode.

Table 7.   MMC timing conditions (high-speed mode)[1]

Symbol	Parameter	Min	Max	Unit
f_{PP}	operating clock frequency	0	(26)/52	MHz
t_{rise}	high-speed mode clock rise time	[2] -	3	ns
t_{fall}	high-speed mode clock fall time	-	3	ns

[1]   Other timing parameters such as hold time, set-up time, high-time and low-time are dependent on the host / MMC interface and are not significantly influenced by the NXP interface conditioning devices.

[2]   Please refer to Ref. 2, chapter 12.7.1 for further details.

3.3 Capacitive load at the interface conditioning device output

Please refer to Section 2.3 for a detailed overview and calculation.

The drawings depicted in Figure 3 show that it is difficult to build an MMC specification-compliant bus system that includes high-level ESD protection and EMI filtering. Nevertheless, most implementations used are basically related to the SD-memory card application and use only slightly higher total channel capacitances, reaching the SD specification for the value of $C_{HOST} + C_{BUS}$.

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4. SD-memory card and MMC interface comparison

A short summary of the main electrical interface parameters of the SD-memory card versus the MMC are listed in the following table:

Table 8.   SD-memory card vs. MMC main electrical parameters

Symbol	Parameter	SD-memory card	MMC	Unit
$V_{sd/MMC}$	memory card supply voltage			
	high-voltage range	2.7 - 3.6	2.7 - 3.6	V
	low-voltage range	-	1.7 - 1.95	V
f_{PP}	operating clock frequency	$50_{(MAX)}$	$52_{(MAX)}$	MHz
$t_{rise/fall}$	high-speed mode clock rise time/fall time	$3_{(MAX)}$	$3_{(MAX)}$	ns
C_L	total bus capacitance for each signal line	$40_{(MAX)}$	$30_{(MAX)}$	pF
C_{CARD}	single card signal line capacitance	$10_{(MAX)}$	-	pF
	C_{MICRO}; MMC only	-	$12_{(MAX)}$	pF
	C_{MOBILE}; MMC only	-	$18_{(MAX)}$	pF
	C_{BGA}; MMC only	-	$12_{(MAX)}$	pF
R_{CMD}	CMD pull-up resistor value	10 - 100	4.7 - 100	kΩ
$R_{DAT7(3)-0}$	external Data7(3) - Data0 pull-up resistor value MMC (SD) to prevent bus floating (except eMMC)	10 - 100	50 - 100	kΩ
$R_{intDAT3}$	eMMC internal Data7- Data0 pull-up resistor value (eMMC only)	-	50 - 150	kΩ
	DAT3/CD (SD)	10 - 90	-	kΩ
L_{ch}	maximum signal line capacitance	$16_{(MAX)}$	$16_{(MAX)}$	nH

5. Passive ESD protection and EMI filter devices

NXP Semiconductors offers a wide range of devices for the interface conditioning of the SD-memory card and/or MMC interface. The product range covers basic EMI filters and ESD protection devices (IP4252CZ12-6 or IP4252CZ16-8) up to a fully integrated interface device containing voltage translators, LDO, EMI filtering, high-level ESD protection, and all required biasing/pull-up/pull-down resistors integrated into a single monolithic IP4853CX24/LF.

Besides the SD-memory card or MMC interface mode, these devices can be used for e.g. Serial Peripheral Interface (SPI)-based interface operation modes, too. In this case, 4-channel devices can be used although this is not the preferred method of data exchange with SD-memory cards due to the lower speed and only single bit access.

A basic overview is given in Table 9 and a detailed description is given in the next chapters.

Passive filter devices are available in leadless plastic packages (DFN) and Wafer Level Chip Size Packages (WLCSP) while the solutions incorporating active devices are available in WLCSP only.

Even though the MMC and SD-memory card specifications state exact minimum and maximum values for the various internal and external pull-up and pull-down resistors, a majority of implemented interfaces in available appliances do not follow these recommendations.

Especially the minimum CMD signal pull-up resistor value is often undercut to guarantee a sufficiently short rise time in an open-drain communication mode.

(OR: This is especially true for the minimum CMD signal pull-up resistor value, which is often undercut to guarantee a sufficiently short rise time in an open-drain communication mode.) The minimum values of the external pull-up resistor values of the MMC specification are also sometimes replaced by values from the SD-memory card specification range.

Therefore, most NXP Integrated Discretes devices can be used in both interface applications, MMCs and SD-memory cards, even though the data sheet is referring to just one interface type!

Today's state-of-the-art memory cards will typically support interfaces which are slightly out of the related general interface specification.

Table 9. **SD-memory card and MMC interface devices overview**

Product name	Device type	Additional features	Number of filter channels	Package type and size
Memory card interface ESD protection and EMI filter devices with integrated biasing (pull-up-/pull-down) resistors, ESD protection level of > 15 kV contact, far exceeding the IEC61000-4-2, level 4 (8 kV contact, 15 kV air)				
IP4051CX11/LF	passive, ESD protection and EMI filter		4	CSP, 0.5 mm pitch [1.96×2.54 mm^2]
IP4052CX20/LF	passive, ESD protection and EMI filter		6	CSP, 0.5 mm pitch [1.96×2.54 mm^2]
IP4060CX16/LF	passive, ESD protection and EMI filter		6	CSP, 0.5 mm pitch [2.01×2.01 mm^2]
IP4350CX24/LF	passive, ESD protection and EMI filter	inclusive WP and CD	6 (+5) [1]	CSP, 0.4 mm pitch [2.01×2.02 mm^2]
IP4352CX24/LF	passive, ESD protection and EMI filter	inclusive WP and CD	6 (+5) [1]	CSP, 0.4 mm pitch [2.01×2.02 mm^2]
Memory card interface ESD protection and EMI filter devices, ESD protection level according IEC61000-4-2, level 4 (8 kV contact, 15 kV air discharge)				
IP4252CZ8-4	passive, ESD protection and EMI filter		4	DFN, 0.4 mm pitch [1.35×1.7 mm^2]
IP4252CZ12-6	passive, ESD protection and EMI filter		6	DFN, 0.4 mm pitch [1.35×2.5 mm^2]
IP4252CZ16-8	passive, ESD protection and EMI filter		8	DFN, 0.4 mm pitch [1.35×3.3 mm^2]

Table 9. **SD-memory card and MMC interface devices overview** *…continued*

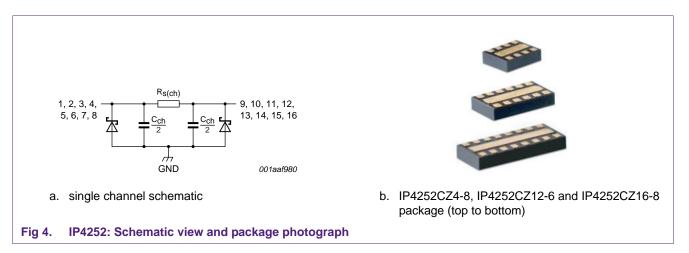| Product name	Device type	Additional features	Number of filter channels	Package type and size
Bidirectional memory card interface voltage translator device, IC level ESD protection according IEC 61340-3-1, HBM, 2 kV				
IP4852CX25/LF	Active, 1.8 V ⇔ 2.9 V voltage translator	voltage translators	6	CSP, 0.4 mm pitch [2.01 × 2.01 mm^2]
LDO, voltage translators, ESD protection and EMI filter and biasing resistors included WP and CD, integrated ESD protection level according IEC61000-4-2, level 4				
IP4853CX24/LF	Active, 1.8 V ⇔ 2.9 V voltage translator	LDO	6 (+3) [1]	CSP, 0.4 mm pitch [2.01 × 2.01 mm^2]

[1] Numbers in brackets represent additional channels such as pull-up and pull-down channels, Write Protect and Card Detect that are not required for the basic data communication.

5.1 ESD protection EMI filter devices in plastic package IP4252CZ8-4, IP4252CZ12-6, IP4252CZ16-8

For memory card interfaces only requiring ESD protection and/or EMI filtering, devices such as IP4252CZ8-4 (4-channel) IP4252CZ12-6 (6-channel) or IP4252CZ16-8 (8-channel) are the devices of choice.

They all contain an RC-based pi-filter (also called Capacitor-Resistor-Capacitor (CRC) filter) consisting of two diodes, acting also as filter capacitors, and a serial channel resistor connected between the cathodes of the diodes.

A schematic of a single filter channel is shown in Figure 4 (left side), while the right side of Figure 4 depicts the package footprint of the DFN plastic package (0.4 mm contact pitch). The maximum package height is 0.5 mm. The most important technical parameters are listed in Table 10.

a. single channel schematic

b. IP4252CZ4-8, IP4252CZ12-6 and IP4252CZ16-8 package (top to bottom)

Fig 4. **IP4252: Schematic view and package photograph**

Table 10. IP4252 parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		−0.5	-	+5.6	V
V_{ESD}	electrostatic discharge voltage	all pins to GND IEC 61000-4-2, level 4				
		contact discharge	−8	-	+8	kV
		air discharge	−15	-	+15	kV
$R_{s(ch)}$	channel series resistance		32	40	48	Ω
C_{ch}	channel capacitance	V_{DC} = 0 V, f = 100 kHz	-	18	-	pF
	$= 2*\dfrac{C_{CH}}{2}$	V_{DC} = 2.5 V, f = 100 kHz	-	12	-	pF

Due to the integrated symmetrical pi-filter structure, also often referred to as CRC structure, all NXP Semiconductors IP425x devices offer a direction-independent and symmetrical ESD protection as well as a direction-independent and symmetrical EMI filter performance.

The integrated pi-filter structures result in a very low ESD clamping voltage compared to single diode ESD protection implementations and/or devices.

5.1.1 Application details of IP4252CZ12-6 and IP4252CZ16-8

The schematic drawing depicted in Figure 5 shows a typical application of IP4252CZ12-6 and/or IP4252CZ16-8 in an SD-memory card interface including both options for card detection. The grey-colored components are optional and depend on the exact details of the interface implementation. Especially with respect to the card detect mechanism, either using a mechanical switch in the card holder (preferred according Ref. 1) or the use of the integrated pull-up resistor at pin DAT3/CD in combination with selectable pull-down / pull-up resistors, the exact resistor values have to be aligned with all details described in Ref. 1.
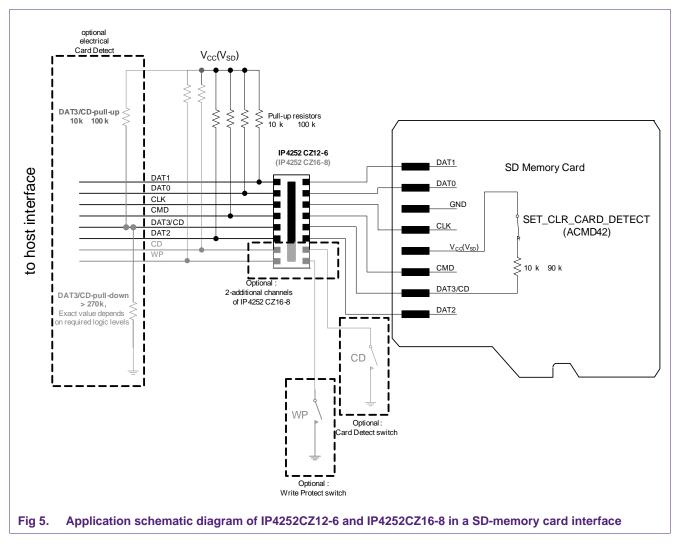
This schematic does not include details concerning card-supply and typical power-supply decoupling capacitors.

For the basic SD-memory card operation an IP4252CZ12-6 and 4 pull-up resistors (10 kΩ to 100 kΩ) are sufficient for the digital data transmission from and to the SD-memory card. MMCs require higher pull-up resistor values starting at 50 kΩ. The card-detection mechanism has to be implemented using a CD channel as depicted in Figure 6, based on a mechanical card-detection switch in case SD and MMC are used with the same interface.
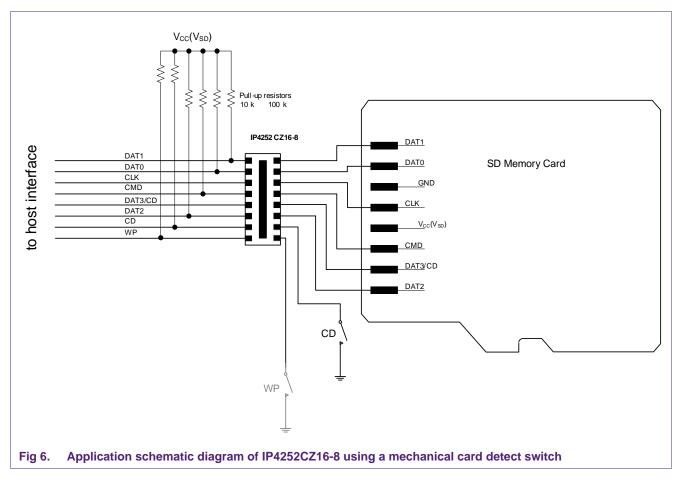
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Fig 5. **Application schematic diagram of IP4252CZ12-6 and IP4252CZ16-8 in a SD-memory card interface**

The implementation of a Write-Protect (WP) contact is only possible in applications which are supporting standard size SD-memory cards. Smaller form-factor versions such as mini-SD or micro-SD do not support this feature. In case the mechanical slider mechanism of the standard size SD-memory card is used, a pull-up resistor is connected to the host supply and a mechanical contact to GND. This contact is open until a WP slider is closing it. (Mechanical adaptors converting a micro or mini SD-memory card into a standard SD-card size do typically not support this feature).

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Fig 6. **Application schematic diagram of IP4252CZ16-8 using a mechanical card detect switch**

In case a mechanical card-detection switch is prohibited e.g. due to size constraints for the card holder, an electrical card-detection can be used as an alternative but only for an SD-memory card interface.

After power-up, DAT3/CD is connected to a 50 kΩ (nominal value, specified range is 10 kΩ to 90 kΩ) pull-up resistor inside the card. In case DAT3/CD is connected to a high-ohmic pull-down resistor (> 270 kΩ to fulfill the logic voltage level requirements[1]), the connected host can detect a logic level change from low to high level. The card internal pull-up resistor should be disconnected during regular data transmission with a SET_CLR_CARD_DETECT (ACMD42) command.

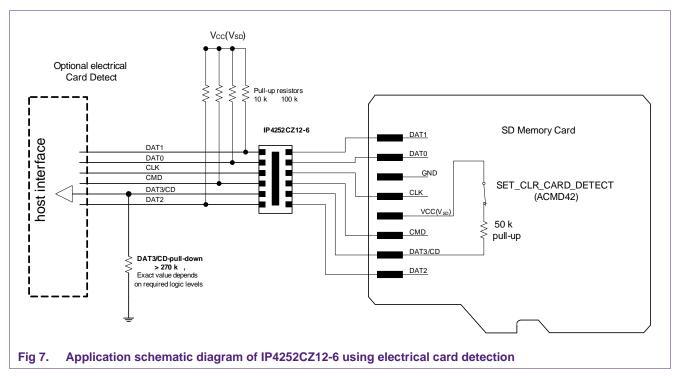The basic schematic diagram for this implementation is shown in Figure 7.

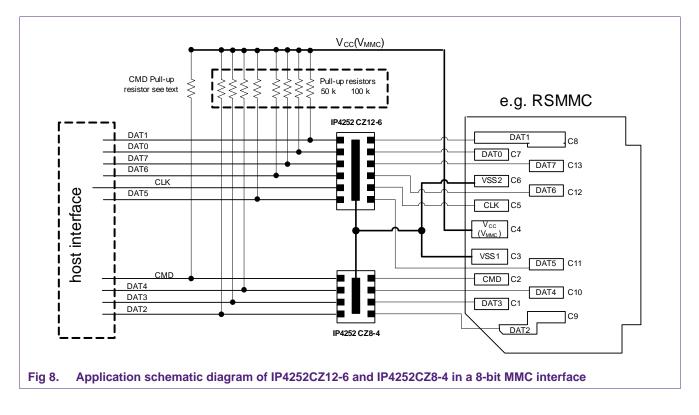1. The exact value depends on the logic level requirements.

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Fig 7.   **Application schematic diagram of IP4252CZ12-6 using electrical card detection**

For the latest 8-bit MMC interface, 10 channels have to be ESD-protected and EMI-filtered. A combination of IP4252CZ8-4 (4-channel) and IP4252CZ12-6 (6-channel) is best-matching filter combination to cover the full interface (Figure 8).

Fig 8.   **Application schematic diagram of IP4252CZ12-6 and IP4252CZ8-4 in a 8-bit MMC interface**

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5.2 ESD protection EMI filter devices CSP IP4051CX11/LF

Both devices contain the exact same circuitry consisting of four ESD-protected and EMI-filtered channels, two of which contain pull-up resistors (see Figure 9). The devices are optimized for the non-high-speed MMC cards but can also be used for the SD-memory card SPI mode. The most important parameters are listed below in Table 11.
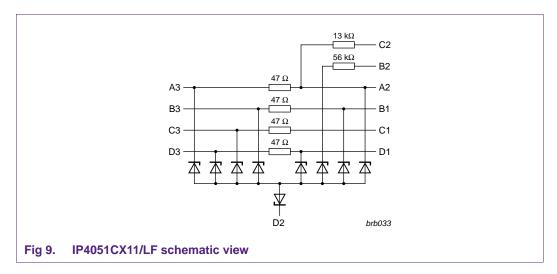
Table 11. IP4051CX11/LF parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	−0.5	-	+5.0	V
V_{ESD}	electrostatic discharge voltage	all pins to ground IEC 61000-4-2, level 4				
		contact discharge [2]	−8(−15)	-	+8(+15)	kV
		air discharge	−15	-	+15	kV
$R_{s(ch)}$	channel series resistance		44.65	47	49.35	Ω
C_{ch}	channel capacitance	V_{DC} = 0 V; f = 100 kHz	-	25	-	pF

[1] V_{CC} is the memory card supply voltage, also named V_{SD} or V_{MMC} in this document.

[2]   Device withstands more than 1000 discharges of ±15 kV contact discharge according the IEC 61000-4-2 model, far exceeding the specified level 4.

Due to the typical channel capacitance of 25 pF, these devices are not recommended for high-speed compliant memory cards and clock speeds higher than 25 MHz.

Fig 9.   IP4051CX11/LF schematic view

5.2.1 Application information of IP4051CX11/LF in an SPI mode SD-memory card interface
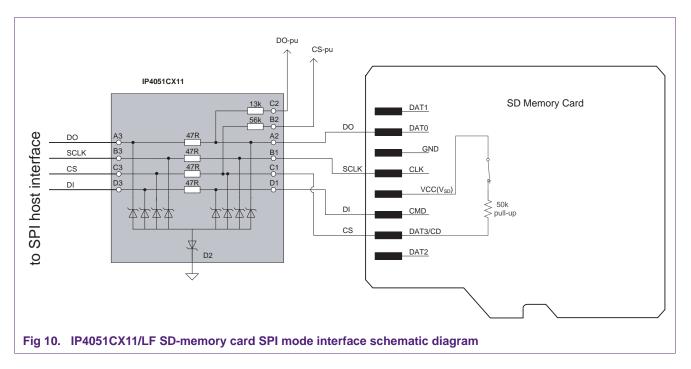
In case a full 4-bit/8-bit memory card interface implementation on the host side is not required or not possible (e.g. too high design-in effort), SD-memory cards/MMC offer an SPI mode interface function. This interface type requires only four interface lines and uses a single-bit physical data transmission with a maximum of 25 MHz clock frequency. Please note that the SPI mode is no longer supported according JESD84-A43, MMC version 4.3 specification. For details, please refer to chapter 9, 'SPI mode' of Ref. 2.

A basic schematic diagram is depicted in Figure 10.

Resistor 'DO-pu' should be connected to V_{CC} in order to avoid bus floating while no card is present.

During power-up, CS (DAT3/CD) should be pulled high using resistor 'CS-pu' during the first 74 clock cycles and pulled low via the host interface drivers while the card is receiving a reset command (CMD0). This will initiate the SPI interface mode.

All unused SD-memory card pins (DAT1 and DAT3) should be pulled high using additional resistors which are not shown here.

Fig 10. IP4051CX11/LF SD-memory card SPI mode interface schematic diagram

5.3 MMC ESD protection and EMI filter device IP4060CX16/LF

The IP4060CX16/LF is a 6-channel MMC device with 5 additionally integrated pull-up resistors in a tiny 0.5 mm ball pitch CSP.

The only channel without a pull-up resistor is the clock channel (see schematic diagram in Figure 11, pin B4 to pin A1). Due to the pull-up resistor implementation, the electrical card detection method cannot be used. Detection using a mechanical switch is mandatory.

The maximum filter channel capacitance is 20 pF which makes the device suitable to work in high clock speed applications, too.

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Table 12. **IP4060CX16/LF parameters**

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	voltage range		[1]	−0.5	-	+5.5	V
V_{ESD}	electrostatic discharge voltage	all pins to ground IEC 61000-4-2, level 4					
		contact discharge	[2]	−8(−15)	-	+8(+15)	kV
		air discharge		−15	-	+15	kV
$R_{s(ch)}$	channel series resistance			40	50	60	Ω
R_{DAT}	data channel pull-up resistor value			52.5	75	97.5	kΩ
R_{CMD}	CMD channel pull-up resistor value			4.9	7	9.1	kΩ
C_{ch}	channel capacitance	V_{DC} = 0 V; f = 100kHz		-	18	20	pF

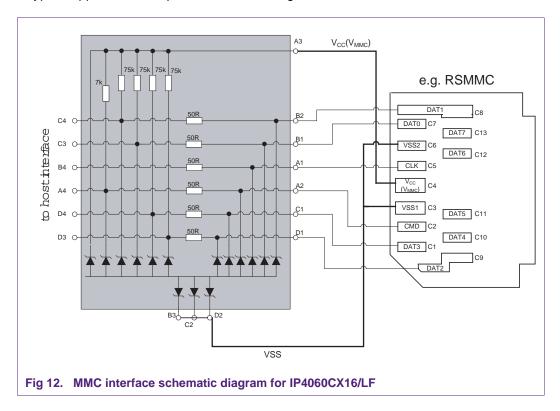[1] V_{CC} is the memory card supply voltage, also named V_{SD} or V_{MMC} in this document.

[2]   Device withstands more than 1000 discharges of ±15 kV contact discharge according the IEC 61000-4-2 model, far exceeding the specified level 4.

Fig 11. Schematic view for IP4060CX16/LF

5.3.1 MMC interfacing using IP4060CX16/LF

The IP4060CX16/LF contains ESD protection, EMI filtering and provides pull-up resistors according to the MMC specification for a 4-bit interface implementation. Even though the CMD line pull-up resistor value is lower than the 10 kΩ recommended in the SD-memory card specification, the IP4060CX16/LF is often used in conjunction with this interface.

A typical application is depicted in the following schematic:

Fig 12.   MMC interface schematic diagram for IP4060CX16/LF

5.4 Memory Card interface using IP4052CX20/LF

Another product suitable for the memory card interface is the IP4052CX20/LF. This ESD protection and EMI filter device contains 6 channels for CMD, CLK and 4 data channels plus 2 spare resistors in order to e.g. bias a card detection switch.

Compared to other devices, the IP4052CX20/LF contains pull-up resistors for the 4 data channels and the CMD channel. In addition, it also contains a relatively low-ohmic pull-up resistor connected to the CMD channel.

The maximum filter channel capacitance is 20 pF which makes the device suitable for high clock-speed applications as well.

Electrical card detection for the SD-memory card is not supported.

The most important electrical parameters are listed in Table 13.

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Table 13.   IP4052CX20/LF parameters

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	−0.5	-	+5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4	[2]				
		contact discharge	[3]	−8(−15)	-	+8(+15)	kV
		air discharge		−15	-	+15	kV
R_{1-6}	channel series resistor value			30	40	50	Ω
$R_{7, 8}$	CD biasing resistor value			37	50	63	kΩ
R_{10-14}	data and CMD pull-up resistor value			18	25	32	kΩ
R_{15}	additional low-ohmic CMD pull-up			0.72	1.0	1.28	kΩ
C_{ch}	channel capacitance	$V_{DC} = 0$ V; f = 100kHz		-	18	24	pF
		$V_{DC} = 2.5$ V; f = 100kHz		-	15	20	pF

[1] V_{CC} is the memory card supply voltage, also named V_{SD} or V_{MMC} in this document.

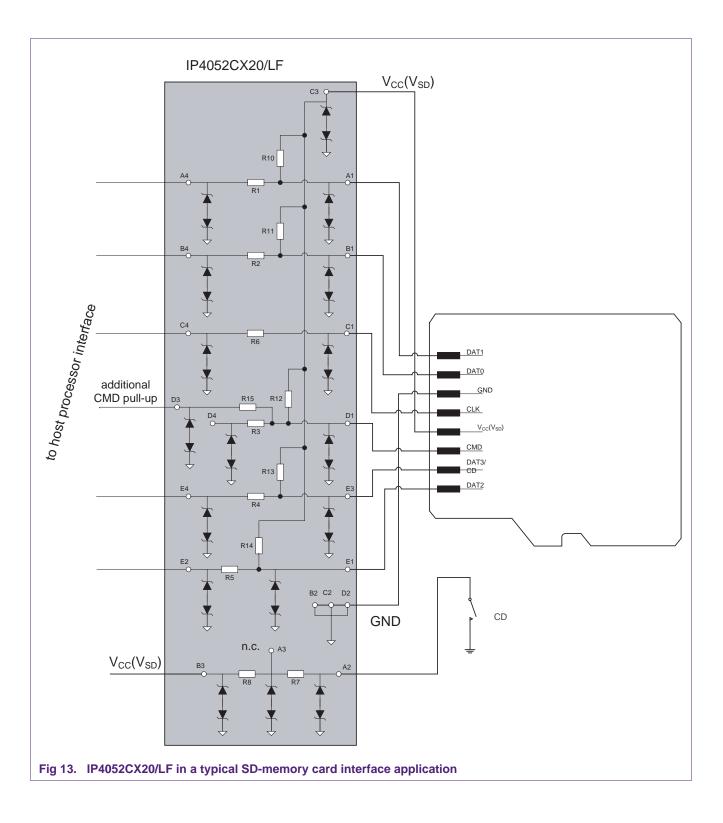[2]   Pins A1, B2, C1, D1, E1, A3, E3 and C3 to ground.

[3]   Device withstands > 1000 discharges of ±15 kV contact discharge according the IEC 61000-4-2 model, far exceeding the specified level 4.

5.4.1 SD-memory card interfacing using IP4052CX20/LF

The low-ohmic CMD pull-up resistor connected to pin D3 is optional. This pin can be connected e.g. to a GPIO pin and set to "high" for the initial open-drain sequence at the CMD card pin. After this initial stage, the GPIO pin can be set to 3-state, so that CMD and the 4 data pins face the same pull-up resistor values.

The CD switch bias resistors R7 and R8 can be interconnected in various ways to generate different total resistor values. The circuitry shown in Figure 13 serves as a reference.

Fig 13. IP4052CX20/LF in a typical SD-memory card interface application

5.5 Very highly integrated memory card interface devices IP4352CX24/LF and IP4350CX24/LF

The IP4350CX24/LF and the IP4352CX24/LF are products demonstrating the highest level of integration, consisting of ESD protection, EMI filter, and biasing resistors in a passive device. As the package is a 0.4 mm pitch CSP type, the total device size is approximately 2×2 mm^2.

Both devices, IP4352CX24/LF and IP4350CX24/LF fully support high-speed memory card interfaces working with clock speeds up 52 MHz.

A special diode structure using a rail-to-rail (also known as "crow-bar") diode concept on the high-level ESD protection side in combination with the single diodes on the low-level ESD protection side guarantee a balanced distribution of the channel capacitance. This leads to symmetrical EMI filter performance which is independent from the read/write direction.

Both, the IP4352CX24/LF and the IP4350CX24/LF support electrical card detection of an SD-memory card using the pins DAT3_PD and R21 connected to GND. A detailed schematic showing the driver and control circuitry required to use electrical card detection is depicted in Figure 15. Electrical card detect is available as long as the "control" inverter is low and 'driver_pu' is 3-stated, so R21 is acting as a pull-down to GND.
If normal operation is needed, the "control" inverter has to drive a high signal to enable the 'driver_pu' buffer, drive a high signal at R11 and also to drive R21 to a high level to avoid any unnecessary quiescent current.
Be aware that the maximum voltage at the pin to the host interface may exceed the host supply voltage as it is derived from: $V_{SD}*(R_{11}/(R_{11} + R_{DAT3/\mathrm{CD\_pu}}))$. In this case a voltage tolerant input has to be selected.

If electrical card detection is not required, DAT3_PU (R11) should be connected to V_{SD} instead.

Please note, that the CMD line is connected to the pull-up resistor R15 which is typically 15 kΩ, so that IP4350CX24/LF can also be used in combination with an MMC.
The MMC can be initialized using a 400 kHz open-drain mode.

The channels for the mechanical 'write protect' WP, the 'card detect' CD, and the combined WP+CD require an additional pull-up resistor which is not integrated. Often pull-up resistors integrated into the GPIOs of the host processor are used for this as they can be switched off after detection.

The basic difference between the IP4352CX24/LF and the IP4350CX24/LF is the channel series resistance, the CMD pull-up resistor value (R15) and the line capacitance. For details, refer to Table 14.

The lower CMD pull-up resistor value and lower total line capacitance value make the IP4350CX24/LF an excellent match for MMC interfaces in case a compliance with the latest standard specification is mandatory.

Three additional channels support any configuration of card-detect and write-protect switches for the various memory card holders.

The most important electrical parameters are listed in Table 14.

Table 14.   IP4350CX24/LF and IP4352CX24/LF parameters

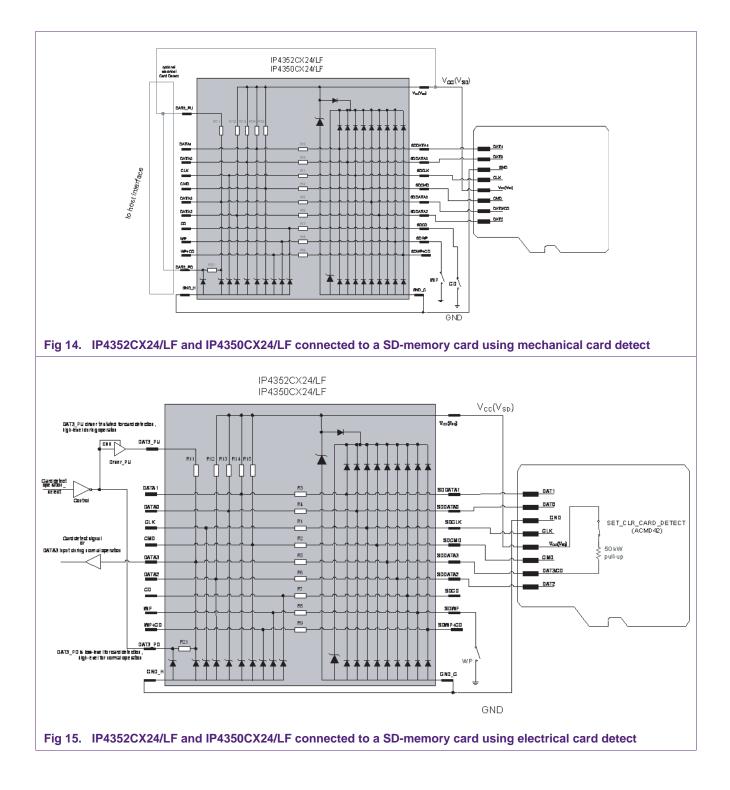| Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{SD}	supply voltage		[1]	−0.5	-	+5.0	V
V_{ESD}	electrostatic discharge voltage	SDxxx pins to GND IEC 61000-4-2, level 4					
		contact discharge	[2]	−8(−15)	-	+8(+15)	kV
		air discharge		−15	-	+15	kV
R_{1-9}	channel series resistance						
	IP4350CX24/LF			12	15	18	Ω
	IP4352CX24/LF			32	40	48	Ω
R_{11-14}	data pull-up resistor value			35	50	65	$k\Omega$
R_{15}	CMD pull-up resistor value						
	IP4350CX24/LF			3.29	4.7	6.11	$k\Omega$
	IP4352CX24/LF			10.5	15	19.5	$k\Omega$
R_{21}	dat3/CD pull-down resistor			329	470	611	$k\Omega$
C_{ch}	channel capacitance	$V_{DC} = 0$ V; f = 100kHz					
	IP4350CX24/LF, data, CMD			-	8.8	-	pF
	IP4350CX24/LF, CLK			-	7.8	-	pF
	IP4352CX24/LF, data, CLK, CMD			-	-	20	pF

[1] V_{CC} is the memory card supply voltage, also named V_{SD} or V_{MMC} in this document.

[2]   Device withstands > 1000 discharges of ±15 kV contact discharge according the IEC 61000-4-2 model, far exceeding the specified level 4.

Fig 14. IP4352CX24/LF and IP4350CX24/LF connected to a SD-memory card using mechanical card detect

Fig 15. IP4352CX24/LF and IP4350CX24/LF connected to a SD-memory card using electrical card detect

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5.6 Active memory card voltage translator circuit IP4852CX25/LF

The IP4852CX25/LF is a voltage translator optimized to be used in conjunction with a 1.8 V operating host interface and an SD-memory card or a high-voltage range MMC.

The device is high-speed compliant, containing a CLK channel with an additional feedback channel and 5 bidirectional voltage translators.

The device size is approximately 2×2 mm^2!

These voltage translators are clustered in three groups, so that e.g. a single-bit interface operation can be conducted without any energy consumption from switching the data1-3 translators.

The host interface (left side of the schematic) voltage range is 1.62 V to 1.9 V.
The SD-memory card interface side (right side of the schematic) is 2.5 V to 3.5 V (see also Table 15).

A schematic showing the internal circuitry of the IP4852CX25/LF is depicted in Figure 16.

The IP4852CX25/LF is an excellent match for e.g. the IP4352CX24/LF or IP4350CX24/LF, the IP4060CX16/LF, and the IP4052CX20/LF, but is also suitable to work with other devices listed in this document in order to implement a level shifting function in combination with ESD protection, EMI filtering, and biasing for memory card interfaces using the smallest possible footprint.

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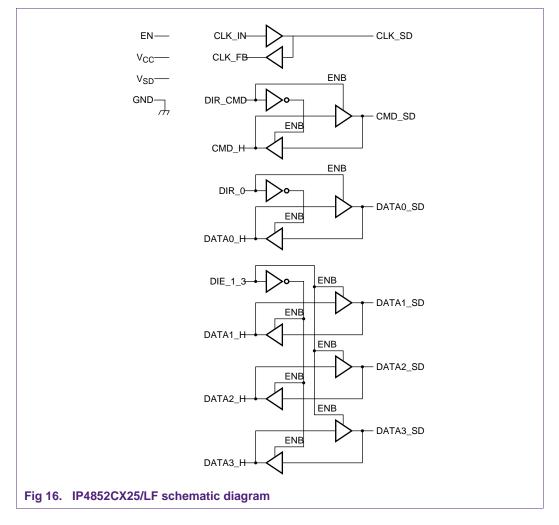
Fig 16. IP4852CX25/LF schematic diagram

Table 15.   IP4852CX25/LF electrical parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SD}	SD-card interface side supply voltage		2.5	2.9	3.5	V
V_{CC}	host interface side supply voltage		1.62	1.8	1.9	V
V_{ESD}	electrostatic discharge voltage	IEC 61340-3-1, HMB	2	-	-	kV

The timing data listed in Table 16 show that the IP4852CX25/LF can easily cope with a 40 pF load, even under worst-case conditions.

Please note that the parameter values under condition T_{amb} = +75 °C are valid for a memory card supply level of 2.5 V only. This supply level is below the minimum requirement of 2.7 V for both, the SD-card and MMC specification.

The used high and low limits of 70 % and 20 % are much harder to be fulfilled than those of the original SD-memory card specification. For details, refer to Table 1.

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Table 16. **Processor side to memory card side timing with HIGH-ref = 0.7*V$_O$, LOW-ref = 0.2*V$_O$**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		T_{amb} = 25 °C; $V_{CC(host\ side)}$ = 1.8 V; $V_{SD(SD\ side)}$ = 2.9 V; HIGH-ref = 70 % * $V_O(V_{SD})$; LOW-ref = 20 % * $V_O(V_{SD})$				
t_r, t_f	rise time, fall time	Z_{load} = 25 pF || 100 kΩ	-	0.7	1.8	ns
		Z_{load} = 40 pF || 100 kΩ	-	1.3	2.6	ns
		T_{amb} = −30 °C; $V_{CC(host\ side)}$ = 1.9 V; $V_{SD(SD\ side)}$ = 3.5 V; HIGH-ref = 70 % * $V_O(V_{SD})$; LOW-ref = 20 % * $V_O(V_{SD})$				
t_r, t_f	rise time, fall time	Z_{load} = 25 pF || 100 kΩ	-	0.6	1.4	ns
		Z_{load} = 40 pF || 100 kΩ	-	1	2.2	ns
		T_{amb} = +75 °C; $V_{CC(host\ side)}$ = 1.62 V; $V_{SD(SD\ side)}$ = 2.5 V; HIGH-ref = 70 % * $V_O(V_{SD})$; LOW-ref = 20 % * $V_O(V_{SD})$				
t_r, t_f	rise time, fall time	Z_{load} = 25 pF || 100 kΩ	-	0.8	2.7	ns
		Z_{load} = 40 pF || 100 kΩ	-	1.5	2.9	ns

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5.7 Active memory card voltage translator, power supply, ESD protection and EMI filter device IP4853CX24/LF

The highest integration level among the various memory card interface products is offered by the IP4853CX24/LF.

This device integrates the level-shifting functionality of the IP4852CX25/LF and the EMI filter/ESD protection of IP4350CX24/LF with an additional power supply unit (LDO) in a 2×2 mm^2 device.

The IP4853CX24/LF voltage translator part is optimized to be used in conjunction with a 1.8 V operating host interface and an SD-memory card or a high-voltage range MMC. It is high-speed compliant, contains a CLK channel with an additional feedback channel and 5 bidirectional voltage translators plus 2 additional pull-up resistors to bias WP and CD switches.

Additionally, the memory card interface pins contain high-level ESD protection diodes (IEC 61000-4-2, level 4, ±8 kV contact), and also EMI filters to avoid any significant radiation from this interface.

Another feature is the integrated LDO that can be connected directly to e.g. a mobile phone battery to generate a supply voltage of 2.9 V for a connected memory card.

The integrated voltage translators are clustered into three groups (as in IP4852CX25/LF), so that e.g. a single-bit interface operation can be conducted without any energy consumed by switching the data1-3 translators.

The host interface (left side of the schematic) voltage range is 1.62 V to 1.9 V the memory card interface is connected to the LDO output side (right side of the schematic, pin V_{SD}) and typically supplies 2.9 V (see also Table 15).
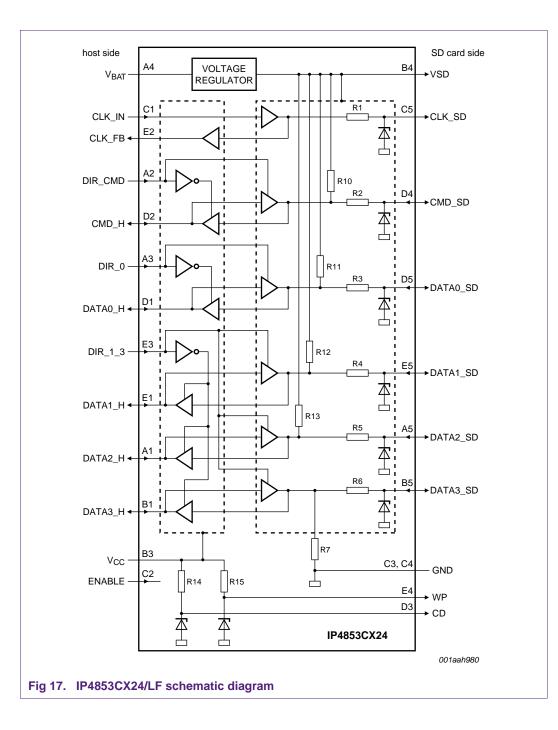
A schematic showing the internal circuitry of the IP4853CX24/LF is depicted in Figure 17.

Fig 17. IP4853CX24/LF schematic diagram

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Table 17. IP4853CX24/LF Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		-	1.62	2.1	V
V_{BAT}	battery supply voltage		-	2.7	5.0	V
V_I	input voltage	host side	-	0	2.1	V
		SD-card side; $V_{BAT} \geq 3.2$ V	-	0	2.9	V
V_O	output voltage	host side; active mode (ENABLE = '1')	-	0	V_{CC}	V
		SD-card side; active mode (ENABLE = '1')	-	0	$V_{O(reg)}$	V
T_{amb}	ambient temperature		-	−30	+85	°C
$\Delta t/\Delta V$	time difference over voltage change	$0.2V_{CC} \leq V_I \leq 0.7V_{CC}$	-	-	2	ns/V

Some timing data are listed in Table 18.

As this device will be located close to the memory card holder and no major additional capacitance will be added to the driving output of the IP4853CX24/LF (EMI filter and ESD protection are already integrated), the high and the low limits are intentionally set to 70 % and 20 % to include some safety margin.

Table 18. Processor side to memory card side timing with HIGH-ref = $0.7V_O$, LOW-ref = $0.2V_O$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HIGH-ref = $0.7V_O$ and LOW-ref = $0.2V_O$; V_{BAT} = 3.5 V; VSD = $V_{O(reg)}$ = 2.9 V						
t_t	transition time	T_{amb} = 25 °C; V_{CC} = 1.8 V				
		Z_{load} = 20 pF || 100 kΩ	-	1.5	2.5	ns
		Z_{load} = 40 pF || 100 kΩ	-	2.7	3.6	ns
		T_{amb} = −30 °C; V_{CC} = 1.9 V				
		Z_{load} = 20 pF || 100 kΩ	-	1.5	2.5	ns
		Z_{load} = 40 pF || 100 kΩ	-	2.7	3.6	ns
		T_{amb} = +70 °C; V_{CC} = 1.62 V				
		Z_{load} = 20 pF || 100 kΩ	-	1.8	2.8	ns
		Z_{load} = 40 pF || 100 kΩ	-	2.9	3.8	ns

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6. Conclusion

NXP Semiconductors offers a comprehensive portfolio of SD-memory card and MMC compatible interface conditioning and protection devices.

This includes EMI filtering, system level ESD protection and biasing devices as well as level translators including also the memory card supply LDO.

As shown before, the devices are optimized for compliance with their respective memory card interface in terms of channel capacitance, serial resistance and biasing resistor values.

The passive devices explained in this document protect from destruction from system level ESD and also prevent disturbance of e.g. wireless interfaces from the harmonics of the digital memory interfaces while the integrated biasing resistors contribute to gain the maximum space savings compared to discrete solutions.

Furthermore, the active devices support level translations, ESD protection, EMI filtering and power supply via an LDO (IP4853CX24 and IP4852CX25) to allow customers the integration of SD-memory cards in 1.8 V level operating systems.

All devices presented support a simple PCB layout, reduce the risk of EMI due to complex layout of scattered discrete components and allow to minimize compliance testing.

The high integration level and the final test of each device before shipment also improve the overall quality, as the Integrated Discretes' components reduce the number of individual components, solder joints and pick and places processes.

7. Abbreviations

Table 19. Abbreviations

Acronym	Description
CD	Card Detect
CDM	Command
CSP	Chip Scale Package
DFN	Dual Flat No-lead
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
IEC	International Electrotechnical Commission
LDO	Low DropOut
MMC	Multi Media Card
PCB	Printed-Circuit Board
RF	Radio Frequencies
SD	Secure Digital
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
WLCSP	Wafer Level Chip Scale Package
WP	Write-Protect

8. References

[1]   SD specifications, part 1, Physical Layer Specification version 2.00, May 9, 2006

[2]   Multi Media Card System Specification version 4.3, JESD84-A43, November 2007

[3]   NXP Semiconductor data sheet IP4853CX24_2

[4]   NXP Semiconductor data sheet IP4852CX25/LF

[5]   NXP Semiconductor data sheet IP4052CX20/LF

[6]   NXP Semiconductor data sheet IP4251_52_53_54_3

[7]   NXP Semiconductor data sheet IP4060CX16LF_1

[8]   NXP Semiconductor data sheet IP4051CX11/LF

[9]   NXP Semiconductor data sheet IP4350CX24_1

[10]   NXP Semiconductor data sheet IP4352CX24_1

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9. Legal information

9.1 Definitions

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