Integrated Device Technology, Inc.

16 x 16-BIT PARALLEL CMOS MULTIPLIERS

IDT7216L
IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 20ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CEMOS™ high-performance technology
- IDT7216L is pin- and functionally-compatible with TRW MPY016H/K and AMD Am29516
- IDT7217L requires only single clock with register enables making it pin- and functionally-compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL- compatible
- Three-state output
- Available in plastic DIP, Shrink-DIP, Fine-Pitch LCC, LCC, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87531 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7216/IDT7217 are high-speed, low-power 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CEMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10th the power consumption.

The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The $\overline{MSPSEL}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The IDT7216/IDT7217 multipliers are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

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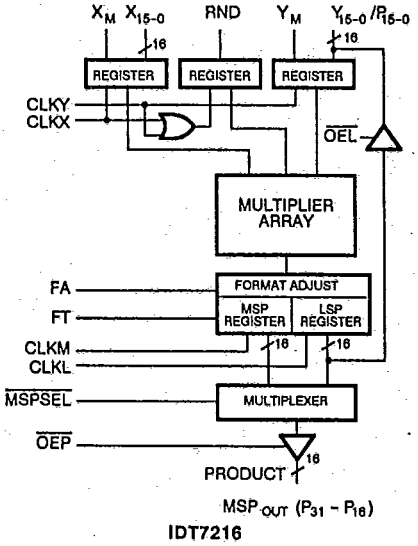
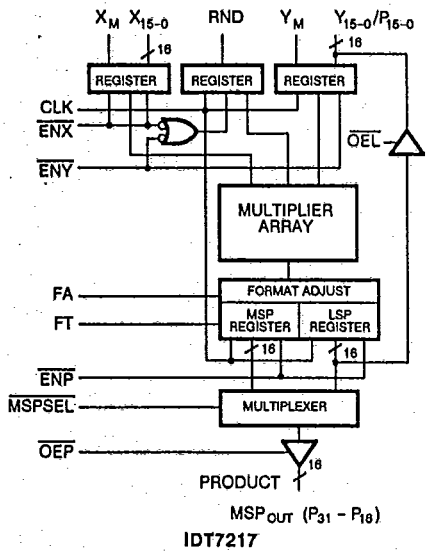
FUNCTIONAL BLOCK DIAGRAMS



IDT7216



IDT7217

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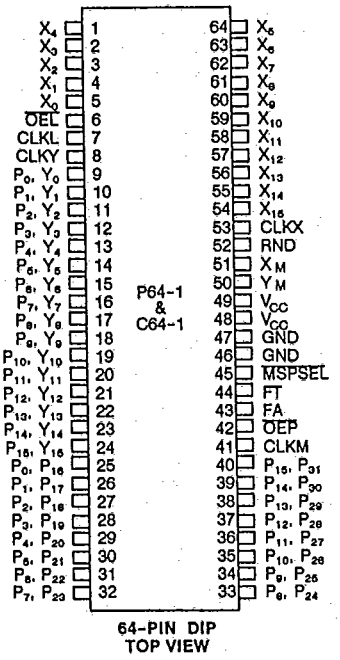
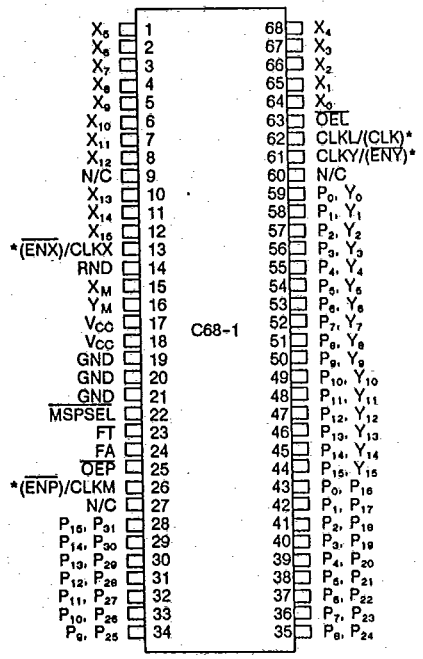
PIN CONFIGURATIONS

IDT7216



64-PIN DIP
TOP VIEW

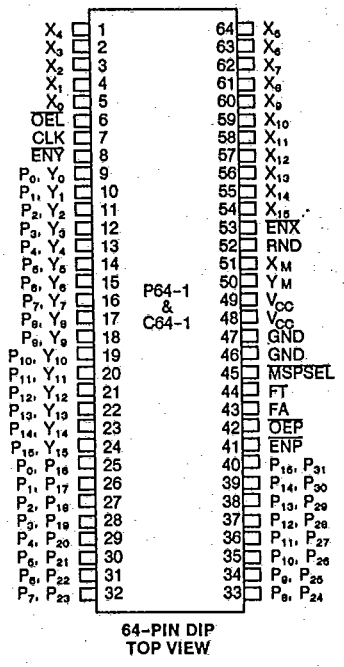
IDT7216/IDT7217



68-PIN SHRINK-DIP
TOP VIEW

* (IDT7217 Pin Designation)

IDT7217



64-PIN DIP
TOP VIEW

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PIN CONFIGURATIONS (CONTINUED)

IDT7216/IDT7217

	A	B	C	D	E	F	G	H	J	K	L
11		NC	X_{13}	X_{15}	RND	Y_M	V_{CC}	GND	FT	$\overline{OEP}$	
10	X_{11}	X_{12}	X_{14}	CLKX or $\overline{ENX}$*	X_M	V_{CC}	GND	$\overline{MSPSEL}$	FA	CLKM or $\overline{ENP}$*	NC
09	X_9	X_{10}								P_{30}, P_{14}	P_{31}, P_{15}
08	X_7	X_8								P_{28}, P_{12}	P_{29}, P_{13}
07	X_5	X_6								P_{26}, P_{10}	P_{27}, P_{11}
06	X_3	X_4				G68-2				P_{24}, P_8	P_{25}, P_9
05	X_1	X_2								P_{22}, P_6	P_{23}, P_7
04	$\overline{OEL}$	X_0								P_{20}, P_4	P_{21}, P_5
03	CLKY or $\overline{ENY}$*	CLKL or $\overline{CLK}$*								P_{18}, P_2	P_{19}, P_3
02	NC	Y_0, P_0	Y_2, P_2	Y_4, P_4	Y_6, P_6	Y_8, P_8	Y_{10}, P_{10}	Y_{12}, P_{12}	Y_{14}, P_{14}	P_{16}, P_0	P_{17}, P_1
01	●	Y_1, P_1	Y_3, P_3	Y_5, P_5	Y_7, P_7	Y_9, P_9	Y_{11}, P_{11}	Y_{13}, P_{13}	Y_{15}, P_{15}	NC	

Pin 1 Designator

*Pin designation for IDT7217

PGA TOP VIEW

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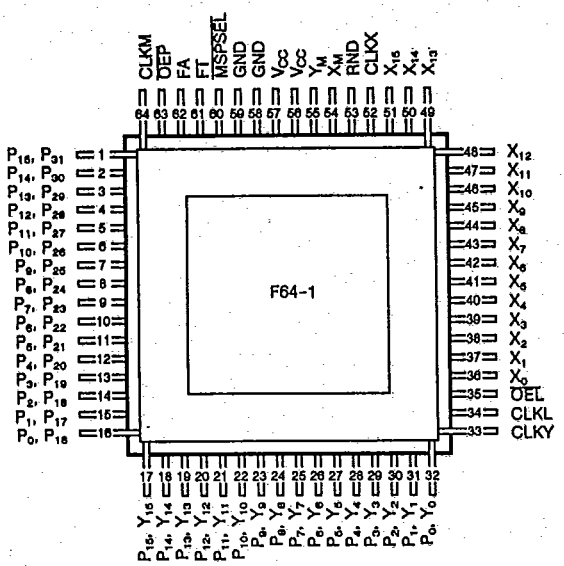
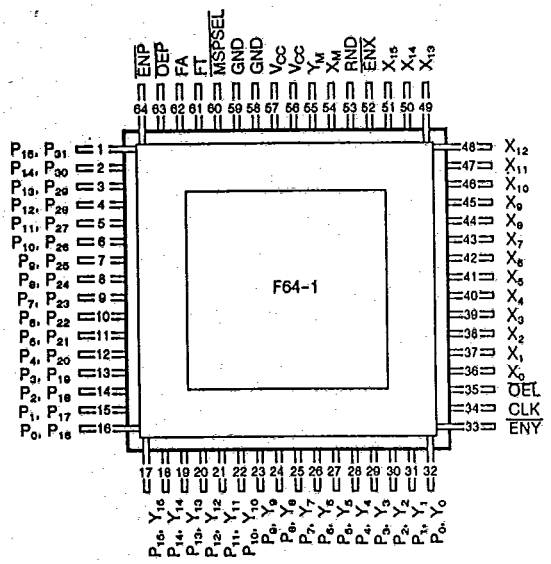
IDT7216



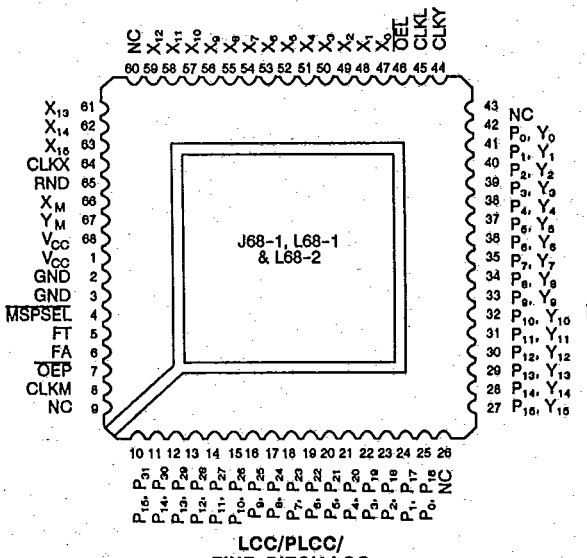
64-LEAD FLATPACK
TOP VIEW

IDT7217



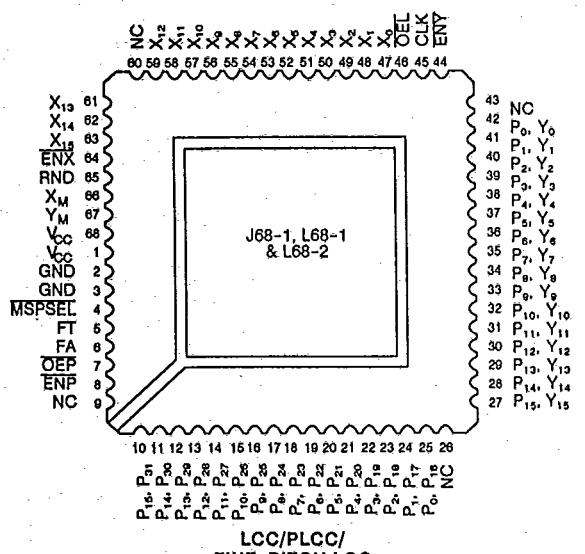
64-LEAD FLATPACK
TOP VIEW

IDT7216



LCC/PLCC/
FINE-PITCH LCC
TOP VIEW

IDT7217



LCC/PLCC/
FINE-PITCH LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

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DC ELECTRICAL CHARACTERISTICS-FAST

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C) for Commercial clocked multiply times of 20, 25, 35, 45, 55, 65ns or Military, 25, 30, 40, 55, 65, 75ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	–	–	10	–	–	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	10	–	–	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	–	40	80	–	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	20	40	–	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	4	20	–	4	25	mA
I_{CC}/f (2,3)	Increase in Power Supply Current MHz	V_{CC} = Max., f > 10MHz	–	–	4	–	–	6	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}(4)	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80 + 4(f-10)mA; for the military range, I_{CC} = 100 + 6(f-10). f = operating frequency in MHz, f = $1/t_{MUC}$ for IDT7216 and f = $1/t_{MC}$ for IDT7217.
3. For frequencies greater than 10MHz.
4. I_{OL} = 8mA for t_{MC} = 20 to 55ns

DC ELECTRICAL CHARACTERISTICS-SLOW

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ±10%, T_A = -55°C to +125°C) for Commercial clocked multiply times of 75, 95, 140ns or Military, 90, 120, 185ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	–	–	2	–	–	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	–	2	–	–	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	–	30	60	–	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	–	10	30	–	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ -0.2V, $V_{IN} \leq$ 0.2V	–	0.1	1.0	–	1.0	2.0	mA
I_{CC}/f (2,3)	Increase in Power Supply Current MHz	V_{CC} = Max., f > 10MHz	–	–	4	–	–	6	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4mA	–	–	0.4	–	–	0.4	V

NOTES:
1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 60 + 4(f-10)mA, where f = operating frequency in MHz; for the military range, I_{CC} = 80 + 6(f-10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

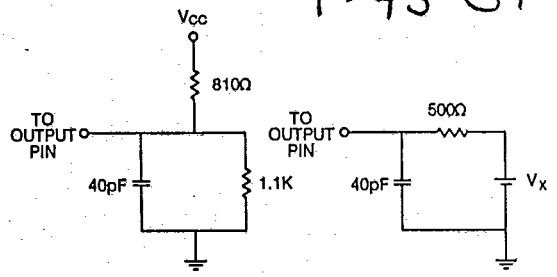
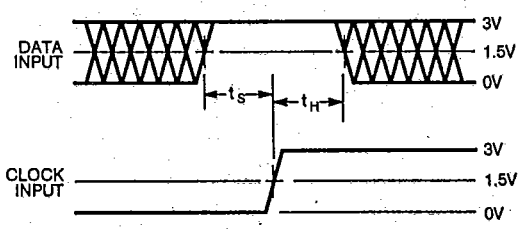
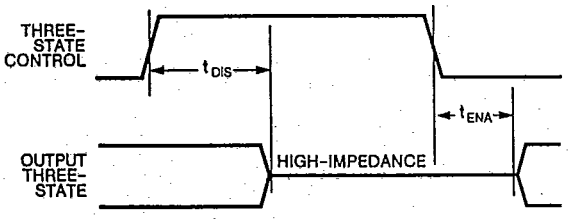


Figure 1. AC Output Test Load

Figure 2. Output Three-State Delay Load (V_X = 0V or 2.6V)





NOTE:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.

Figure 3. Set-Up And Hold Time

Figure 4. Three-State Control Timing Diagram

AC ELECTRICAL CHARACTERISTICS COMMERCIAL[3] (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7216L20/25 7217L20/25 MIN.	MAX.	7216L35/45 7217L35/45 MIN.	MAX.	7216L55/65 7217L55/65 MIN.	MAX.	7216L75/90 7217L75/90 MIN.	MAX.	7216L140 7217L140 MIN.	MAX.	UNIT
t_{MUC}	Unclocked Multiply Time	–	30/38	–	55/65	–	75/85	–	100/125	–	180	ns
t_{MC}	Clocked Multiply Time	–	20/25	–	35/45	–	55/65	–	75/90	–	140	ns
t_S	X, Y, RND Set-up Time	10/12	–	12/15	–	20	–	25	–	25	–	ns
t_H	X, Y, RND Hold Time	0/2	–	3	–	3	–	2/0	–	0	–	ns
t_{PWH}	Clock Pulse Width High	9/10	–	10/15	–	15	–	20	–	25	–	ns
t_{PWL}	Clock Pulse Width Low	9/10	–	10/15	–	20	–	20	–	25	–	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	–	18/20	–	25	–	25/30	–	30/35	–	40	ns
t_{PDP}	Output Clock to P	–	18/20	–	25	–	30	–	35	–	40	ns
t_{PDY}	Output Clock to Y	–	18/20	–	25	–	30	–	35	–	40	ns
t_{ENA}	3-State Enable Time[2]	–	18/20	–	25	–	30/35	–	35	–	40	ns
t_{DIS}	3-State Disable Time[2]	–	15/18	–	22	–	25	–	30	–	40	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	–	10	–	10	–	25	–	25	–	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0/2	–	3	–	3	–	3	–	3	–	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1]	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured +500mV from steady state voltage with loading specified in Figure 2.
3. For test load, see Figure 1.

AC ELECTRICAL CHARACTERISTICS MILITARY [3] (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	7216L25/30 7217L25/30 MIN.	MAX.	7216L40/55 7217L40/55 MIN.	MAX.	7216L65/75 7217L65/75 MIN.	MAX.	7216L90/120 7217L90/120 MIN.	MAX.	7216L185 7217L185 MIN.	MAX.	UNIT
t_{MUC}	Unclocked Multiply Time	–	38/43	–	60/75	–	85/95	–	125/160	–	230	ns
t_{MC}	Clocked Multiply Time	–	25/30	–	40/55	–	65/75	–	90/120	–	185	ns
t_S	X, Y, RND Set-up Time	12	–	15/20	–	25	–	30	–	30	–	ns
t_H	X, Y, RND Hold Time	2	–	3	–	3	–	2/0	–	0	–	ns
t_{PWH}	Clock Pulse Width High	10	–	15	–	15	–	25/30	–	30	–	ns
t_{PWL}	Clock Pulse Width Low	10	–	15	–	15	–	25/30	–	30	–	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	–	20	–	25/30	–	35	–	40	–	45	ns
t_{PDP}	Output Clock to P	–	20	–	25/30	–	30/35	–	40	–	45	ns
t_{PDY}	Output Clock to Y	–	20	–	25/30	–	30/35	–	40	–	45	ns
t_{ENA}	3-State Enable Time [2]	–	20	–	25	–	35/40	–	40	–	45	ns
t_{DIS}	3-State Disable Time [2]	–	18	–	25	–	25	–	40	–	45	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	–	12/15	–	15	–	30	–	30	–	ns
t_H	Clock Enable Hold Time (IDT7217 only)	2	–	3	–	3	–	3	–	3	–	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only) [1]	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured +500mV from steady state voltage with loading specified in Figure 2.
3. For test load, see Figure 1.

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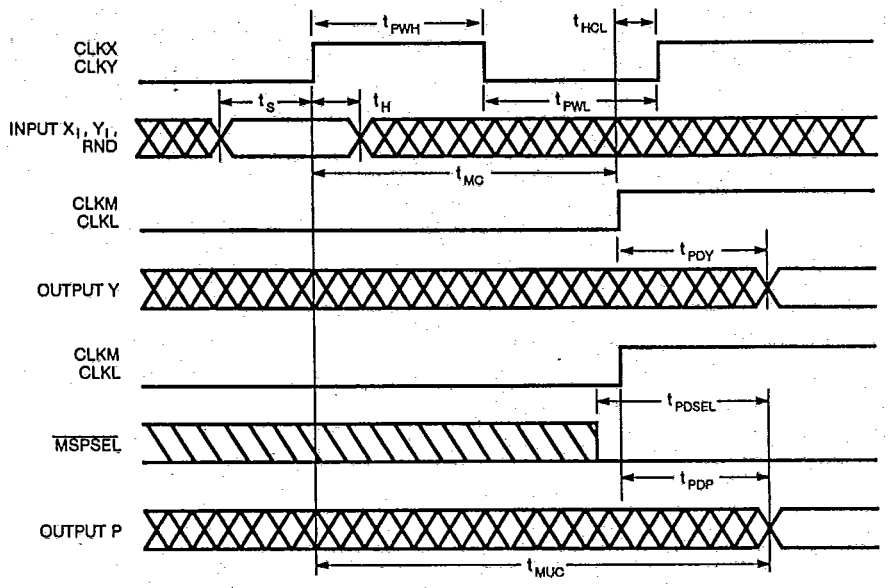

Figure 5. IDT7216 Timing Diagram

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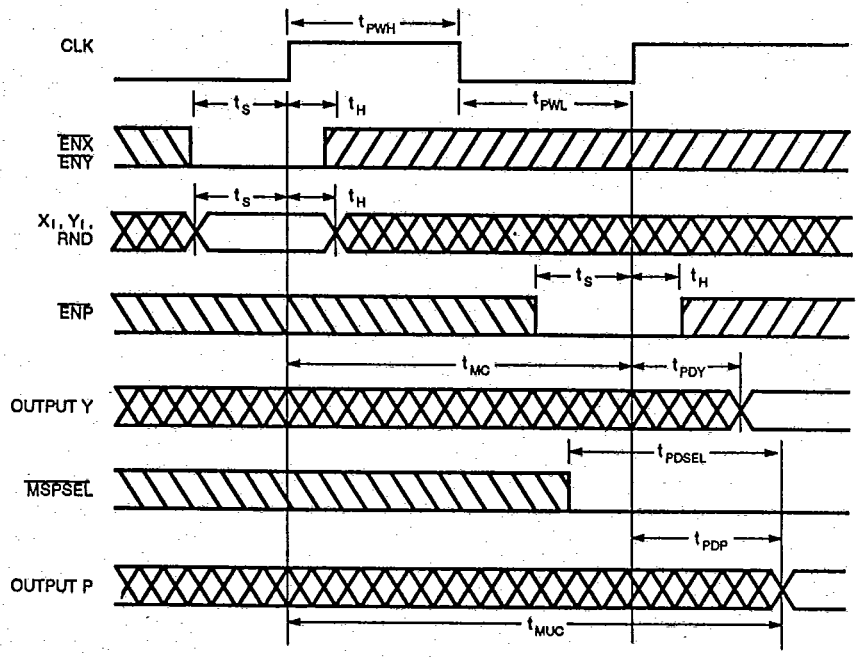

Figure 6. IDT7217 Timing Diagram

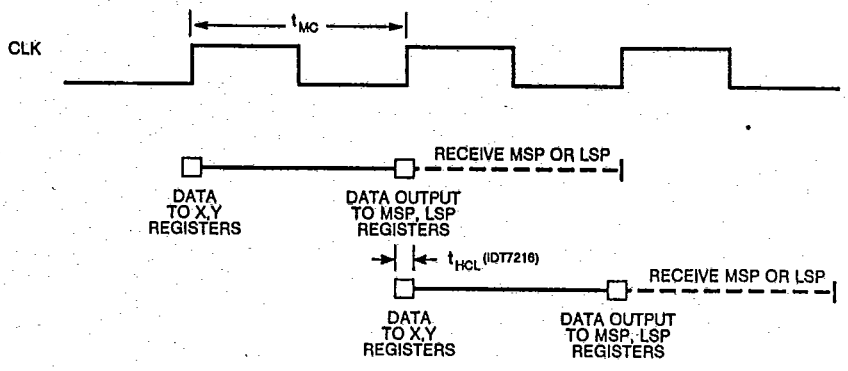

Figure 7. Simplified Timing Diagram–Typical Application

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SIGNAL DESCRIPTIONS

INPUTS:

X_{IN} (X_{15} through X_0)
Sixteen Multiplicand Data Inputs.

Y_{IN} (Y_{15} through Y_0)
Sixteen Multiplier Data Inputs. (This is also an output port for P_{15-0}.)

INPUT CLOCKS (IDT7216 ONLY)

CLKX
The rising edge of this clock loads the X_{15-0} data input register along with the X mode and round registers.

CLKY
The rising edge of this clock loads the Y_{15-0} data input register along with the Y mode and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7217 ONLY)

CLK
The rising edge of this clock loads all registers.

$\overline{ENX}$
Register enable for the X_{15-0} data input register along with the X mode and round registers.

$\overline{ENY}$
Register enable for the Y_{15-0} data input register along with the Y mode and round registers.

$\overline{ENP}$
Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS

X_M, Y_M (TCX, TCY)[1]
Mode control inputs for each data word. A LOW input designates unsigned data input and a HIGH input designates two's complement.

FA (RS)[1]
When the format adjust control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications (see Multiplier Input/Output Formats).

FT
When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are transparent.

$\overline{OEL}$
Three-state enable for routing LSP through Y_{IN} /LSP_{OUT} port.

$\overline{OEP}$
Three-state enable for the product output port.

RND
Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the format adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the 2^{-16} bit (P_{14}). If FA is HIGH when RND is HIGH, a one will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MSPSEL}$
When the $\overline{MSPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

OUTPUTS

MSP (P_{31} through P_{16})
Most Significant Product output.

LSP (P_{15} through P_0)
Least Significant Product output.

Y_{15-0} /LSP_{OUT} (Y_{15} through Y_0 or P_{15} through P_0)
Least Significant Product (LSP) Output available when $\overline{OEL}$ is LOW. This is also an output port for Y_{15-0}.

NOTE:
1. TRW MPY016H/K pin designation.

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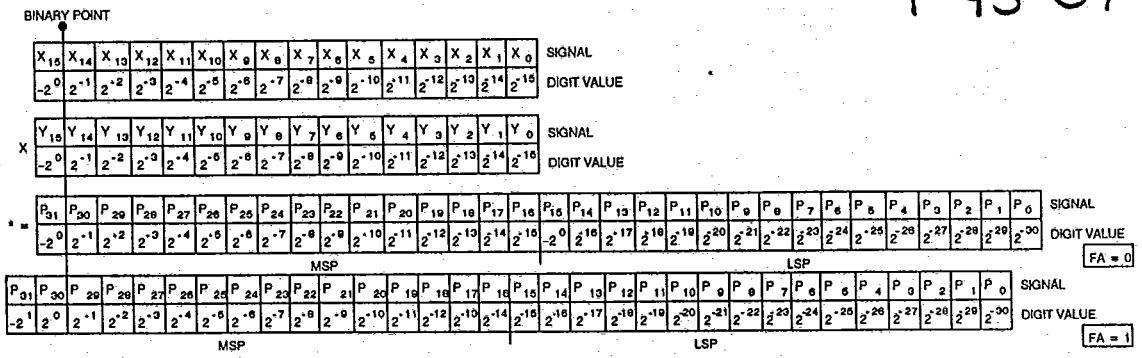

Figure 8. Fractional Two's Complement Notation

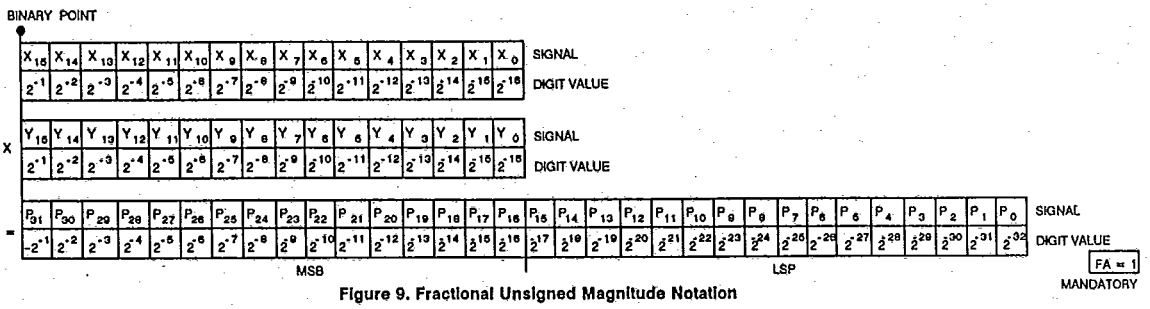

Figure 9. Fractional Unsigned Magnitude Notation

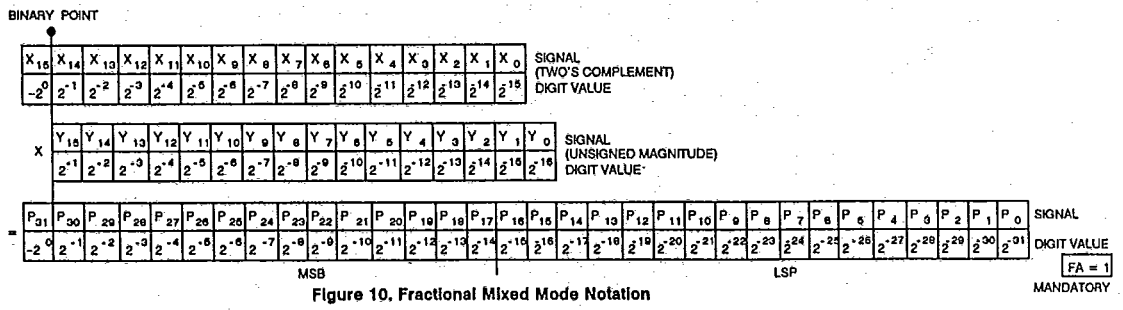

Figure 10. Fractional Mixed Mode Notation

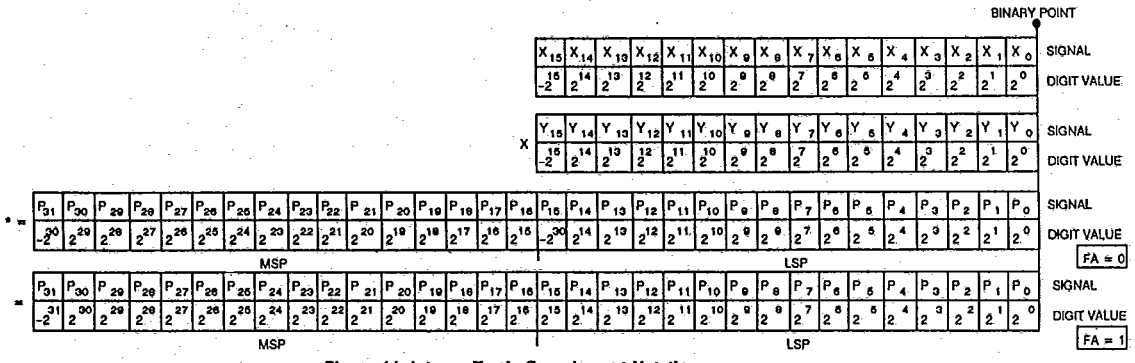

Figure 11. Integer Two's Complement Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000.0 yielding an erroneous product of −1 in the fraction case and -2^{30} in the integer case.

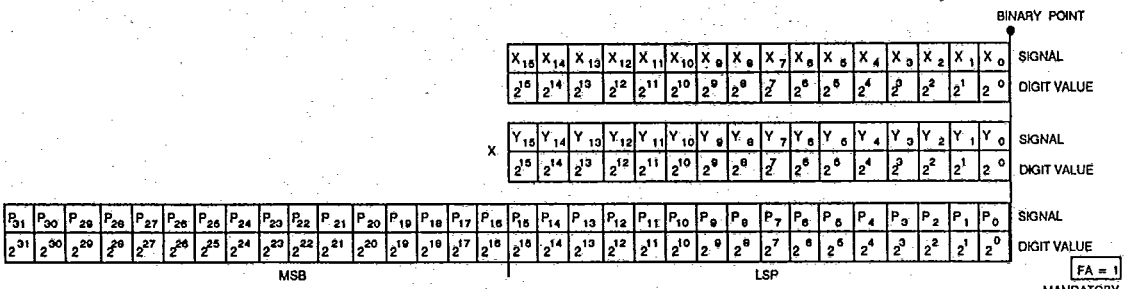

Figure 12. Integer Unsigned Magnitude Notation

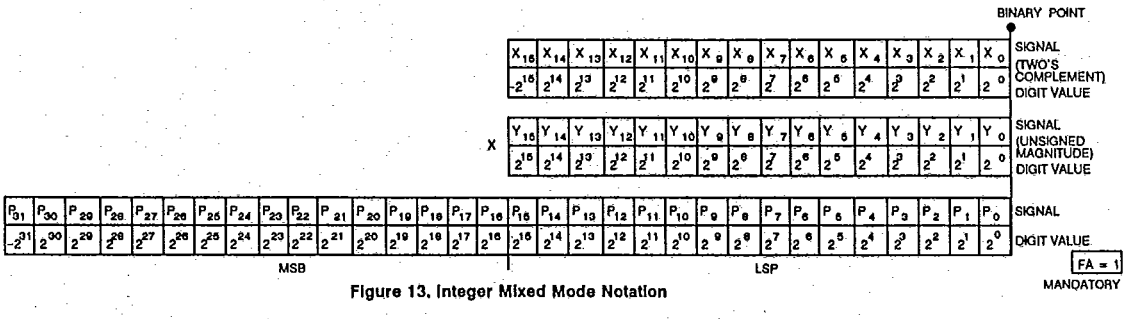

Figure 13. Integer Mixed Mode Notation

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ORDERING INFORMATION