DATA SHEET

HM 65772

4 k x 4
HIGH SPEED CMOS SRAM
SEPARATE I/O

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FEATURES

- **FAST ACCESS TIME**
  MILITARY : 25/35/45 ns (max)
  COMMERCIAL : 20/25/35/45 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 385 mW (max)
  STANDBY : 27.5 mW (max)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**
- **SEPARATE INPUT/OUTPUT**

DESCRIPTION

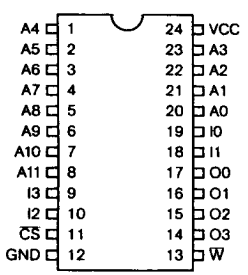
The HM 65772 is a high speed CMOS static RAM organized as 4096 x 4 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 385 mW.
The HM 65772 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 10 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$), four separate input/output buffers and three state drivers.
All inputs and outputs of the HM 65772 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65772 is processed following the test methods of MIL STD 883C.

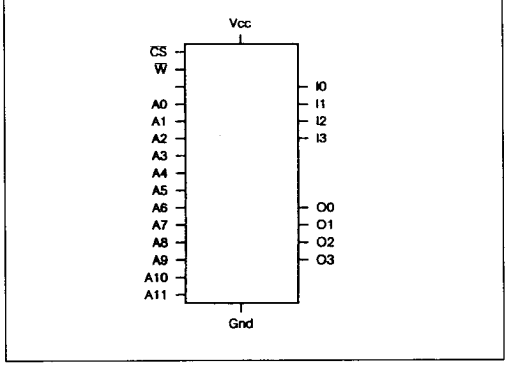
PACKAGES

Plastic 300 mils, 24 pins, DIL.
Ceramic 300 mils, 24 pins, DIL.
SO 300 mils, 24 pins, DIL.
L = low, H = high, X = H

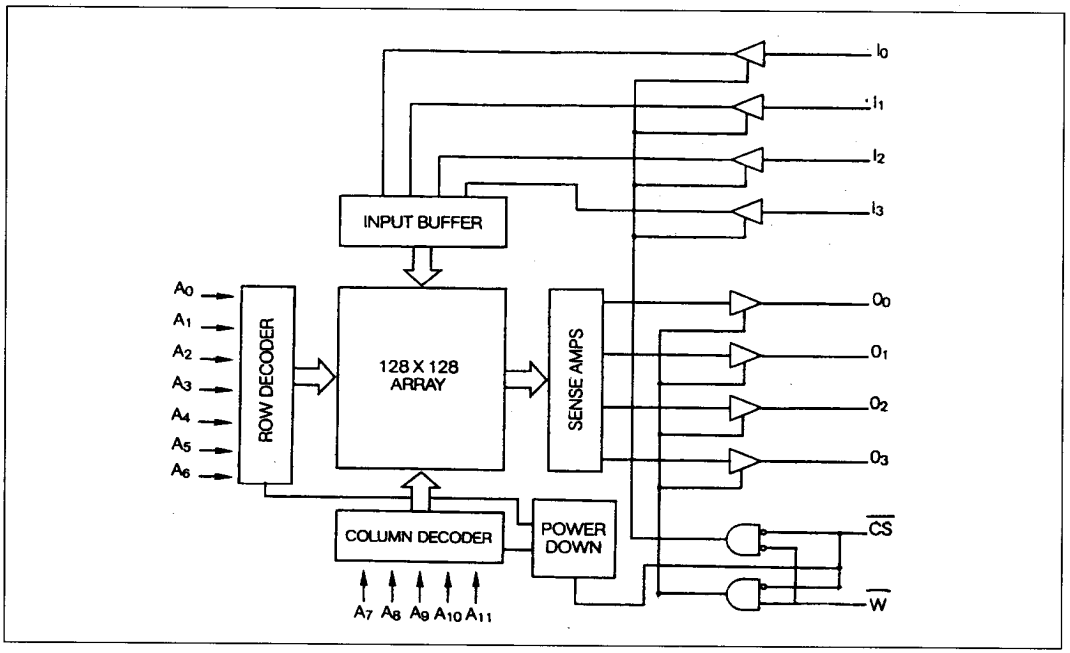
Pinout DIL 24 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A11	: Address inputs	$\overline{CS}$	: Chip Select
I0–I3	: Inputs	VCC	: Power
O0–O3	: Outputs	GND	: Ground
$\overline{W}$	: Write enable		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

or L, Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

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CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	4	pF
Cout	(1)	Output Capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

AC TEST LOADS WAVEFORMS

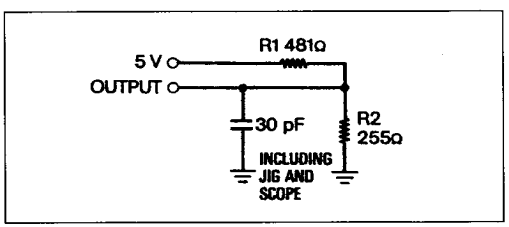


Fig. 1a.

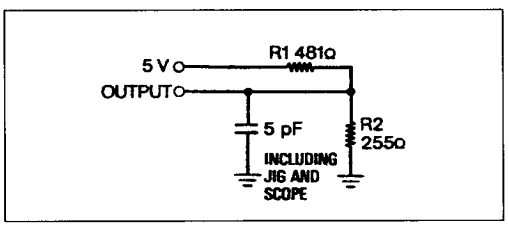
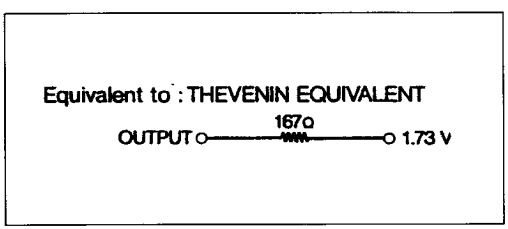


Fig. 1b.



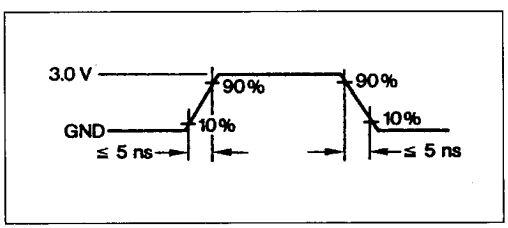


Fig. 2.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	– 10.0	–	10.0	µA
IOZ (3)	Output leakage current	– 15.0	–	10.0	µA
IOS (3)	Output short circuit current	–	–	– 350.0	mA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output High voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

Consumption for Commercial specification :

SYMBOL	PARAMETER	65772 F-5	65772 H-5	65772 K-5	65772 M-5	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	20	mA	max
ICCOP (7)	Operating supply current	80	70	70	70	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65772 H-2	65772 K-2	65772 M-2	UNIT	VALUE
ICCSB (6)	Standby supply current	20	20	20	mA	max
ICCOP (7)	Operating supply current	90	90	90	mA	max

Notes : 6. $\overline{CS} \geq$ VIH, a pull up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values given.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels :1.5 V
Output loading IOL/IOH (see figure 1a and 1b) : + 30 pF

WRITE CYCLE : Commercial specification

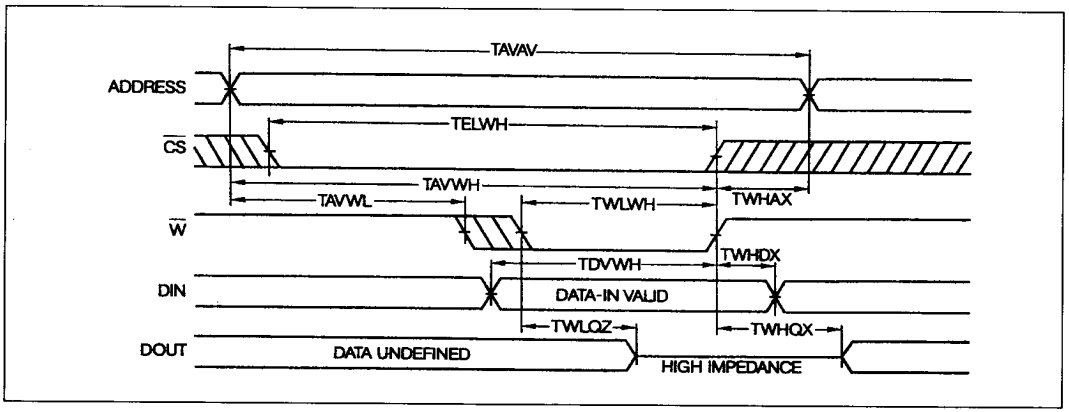
SYMBOL	PARAMETER	65772 F-5	65772 H-5	65772 K-5	65772 M-5	UNIT	VALUE
TAVAV	Write Cycle time	20	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	15	20	30	40	ns	min
TDVWH	Data set-up time	10	15	15	20	ns	min
TELWH	$\overline{CS}$ low to write end	15	20	30	40	ns	min
TWLQZ (8)	Write low to high Z	10	10	15	20	ns	max
TWLWH	Write pulse width	15	20	30	40	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWDHX	Data hold time	0	0	0	3	ns	min
TWHQX (8)	Write high to low Z	3	6	6	6	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65772 H-2	65772 K-2	65772 M-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	45	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	25	30	40	ns	min
TDVWH	Data set-up time	20	20	20	ns	min
TELWH	$\overline{CS}$ low to write end	25	30	40	ns	min
TWLQZ (8)	Write low to high Z	10	15	20	ns	max
TWLWH	Write pulse width	20	30	40	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWDHX	Data hold time	0	0	3	ns	min
TWHQX (8)	Write high to low Z	6	6	6	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 10)



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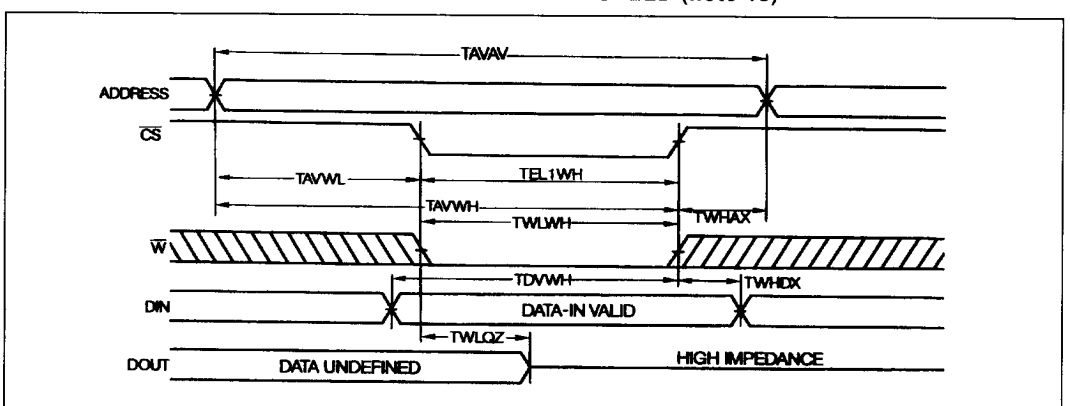
WRITE CYCLE 2 $\overline{CS}$ CONTROLLED (note 10)



Note : 10. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65772 F-5	65772 H-5	65772 K-5	65772 M-5	UNIT	VALUE
TAVAV	READ Cycle time	20	25	35	45	ns	min
TAVQV	Address access time	20	25	35	45	ns	min
TAVQX	Address valid to low Z	2	3	3	3	ns	min
TELQV	Chip-select access time	20	15	25	30	ns	min
TELQX	$\overline{CS}$ low to low Z	3	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	25	30	ns	max

READ CYCLE : Military specification

SYMBOL	PARAMETER	65772 H-2	65772 K-2	65772 M-2	UNIT	VALUE
TAVAV	Write Cycle time	25	35	45	ns	min
TAVQV	Address access time	25	35	45	ns	min
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	25	35	45	ns	min
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	20	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	25	25	30	ns	max

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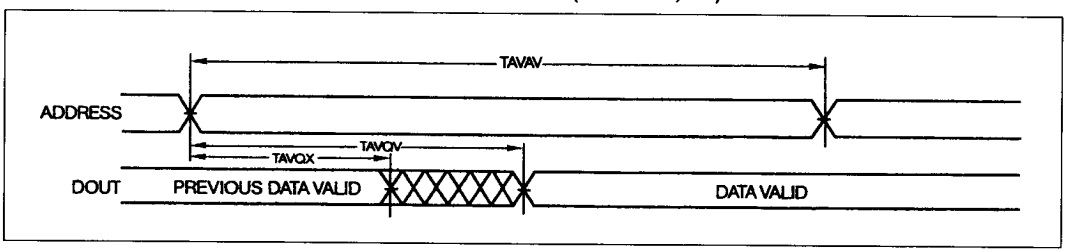
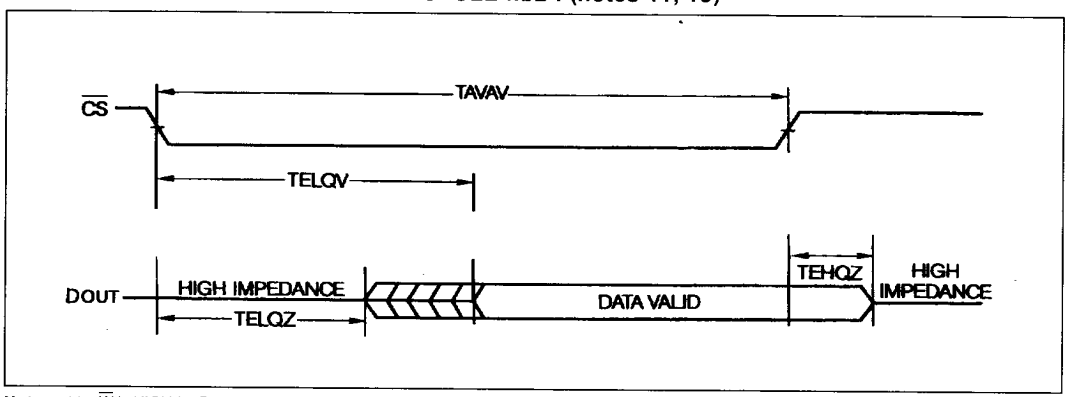
READ CYCLE nb1 : (notes 11, 12)



READ CYCLE nb2 : (notes 11, 13)



Note : 11. $\overline{W}$ is HIGH for Read cycle.
Notes : 12. Device is continuously selected, $\overline{CS}$ = VIL.
13. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

ORDERING INFORMATION

Package	Device	Grade	Level
HM1	65772	K	– 5
0 - Chip form 1 - Ceramic 28 pins 3 - Plastic 28 pins T - SOIC 24 pins	4 k x 4 high speed static RAM with separate I/O	F = 20 ns H = 25 ns K = 35 ns M = 45 ns	– 5 : Commercial – 5+ : Commercial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 24 pins : 043
Ceramic DIL, 300 mils, 24 pins : C25
SOIC DIL, 300 mils, 24 pins : TBD.