



**ELAN MICROELECTRONICS CORPORATION**

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# **EM78567/566/565**

**8-BIT MICRO-CONTROLLER**

Version 1.2

ELAN MICROELECTRONICS CORP.  
No. 12, Innovation 1<sup>st</sup> RD., Science-Based Industrial Park  
Hsin Chu City, Taiwan, R.O.C.  
TEL: (03) 5639977  
FAX: (03)5782037 (SL) 5780617 (SA2)

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## User Application Note

### 1. ROM, OTP, ICE

| ROM             | OTP      | ICE    |
|-----------------|----------|--------|
| EM78567/566/565 | EM78P567 | ICE567 |

### 2. Main Function Difference

|                   | EM78567/566/565 | EM78P567    |
|-------------------|-----------------|-------------|
| Operation voltage | 2.5V ~ 5.5V     | 2.5V ~ 5.5V |
| A/D, D/A          | Built-in        | Built-in    |

### 3. POVD voltage difference

|              | EM78567/566/565 | EM78P567 |
|--------------|-----------------|----------|
| POVD voltage | 2.0V            | 2.2V     |

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## I. General Description

The EM78567/566/565 is an 8-bit RISC type microprocessor with low power , high speed CMOS technology . There are 16Kx13/8Kx13/4Kx13 bits ROM within it.

The EM78567/566/565 is integrated onto a single chip are on\_chip watchdog (WDT) , RAM , A/D , D/A , tone generator, programmable real time clock /counter , internal interrupt , power down mode and tri-state I/O .

## II. Feature

### CPU

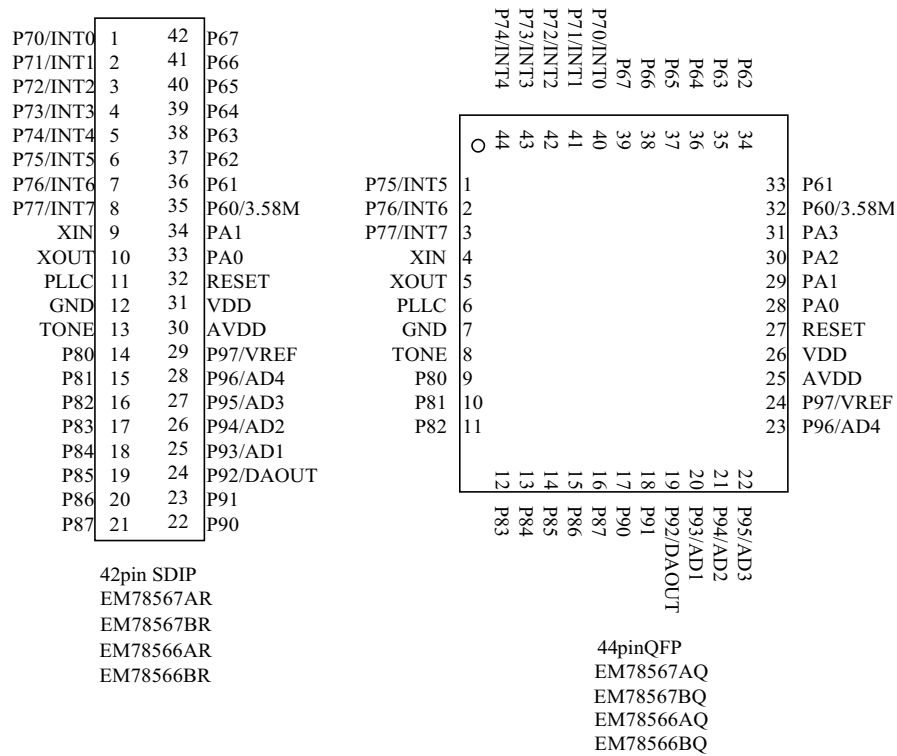
- Operating voltage range : 2.5V ~ 5.5V
- 16Kx13 Read Only Memory (EM78567)
- 8Kx13 Read Only Memory (EM78566)
- 4Kx13 Read Only Memory (EM78565)
- 0.5Kx8 on chip RAM
- Up to 36 bi-directional tri-state I/O ports (EM78567, EM78566)
- Up to 24 bi-directional tri-state I/O ports (EM78565)
- 8 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- A 8 bit counters (COUNTER1) with a 8 bit prescaler which can be a interrupt source.
- A 8 bit counters (COUNTER2) with a 8 bit prescaler which can be a interrupt source.
- Selective signal sources and with overflow interrupt
- Programmable free running on chip watchdog timer
- 99.9% single instruction cycle commands
- Four modes (internal clock 3.58MHz, external clock 32.768KHz)
  1. Sleep mode : CPU and 3.58MHz clock turn off, 32.768KHz clock turn off
  2. IDLE mode : CPU and 3.58MHz clock turn off, 32.768KHz clock turn on
  3. Green mode : 3.58MHz clock turn off, CPU and 32.768KHz clock turn on
  4. Normal mode : 3.58MHz clock turn on , CPU and 32.768KHz clock turn on
- Four open drain ports
- Input port interrupt function
  - Four channels A/D circuit with 8 bits resolution.
  - I/O internal pull high
- 12 interrupt source , 8 external , 4 internal
- Dual clocks operation (Internal PLL 3.58MHz , External 32.768KHz)
- 28 pin SOP(EM78565AM, POVD disable) (EM78565BM, POVD enable) or Chip (EM78565H)
- 32 pin SOP(EM78565AWM, POVD disable)(EM78565BWM, POVD enable) or Chip (EM78565H)
- 42 pin SDIP (EM78566AR, POVD disable) (EM78566BR, POVD enable) or Chip (EM78566H)
- 42 pin SDIP (EM78567AR, POVD disable) (EM78567BR, POVD enable) or Chip (EM78567H)
- 44 pin QFP (EM78566AQ, POVD disable) (EM78566BQ, POVD enable) or Chip (EM78566H)
- 44 pin QFP (EM78567AQ, POVD disable) (EM78567BQ, POVD enable) or Chip (EM78567H)
- 48 pin SSOP(EM78566AM, POVD disable) (EM78566BM, POVD enable) or Chip (EM78566H)
- 48 pin SSOP(EM78567AM, POVD disable) (EM78567BM, POVD enable) or Chip (EM78567H)
- Build in 8-bit D/A converter (R-2R)
- Dual Tone generators
- 3.58MHz clock output shared with IO PORT



### III. Application

1. adjunct units
2. answering machines
3. feature phones
4. cordless phones

### IV. Pin Configuration



\* This specification are subject to be changed without notice.



|           |    |    |           |
|-----------|----|----|-----------|
| P70/INT0  | 1  | 32 | P67       |
| P71/INT1  | 2  | 31 | P66       |
| P72/INT2  | 3  | 30 | P65       |
| P73/INT3  | 4  | 29 | P64       |
| P74/INT4  | 5  | 28 | P63       |
| P75/INT5  | 6  | 27 | P62       |
| P76/INT6  | 7  | 26 | P61       |
| P77/INT7  | 8  | 25 | P60/3.58M |
| XIN       | 9  | 24 | RESET     |
| XOUT      | 10 | 23 | VDD       |
| PLL       | 11 | 22 | AVDD      |
| GND       | 12 | 21 | P97/VREF  |
| TONE      | 13 | 20 | P96/AD4   |
| P90       | 14 | 19 | P95/AD3   |
| P91       | 15 | 18 | P94/AD2   |
| P92/DAOUT | 16 | 17 | P93/AD1   |

32 pin SOP  
EM78565AWM  
EM78565BWM

|           |    |    |           |
|-----------|----|----|-----------|
| P67       | 1  | 28 | P66       |
| P73/INT3  | 2  | 27 | P65       |
| P74/INT4  | 3  | 26 | P64       |
| P75/INT5  | 4  | 25 | P63       |
| P76/INT6  | 5  | 24 | P62       |
| P77/INT7  | 6  | 23 | P61       |
| XIN       | 7  | 22 | P60/3.58M |
| XOUT      | 8  | 21 | RESET     |
| PLL       | 9  | 20 | AVDD,VDD  |
| GND       | 10 | 19 | P97/VREF  |
| TONE      | 11 | 18 | P96/AD4   |
| P90       | 12 | 17 | P95/AD3   |
| P91       | 13 | 16 | P94/AD2   |
| P92/DAOUT | 14 | 15 | P93/AD1   |

28 pin SOP  
EM78565AM  
EM78565BM

Fig1. Pin Assignment

### V.Functional Block Diagram

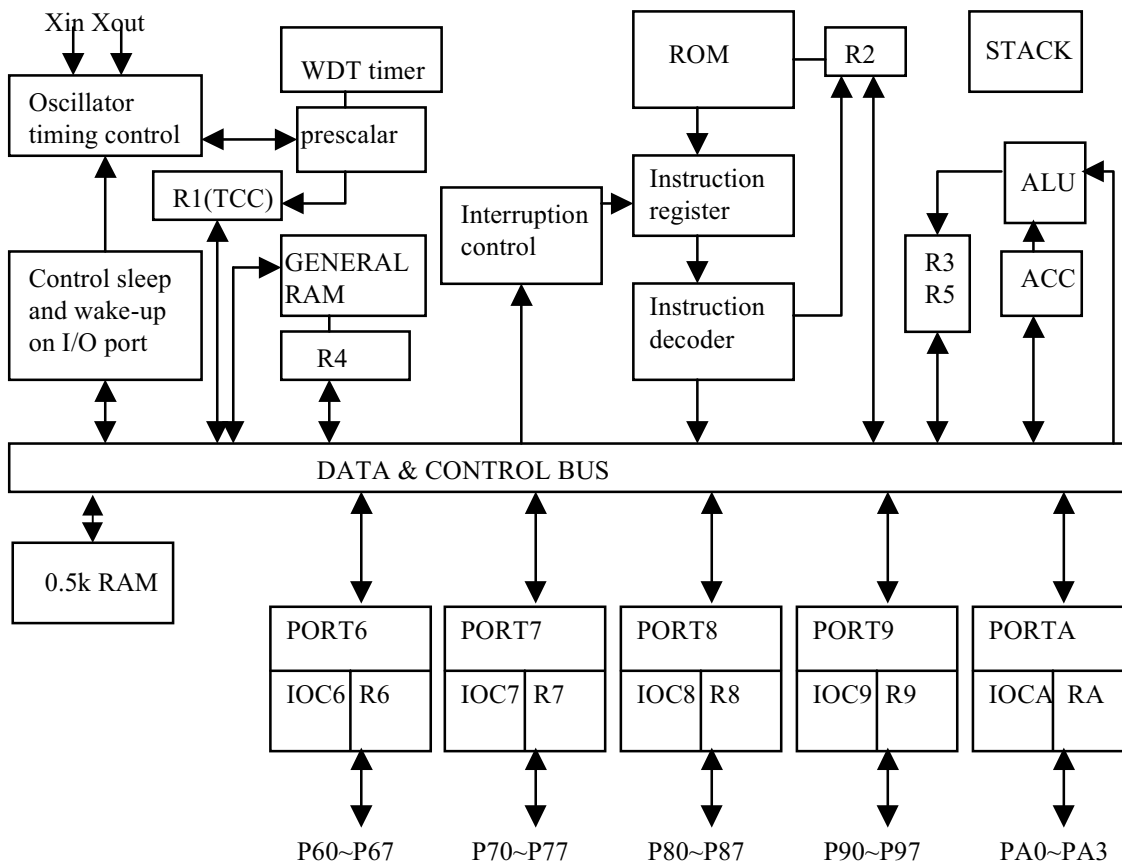


Fig2. Block diagram



## VI.Pin Descriptions

| PIN        | I/O      | DESCRIPTION  |
|------------|----------|--|
| VDD        | POWER    | Digital power  |
| AVDD       |          | Analog power   |
| GND        | POWER    | Ground   |
| Xin        | I        | Input pin for 32.768 kHz oscillator  |
| Xout       | O        | Output pin for 32.768 kHz oscillator   |
| PLLC       | I        | Phase loop lock capacitor, connect a capacitor 0.01u to 0.047u with GND .  |
| INT0       | PORT7(0) | External interrupt   |
| INT1       | PORT7(1) |  |
| INT2       | PORT7(2) |  |
| INT3       | PORT7(3) |  |
| INT4       | PORT7(4) |  |
| INT5       | PORT7(5) |  |
| INT6       | PORT7(6) |  |
| INT7       | PORT7(7) |  |
| P7.0 ~P7.7 | PORT7    | PORT 7 can be INPUT or OUTPUT port each bit. Internal Pull high function.  |
| P6.0 ~P6.7 | PORT6    | PORT 6 can be INPUT or OUTPUT port each bit. Internal Pull high function.  |
| P8.0 ~P8.7 | PORT8    | PORT 8 can be INPUT or OUTPUT port each bit.   |
| P9.0 ~P9.7 | PORT9    | PORT 9 can be INPUT or OUTPUT port each bit. P90 to P93 have Open drain function.                                  |
| VREF       | PORT9(7) | Reference voltage input of AD converter-circuit . User use internal reference voltage. This pin is normal IO PORT. |
| AD1        | PORT9(3) | The first input of A/D converter.  |
| AD2        | PORT9(4) | The second input of A/D converter.   |
| AD3        | PORT9(5) | The third input of A/D converter.  |
| AD4        | PORT9(6) | The fourth input of A/D converter.   |
| DAOUT      | PORT9(2) | DA signal output   |
| PA.0 ~PA.3 | PORTA    | PORTA can be INPUT or OUTPUT port each bit.  |
| TONE       | O        | Dual Tone generator output   |
| RESET      | I        | Normally high  |
| 3.58M      | PORT6(0) | 3.58MHz clock output shared with PORT6(0)  |

## VII.Functional Descriptions

### VII.1 Operational Registers

#### 1. R0 (Indirect Addressing Register)

\* R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

#### 2. R1 (TCC)

\* Increased by an external signal edge applied to TCC , or by the instruction cycle clock.

Written and read by the program as any other register.

#### 3. R2 (Program Counter)

\* The structure is depicted in Fig. 3.

\* Generates 16K × 13 on-chip ROM addresses to the relative programming instruction codes.

\* This specification are subject to be changed without notice.

- \* "JMP" instruction allows the direct loading of the low 10 program counter bits.
- \* "CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.
- \* "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.
- \* "MOV R2,A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".
- \* "ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".
- \* "TBL" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change. The most significant bit (A10~A13) will be loaded with the content of bit PS0~PS3 in the status register (R5) upon the execution of a "JMP", "CALL", "ADD R2,A", or "MOV R2,A" instruction.

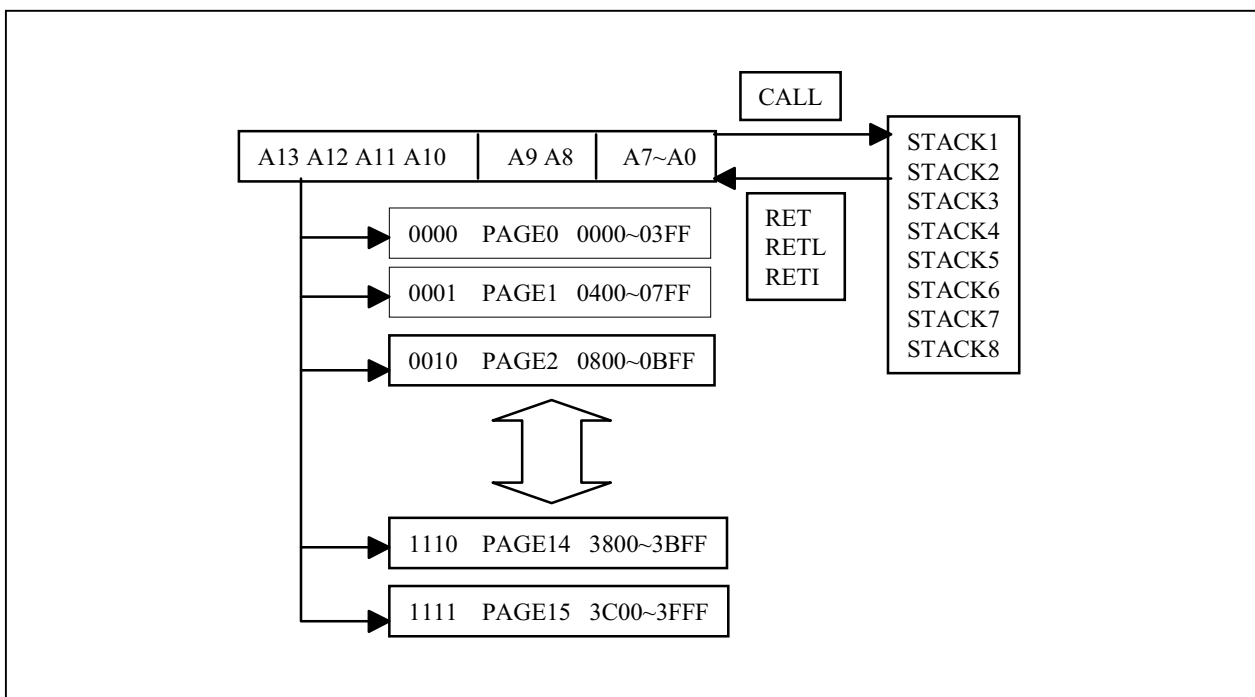


Fig.3 Program counter organization



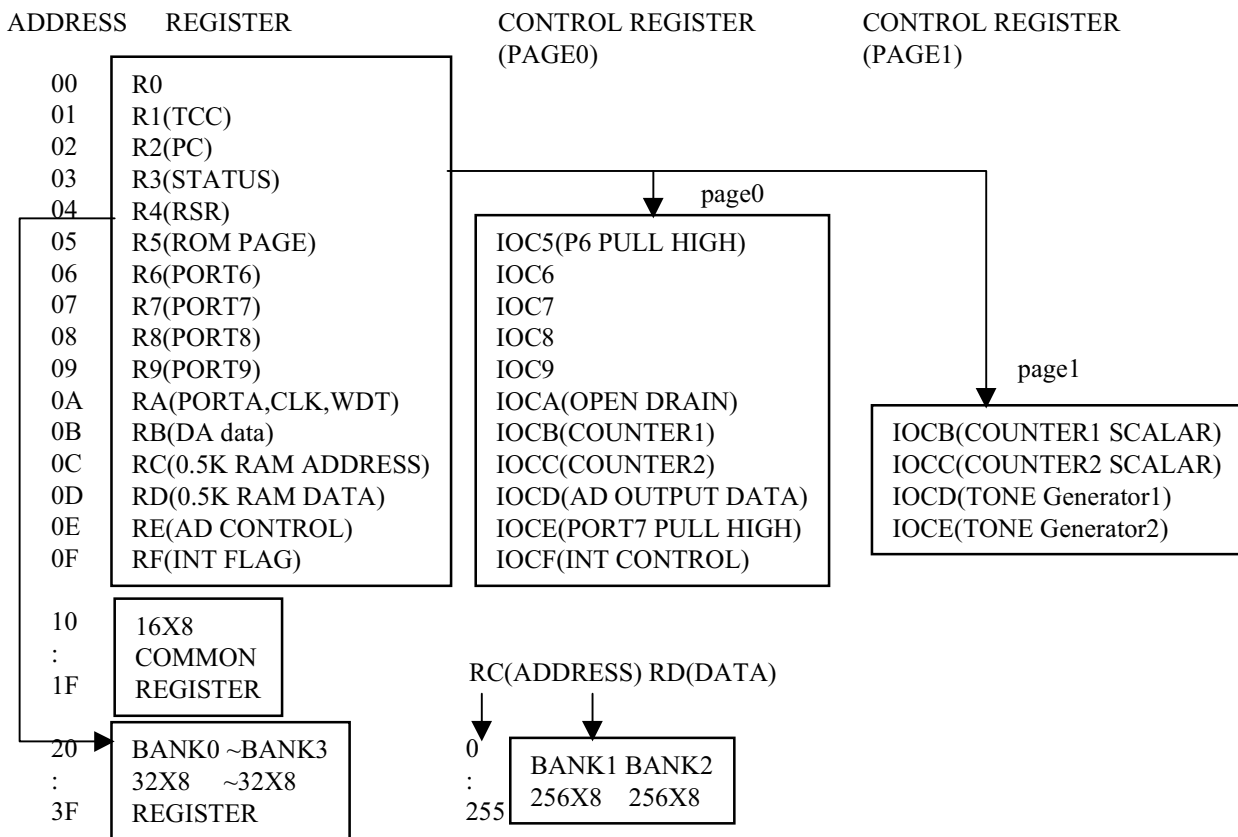


Fig.4 Data memory configuration

4. R3 (Status Register)

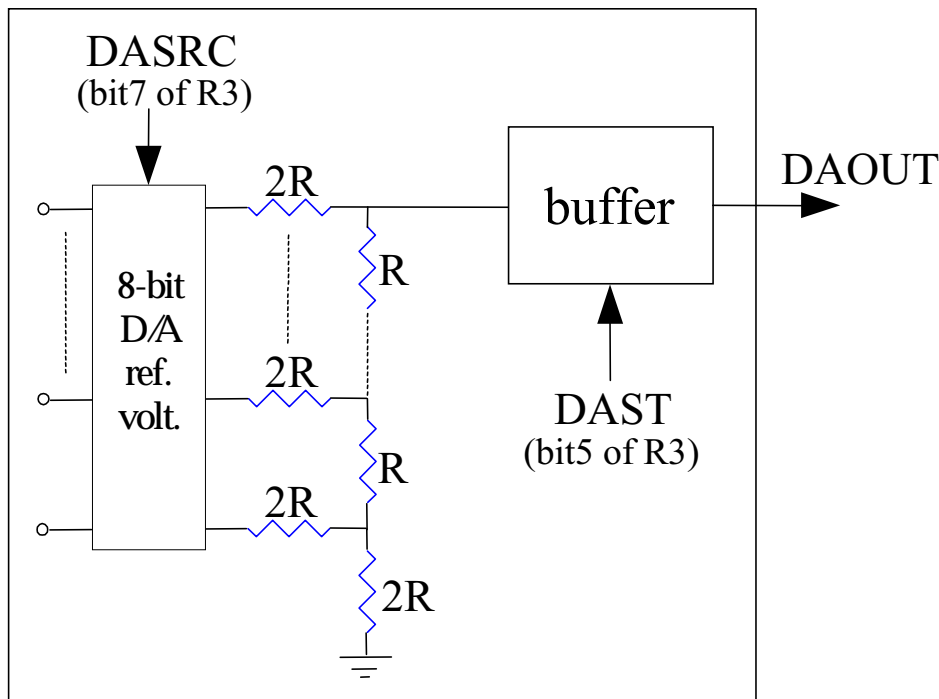
|       |      |      |   |   |   |    |   |
|-------|------|------|---|---|---|----|---|
| 7     | 6    | 5    | 4 | 3 | 2 | 1  | 0 |
| DASRC | PAGE | DAST | T | P | Z | DC | C |

- \* Bit 0 (C) Carry flag
- \* Bit 1 (DC) Auxiliary carry flag
- \* Bit 2 (Z) Zero flag
- \* Bit 3 (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- \* Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

| EVENT                         | T | P | REMARK |
|-------------------------------|---|---|--------|
| WDT wake up from sleep mode   | 0 | 0 |        |
| WDT time out (not sleep mode) | 0 | 1 |        |
| /RESET wake up from sleep     | 1 | 0 |        |
| power up                      | 1 | 1 |        |

- \* Bit 5 (DAST) DA START signal. When R3 bit5 is set by software in NORMAL mode . The DA converter start converting. If user clean this bit , DA converter will stop. DAOUT pin send DA signal. 0/1= STOP/START

- \* Bit 6 PAGE : change IOCB ~ IOCC to another page , 0/1 => page0 / page1
- \* Bit 7 (DASRC) DA convert circuit 's reference voltage. 0/1 =>VDD/2.55V



#### 5. R4 (RAM Select Register)

- \* Bits 0 ~ 5 are used to select up to 64 registers in the indirect addressing mode.
- \* Bits 6 ~ 7 determine which bank is activated among the 4 banks.
- \* See the configuration of the data memory in Fig. 4.

#### 6. R5 (Program Page Select Register)

|        |        |         |         |     |     |     |     |
|--------|--------|---------|---------|-----|-----|-----|-----|
| 7      | 6      | 5       | 4       | 3   | 2   | 1   | 0   |
| ADCLK1 | ADCLK0 | P_TONE2 | P_TONE1 | PS3 | PS2 | PS1 | PS0 |

\* Bit 0 (PS0) ~ 3 (PS3) Page select bits

Page select bits

| PS3 | PS2 | PS1 | PS0 | Program memory page (Address) |
|-----|-----|-----|-----|-------------------------------|
| 0   | 0   | 0   | 0   | Page 0                        |
| 0   | 0   | 0   | 1   | Page 1                        |
| 0   | 0   | 1   | 0   | Page 2                        |
| 0   | 0   | 1   | 1   | Page 3                        |
| 0   | 1   | 0   | 0   | Page 4                        |
| 0   | 1   | 0   | 1   | Page 5                        |
| 0   | 1   | 1   | 0   | Page 6                        |
| 0   | 1   | 1   | 1   | Page 7                        |
| 1   | 0   | 0   | 0   | Page 8                        |
| 1   | 0   | 0   | 1   | Page 9                        |
| 1   | 0   | 1   | 0   | Page 10                       |



|   |   |   |   |         |
|---|---|---|---|---------|
| 1 | 0 | 1 | 1 | Page 11 |
| 1 | 1 | 0 | 0 | Page 12 |
| 1 | 1 | 0 | 1 | Page 13 |
| 1 | 1 | 1 | 0 | Page 14 |
| 1 | 1 | 1 | 1 | Page 15 |

\*User can use PAGE instruction to change page. To maintain program page by user. Otherwise, user can use far jump (FJMP) or far call (FCALL) instructions to program user's code. And the program page is maintained by EMC's compiler. It will change user's program by inserting instructions within program.

**\*Bit4: Power control bit of Tone generator 1 . User can use this bit to power on the tone generator.**

**\*Bit5: Power control bit of Tone generator 2 . User can use this bit to power on the tone generator.**

| R5(5,4) | Tone generator2 | Tone generator1 |
|---------|-----------------|-----------------|
| 00      | Power off       | Power off       |
| 01      | Power off       | Power on        |
| 10      | Power on        | Power off       |
| 11      | Power on        | Power on        |

\*Bit 6~7: AD circuit 's sampling clock source.

| ADCLK1 | ADCLK0 | Sampling rate | Operation voltage |
|--------|--------|---------------|-------------------|
| 0      | 0      | 44K           | >=3V              |
| 0      | 1      | 22K           | >=2.5V            |
| 1      | 0      | 11K           | >=2.5V            |
| 1      | 1      | 5.5K          | >=2.5V            |

#### 6. R6 ~ R9 (Port 6 ~ Port 9)

\* Five 8-bit I/O registers.

#### 7. RA (clock and RA register)

| 7    | 6     | 5     | 4    | 3   | 2   | 1   | 0   |
|------|-------|-------|------|-----|-----|-----|-----|
| IDLE | /358E | /WDTE | RAMS | PA3 | PA2 | PA1 | PA0 |

\* Bit0 ~ Bit3 : I/O register

\* Bit4 : (RC RD controlled General RAM selection bit)

0/1 = bank0/bank1.

\* Bit5: (/WDTE , Watch Dog Timer register)

This control bit used to enable Watchdog timer.

0/1=disable/enable

\* Bit6(PLL enable signal)

0/1=DISABLE(GREEN MODE) / ENABLE (NORMAL MODE)

The relation between 32.768K and 3.58M can see Fig5.

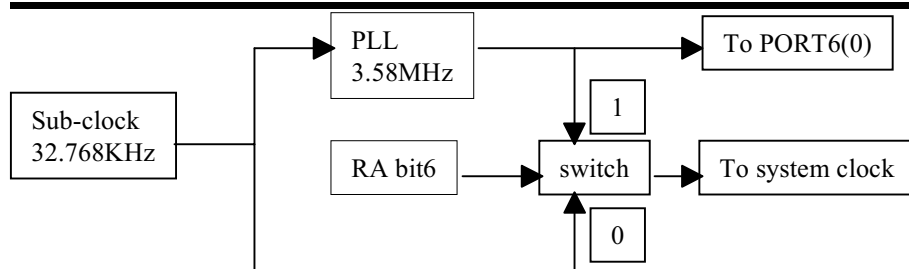


Fig5. The relation between 32.768KHz and 3.58MHz .

**\* Bit7 IDLE: sleep mode selection bit**

0/1=sleep mode/IDLE mode. This bit will decide SLEP instruction which mode to go.  
 Sub-clock and CPU will close in sleep mode. CUP will close in IDLE mode but sub-clock.

|              | SLEEP mode                       | IDLE mode                                    | GREEN mode                       | NORMAL mode                      |
|--------------|----------------------------------|--|----------------------------------|----------------------------------|
| Into         | RA(7,6)=(0,0)<br>+ SLEP          | RA(7,6)=(1,0)<br>+ SLEP                      | RA(7,6)=(x,0)<br>no SLEP         | RA(7,6)=(x,1)<br>no SLEP         |
| TCC time out | X                                | Wake-up<br>+ Interrupt<br>+ Next instruction | Interrupt                        | Interrupt                        |
| WDT time out | RESET<br>Run from<br>address "0" | X  | RESET<br>Run from<br>address "0" | RESET<br>Run from<br>address "0" |
| Port7 bit0   | X                                | Wake-up<br>+ Interrupt<br>+ Next instruction | Interrupt                        | Interrupt                        |

\*Port7 bit0 is a falling edge trigger port.

\*"X" is mean no function

**8. RB(DA data register)**

| 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|
| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |

\* **Bit 7 – Bit0 are DA converter data control register. Bit7 is MSB and bit0 is LSB.**

\* **Please set to NORMAL mode before DA converter start.**

\* **User can select reference voltage by R3 bit7. And enable or disable power of DA converter by R3 bit5.**

**9. RC (RAM ADDRESS)**

| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CIDA7 | CIDA6 | CIDA5 | CIDA4 | CIDA3 | CIDA2 | CIDA1 | CIDA0 |

\* Bit 0 ~ Bit 7 select General RAM address up to 256. User can select two banks by RA bit4.

**10. RD(RAM DATA)**

\* Bit 0 ~ Bit 8 are 0.5K RAM indirect data transfer register.

User can see RA register how to select RAM banks.

**11. RE( AD control)**

| 7    | 6    | 5    | 4     | 3     | 2     | 1   | 0   |
|------|------|------|-------|-------|-------|-----|-----|
| SAD3 | SAD2 | SAD1 | SVREF | START | ADPWR | IN1 | IN0 |



\* Bit1~Bit0 (input of AD converter selection ) : These two bits can choose one of three AD input.

| (IN1,IN0) | INPUT |
|-----------|-------|
| 0 0       | AD1   |
| 0 1       | AD2   |
| 1 0       | AD3   |
| 1 1       | AD4   |

\* Bit2 (ADPWR: AD converter power control register): 1/0=enable/disable

\* Bit3 (START: AD converter start to sample): Set to "1", the AD will start to sample data. This bit will be cleared by hardware automatically after a sampling.

\* Bit4 This register can switch AD converter reference voltage coming from internal or external voltage.

If the register set to internal, then the voltage will be VDD and port9 bit7 is a normal I/O PORT. If it set to external reference voltage, then the voltage will connected to PORT9 bit7.

0/1=internal/external reference voltage.

\* Bit5 This register can switch PORT9 bit3 as IO port or AD converter input1. 0/1= IO PORT / AD input

\* Bit6 This register can switch PORT9 bit4 as IO port or AD converter input2. 0/1= IO PORT / AD input

\* Bit7 This register can switch PORT9 bit5 as IO port or AD converter input3. 0/1= IO PORT / AD input

And it can switch PORT9 bit6 as IO port or AD converter input4. 0/1= IO PORT / AD input

This is a CMOS multi-channel 8-bit successive approximation A/D converter.

#### Features

- 44kHz maximum conversion speed at 5V.
- Adjusted full scale input
- External reference voltage input or internal reference voltage
- 4 analog inputs multiplexed into one A/D converter
- Power down mode for power saving
- A/D conversion complete interrupt
- Interrupt register, A/D control and status register, and A/D data register

#### 12. RF (Interrupt Status Register)

| 7 | 6 | 5   | 4       | 3       | 2    | 1    | 0    |
|---|---|-----|---------|---------|------|------|------|
| 0 | 0 | ADI | EXTINT2 | EXTINT1 | CNT2 | CNT1 | TCIF |

\* "1" means interrupt request, "0" means non-interrupt

\* Bit 0 (TCIF) TCC timer overflow interrupt flag. Set when TCC timer overflows .

\* Bit 1 (CNT1) counter1 interrupt flag.

\* Bit 2 (CNT2) counter2 interrupt flag .

\* Bit 3 (EXTINT1) external pin interrupt flag (INT0 ~INT3) .

\* Bit 4 (EXTINT2) external pin interrupt flag (INT4 ~INT7) .

\* Bit 5 (ADI) AD interrupt flag after a sampling .

\* Bit 6~7: '0' always

\* High to low edge trigger , Refer to the Interrupt subsection.

\* IOCF is the interrupt mask register. User can read and clear RF register.

#### 13. R10~R3F (General Purpose Register)

\* R10~R3F (Banks 0~3) all are general purpose registers.



## VII.2 Special Purpose Registers

### 1. A (Accumulator)

- \* Internal data transfer, or instruction operand holding
- \* It's not an addressable register.

### 2. CONT (Control Register)

|   |     |    |   |     |      |      |      |
|---|-----|----|---|-----|------|------|------|
| 7 | 6   | 5  | 4 | 3   | 2    | 1    | 0    |
| 0 | INT | TS | 0 | PAB | PSR2 | PSR1 | PSR0 |

\* Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

| PSR2 | PSR1 | PSR0 | TCC Rate | WDT Rate |
|------|------|------|----------|----------|
| 0    | 0    | 0    | 1:2      | 1:1      |
| 0    | 0    | 1    | 1:4      | 1:2      |
| 0    | 1    | 0    | 1:8      | 1:4      |
| 0    | 1    | 1    | 1:16     | 1:8      |
| 1    | 0    | 0    | 1:32     | 1:16     |
| 1    | 0    | 1    | 1:64     | 1:32     |
| 1    | 1    | 0    | 1:128    | 1:64     |
| 1    | 1    | 1    | 1:256    | 1:128    |

\* Bit 3 (PAB) Prescaler assignment bit.

0/1 : TCC/WDT

\* **Bit 4 unused**

\* Bit 5 (TS) TCC signal source

0: internal instruction cycle clock

1: 16.38KHz

\* **Bit 6 : (INT)INT enable flag**

**0: interrupt masked by DISI or hardware interrupt**

**1: interrupt enabled by ENI/RETI instructions**

\* Bit 7 : unused

\* CONT register is readable and writable.

### 3. IOC5 (PORT6 pull high control register)

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| P6PH7 | P6PH6 | P6PH5 | P6PH4 | P6PH3 | P6PH2 | P6PH1 | P6PH0 |

\* IOC5 can control the pull high circuit of PORT6 individually.

\* 0/1 = disable /enable pull high circuit

### 4. IOC6 ~ IOC9 (I/O Port Control Register)

\* Five I/O direction control registers.

\* "1" put the relative I/O pin into high impedance (input port), while "0" put the relative I/O pin as output.

### 5. IOCA (OPEN DRAIN and IOCA)

|     |     |     |     |       |       |       |       |
|-----|-----|-----|-----|-------|-------|-------|-------|
| 7   | 6   | 5   | 4   | 3     | 2     | 1     | 0     |
| OD3 | OD2 | OD1 | OD0 | IOCA3 | IOCA2 | IOCA1 | IOCA0 |

\* Bit0 ~ bit3: PortA I/O direction control registers. "1" put the relative I/O pin into high impedance (input port), while "0" put the relative I/O pin as output.

\* Bit4: OD0 : Open drain control register on PORT9 bit0. 0/1= disable/enable open-drain function.

\* Bit5: OD1 : Open drain control register on PORT9 bit1. 0/1= disable/enable open-drain function.

\* Bit6: OD2 : Open drain control register on PORT9 bit2. 0/1= disable/enable open-drain function.

\* Bit7: OD3 : Open drain control register on PORT9 bit3. 0/1= disable/enable open-drain function.



## 6. IOCB (COUNTER1)

PAGE0 :

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| CNT1B7 | CNT1B6 | CNT1B5 | CNT1B4 | CNT1B3 | CBT1B2 | CNT1B1 | CNT1B0 |

Control register for 8 bit up-counter (COUNTER1) preset and read . ( write = preset INSTRUCTION: IOW 0x0B ).  
After a interruption , it will count from “00”.

PAGE1:

|   |   |             |        |         |     |     |     |
|---|---|-------------|--------|---------|-----|-----|-----|
| 7 | 6 | 5           | 4      | 3       | 2   | 1   | 0   |
| 0 | 0 | <b>P92S</b> | S3.58M | CNT1CLK | PS2 | PS1 | PS0 |



Bit0~Bit2: COUNTER1 prescaler

| PS2 | PS1 | PS0 | COUNTER1 |
|-----|-----|-----|----------|
| 0   | 0   | 0   | 1:2      |
| 0   | 0   | 1   | 1:4      |
| 0   | 1   | 0   | 1:8      |
| 0   | 1   | 1   | 1:16     |
| 1   | 0   | 0   | 1:32     |
| 1   | 0   | 1   | 1:64     |
| 1   | 1   | 0   | 1:128    |
| 1   | 1   | 1   | 1:256    |

Bit3: COUNTER1 clock source. 0/1 = 16.38KHz/system clock

**Bit4: S3.58M . It can switch PORT6 bit0 as IO port or 3.58Mhz clock output .**

**0/1= IO PORT / 3.58MHz clock**

**Bit5: P92S . It can switch PORT9 bit2 as IO port or DA signal output .**

**0/1= IO PORT / DA signal output.**

Bit6 ~Bit7: '0'always

#### 7. IOCC (COUNTER2)

PAGE0 :

|        |        |        |        |        |        |        |        |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| CNT2B7 | CNT2B6 | CNT2B5 | CNT2B4 | CNT2B3 | CBT2B2 | CNT2B1 | CNT2B0 |

Control register for 8 bit up-counter (COUNTER2) preset and read . ( write = preset INSTRUCTION: IOW 0x0B ).  
After a interruption , it will count from "00".

PAGE1:

|   |   |   |   |         |      |      |      |
|---|---|---|---|---------|------|------|------|
| 7 | 6 | 5 | 4 | 3       | 2    | 1    | 0    |
| 0 | 0 | 0 | 0 | CNT2CLK | PPS2 | PPS1 | PPS0 |

Bit0~Bit2: COUNTER2 prescaler

| PPS2 | PPS1 | PPS0 | COUNTER1 |
|------|------|------|----------|
| 0    | 0    | 0    | 1:2      |
| 0    | 0    | 1    | 1:4      |
| 0    | 1    | 0    | 1:8      |
| 0    | 1    | 1    | 1:16     |
| 1    | 0    | 0    | 1:32     |
| 1    | 0    | 1    | 1:64     |
| 1    | 1    | 0    | 1:128    |
| 1    | 1    | 1    | 1:256    |

Bit3:COUNTER2 clock source. 0/1 = 16.38KHz/system clock

Bit4~Bit7: '0'always

#### 8. IOCD (AD converter data register)

PAGE0:

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |

\* Bit 0 ~ 7 : AD converter 's output data

PAGE1:

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| T17 | T16 | T15 | T14 | T13 | T12 | T11 | T10 |

**Tone generator 1 's frequency divider. Please Run in Normal mode .**





**Clock source = 111843Hz**

**T17~T10 = '11111111' => Tone generator1 will has 438Hz SIN wave output.**

:

**T17~T10 = '00000010' => Tone generator1 will has 55921Hz SIN wave output.**

**T17~T10 = '00000001' => Tone generator1 will has 111843Hz SIN wave output.**

**T17~T10 = '00000000' => no used**

#### 9. IOCE (port7 pull high control Register)

**PAGE0:**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| P7PH7 | P7PH6 | P7PH5 | P7PH4 | P7PH3 | P7PH2 | P7PH1 | P7PH0 |

\* IOCE page0 can control the pull high circuit of PORT7 individually.

\* 0/1 = disable /enable pull high circuit

**PAGE1:**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| T27 | T26 | T25 | T24 | T23 | T22 | T21 | T20 |

**Tone generator 2 's frequency divider. Please Run in Normal mode.**

**Clock source = 111843Hz**

**T27~T20 = '11111111' => Tone generator1 will has 438Hz SIN wave output.**

:

**T27~T20 = '00000010' => Tone generator1 will has 55921Hz SIN wave output.**

**T27~T20 = '00000001' => Tone generator1 will has 111843Hz SIN wave output.**

**T27~T20 = '00000000' => no used**

| TONE1(IOCD) | ROW FREQ. |               |              |              |              |
|-------------|-----------|---------------|--------------|--------------|--------------|
| (0xA0)      | 699.02Hz  | 1             | 2            | 3            | A            |
| (0x91)      | 771.33Hz  | 4             | 5            | 6            | B            |
| (0X83)      | 853.76Hz  | 7             | 8            | 9            | C            |
| (0X77)      | 939.86Hz  | *             | 0            | #            | D            |
|             |           | 1202.6 (0X5D) | 1331.5(0X54) | 1471.7(0X4C) | 1644.8(0X44) |
|             |           | TONE2(IOCE)   |              |              |              |

#### 10. IOCF (Interrupt Mask Register)

|   |   |     |         |         |      |      |      |
|---|---|-----|---------|---------|------|------|------|
| 7 | 6 | 5   | 4       | 3       | 2    | 1    | 0    |
| 0 | 0 | ADI | EXTINT2 | EXTINT1 | CNT2 | CNT1 | TCIF |

\* Bit 0 ~ 5 interrupt enable bit.

0: disable interrupt

1: enable interrupt

\* IOCF Register is readable and writable.

It is very important to save ACC,R3 and R5 when processing a interruption.

| Address | Instruction     | Note                    |
|---------|-----------------|-------------------------|
| 0x08    | MOV A_BUFFER,A  | ;Save ACC               |
| 0x09    | SWAP A_BUFFER   |                         |
| 0x0A    | SWAPA 0x03      | ;Save R3 status         |
| 0x0B    | MOV R3_BUFFER,A |                         |
| 0x0C    | MOV A,0x05      | ;Save ROM page register |
| 0x0D    | MOV R5_BUFFER,A |                         |

|      |                 |             |
|------|-----------------|-------------|
| 0x0E | PAGE @0         | ;set page0  |
| :    | :               | :           |
| :    | :               | :           |
| :    | MOV A,R5_BUFFER | ;Return R5  |
| :    | MOV 0X05,A      |             |
| :    | SWAPA R3_BUFFER | ;Return R3  |
| :    | MOV 0X03,A      |             |
| :    | SWAPA A_BUFFER  | ;Return ACC |
| :    | RETI            |             |

### VII.3 TCC/WDT Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

- An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.
- See the prescaler ratio in CONT register.
- Fig. 6 depicts the circuit diagram of TCC/WDT.
- Both TCC and prescaler will be cleared by instructions which write to TCC each time.
- The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.
- **The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.**

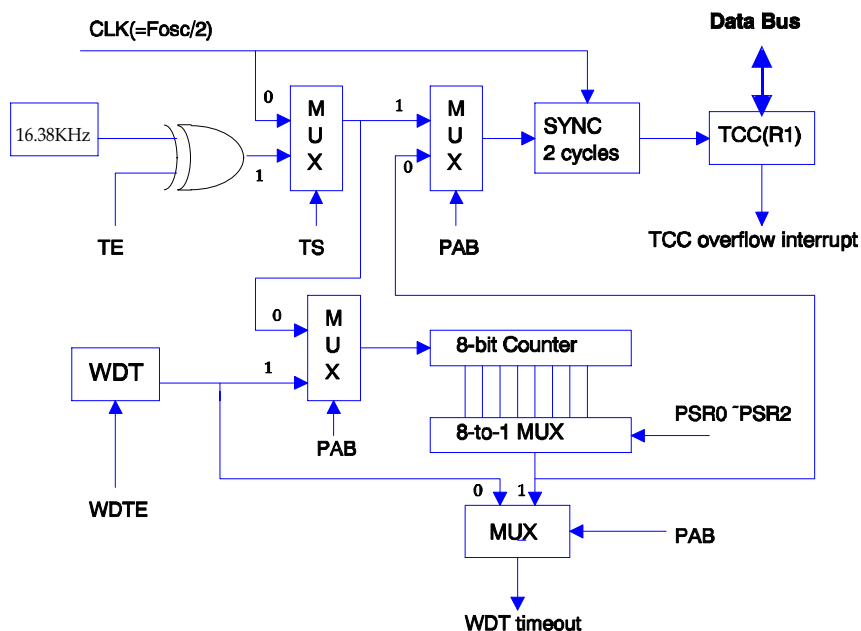


Fig. 6 Block diagram of TCC WDT

### VII.4 I/O Ports

The I/O registers, Port 6 ~ Port A, are bi-directional tri-state I/O ports. Port 6,7 can be pulled-high internally by software control. The I/O ports can be defined as "input" or "output" pins by the I/O control registers (IOC6 ~ IOCA ) under program control. The I/O registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.7. Port9 bit0 to bit3 have open drain function.

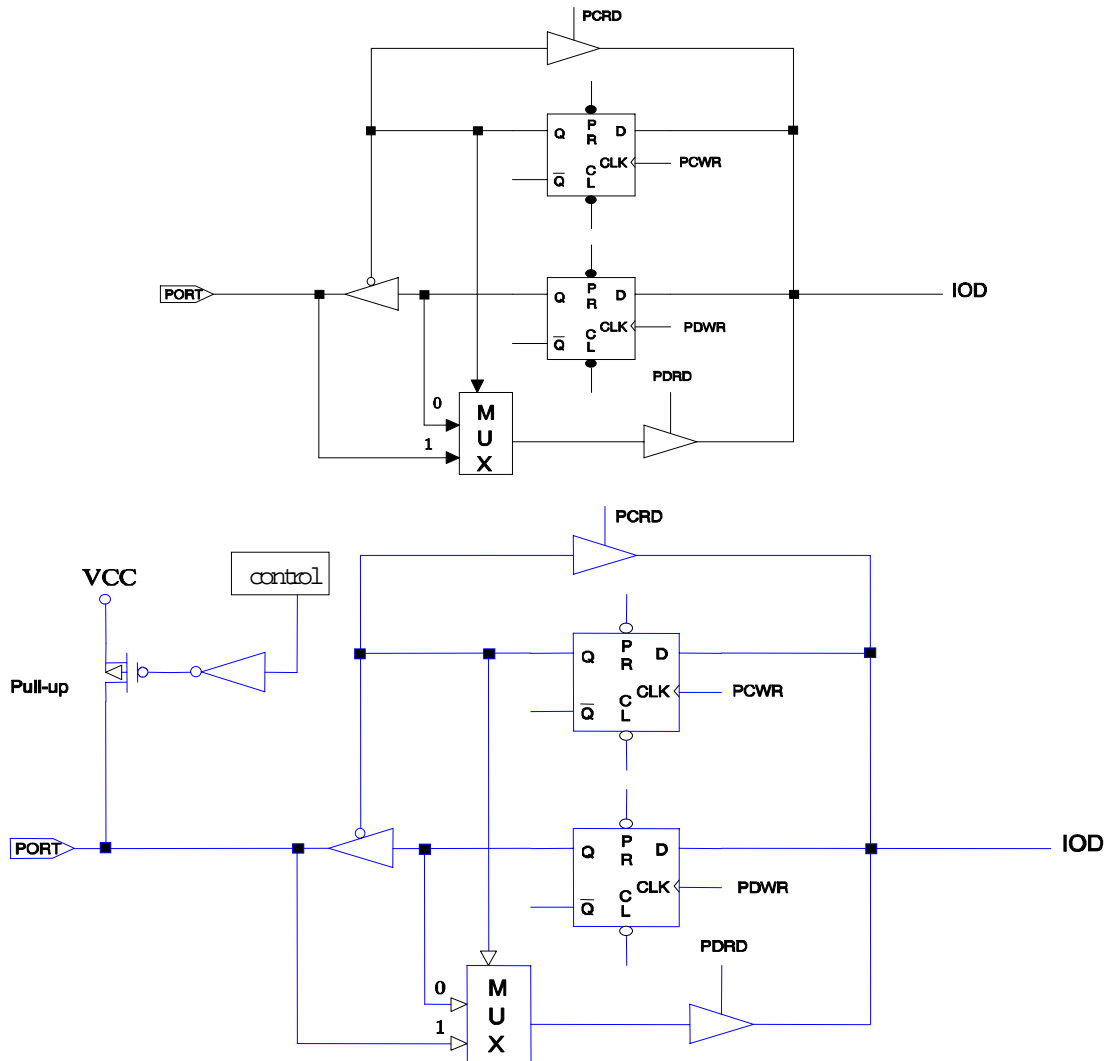


Fig. 7 The circuit of I/O port and I/O control register

## VII.5 RESET and Wake-up

The RESET can be caused by

- (1) Power on reset, or Voltage detector

**(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)**

Note that only Power on reset, or only Voltage detector in Case(1) is enabled in the system by CODE Option bit. If Voltage detector is disabled, Power on reset is selected in Case (1). Refer to Fig. 8.

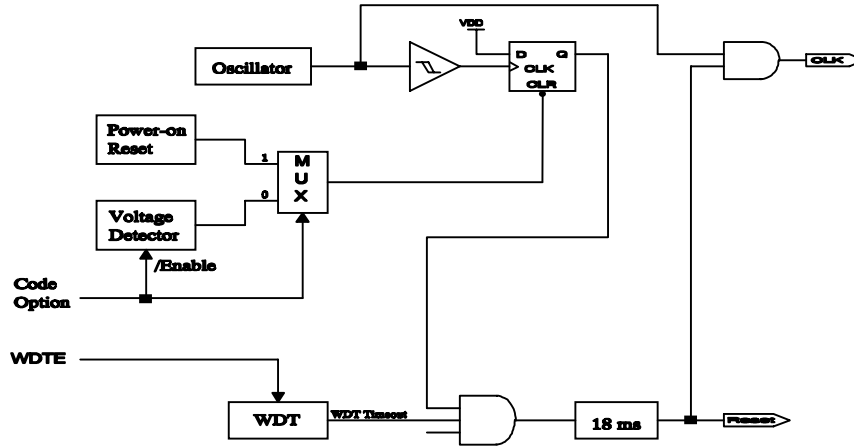


Fig. 8 Block diagram of Reset of controller

**Once the RESET occurs, the following functions are performed.**

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit7..bit0)

|                 |                         |                         |
|-----------------|-------------------------|-------------------------|
| R5 = "00000000" | IOC5 = "00000000"       |                         |
| R6 = PORT       | IOC6 = "11111111"       |                         |
| R7 = PORT       | IOC7 = "11111111"       |                         |
| R8 = PORT       | IOC8 = "11111111"       |                         |
| R9 = PORT       | IOC9 = "11111111"       |                         |
| RA = "0000xxxx" | IOCA = "00001111"       |                         |
| RB = "11111111" | Page0 IOCB = "xxxxxxx"  | Page1 IOCB = "00000000" |
| RC = "00000000" | Page0 IOCC = "xxxxxxx"  | Page1 IOCC = "00000000" |
| RD = "xxxxxxx"  | Page0 IOCD = "xxxxxxx"  | Page1 IOCD = "11111111" |
| RE = "00000000" | Page0 IOCE = "00000000" | Page1 IOCE = "11111111" |
| RF = "00000000" | IOCF = "00000000"       |                         |

The controller can be awakened from SLEEP mode or IDLE mode (execution of "SLEP" instruction, named as SLEEP MODE or IDLE mode) by (1)TCC time out (IDLE mode only) (2) WDT time-out (if enabled) The two cases will cause the controller wake up and run from next instruction in IDLE mode and reset in SLEEP mode . After wake-up , user should control WATCH DOG in case of reset in GREEN mode or NORMAL mode. The WATCH DOG should be open RA register before into SLEEP mode or IDLE mode . The first one case will set a flag in RF bit0 . And it will go to address 0x08 when TCC generate a interrupt and it will jump to next instruction from "SLEP" after return interrupt.

|              | SLEEP mode              | IDLE mode               | GREEN mode               | NORMAL mode              |
|--------------|-------------------------|-------------------------|--------------------------|--------------------------|
| Into         | RA(7,6)=(0,0)<br>+ SLEP | RA(7,6)=(1,0)<br>+ SLEP | RA(7,6)=(x,0)<br>no SLEP | RA(7,6)=(x,1)<br>no SLEP |
| TCC time out | x                       | Wake-up<br>=> Interrupt | Interrupt                | Interrupt                |



|              |                               |                               |                               |                               |
|--------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|
|              |                               | => Next instruction           |                               |                               |
| WDT time out | RESET<br>Run from address "0" | Wake-up<br>+ Next instruction | RESET<br>Run from address "0" | RESET<br>Run from address "0" |

## VII.6 Interrupt

The IC has internal interrupts which are falling edge triggered, as followed : TCC timer overflow interrupt (internal) , two 8-bit counters overflow interrupt and AD converter interrupt.

If these interrupt sources change signal from high to low , then RF register will generate '1' flag to corresponding register if you enable IOCF register.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine the source of the interrupt can be determined by polling the flag bits in the RF register. The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

There are eight external interrupt pins including INT0 .. INT7 .

External interrupt INT0 , INT1 , INT2 , INT3 signals are from PORT7 bit0 to bit3 . If IOCF bit 3 (EXTINT1) is enable then these signal will cause interrupt and set a flag to RF bit3 , or these signals will be treated as general input data .

External interrupt INT4 , INT5 , INT6 , INT7 signals are from PORT7 bit4 to bit7 . If IOCF bit 4 (EXTINT2) is enable then these signal will cause interrupt and set a flag to RF bit4 , or these signals will be treated as general input data .

After reset, the next instruction will be fetched from address 000H and the instruction inturrept is 001H and the hardware inturrept is 008H.

TCC will go to address 0x08 in GREEN mode or NORMAL mode after time out. It will go to address 0x08 for interrupt sub-routine and run next instruction from "SLEP" instruction after return interrupt in IDLE mode . These two cases will set a RF flag.

Please save R3,R5 and ACC value before processing interrupt sub-routine. And return buffer value before RETI instruction.

It is very important to save ACC,R3 and R5 when processing a interruption.

| Address | Instruction     | Note                    |
|---------|-----------------|-------------------------|
| 0x08    | MOV A_BUFFER,A  | ;Save ACC               |
| 0x09    | SWAP A_BUFFER   |                         |
| 0x0A    | SWAPA 0x03      | ;Save R3 status         |
| 0x0B    | MOV R3_BUFFER,A |                         |
| 0x0C    | MOV A,0x05      | ;Save ROM page register |
| 0x0D    | MOV R5_BUFFER,A |                         |
| 0x0E    | PAGE @0         | ;set page0              |
| :       | :               | :                       |
| :       | :               | :                       |
| :       | MOV A,R5_BUFFER | ;Return R5              |
| :       | MOV 0X05,A      |                         |
| :       | SWAPA R3_BUFFER | ;Return R3              |
| :       | MOV 0X03,A      |                         |
| :       | SWAPA A_BUFFER  | ;Return ACC             |
| :       | RETI            |                         |

## VII.7 Instruction Set

\* This specification are subject to be changed without notice.



Instruction set has the following features:

- (1). Every bit of any register can be set, cleared, or tested directly.
- (2). The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

| INSTRUCTION BINARY | HEX  | MNEMONIC | OPERATION                               | STATUS AFFECTED |
|--------------------|------|----------|---|-----------------|
| 0 0000 0000 0000   | 0000 | NOP      | No Operation                            | None            |
| 0 0000 0000 0001   | 0001 | DAA      | Decimal Adjust A                        | C               |
| 0 0000 0000 0010   | 0002 | CONTW    | A → CONT                                | None            |
| 0 0000 0000 0011   | 0003 | SLEP     | 0 → WDT, Stop oscillator                | T,P             |
| 0 0000 0000 0100   | 0004 | WDTC     | 0 → WDT                                 | T,P             |
| 0 0000 0000 rrrr   | 000r | IOW R    | A → IOCR                                | None            |
| 0 0000 0001 0000   | 0010 | ENI      | Enable Interrupt                        | None            |
| 0 0000 0001 0001   | 0011 | DISI     | Disable Interrupt                       | None            |
| 0 0000 0001 0010   | 0012 | RET      | [Top of Stack] → PC                     | None            |
| 0 0000 0001 0011   | 0013 | RETI     | [Top of Stack] → PC<br>Enable Interrupt | None            |
| 0 0000 0001 0100   | 0014 | CONTR    | CONT → A                                | None            |
| 0 0000 0001 rrrr   | 001r | IOR R    | IOCR → A                                | None            |
| 0 0000 0010 0000   | 0020 | TBL      | R2+A → R2 bits 9,10 do not clear        | Z,C,DC          |
| 0 0000 01rr rrrr   | 00rr | MOV R,A  | A → R                                   | None            |
| 0 0000 1000 0000   | 0080 | CLRA     | 0 → A                                   | Z               |
| 0 0000 11rr rrrr   | 00rr | CLR R    | 0 → R                                   | Z               |
| 0 0001 00rr rrrr   | 01rr | SUB A,R  | R-A → A                                 | Z,C,DC          |
| 0 0001 01rr rrrr   | 01rr | SUB R,A  | R-A → R                                 | Z,C,DC          |
| 0 0001 10rr rrrr   | 01rr | DECA R   | R-1 → A                                 | Z               |
| 0 0001 11rr rrrr   | 01rr | DEC R    | R-1 → R                                 | Z               |
| 0 0010 00rr rrrr   | 02rr | OR A,R   | A ∨ VR → A                              | Z               |
| 0 0010 01rr rrrr   | 02rr | OR R,A   | A ∨ VR → R                              | Z               |
| 0 0010 10rr rrrr   | 02rr | AND A,R  | A & R → A                               | Z               |
| 0 0010 11rr rrrr   | 02rr | AND R,A  | A & R → R                               | Z               |
| 0 0011 00rr rrrr   | 03rr | XOR A,R  | A ⊕ R → A                               | Z               |
| 0 0011 01rr rrrr   | 03rr | XOR R,A  | A ⊕ R → R                               | Z               |
| 0 0011 10rr rrrr   | 03rr | ADD A,R  | A + R → A                               | Z,C,DC          |
| 0 0011 11rr rrrr   | 03rr | ADD R,A  | A + R → R                               | Z,C,DC          |
| 0 0100 00rr rrrr   | 04rr | MOV A,R  | R → A                                   | Z               |
| 0 0100 01rr rrrr   | 04rr | MOV R,R  | R → R                                   | Z               |
| 0 0100 10rr rrrr   | 04rr | COMA R   | /R → A                                  | Z               |
| 0 0100 11rr rrrr   | 04rr | COM R    | /R → R                                  | Z               |
| 0 0101 00rr rrrr   | 05rr | INCA R   | R+1 → A                                 | Z               |
| 0 0101 01rr rrrr   | 05rr | INC R    | R+1 → R                                 | Z               |
| 0 0101 10rr rrrr   | 05rr | DJZA R   | R-1 → A, skip if zero                   | None            |
| 0 0101 11rr rrrr   | 05rr | DJZ R    | R-1 → R, skip if zero                   | None            |
| 0 0110 00rr rrrr   | 06rr | RRCA R   | R(n) → A(n-1)<br>R(0) → C, C → A(7)     | C               |
| 0 0110 01rr rrrr   | 06rr | RRC R    | R(n) → R(n-1)                           | C               |

\* This specification are subject to be changed without notice.



|          |             |             |             |             |               |                                     |             |
|----------|-------------|-------------|-------------|-------------|---------------|-------------------------------------|-------------|
|          |             |             |             |             |               | R(0) → C, C → R(7)                  |             |
| 0        | 0110        | 10rr        | rrrr        | 06rr        | RLCA R        | R(n) → A(n+1)<br>R(7) → C, C → A(0) | C           |
| 0        | 0110        | 11rr        | rrrr        | 06rr        | RLC R         | R(n) → R(n+1)<br>R(7) → C, C → R(0) | C           |
| 0        | 0111        | 00rr        | rrrr        | 07rr        | SWAPA R       | R(0-3) → A(4-7)<br>R(4-7) → A(0-3)  | None        |
| 0        | 0111        | 01rr        | rrrr        | 07rr        | SWAP R        | R(0-3) ↔ R(4-7)                     | None        |
| 0        | 0111        | 10rr        | rrrr        | 07rr        | JZA R         | R+1 → A, skip if zero               | None        |
| 0        | 0111        | 11rr        | rrrr        | 07rr        | JZ R          | R+1 → R, skip if zero               | None        |
| 0        | 100b        | bbrr        | rrrr        | 0xxx        | BC R,b        | 0 → R(b)                            | None        |
| 0        | 101b        | bbrr        | rrrr        | 0xxx        | BS R,b        | 1 → R(b)                            | None        |
| 0        | 110b        | bbrr        | rrrr        | 0xxx        | JBC R,b       | if R(b)=0, skip                     | None        |
| 0        | 111b        | bbrr        | rrrr        | 0xxx        | JBS R,b       | if R(b)=1, skip                     | None        |
| 1        | 00kk        | kkkk        | kkkk        | 1kkk        | CALL k        | PC+1 → [SP]<br>(Page, k) → PC       | None        |
| 1        | 01kk        | kkkk        | kkkk        | 1kkk        | JMP k         | (Page, k) → PC                      | None        |
| 1        | 1000        | kkkk        | kkkk        | 18kk        | MOV A,k       | k → A                               | None        |
| 1        | 1001        | kkkk        | kkkk        | 19kk        | OR A,k        | A ∨ k → A                           | Z           |
| 1        | 1010        | kkkk        | kkkk        | 1Akk        | AND A,k       | A & k → A                           | Z           |
| 1        | 1011        | kkkk        | kkkk        | 1Bkk        | XOR A,k       | A ⊕ k → A                           | Z           |
| 1        | 1100        | kkkk        | kkkk        | 1Ckk        | RETL k        | k → A, [Top of Stack] → PC          | None        |
| 1        | 1101        | kkkk        | kkkk        | 1Dkk        | SUB A,k       | k-A → A                             | Z,C,DC      |
| 1        | 1110        | 0000        | 0001        | 1E01        | INT           | PC+1 → [SP]<br>001H → PC            | None        |
| <b>1</b> | <b>1110</b> | <b>1000</b> | <b>kkkk</b> | <b>1E8k</b> | <b>PAGE k</b> | <b>K-&gt;R5</b>                     | <b>None</b> |
| 1        | 1111        | kkkk        | kkkk        | 1Fkk        | ADD A,k       | k+A → A                             | Z,C,DC      |

## VII.8 CODE Option Register

The chip has one CODE option register which is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

|   |   |               |             |             |             |             |              |
|---|---|---------------|-------------|-------------|-------------|-------------|--------------|
| 7 | 6 | 5             | 4           | 3           | 2           | 1           | 0            |
| - | - | <b>TONEEN</b> | <b>DAEN</b> | <b>ADEN</b> | <b>ROM2</b> | <b>ROM1</b> | <b>/povd</b> |

\* Bit 0 (:/POVD) : Power on voltage detector.

0: enable  
1: disable

| /POVD | 2.0V POVD Reset | 1.8V power on Reset | Sleep mode current |
|-------|-----------------|---------------------|--------------------|
| 1     | No              | yes                 | 1uA                |
| 0     | Yes             | yes                 | 15uA               |

| 2.0V POVD reset Suggestion    | POVD    |
|-------------------------------|---------|
| EM78P567 Normal mode          | Disable |
| EM78P567 GREEN mode IDLE mode | Disable |

\* This specification are subject to be changed without notice.



|  |                          |
|--|--------------------------|
| <b>SLEEP mode</b>  |                          |
| <b>EM78567<br/>Normal mode</b>                             | <b>Disable</b>           |
| <b>EM78567<br/>GREEN mode<br/>IDLE mode<br/>SLEEP mode</b> | <b>Enable or disable</b> |

\* Bits 2~1: ROM2 and ROM1 bits can select three type of chip

(ROM2,ROM1) = (1,1)= EM78567; (ROM2,ROM1) = (1,0)= EM78566; (ROM2,ROM1) = (0,0)= EM78565

\* Bit3: ADEN: A bit to enable or disable AD circuit. 1/0 = AD valid / AD invalid

\* Bit4: DAEN: A bit to enable or disable DA circuit. 1/0 = DA valid / DA invalid

\* Bit5: TONEEN: A bit to enable or disable AD circuit. 1/0 = TONE valid / TONE invalid

\* Bit6,7 : unused

In OTP version, we name disabled POVD as A-type OTP and enabled POVD as B-type OTP.

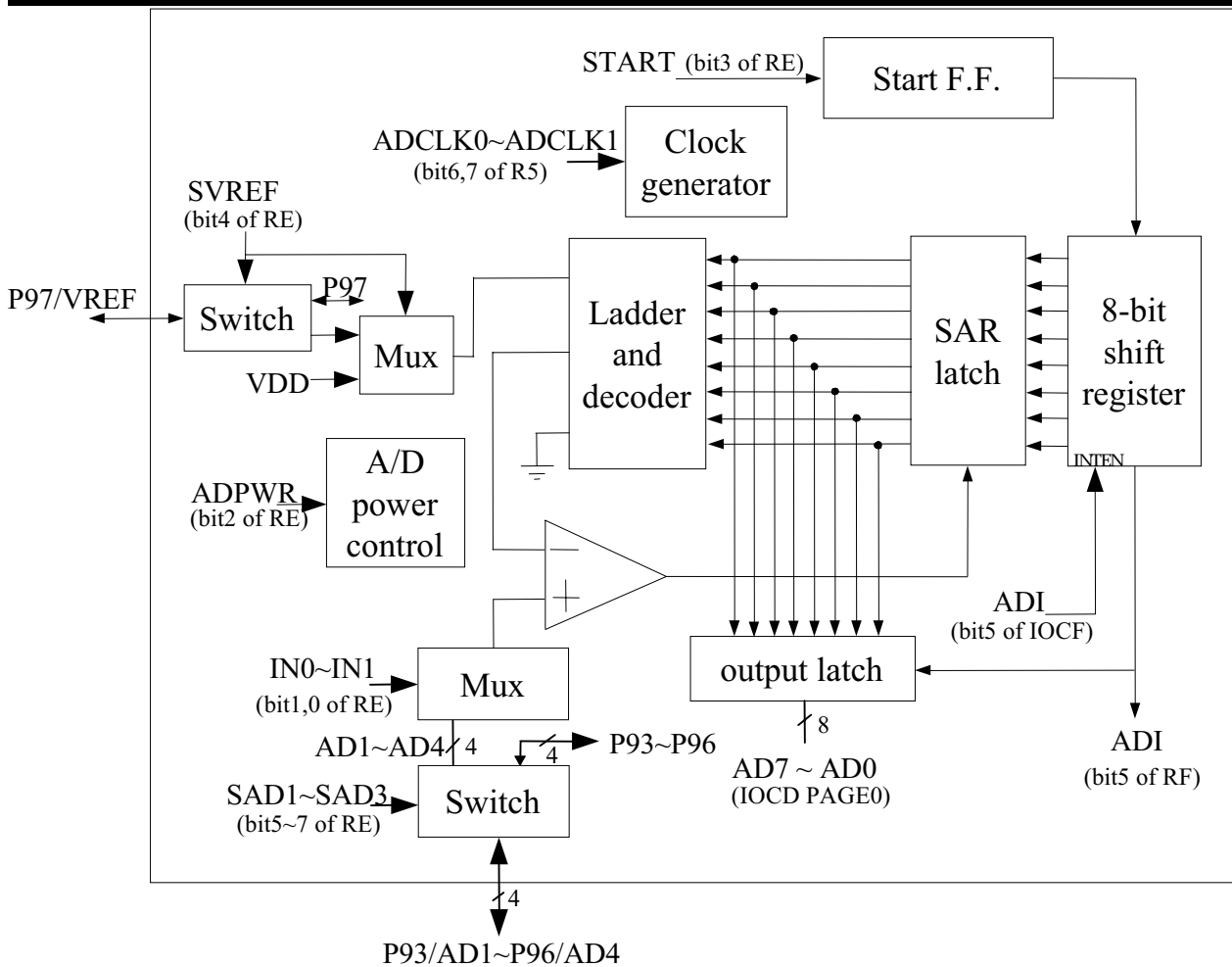
## VII.9 AD converter

This is a CMOS multi-channel 8-bit successive approximation A/D converter.

### Features

- 44kHz maximum conversion speed at 5V.
- Adjusted full scale input
- External reference voltage input or internal reference voltage
- 4 analog inputs multiplexed into one A/D converter
- Power down mode for power saving
- A/D conversion complete interrupt
- Interrupt register, A/D control and status register, and A/D data register




**RE( AD control)**

|      |      |      |       |       |       |     |     |
|------|------|------|-------|-------|-------|-----|-----|
| 7    | 6    | 5    | 4     | 3     | 2     | 1   | 0   |
| SAD3 | SAD2 | SAD1 | SVREF | START | ADPWR | IN1 | IN0 |

\* Bit1~Bit0 (input of AD converter selection) : These two bits can choose one of three AD input.

| (IN1,IN0) | INPUT |
|-----------|-------|
| 0 0       | AD1   |
| 0 1       | AD2   |
| 1 0       | AD3   |
| 1 1       | AD4   |

\* Bit2 (ADPWR: AD converter power control register): 1/0=enable/disable

\* Bit3 (START: AD converter start to sample): Set to "1", the AD will start to sample data. This bit will be cleared by hardware automatically after a sampling.

\* Bit4 This register can switch AD converter reference voltage coming from internal or external voltage.

If the register set to internal, then the voltage will be VDD and port9 bit7 is a normal I/O PORT. If it set to external reference voltage, then the voltage will be connected from PORT9 bit7. 0/1=internal/external reference voltage.

- \* Bit5 This register can switch PORT9 bit3 as IO port or AD converter input1. 0/1= IO PORT / AD input
  - \* Bit6 This register can switch PORT9 bit4 as IO port or AD converter input2. 0/1= IO PORT / AD input
  - \* Bit7 This register can switch PORT9 bit5 as IO port or AD converter input3. 0/1= IO PORT / AD input
- And it can switch PORT9 bit6 as IO port or AD converter input4. 0/1= IO PORT / AD input

**RF (Interrupt Status Register)**

|   |   |     |   |   |   |   |   |
|---|---|-----|---|---|---|---|---|
| 7 | 6 | 5   | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | ADI | - | - | - | - | - |

**IOCD (AD converter data register)**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |

**IOCF (Interrupt Mask Register)**

|   |   |     |   |   |   |   |   |
|---|---|-----|---|---|---|---|---|
| 7 | 6 | 5   | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | ADI | - | - | - | - | - |

**There are four registers for A/D converter. Use one bit of interrupt control register (IOCF bit5) for A/D conversion complete interrupt. The status and control register of A/D (RE and RF) responses the A/D conversion status or takes control on A/D. The A/D data register (IOCD) stores A/D conversion result.**

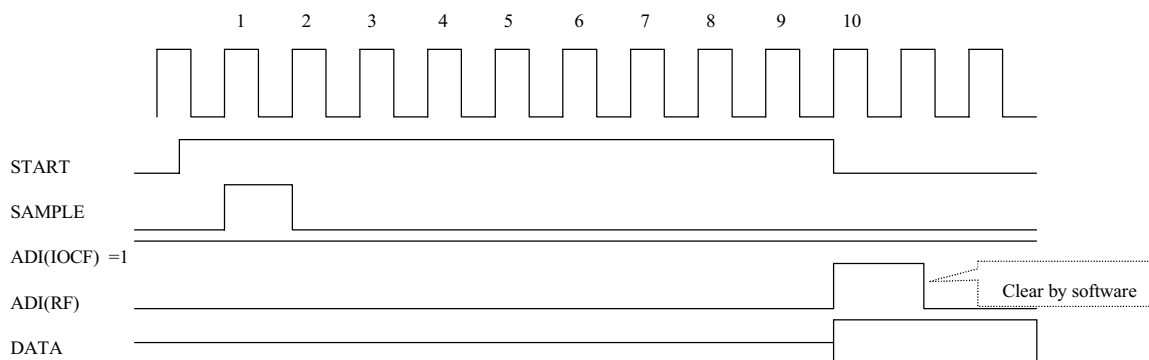
ADI bit in IOCF register is end of A/D conversion complete interrupt enable/disable. It enables/disables ADI flag in RF register when A/D conversion is complete. ADI flag indicates the end of an A/D conversion. The A/D converter sets the interrupt flag, ADI in RF register when a conversion is complete. The interrupt can be disabled by setting ADI bit in IOCF register to '0'.

The A/D converter has four analog input channels AD1~AD3 multiplexed into one sample and hold to A/D module. Reference voltage can be driven from VREF pin or internal power. The A/D converter itself is of an 8-bit successive approximation type and produces an 8-bit result in the IOCD data register. A conversion is initiated by setting a control bit START in RE register. Prior to conversion, the appropriate channel must be selected by setting IN0~IN1 bits in RE register and allowed for enough time to sample data. Every conversion data of A/D need 10-clock cycle time. The minimum conversion time required is 20 us (50K sample rate). START bit in RE register must be set to begin a conversion. It will be automatically reset in hardware when conversion is complete. At the end of conversion, the START bit is cleared and the A/D interrupt is activated if ADIE in IOCF = 1. ADI will be set when conversion is complete. It can be reset in software.

If ADI = 0 in IOCF, when A/D start conversion by setting START= 1 then A/D will continue conversion without stop and hardware won't reset START bit. In this condition, ADI is deactivated. After ADI in IOCF set, ADI in RF will activate again.

To minimum operating current, all biasing circuits in the A/D module that consume DC current are power down when ADPWR bit in RE register is a '0'. When ADPWR bit is a '1', A/D converter module is operating.

User has to set PORT93 to PORT97 as AD converter input pin or bi-direction IO PORT.





## VIII. Absolute Operation Maximum Ratings

| RATING                      | SYMBOL          | VALUE                        | UNIT |
|-----------------------------|-----------------|------------------------------|------|
| DC SUPPLY VOLTAGE           | V <sub>dd</sub> | -0.3 To 6                    | V    |
| INPUT VOLTAGE               | V <sub>in</sub> | -0.5 TO V <sub>dd</sub> +0.5 | V    |
| OPERATING TEMPERATURE RANGE | T <sub>a</sub>  | 0 TO 70                      | °C   |

## IX DC Electrical Characteristic

(T<sub>a</sub>=0°C ~ 70°C, V<sub>DD</sub>=5V±5%, V<sub>SS</sub>=0V)

| Symbol     | Parameter                                      | Condition   | Min | Typ | Max | Unit |
|------------|--|---|-----|-----|-----|------|
| IIL1       | Input Leakage Current for input pins           | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>SS</sub>   |     |     | ±1  | μA   |
| IIL2       | Input Leakage Current for bi-directional pins  | V <sub>IN</sub> = V <sub>DD</sub> , V <sub>SS</sub>   |     |     | ±1  | μA   |
| VIH        | Input High Voltage                             |   | 2.5 |     |     | V    |
| VIL        | Input Low Voltage                              |   |     |     | 0.8 | V    |
| VIHT       | Input High Threshold Voltage                   | /RESET, TCC   | 2.0 |     |     | V    |
| VILT       | Input Low Threshold Voltage                    | /RESET, TCC   |     |     | 0.8 | V    |
| VIHX       | Clock Input High Voltage                       | OSCI  | 3.5 |     |     | V    |
| VILX       | Clock Input Low Voltage                        | OSCI  |     |     | 1.5 | V    |
| VOH1       | Output High Voltage (port6,7,8,A)              | I <sub>OH</sub> = -1.6mA  | 2.4 |     |     | V    |
|            | (port9)  | I <sub>OH</sub> = -6.0mA  | 2.4 |     |     | V    |
| VOL1       | Output Low Voltage (port6,7,8,A)               | I <sub>OL</sub> = 1.6mA   |     |     | 0.4 | V    |
|            | (port9)  | I <sub>OL</sub> = 5.0mA   |     |     | 0.4 | V    |
| IPH        | Pull-high current                              | Pull-high active input pin at V <sub>SS</sub>   |     | -15 | -20 | μA   |
| ISB1       | Power down current (SLEEP mode)                | All input and I/O pin at V <sub>DD</sub> , output pin floating, WDT disabled  |     | 2   | 4   | μA   |
| ISB1(povd) | Power down current (SLEEP mode) (/POVD enable) | All input and I/O pin at V <sub>DD</sub> , output pin floating, WDT disabled  |     | 15  | 20  | μA   |
| ISB2       | Low clock current (IDLE mode)                  | CLK=32.768KHz, AD, DA, Tone generator block disable, All input and I/O pin at V <sub>DD</sub> , output pin floating, WDT disabled |     | 20  | 35  | μA   |
| ISB3       | Low clock current (GREEN mode)                 | CLK=32.768KHz, AD, DA, Tone generator block disable, All input and I/O pin at V <sub>DD</sub> , output pin floating, WDT disabled |     | 30  | 50  | μA   |
| ISB3(povd) | Low clock current (GREEN mode) (/POVD enable)  | CLK=32.768KHz, AD, DA, Tone generator block disable, All input and I/O  |     | 45  | 70  | μA   |

\* This specification are subject to be changed without notice.



|       |  |  |            |     |      |     |
|-------|--|--|------------|-----|------|-----|
|       |  | pin at VDD, output pin floating, WDT disabled  |            |     |      |     |
| ICC   | Operating supply current (NORMAL mode)     | /RESET = High, CLK=3.58MHz, All input and I/O pin at VDD, output pin floating, AD, DA , Tone generator block disable |            | 1.6 | 2.0  | mA  |
| ITONE | Operating supply current (Tone generators) | for Tone generators only   |            | 0.4 | 0.65 | mA  |
| IDA   | Operating supply current (DA converter)    | for DA only  |            | 0.8 | 1.2  | mA  |
| IAD   | Operating supply current (AD converter)    | for AD only  |            | 0.5 | 0.8  | mA  |
| Vref1 | DA DC reference voltage                    |  | 2.25       |     | VDD  | V   |
| Vref2 | Tone generator reference voltage           |  | 0.5        |     | 0.7  | VDD |
| Vref3 | AD external reference voltage              |  | 1.8        |     | VDD  | V   |
| V1rms | Tone1 signal strength                      | Root mean square voltage   | 130        | 155 | 180  | mV  |
| V2rms | Tone2 signal strength                      | Root mean square voltage   | 1.259V1rms |     |      | mV  |
| Enl   | Differential nonlinear error               |  |            |     | ±1   | LSB |
| Einl  | Integral nonlinear error                   |  |            |     | ±2   | LSB |
| Tev   | Conversion time                            | Set sampling rate =44KHz   |            |     | 20   | uS  |
| Tda   | DA output valid time                       |  |            |     | 3    | uS  |

Ps. V1rms and V2rms has 2 dB difference. It means  $20\log(V2rms/V1rms) = 20\log1.259 = 2$  (dB)



## IX AC Electrical Characteristic

(Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

| Symbol                   | Parameter  | Conditions  | Min         | Typ       | Max         | Unit       |
|--------------------------|--|---|-------------|-----------|-------------|------------|
| Dclk                     | Input CLK duty cycle   |   | 45          | 50        | 55          | %          |
| Tins                     | Instruction cycle time   | 32.768K<br>3.58M  |             | 60<br>550 |             | us<br>ns   |
| Tdrh                     | Device delay hold time   |   |             | 18        |             | ms         |
| Ttcc                     | TCC input period   | Note 1  | (Tins+20)/N |           |             | ns         |
| Twdt                     | Watchdog timer period  | Ta = 25°C   |             | 18        |             | ms         |
| $\Delta f_{CLK}/f_{CLK}$ | <b>PLL main clock tolerance</b><br><b>Output clock to 3.58M pin</b><br><b>= fCLK ± Δ fCLK</b><br><b>where fCLK = 3.582635MHz</b> | <b>Input clock</b><br><b>to XIN pin =</b><br><b>32.768kHz</b> | <b>-500</b> |           | <b>+500</b> | <b>ppm</b> |

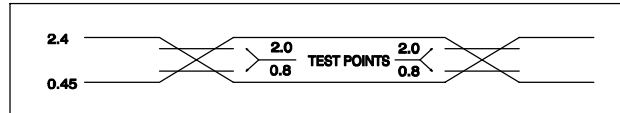
Note 1: N= selected prescaler ratio.

(OTP AC Characteristic)

| Description                 | Symbol | Min | Typ | Max | Unit |
|-----------------------------|--------|-----|-----|-----|------|
| Vpp to VDD level setup time | Trs    | 2   |     |     | uS   |
| Mode code setup time        | Tcsu   | 3   |     |     | uS   |
| Mode code hold time         | Tchd   | 2   |     |     | uS   |
| Data setup time             | Tdsu   | 100 |     |     | nS   |
| Data hold time              | Tdhd   | 100 |     |     | nS   |
| Program write pulse width   | Tpwd   |     | 200 |     | uS   |
| Output enable setup time    | Toed   | 300 |     |     | nS   |
| Data clock pulse width      | Tph    | 100 |     |     | nS   |
|                             |        |     |     |     |      |

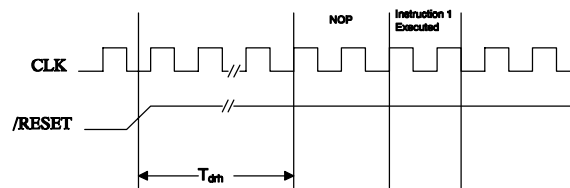
## XI. Timing Diagrams

AC Test Input/Output Waveform



AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing



TCC Input Timing

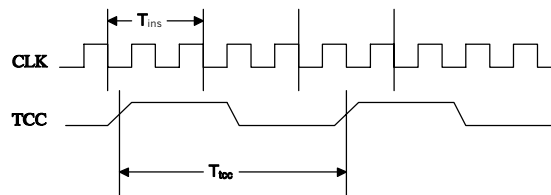


Fig.10 AC timing

## XII. Application Circuit

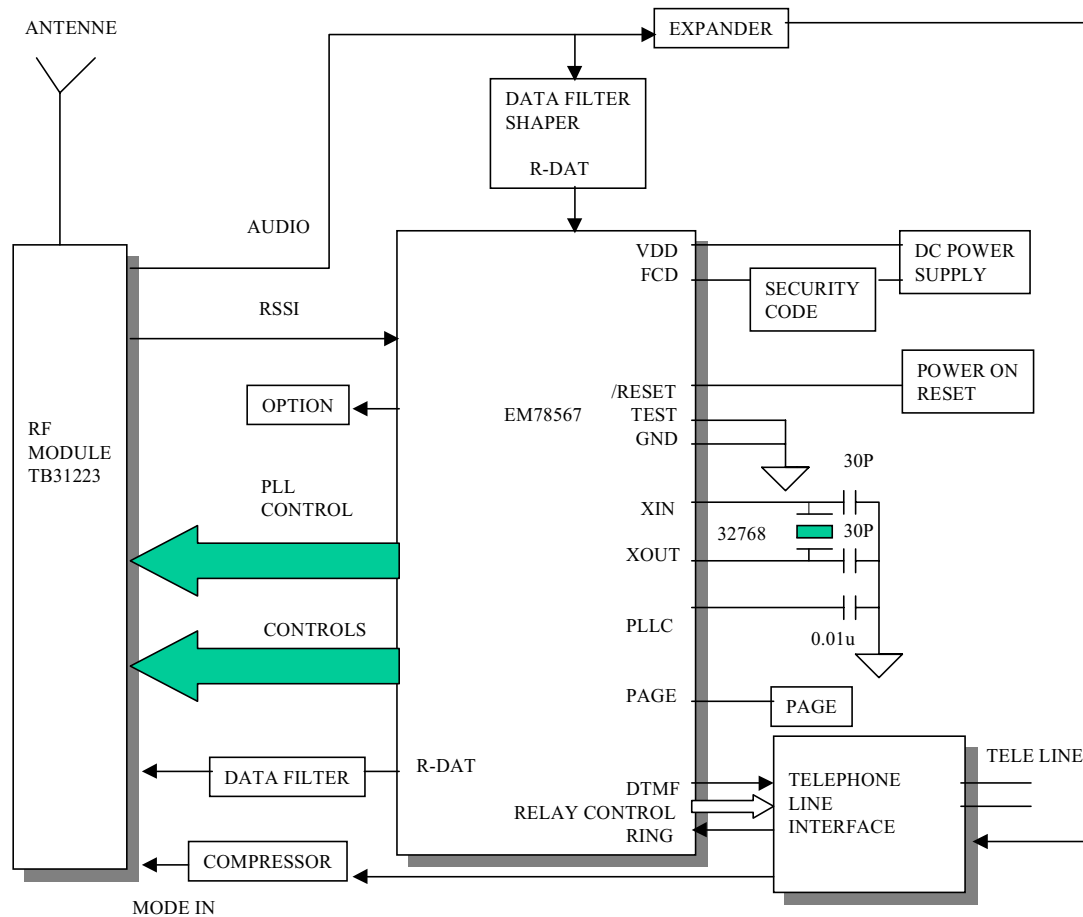


Fig.11.application circuit1 (Base unit)

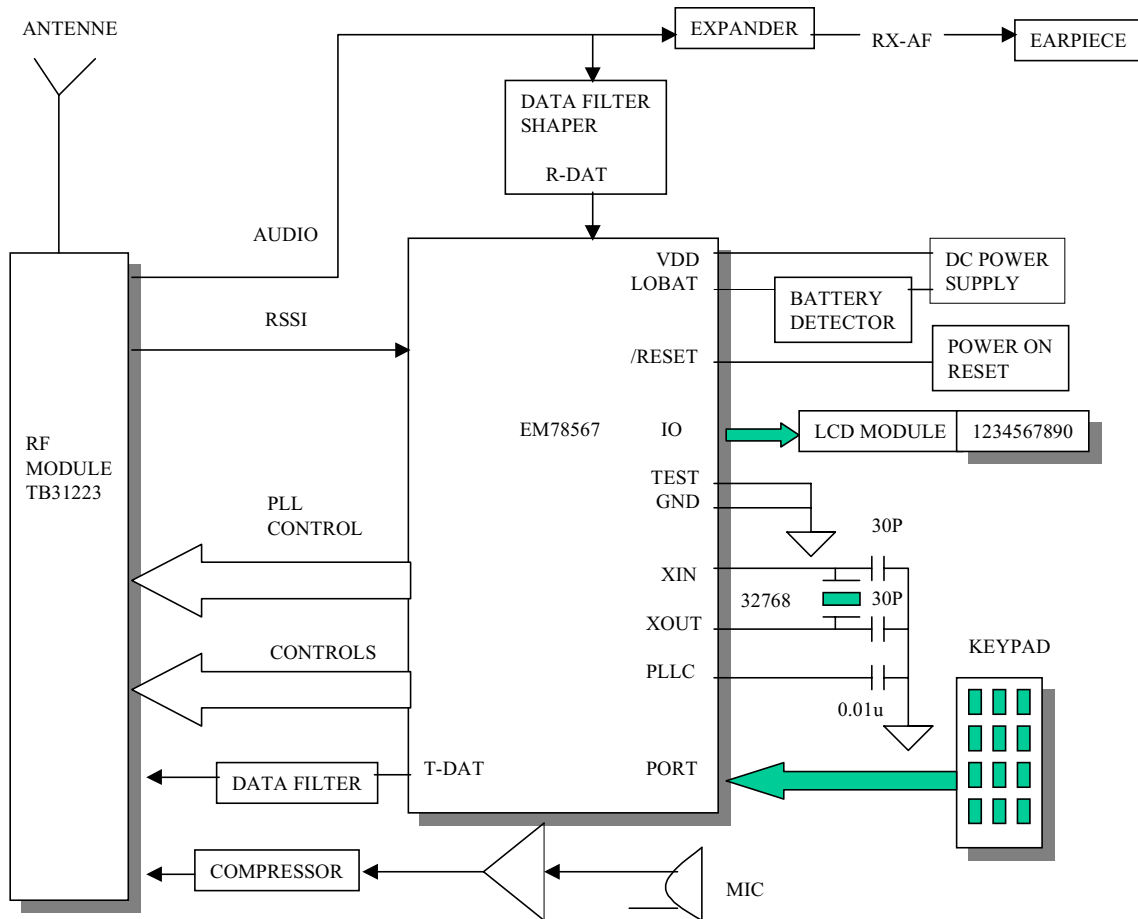


Fig.12.application circuit2 (Handset unit)