EF9367

GRAPHIC DISPLAY PROCESSOR

ADVANCE INFORMATION

This GDP is a true high resolution graphic display processor, which contains all the functions required to process vector generation at a very high speed and to generate all the timing signals required for interfacing interlaced or non interlaced video data on a raster scan CRT display compatible with 525 line or the CCIR 625 line standards.

The GDP's main features are :

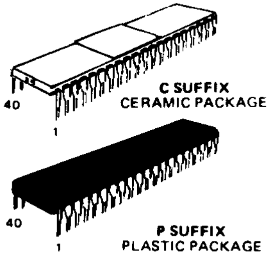
- Selectable resolutions in black and white or color :
  Vertical resolution : 525 line monitor (208 or 416). 625 line monitor (256 or 512).
  Horizontal resolution : 256, 320*, 384*, 512, 640*, 768*, 1024, full screen. (*) with external PROM.
- High speed vector plot well suited to animation - 4 types of lines.
- Multiplexed address and refresh for 16K or 64K dynamic RAMs.
- No limitation on the number of selectable memory planes (colors, grey levels or any other attributes)
- Multipage application capability
- On-chip full ASCII character generator (96) - maximum alphanumeric screen density : 170 x 57 - programmable sizes and orientations
- Direct interfacing with the monitor through the composite synchro and blanking signals
- Automatic allocation of display memory in refresh, write, dump, and display cycles
- Light pen registers and control signals
- Three types of interrupt requests
- Fully static design
- TTL compatible I/O
- Single + 5 volt supply.

MOS

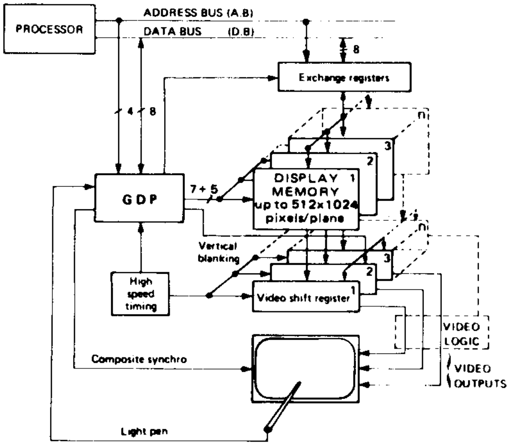
(N - CHANNEL, SILICON - GATE)

GRAPHIC DISPLAY PROCESSOR (GDP)

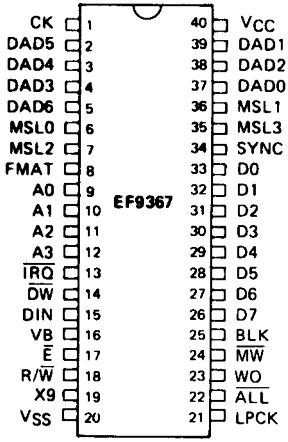
CASE CB-182



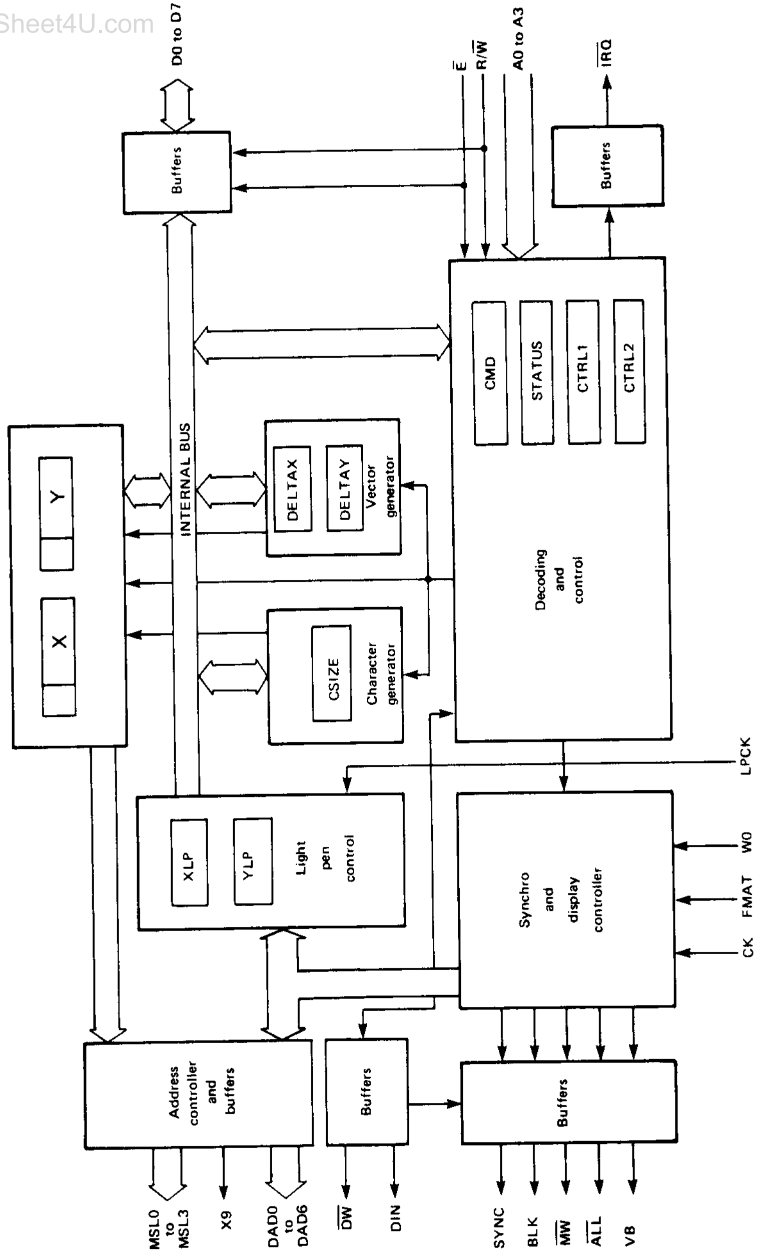
TYPICAL APPLICATION



PIN ASSIGNMENT



BLOCK DIAGRAM



GENERAL DESCRIPTION

Developed using NMOS technology, the GDP is an intelligent raster scan video display controller, fully programmable via an eight-bit microprocessor bus. Besides all the timing logic functions required to generate the video, sync and blanking signals, the GDP includes two hardwired display processors : a vector and a character generator.

This unique feature allows an ultrafast screen writing speed (the 1024 dot diagonal may be written in less than 1.4 ms) at almost no microprocessor processing cost.

The GDP is particularly well-suited to all applications in which the display memory is not directly addressed by the MPU. This feature allows a total asynchronism between the MPU and the GDP memory cycles and preserves the whole MPU memory addressing space.

Nevertheless, where direct exchange between the microprocessor and the memory is necessary, the on-chip allocation controller will allow this exchange without display interference.

The GDP is programmable using 11 internal registers occupying 16 consecutive addresses. These registers can also be modified by the GDP's hardwired processors while a command is being executed.

Note : A summary of data codes and registers is given in the **Register address table.** Hexadecimal values are subscripted 16 and the register bits are numbered as follows :

MSB	7	6	5	4	3	2	1	0	LSB

MAXIMUM RATINGS

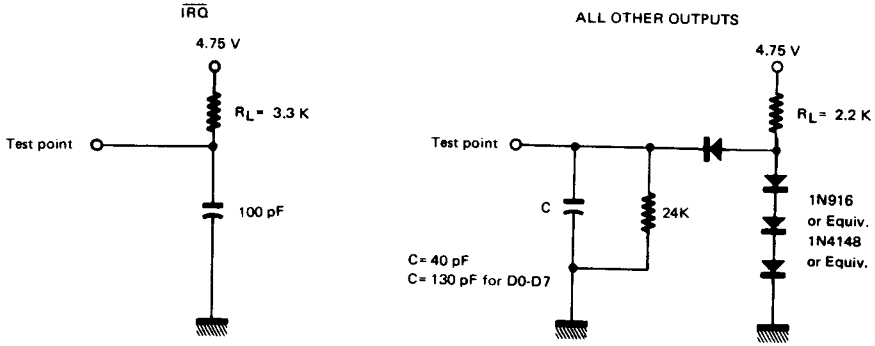
Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	–0.3 to + 7.0	V
Input voltage	V_{in}	–0.3 to + 7.0	V
Operating temperature	T_A	0 to + 70	°C
Storage temperature	T_{stg}	– 55 to + 150	°C

The GDP inputs are protected against high static voltages and electric fields ; nevertheless, normal precautions should be taken to avoid voltages above the limit values on this high impedance circuit.

STATIC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage except CK	V_{IH}	V_{SS} + 2.2	–	V_{CC}	V
Input high voltage CK	V_{IHCK}	V_{SS} + 3.5	–	V_{CC}	V
Input low voltage	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	V
Input leakage current (V_{in} = 0 to 5.25 V, V_{CC} = max)	I_{in}	–	1.0	2.5	µA
Output high voltage (I_{load} = –100 µA, V_{CC} = min)	V_{OH}	V_{SS} + 2.4	–	–	V
Output low voltage (I_{load} = 1.6 mA, V_{CC} = min)	V_{OL}	–	–	V_{SS} + 0.4	V
Supply current	I_{CC}	–	80	–	mA
Capacitance (V_{in} = 0, T_A = 25° C, f = 1.0 MHz)	C_{in}, C_{out}	–	–	12	pF

TEST LOADS

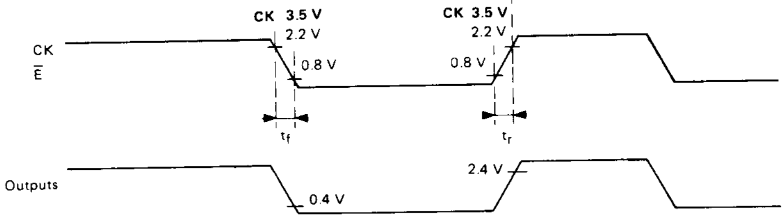


DYNAMIC OPERATING CONDITIONS

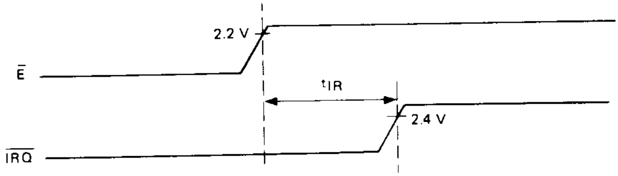
(V_{DD} = 5,0 V ± 5 %, V_{SS} = 0V ; T_A = 0 to + 70° C unless otherwise noted)

Time (ns)	Symbol	Min	Max
Clock period	t_{CK}	560	
CK pulse width, low	t_{CKL}	330	
CK pulse width, high	t_{CKH}	190	
CK low to valid DAD	CKLDAD		320
CK high to valid DAD	CKHDAD		180
CK low to valid SYNC	CKLSYNC		300
CK low to valid BLK	CKLBLK		310
CK low to valid VB	CKLVB		500
CK low to valid $\overline{\text{ALL}}$	CKLALL		300
CK low to valid MSL	CKLMSL		300
CK low to valid $\overline{\text{DW}}$	CKLDW		310
CK low to valid $\overline{\text{MFREE}}$ low	CKLMFRL		330
CK low to valid $\overline{\text{MFREE}}$ high	CKLMFRH		500
CK low to valid DIN	CKLDIN		310
CK low to valid $\overline{\text{IRQ}}$	CKLIRQ		1500
CK low to valid $\overline{\text{WHITE}}$	CKLWHI		530
$\overline{\text{E}}$ pulse width, low	t_{EL}	450	
$\overline{\text{E}}$ pulse width, high	t_{EH}	430	
Address pre-setup time	t_{AS}	160	
Address hold time	t_{AH}	10	
Data pre-setup time (write)	t_{DSW}	195	
Data setup time (read)	t_{DDR}		320
Data hold time (read)	t_{DHR}	10	
$\overline{\text{IRQ}}$ release time	t_{IR}		1600
LPCK high to $\overline{\text{WHITE}}$ high (if command 08_{16})	LPHW		1600
LPCK high to $\overline{\text{IRQ}}$ low	LPHIRQ		1600
LPCK high hold time	t_{LPCKH}	150	
CK and $\overline{\text{E}}$ rise times	t_r		20
CK and $\overline{\text{E}}$ fall times	t_f		20

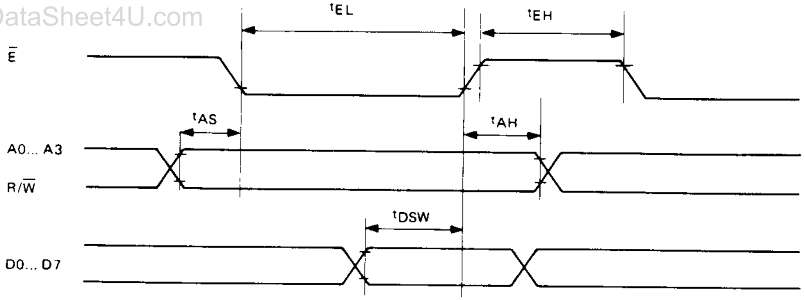
CLOCK AND OUTPUT CHARACTERISTICS



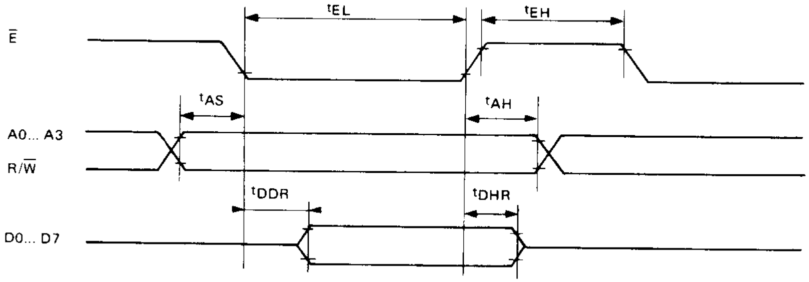
$\overline{\text{IRQ}}$ RELEASE TIME



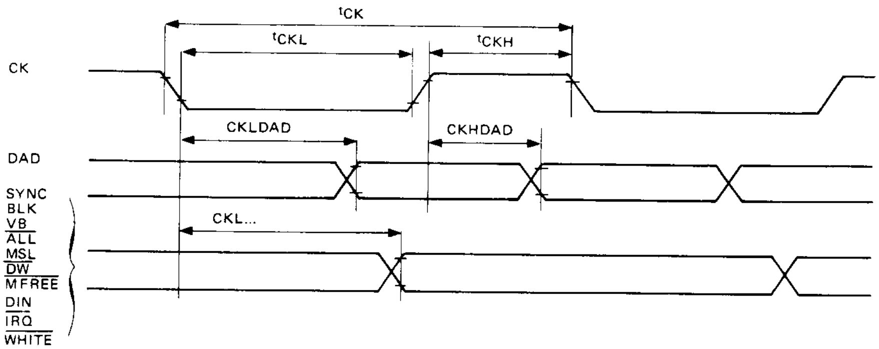
MICROPROCESSOR BUS, WRITE ACCESS



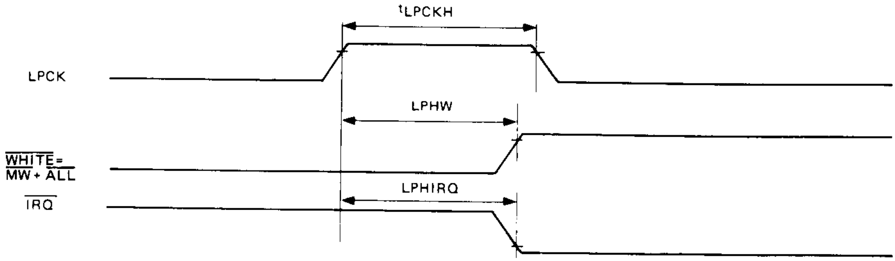
MICROPROCESSOR BUS, READ ACCESS



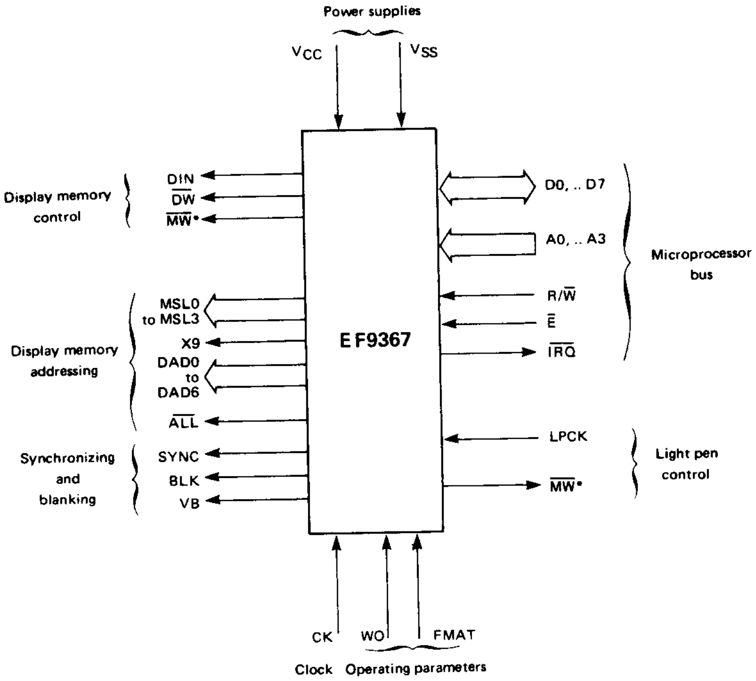
SYNCHRONOUS SIGNALS WITH CK INPUT



LIGHT PEN SIGNALS



PIN DESCRIPTION



*This pin outputs two items of data multiplexed by signal $\overline{\text{ALL}}$.

POWER SUPPLY, CLOCK AND OPERATING PARAMETERS

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
V_{SS}	S	20	Power supply	Ground
V_{CC}	S	40	Power supply	+ 5 V
CK	I	1	Clock	Master clock. All internal processor states are modified on the falling edge of this signal. The whole circuit logic is static and the cycle of this clock needs only to be ajusted according to the shape and accuracy the synchronizing signals should feature. DAD memory address multiplexing signal. If CK is low, low addresses (or row addresses for the memory) are those that are output on DAD. The frequency of CK is a multiple of the image refresh frequency : - interlaced scanning : f (CK) = f (1/2 frame) x (625 or 525) x 96 - non-interlaced scanning : f (CK) = f (frame) x (312 or 262) x 96.
FMAT	I	8	Format	This pin is connected to V_{CC}, V_{SS}, CK or $\overline{CK}$ and sets the number of monitor and image lines : V_{CC} : 625 line monitor, interlaced synchronization, 512 lines displayed CK : 525 line monitor, interlaced synchronization, 416 lines displayed $\overline{CK}$: 525 line monitor, non-interlaced synchro, 208 lines displayed V_{SS} : 625 line monitor, non-interlaced synchro, 256 lines displayed.
WO	I	23	Write only	When WO is high, memory refresh nor display no longer exist. The hard wired write processors may operate without being interrupted. The $\overline{ALL}$ signal is always high.

SYNCHRONIZING AND BLANKING SIGNALS

SYNC	O	34	Video monitor synchronizing	Video monitor line and frame synchronization signal. For example, if CK is at 1.5 MHz and FMAT is high, signal SYNC is to CCIR 625 line 50 Hz standard. This output is independent of input WO and ɔf register CTRL1.
BLK	O	25	Blanking	This signal is high apart from the display window (writing or refresh). It is always high if bit 2 in register CTRL1 is high, but it is not affected by the WO input.
VB	O	16	Vertical blanking	This signal is not affected by WO and register CTRL1. High during vertical blanking.

DISPLAY MEMORY ADDRESSING SIGNALS

DAD0 to DAD6	O	37,39, 38,4 3,2,5	Display address	Addresses that are multiplexed by the CK signal. Provided for the automatic refresh of the 16 K or 64 K dynamic memories.
X9	O	19	Memory address	Horizontal pointer extension bit for write operations (horizontal resolutions greater than 512).
MSL0 to MSL3	O	6,36 7,35	Memory select	Pixel write select signals (see section : **Display memory configuration.)**
$\overline{ALL}$	O	22	Access to all memory units	This signal makes it possible to discriminate between the collective memory accesses to all chips (display, refresh or erase), and the memory accesses to a single pixel for vector or character writing purposes. This signal is low for collective access.

DISPLAY MEMORY CONTROL SIGNALS

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
DIN	O	15	Display in	Selection of the memory data code corresponding to the display screen in the 'off' condition (active when high). For a black-and-white display (1 bit per pixel), DIN may directly be the storage entry data.
$\overline{\text{DW}}$	O	14	Display write	Display memory write signal. Active when low.
$\overline{\text{MW}}$	O	24	Memory available	This pin outputs $\overline{\text{MFREE}}$ and $\overline{\text{WHITE}}$ signals which are externally demultiplexed by signal $\overline{\text{ALL}}$: $\overline{\text{MFREE}} = \overline{\text{MW}} + \text{ALL}$; $\overline{\text{WHITE}} = \overline{\text{MW}} + \overline{\text{ALL}}$ **Memory free ($\overline{\text{MFREE}}$) :** Signal low during the next memory idle period following the $0F_{16}$ command. This signal allows exchanges between the microprocessor and the X and Y flagged memory segment without affecting the display. **Forcing to white level ($\overline{\text{WHITE}}$) :** Forces white level on video signal, for use of the light pen. Active when low.

MICROPROCESSOR BUS SIGNALS

D0-D7	I/O	33 to 26	Data bus	I/O buffers opening is controlled through $\overline{\text{E}}$, and the related direction through R/$\overline{\text{W}}$.
A0-A3	I	9 to 12	Address bus	Address of the register involved in microprocessor access.
R/$\overline{\text{W}}$	I	18	Read/write signal	Read/write signal. Write when low.
$\overline{\text{E}}$	I	17	Enable	Bus exchange synchronizing and enabling signal.
$\overline{\text{IRQ}}$	O	13	Interrupt request	Interrupt request towards the microprocessor, programmable through register CTRL1. Open drain output.

LIGHT PEN OPERATING SIGNALS

LPCK	I	21	Light pen strobe	Light pen input. When the mechanism is set, a rising edge loads into registers XLP and YLP the current display address and sets the XLP register's LSB high.

REGISTER DESCRIPTION

X AND Y REGISTERS (Addresses : 8_{16}, 9_{16}, A_{16}, B_{16})

The X and Y registers are 12-bit read-write registers. They indicate the position of the next dot to be written into the display memory. They have no connection at all with the video signal generating scan, but they point the write address, in the same way as the pen address on a plotter.

These 2 registers are incremented or decremented, prior to each write operation into the display memory, by the internal vector and character generators, or they may be directly positioned by the microprocessor.

This 2 x 12 bit write address covers a 4096 x 4096 point addressing space. Only the LSBs are used here, since the maximum definition of the picture actually stored is 512 x 1024 pixels (picture elements).

In practice, the GDP assumes that it has a memory space of 1024 x 512 (FMAT = V_{CC} or CK) or 1024 x 256 (FMAT = V_{SS} or $\overline{CK}$) and disables writing outside this space, unless bit 3 of CTRL 1 is set.

The above features along with the relative mode description of all picture component elements make it possible to automatically solve the great majority of edge cut-off problems.

DELTAX AND DELTAY REGISTERS (Addresses : 5_{16}, 7_{16}).

The DELTAX and DELTAY registers are 8-bit read-write registers. They indicate to the vector generator the projections of the next vector to be plotted, on the X and Y axes respectively. Such values are unsigned integers. The plotting of a vector is initiated by a write operation in the command register (CMD).

CSIZE REGISTER (Address : 3_{16})

The CSIZE register is an 8-bit read-write register. It indicates the scaling factors of X and Y registers for the symbols and characters. 98 characters are generated from a 5 x 8 pixel matrix defined by an internal ROM. In the standard version, it contains the alphanumeric characters in the ASCII code which may be printed, together with a number of special symbols.

MSB	P	Q	LSB

Each symbol can be increased by a factor P(X) or Q(Y). These factors are independent integers which may each vary from 1 to 16 and which are defined by the CSIZE register. The symbol generation sequence is started after writing the ASCII code of the symbol to be represented in the CMD register.

CTRL1 REGISTER (Address : 1_{16}).

The CTRL1 register is a 7-bit read-write register, through which the general circuit operation may be fed with the required parameters.

Bit 0 : When low, this bit inhibits writing in display memory (equivalent to pen or eraser up).
When high, this bit enables writing in display memory (pen or eraser down).
This bit controls the $\overline{DW}$ output.

Bit 1 : When low, this bit selects the eraser.
When high, this bit selects the pen.
This bit controls the DIN output.

Bit 2 : When low, this bit selects normal writing mode (writing apart from the display and refresh periods, which are a requirement for the dynamic storages) in display memory.
When high, this bit selects the high speed writing mode : the display periods are deleted. Only the dynamic storage refresh periods are retained.

Bit 3 : When low, this bit indicates that the 4096 x 4096 space is being used (the 12 X and Y bits are significant)
When high, this bit selects the cyclic screen operating mode.

Bit 4 : When low, this bit inhibits the interrupt triggered by the light pen sequence completion.
When high, this bit enables the interrupt.

Bit 5 : When low, this bit inhibits the interrupt release by vertical blanking.
When high, this bit enables the interrupt.

Bit 6 : When low, this bit inhibits the interrupt indicating that the system is ready for a new command.
When high, this bit enables the interrupt.

Bit 7 : Not used. Always low in read mode.

CTRL2 REGISTER (Address : 2_{16})

The CTRL2 register is a 4-bit read/write register, through which the plotting of vectors and characters may be denoted by parameters.

Bit 0, 1 : These 2 bits define 4 types of lines (continuous, dotted, dashed, dash-dotted).

Bit 2 : When low, this bit defines straight writing.
When high, it defines tilted characters.

Bit 3 : When low, this bit defines writing along an horizontal line.
When high, this bit defines writing along a vertical line.

Bit 4, 5, 6, 7 : Not used. Always low in read mode.

CMD COMMAND REGISTER (Address : 0_{16})

The CMD register is an 8-bit write-only register. Each write operation in this register causes a command to be executed, upon completion of the time necessary for synchronizing the microprocessor access and the GDP's CK clock.

Several types of command are available :

- vector plotting
- character plotting
- screen erase
- light pen circuitry setting
- access to the display memory through an external circuitry.
- indirect modification of the other registers (commands that make it possible for the X, Y, DELTAX, DELTAY, CTRL1, CTRL2 and CSIZE registers to be amended or scratched).

STATUS REGISTER (Address 0_{16} or F_{16})

The STATUS register is an 8-bit read-only register. It is used to monitor the status of the executing statements entered into the circuit, and more specifically to avoid the need for modifying a register that is already used for the command currently executing.

Bit 0 : When low, this bit indicates that a light pen sequence is currently executing.
When high, it indicates that no light pen sequence is currently executing.

Bit 1 : This bit is high during vertical blanking. It is the VB signal recopy.

Bit 2 : When low, this bit indicates that a command is currently executing.
When high, this bit indicates that the circuit is ready for a new command.

Bit 3 : This bit when low indicates that registers X and Y are pointing within the assumed memory space.
This bit is obtained by applying the logical OR function to the unused most significant bits of registers X and Y.
If FMAT = V_{CC} or CK, the assumed memory space is 1024 x 512.
If FMAT = V_{SS} or $\overline{CK}$, the assumed memory space is 1024 x 256.

Bit 4 : When high, this bit indicates that an interrupt has been initiated by the completion of a light pen running sequence and that this interrupt has been enabled by bit 4 in CTRL1 register.

Bit 5 : When high, this bit indicates that an interrupt has been initiated by vertical blanking and that this interrupt has been enabled by bit 5 in CTRL1 register.

Bit 6 : When high, this bit indicates that an interrupt has been initiated by the completion of execution of a command and that this interrupt has been enabled by bit 6 in CTRL1 register.

Bit 7 : When high, this bit indicates that an interrupt has been initiated. It is the logic OR of bits 4, 5 and 6 in STATUS register. The $\overline{IRQ}$ output state is always the opposite of the status of this bit.

Note : Bits 4, 5, 6 and 7 are reset low by reading the STATUS register at address 0_{16}. Reading at address F_{16} does not modify their state.

XLP AND YLP REGISTERS (Addresses C_{16} and D_{16})

The XLP and YLP registers are read-only registers, with 7 and 8 bits respectively. Upon completion of a light pen running sequence, they contain the display address sampled by the first edge appearing rising on the LPCK input. The use of such registers is discussed in section : **Use of light pen circuitry.**

NOTES :

1. All internal registers may be read or written at any time by the microprocessor. However, the precautions outlined below should be observed :

   – Do not write into the CMD register if execution of the previous command is not completed (bit 2 of STATUS register).

   – Do not alter any register if it is used as an input parameter for the internal hardwired systems (e. g. : modifying the DELTAX register while a vector plotting sequence is in progress).

   – Do not read a register that is being asynchronously modified by the internal hardwired systems (e.g. : reading the X register while a vector plotting sequence is in progress may be erroneous if CK and $\overline{E}$ are asynchronous).

2. On powering up, the writing devices may have any status. Before entering a command for the first time, it is necessary to wait until all functions currently underway are completed, which information can be derived from the STATUS register.

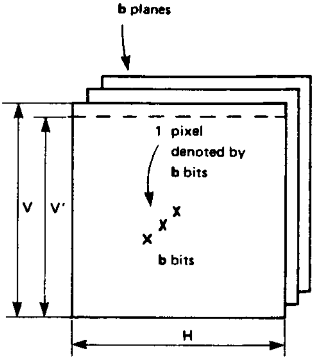
DISPLAY MEMORY CONFIGURATION

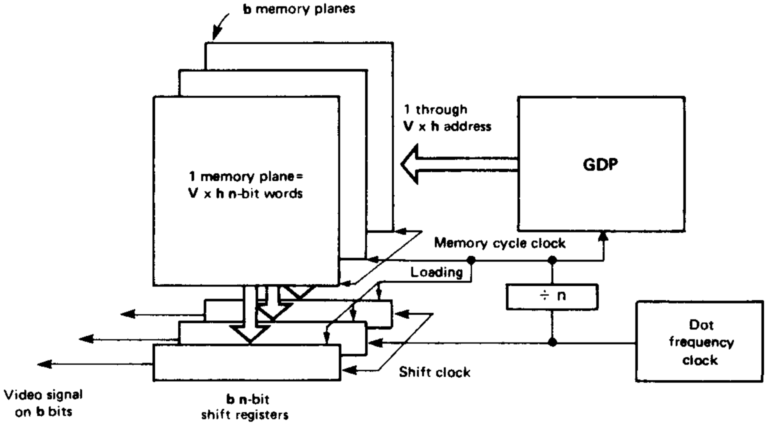
Assume a V x H pixel picture. Assume that each pixel is able to adopt 2^b different states. A V x H x b bit display memory is thus required.

In those applications where H features a high value, the video signal frequency exceeds the maximum frequency of memory read access.

Example : H = 512 with a television line frequency : the pixel succession period on the video signal is 83 ns.

It is mandatory that a line of H dots be cut into h adjoining segments of n bits each, read at the same time in the display memory, and thereafter converted to serial form to produce the video signal. h memory accesses per line are necessary. Each access loads b n-bit shift registers. The memory contains V x h x b n-bit words.





The EF9367 is designed for the following stored image formats :

V	=	512 or 256 (50 Hz)
V'	=	416 or 208 (60 Hz)
H	=	h x n
H	=	1024 or lower multiples of 64
h	=	64
n	=	16, 8, 4, 2, 1 (or any value below 16 using external PROM encoding)
b	=	any value (addressing is same for all memory planes, management of these planes is external to the GDP).

In so far as the overflow tests are concerned, the circuit assumes that it still has the maximum memory space for X (1024). The test for Y is effected in the following memory spaces :

512 if FMAT = V_{CC} or $\overline{CK}$
256 if FMAT = V_{SS} or $\overline{CK}$

512 or 256 vertical resolution : the displayed space is identical to the space in memory (unless a greater memory capacity is deliberately selected).

416 or 208 vertical resolution : the displayed space is smaller than the memory space.

Lines not displayed are displayable using an external adder to dejustify the display addresses (this arrangement may be used for smooth roll-up/roll down.

DAD AND MSL OUTPUT STATUS TABLES

The internal counters which address the display memory are made up of :

- 6 horizontal address bits (h = 64)
  $h_0, h_1, h_2, h_3, h_4, h_5$ (h_0 = LSB)
- **9 vertical address bits (V ⩽ 512)**
  t, $V_0, V_1, V_2, V_3, V_4, V_5, V_6, V_7$

t is here the LSB. It denotes the line parity and changes every frame because of interlaced scan. Within a same frame, V_0 denotes the LSB.

The write address is made up of the LSBs of the X and Y internal registers.

$X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_9$
$Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7, Y_8$

The GDP produces addressing signals in the sequences shown in the tables opposite :

FMAT = V_{CC} or CK

		MSL				X_9	DAD						
$\overline{ALL}$	CK	0	1	2	3		0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	V_1	X_9	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1						V_7	V_6	V_5	V_4	V_3	V_2	t
1	0	X_0	X_1	X_2	Y_2	X_9	X_8	X_7	X_6	X_5	X_4	X_3	Y_1
1	1						Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_0

FMAT = V_{SS} or $\overline{CK}$

		MSL				X_9	DAD						
$\overline{ALL}$	CK	0	1	2	3		0	1	2	3	4	5	6
0	0	X_0	X_1	X_2	1	X_9	h_5	h_4	h_3	h_2	h_1	h_0	V_0
0	1						V_7	V_6	V_5	V_4	V_3	V_2	V_1
1	0	X_0	X_1	X_2	1	X_9	X_8	X_7	X_6	X_5	X_4	X_3	Y_0
1	1						Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

DESCRIPTION OF DISPLAYABLE FORMATS

NON INTERLACED SCANNING

256 x 512 or 208 x 512 pixel formats (H = 512, n = 8)

Input FMAT must be low or connected to $\overline{CK}$.
The memory is made up of 16 K bytes per memory plane. The byte address is made up of 14 bits which are output on two runs on the DAD pins. The three MSL0, MSL1, MSL2 outputs are used to select one pixel out of the eight featuring the same address. They issue the number of the pixel, encoded on three bits. MSL3 is high, and is not used.

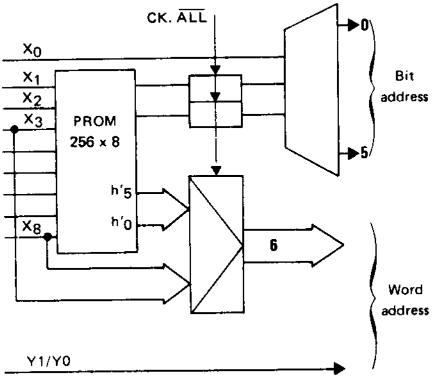
256 x 384 or 208 x 384 pixel formats (H = 384, n = 6)

Input FMAT must be low or connected to $\overline{CK}$.
The memory is organized as 16 K words x 6 bits.

The signals produced by the chip in the sequence indicated for the 256 x 512 format are transcoded externally as shown in the opposite diagram.

256 x 320 or 208 x 320 pixel formats (H = 320, n = 5)

The same schematic as for 384 horizontal resolution should be used with a memory organized in 5 bit words.



256 x 256 or 208 x 256 pixel formats (H = 256, n = 4)

Input FMAT must be low or connected to $\overline{CK}$.
The memory is made up of 16 K words x 4 bits. The word address is made up of 14 bits which are output in two runs on the DAD pins. One of the four chips is selected by decoding pins MSL1 and MSL2 (that leads to ignore X_0 : the X computation space is changed to 2048 pixels and horizontal overflow detected at 512 pixels).

INTERLACED SCANNING

512 x 1024 or 416 x 1024 pixel formats (H = 1024, n = 16)

Input FMAT must be connected to V_{CC} or CK.
The memory comprises 32 K words x 16 bits, organized in two blocks of 16 K words each.

The signals produced by the circuit in the sequence indicated for the 512 x 512 format are combined externally as shown at the end of the data sheet.

512 x 768 or 416 x 768 pixel formats (H = 768, n = 12)

Input FMAT must be connected to V_{CC} or CK.
The memory comprises 32 K words x 12 bits, organized in two blocks of 16 K words each.

The signals produced by the chip in the sequence indicated for the 512 x 512 format are transcoded externally as shown in the diagram below.

512 x 640 or 416 x 640 pixel formats (H = 640, n = 10)

The same schematic as below should be used with a memory organized in 10 bit words.

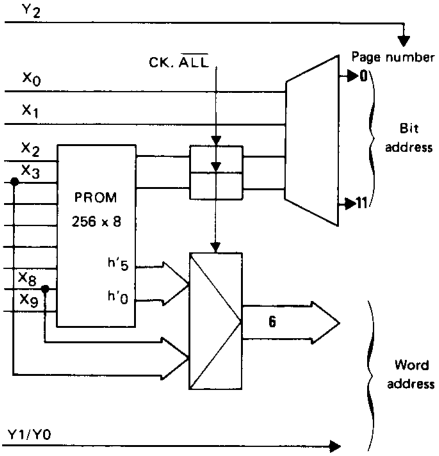
512 x 512 or 416 x 512 pixel formats (H = 512, n = 8)

The FMAT input should be tied to V_{CC} or CK. The memory is made up of V x h bytes = 32 K bytes per memory plane.

The byte address is made up of 15 bits :

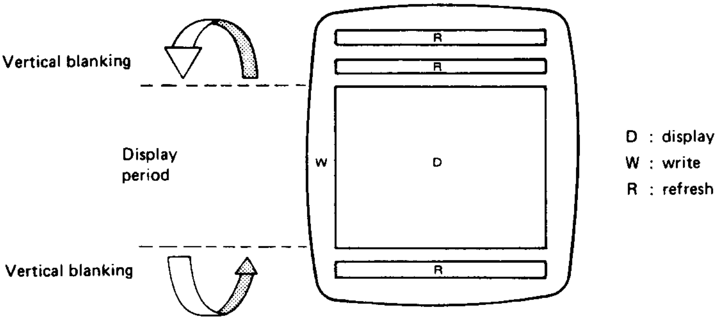
- 14 are output in 2 runs on the DAD pins for the purpose of using 16 K x 1 bit dynamic RAMs,
- the 15th one is output on pin MSL3.

The 3 MSL0, 1 and 2 outputs allow to select one pixel out of the 8 featuring the same address, for pixel-to-pixel write applications. They issue the number of the involved pixel, encoded on 3 bits.



MEMORY OPERATION SEQUENCE ALONG ONE FRAME

Apart from the window where the memory is used for display purposes exclusively, write operations may be performed, except during 3 refresh periods.



The three period types, D, W and R, respectively, are indicated outside the circuit through the BLK and $\overline{\text{ALL}}$ signals :

	BLK	$\overline{\text{ALL}}$
D	0	0
W	1	1
R	1	0

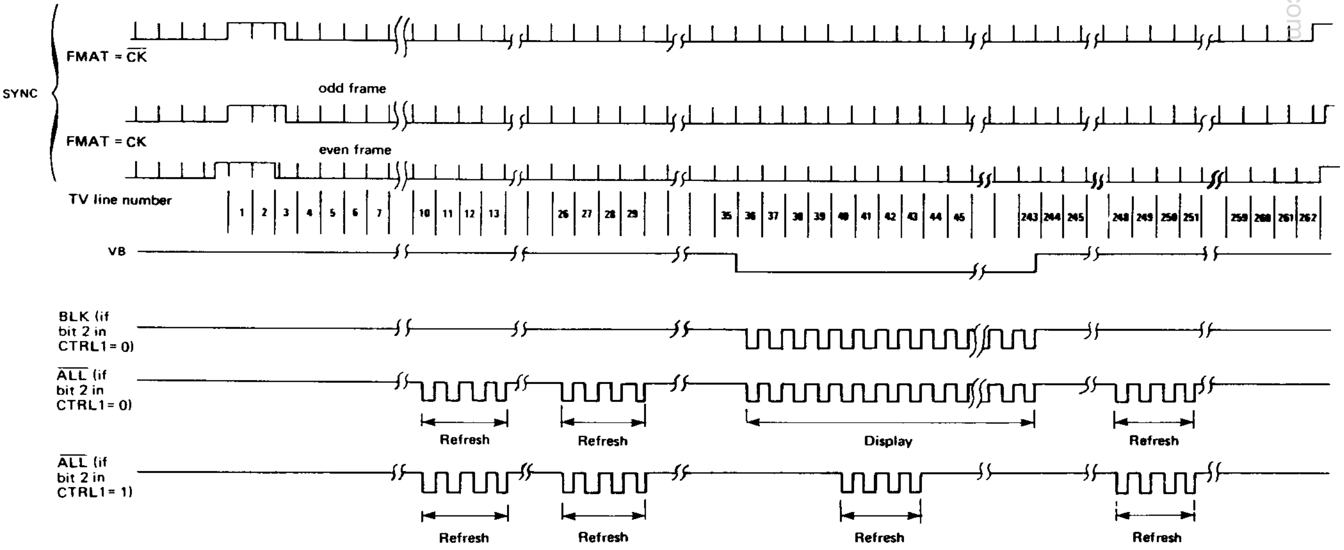
The refresh of dynamic RAMs is automatically performed by the GDP. During display, the memory is entirely refreshed each 4 lines (256 accesses).
During vertical blanking, 3 refresh cycles of 4 lines each are executed.

Exceptions :

- If bit 2 in register CTRL1 is high (high speed write), the display period is suppressed and 19 refresh cycles of 4 lines each are executed during one frame.
- As long as the WO input is high, the circuit is set to write mode, and BLK retains the same outline as it has under normal operating conditions.

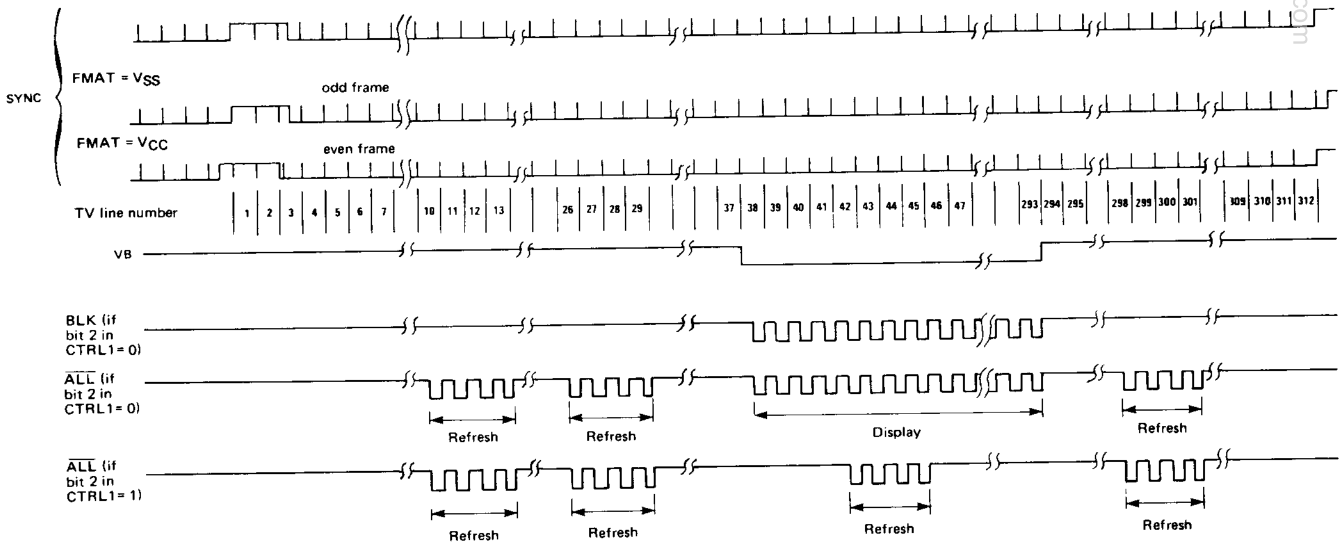
  In these two cases, executing codes 04_{16}, 06_{16}, 07_{16} and $0C_{16}$ triggers a complete D sequence for a high-speed scan of all addresses. This lasts two frames if FMAT is high (or tied to CK) and one frame if FMAT is low (or tied to $\overline{\text{CK}}$).

FRAME SEQUENCE – 525 LINE SYNCHRONIZATION



Note : $\overline{\text{ALL}}$ signal high denotes write periods.

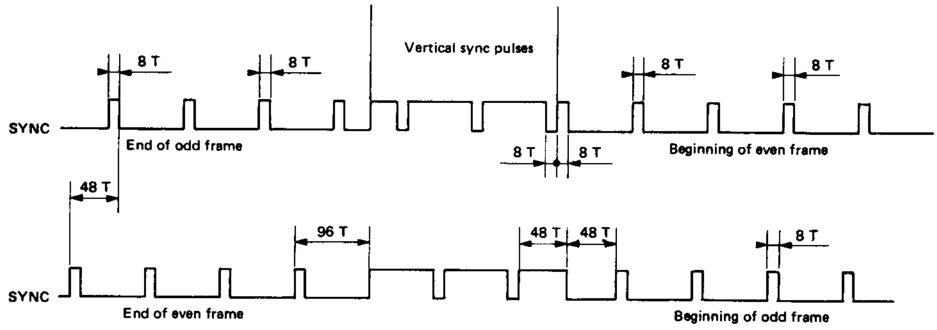
FRAME SEQUENCE – 625 LINE SYNCHRONIZATION



Note : $\overline{\text{ALL}}$ signal high denotes write periods.

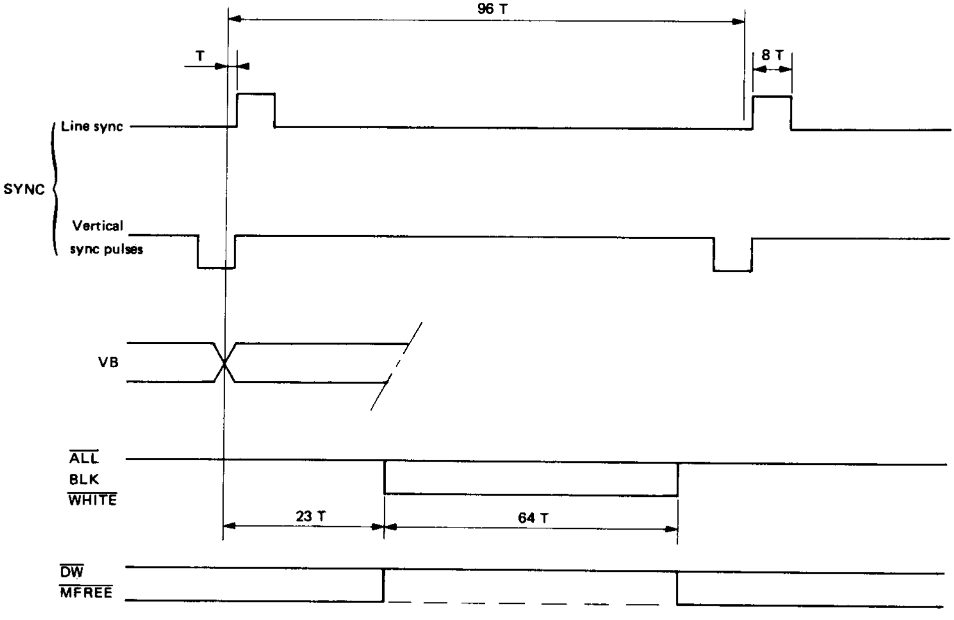
COMPOSITE SYNC AROUND FRAME SYNC

T : CK input period (667 ns in typical application where TV line duration is 64 μs)



Note : If FMAT is low or tied to $\overline{\text{CK}}$, the pattern of the second line is repeated for each frame.

DETAILED LINE DIAGRAM



HARDWIRED WRITE PROCESSOR OPERATION IN DISPLAY MEMORY

The hardwired write processors are sequenced by the master clock CK. They receive their parameters from the microprocessor bus. They control the X, Y write address, and the DIN, $\overline{DW}$, $\overline{MW}$ and $\overline{IRQ}$ outputs.

These harwired processors operate in continuous mode. In the event of conflicting access to the display memory, the display and refresh processors have priority.

Since command decoding is synchronous with the CK master clock, any write operation into the (CMD) command register triggers a synchronizing mechanism which engages the circuit for a maximum of 2 CK cycles when the $\overline{E}$ input returns high. The circuit remains engaged throughout command execution.

No further command should be entered as long as bit 2 in STATUS register is low.

VECTOR PLOTTING

The internal vector generator makes it possible to modify, within the display memory, all the dots which form the approximation of a straight line segment. All vectors plotted are described by the origin dot and the projections on the axes.

The starting point co-ordinates are defined by the X, Y register value, prior to the plotting operation.
Projections onto the axes are defined as absolute values by the DELTAX and DELTAY registers, with the sign in the command byte that initiates the vector plotting process.

The vector approximation achieved here is that established by J. F. BRESENHAM ("Algorithm for computer control of a digital plotter"). This algorithm is executed by a hardwired processor which allows for a further vector component dot to be written in each CK clock cycle.

During plotting, the display memory is addressed by the X, Y registers, which are incremented or decremented.

On completion of vector plotting, they point to the end of this vector.

All vectors may be plotted using any of the following line patterns : continuous, dotted, dashed, dash-dotted, according to the 2 LSBs in register CTRL2.

Irrespective of such patterns, the plotting speed remains unchanged. The "pen down-pen up" statement required for plotting non-continuous lines is controlled by the $\overline{DW}$ output.

For a specified non-continuous line plotted vector, defined by DELTAX, DELTAY, CTRL2, CMD, the $\overline{DW}$ sequencing during the plotting process is always the same, irrespective of vector origin and of the nature of previous plots. This feature guarantees that a specified vector can be deleted by plotting it again after moving X and Y to the starting point, and complementing bit 1 in register CTRL1.

Since the vector plotting initiation command defines the sign of the projections onto the axes, all vectors may be plotted using 4 different commands.

For increased programming flexibility, the system incorporates 16 different commands, supplemented by a set of 128 commands which make it possible to plot small size vectors by ignoring the DELTAX and DELTAY registers.

Such commands are as follows :

- Basic commands

0	0	0	1	0	X	X	1

→ DELTAX sign } 0 if positive
→ DELTAY sign } 1 if negative

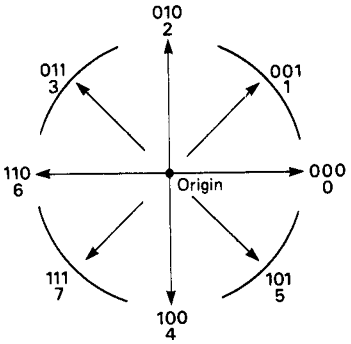
- Commands which allow ignoring the DELTAX or DELTAY registers by considering them as of zero value.

0	0	0	1	0	X	X	0

0 0 DELTAY ignored, DELTAX > 0
0 1 DELTAX ignored, DELTAY > 0
1 0 DELTAX ignored, DELTAY < 0
1 1 DELTAY ignored, DELTAX < 0

Note : Bits 1 and 2 always have the same sign meaning.

These 8 codes may be summarized by the following diagram :



- Commands which allow ignoring the smaller of the two DELTAX and DELTAY registers, by considering it as being equal to the larger one, which is the same as plotting vectors parallel to the axes or diagonals, using a single DELTA register.

0	0	0	1	1	X	X	X

Same direction codes as above.

- Commands in which the two registers DELTAX and DELTAY may be ignored by specifying the projections through the CMD register (0 to 3 steps for each projection).

1	X	X	X	X	X	X	X

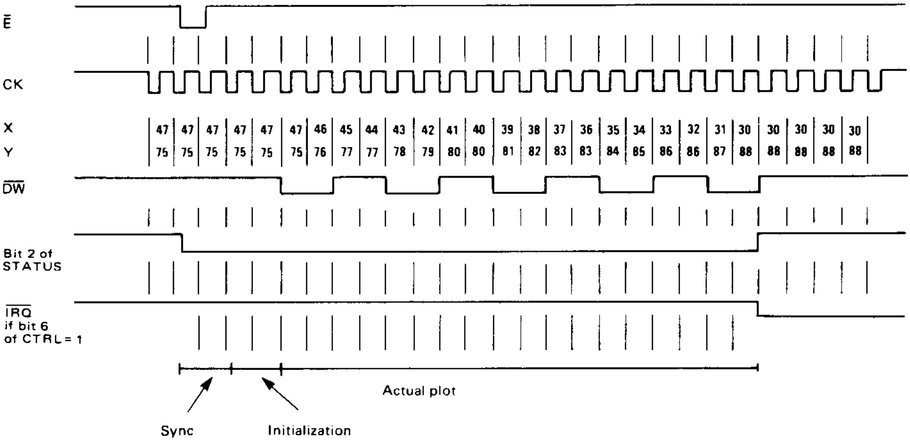
ΔX ΔY
(Unsigned integer values) → Same direction code as previously

Origin : $\begin{cases} X = 47_{10} \\ Y = 75_{10} \end{cases}$

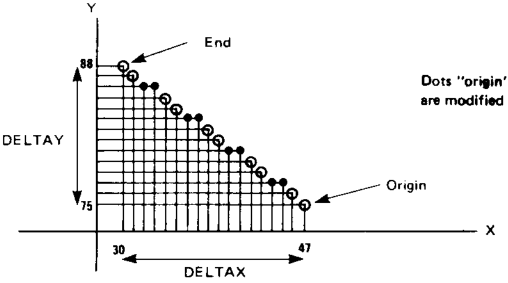
Projections: $\begin{cases} DELTAX = 17_{10} \\ DELTAY = 13_{10} \end{cases}$

CMD = 13_{16}	Corresponding to · Basic command, · DELTAX < 0 · DELTAY > 0
CTRL1 = 03_{16}	Pen down
CTRL2 = 1_{16}	Dotted vector : 2 dots on, 2 dots off.

Plotting cycle sequence : (It is assumed that the vector generator is not interrupted by the display or refresh cycle).



X	47	47	47	47	47	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	30	30	30	30
Y	75	75	75	75	75	75	76	77	77	78	79	80	80	81	82	83	83	84	85	86	86	87	88	88	88	88	88



Dots "origin" and "end" are modified

Display shows : ● unmodified dot
O dot on

Note :

Plotting a vector with DELTAX = DELTAY = 0 writes the dot X, Y in memory. It occupies the vector generator for synchronization, initialization and one write cycle.

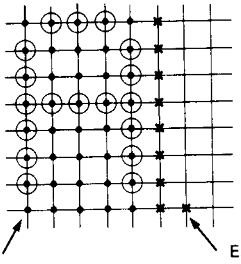
CHARACTER AND SYMBOL GENERATOR

The character generator operates in the same way as the vector generator, i.e. through incrementing or decrementing the X, Y registers, in conjunction with a $\overline{DW}$ output control.

It receives parameters from the CSIZE, CTRL2 and CMD registers. The characters plotted are selected, according to the CMD value, out of 98 matrices (97 8-dot high x 5-dot wide rectangular matrices, and one 4 dot x 4 dot matrix) defined in an internal ROM. Two scaling factors may be applied to the characters plotted using X and Y defined by the CSIZE register. The characters may be tilted, according to the content of register CTRL2.

Basic matrix

Upon completion of a character writing process, the X and Y registers are positioned for writing a further character next to the previous one, with a 1 dot spacing, i.e. Y is restored to its original value and X is incremented by 6.



- ● Unchanged
- ⊙ Altered dots

} if CMD = 41_{16} (in the ROM standard version)

× Computed dots, not defined into the ROM (not modifiable).

Scaling factors

Each individual dot in the 5 x 8 basic matrix may be replaced by a P x Q size block.

P : X co-ordinate scaling factor
Q : Y co-ordinate scaling factor

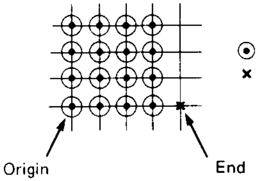
The character size becomes 5P x 8Q. Upon completion of the writing process, X is incremented by 6P. The CK clock cycle count required is 6P x 8Q.

P and Q may each take values from 1 through 16. They are defined by the CSIZE register. Each value is encoded on 4 bits, value 16 being encoded as 0_{16}.

In register CSIZE, P is encoded on the 4 MSBs and Q on the 4 LSBs.

Among the 97 rectangular matrices available in the standard ROM, 96 correspond to CMD values ranging from 20_{16} to $7F_{16}$, and the 97th matrix to $0A_{16}$. In the standard version, these values correspond to the 96 printable characters in the ASCII set. The 97th character is a 5P x 8Q block which may be used for deleting the other characters.

The 98th code ($0B_{16}$) is used to plot a 4P x 4Q graphic block. It locates X, Y, without spacing for the next symbol. Such a block makes it possible to pad uniform areas on the screen.



- ⊙ Modified dots
- × Computed dot not defined in ROM (not modifiable)

Tilted characters

All characters may be modified to produce tilted characters or to mark the vertical co-ordinate with straight or tilted type symbols. Such changes may be achieved using bits 2 and 3 in register CTRL2.

Note : Scaling factors P and Q are always applied within the co-ordinates of the character before conversion.

Character deletion

A character may be deleted using either the same command code or command code $0A_{16}$. In either case, bit 1 in register CTRL1 should be inverted, the origin should be the same as prior to a character plotting operation, as should the scaling factors.

Note : Vector generator and character generator operate in similar ways :

	VECTOR	CHARACTER
Dimensions	DELTAX, DELTAY	CSIZE, tilting
$\overline{DW}$ modulation	Type of line	Character code

USE OF LIGHT PEN CIRCUITRY

A rising edge on the LPCK input is used to sample the current display address in the XLP and YLP registers, provided that this edge is present in the frame immediately following loading of the 08_{16} or 09_{16} code into the CMD register.

Here, the frame origin is counted starting with the VB falling edge. With code 08_{16}, the $\overline{MW}$ output recopies the BLK signal from the frame origin up to the rising edge on the LPCK input, or when VB starts rising again, if the LPCK input remains low for the entire frame. With code 09_{16}, the $\overline{MW}$ output is not activated.

The YLP address is 8-bit coded since there are 256 display lines in each frame. The XLP address is 6-bit coded since there are 64 display cycles in each line.

These 6 bits left-justified in register XLP indicate the number of the segment (h = 0 to 63) to which the point indicated by the light pen belongs.

The address sampled into XLP corresponds to the current memory cycle. Dots detected by the light pen were addressed in the memory during the previous cycle. Hence, 1 should be subtracted from bit 2 in XLP register where the light pen electronic circuitry does not produce any additional delay.

If the rising edge on input LPCK occurs while VB is low, then the LSB in XLP is set high. This bit acts as a status signal which is reset to the low state by reading register XLP or YLP.

The rising edge first received (LPCK or VB) sets bit 0 in STATUS register high. An interrupt is initiated if bit 4 in CTRL1 is high.

When commands 08_{16} or 09_{16} have been decoded, bit 2 of the status register goes high (circuit ready for any further command) and bit 0 goes low (light pen operating sequence underway).

SCREEN BLANKING COMMANDS

Three commands (04_{16}, 06_{16}, 07_{16}) will set the whole display memory to a status corresponding to a "black display screen" condition. Another command ($0C_{16}$) may be used to set the whole memory to a status other than black (this condition being determined by bit 1 in register CTRL1).

The 4 commands outlined above use the planned scanning of the memory addresses achieved by the display stage. The X and Y registers are not affected by commands 04_{16} and $0C_{16}$. Hence, the time required is that corresponding to one frame (FMAT = 0 or $\overline{CK}$) or two frames (FMAT = 1 or CK). The time corresponding to the completion of the frame currently executing when the CMD register is loaded, should be added to the above time.

For the screen blanking process, the frame origin is counted starting with the VB falling edge.
The only signals affected here are the $\overline{DW}$ output, which remains low when VB is low, and the DIN output which is forced high where the 04_{16}, 06_{16} and 07_{16} commands are entered.

Such commands are activated without requiring action by WO input or bit 2 in register CTRL1. While these commands are executing, bit 2 in STATUS register remains low.

EXTERNAL REQUEST FOR DISPLAY MEMORY ACCESS ($\overline{MW}$ OUTPUT)

On writing code $0F_{16}$ into the CMD register, the $\overline{MW}$ output is set low by the circuitry, during the next free memory cycle.

Apart from the display and refresh periods, this cycle is the first complete cycle that occurs after input $\overline{E}$ is reset high.

During this cycle, those addresses output on DAD and MSL correspond to the X and Y register contents : $\overline{DW}$ is high, $\overline{ALL}$ is high.

Should the memory be engaged in a display or refresh operation, (which is the case when $\overline{ALL}$ is low), then this cycle is postponed to be executed after $\overline{ALL}$ is reset high. The maximum waiting time is thus 64 cycles.

The $\overline{MW}$ signal may be used e. g. for performing a read or write operation into a register located between the display memory and the microprocessor bus.

INTERRUPTS OPERATION

An interrupt may be initiated by three situations denoted by internal signals :

- Circuit ready for a further command
- Vertical blanking signal
- Light pen sequence completed.

These three signals appear in real time in the STATUS register (bits 0, 1, 2). Each signal is cross-referenced to a mask bit in the register CTRL1 (bits 4, 5, 6).

If the mask bit is high, the first rising edge that occurs on the interrupt initiating signal sets the related interrupt flip-flop circuit high.

The outputs from these three flip-flop circuits appear in the STATUS register (bits 4, 5, 6). If one flip-flop circuit is high, bit 7 in the STATUS register is high, and pin $\overline{IRQ}$ is forced low.

A read operation in the STATUS register at address 0_{16} resets its 4 MSBs low, after input $\overline{E}$ is reset high (a read at address F_{16} maintains their value).

The three interrupt control flip-flops are duplicated to prevent the loss of an interrupt coming during a read cycle of the STATUS register.

The status of bits 4, 5 and 6 corresponds to the interrupt control flip-flop circuit output, before input $\overline{E}$ goes low.

An interrupt coming during a read cycle of the STATUS register does not appear in bits 4, 5 and 6 during this read sequence, but during the following one. However, it may appear in bits 0, 1, 2 or on pin $\overline{IRQ}$.

TABLE 1 – REGISTER ADDRESS

ADDRESS REGISTER					REGISTER FUNCTIONS		Number of bits
Binary				Hexa	Read R/$\overline{W}$ = 1	Write R/$\overline{W}$ = 0	
A3	A2	A1	A0				
0	0	0	0	0	STATUS	CMD	8
0	0	0	1	1	CTRL 1 (Write control and interrupt control)		7
0	0	1	0	2	CTRL 2 (Vector and symbol type control)		4
0	0	1	1	3	CSIZE (Character size)		8
0	1	0	0	4	Reserved		—
0	1	0	1	5	DELTAX		8
0	1	1	0	6	Reserved		—
0	1	1	1	7	DELTAY		8
1	0	0	0	8	X MSBs		4
1	0	0	1	9	X LSBs		8
1	0	1	0	A	Y MSBs		4
1	0	1	1	B	Y LSBs		8
1	1	0	0	C	XLP (Light-pen)	Reserved	7
1	1	0	1	D	YLP (Light-pen)	Reserved	8
1	1	1	0	E	Reserved		—
1	1	1	1	F	STATUS	Reserved	8

Reserved : These addresses are reserved for future versions of the circuit. In read mode, output buffers D0-D7 force a high state on the data bus.

TABLE 2 – COMMAND REGISTER

b7		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
b6		0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
b5		0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
b4		0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
b3 b2 b1 b0		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0	0	Set bit 1 of CTRL1 : Pen selection	Vector generation (for b2, b1, b0 see small vector definition)	SPACE	0	@	P	`	p								
0 0 0 1	1	Clear bit 1 of CTRL 1 : Eraser selection		!	1	A	Q	a	q								
0 0 1 0	2	Set bit 0 of CTRL1 : Pen/Eraser down selection		"	2	B	R	b	r								
0 0 1 1	3	Clear bit 0 of CTRL 1 : Pen/Eraser up selection		#	3	C	S	c	s								
0 1 0 0	4	Clear screen		$	4	D	T	d	t								
0 1 0 1	5	X and Y registers reset to 0		%	5	E	U	e	u								
0 1 1 0	6	X and Y reset to 0 and clear screen		&	6	F	V	f	v								
0 1 1 1	7	Clear screen, set CSIZE to code "minsize" All other registers reset to 0 (except XLP, YLP)		'	7	G	W	g	w								
1 0 0 0	8	Light-pen initialization ($\overline{\text{WHITE}}$ forced low)	Special direction vectors (for b2, b1, b0 see small vector definition)	(	8	H	X	h	x								
1 0 0 1	9	Light-pen initialization		)	9	I	Y	i	y								
1 0 1 0	A	5 x 8 block drawing (size according to CSIZE)		*	:	J	Z	j	z								
1 0 1 1	B	4 x 4 block drawing (size according to CSIZE)		+	;	K	[	k	{								
1 1 0 0	C	Screen scanning : Pen or Eraser as defined by CTRL1		,	<	L	\	l	¦								
1 1 0 1	D	X register reset to 0		_	=	M	]	m	}								
1 1 1 0	E	Y register reset to 0		.	>	N	↑	n	¬								
1 1 1 1	F	Direct image memory access request for the next free cycle.		/	?	O	←	o	▒								

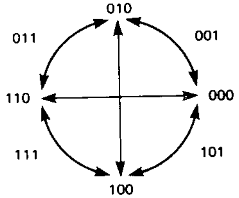
SMALL VECTOR DEFINITION :

b7	b6 b5	b4 b3	b2 b1 b0
1	|ΔX|	|ΔY|	Direction

Dimension

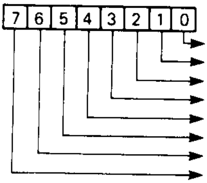
ΔX or ΔY		Vector length
0	0	0 step
0	1	1 step
1	0	2 steps
1	1	3 steps

Direction



OTHER REGISTERS

STATUS REGISTER (Read only)



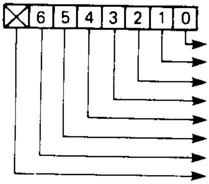
HIGH = light-pen sequence ended
HIGH = vertical blanking (idem on pin VB)
HIGH = ready for a new command ; LOW = busy
} These 3 bits are not latched and not masked

HIGH = pen out of display window (logical OR of the 6 MSBs of the X and Y registers)

HIGH = light-pen sequence ended IRQ (if enabled)
HIGH = vertical blanking IRQ (if enabled)
HIGH = ready for a new command IRQ (if enabled)
} These 3 bits are reset after a read cycle of the status register at address 0_{16}.

IRQ : logical OR of bits 4,5,6 ; HIGH when $\overline{IRQ}$ output is low.

CONTROL REGISTER 1 (Read/Write)

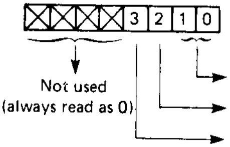


HIGH = pen down ; LOW = pen up (control $\overline{DW}$ output)
HIGH = pen ; LOW = eraser (control DIN output)
HIGH = high speed write : no video (BLK output is high, mini. of memory refresh cycles)
HIGH = cyclic screen (memory display write even if bit 3 of the status register is high)

HIGH = enable end of the light pen sequence IRQ
HIGH = enable VB IRQ
HIGH = enable ready for a new command IRQ
} Interrupt masks

Not used (0 for reading)

CONTROL REGISTER 2 (Read/Write)



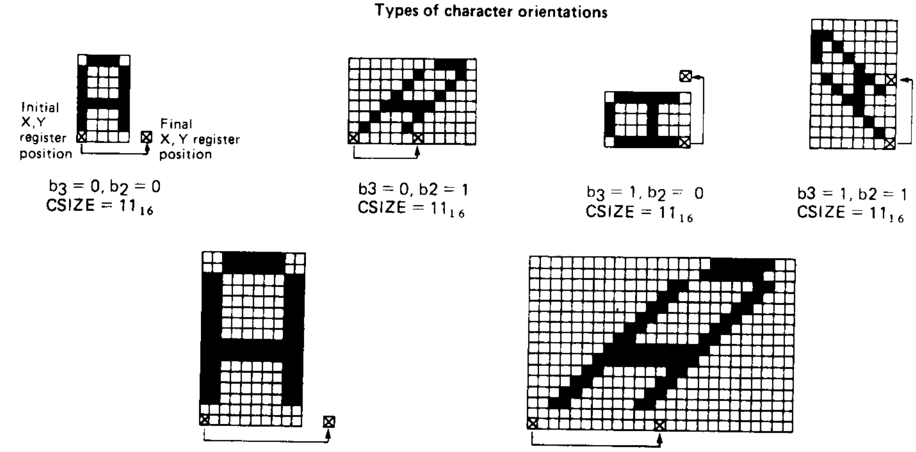
Type of vectors

HIGH = tilted character

HIGH = character on vertical axis

b1	b0	Type of vectors	
0	0	——— continuous	
0	1	------- dotted	2 dots on, 2 dots off
1	0	— — — dashed	4 dots on, 4 dots off
1	1	—·—· dotted-dashed	10 dots on, 2 dots off, 2 dots on, 2 dots off.

Types of character orientations



b3 = 0, b2 = 0
CSIZE = 11_{16}

b3 = 0, b2 = 1
CSIZE = 11_{16}

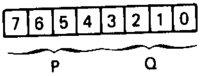
b3 = 1, b2 = 0
CSIZE = 11_{16}

b3 = 1, b2 = 1
CSIZE = 11_{16}

b3 = 0, b2 = 0
CSIZE = 22_{16}

b3 = 0, b2 = 1
CSIZE = 22_{16}

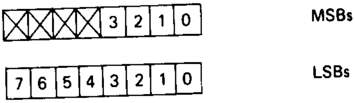
C-SIZE REGISTER (Read/Write)



P : Scaling factor on X axis
Q : Scaling factor on Y axis

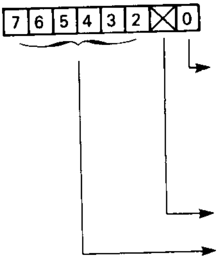
P and Q may take any value between 1 and 16. This value is given by the leftmost or rightmost 4 bits for P and Q respectively. Binary value (0) means 16.

X AND Y REGISTERS (Read/Write)



The 4 leftmost MSBs are always 0.

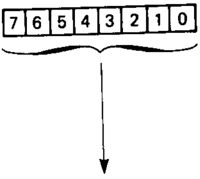
XLP and YLP REGISTERS



Status bit indicating if a rising edge has been applied on LPCK during the first complete frame following light-pen initialization. This bit is reset by a read on XLP or YLP.

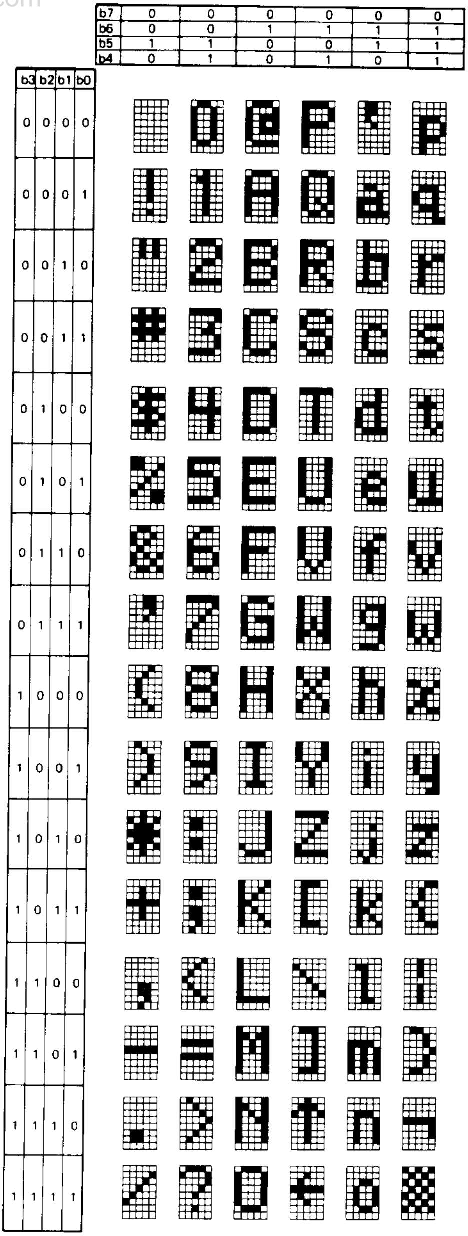
always 0

6 bit XLP value

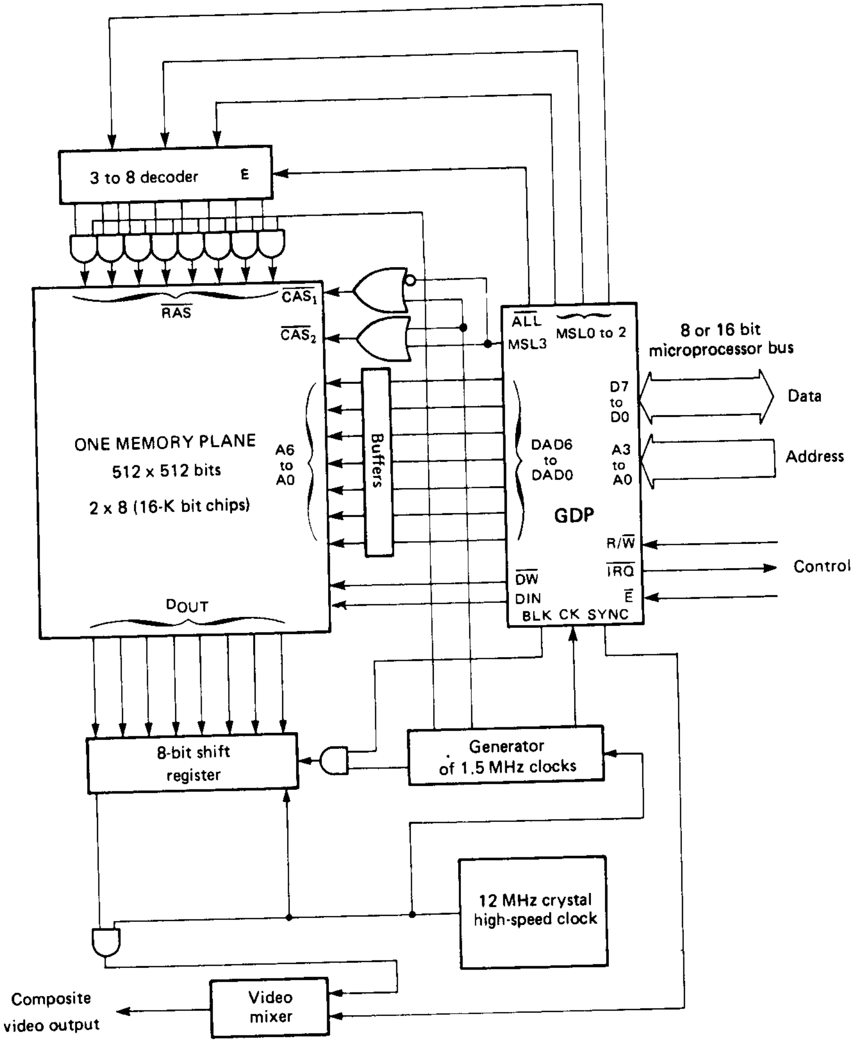


8 bit YLP value

ASCII CHARACTER GENERATOR (5 x 8 matrix)


b7 0 0 0 0 0 0
b6 0 0 1 1 1 1
b5 1 1 0 0 1 1
b4 0 1 0 1 0 1
b3 b2 b1 b0
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1

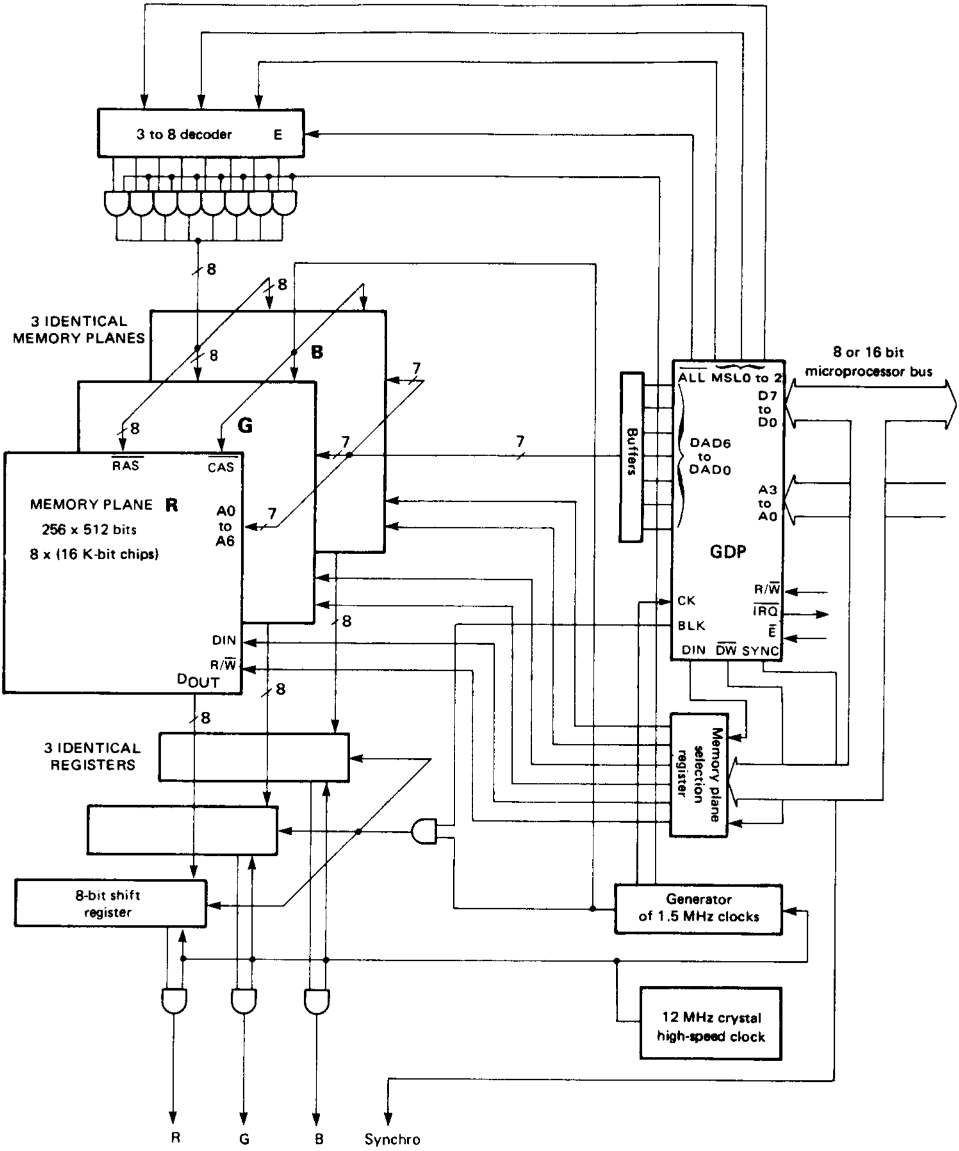
EXAMPLE OF A MONOCHROME APPLICATION : 512 x 512 or 416 x 512



Note : FMAT = V_{CC} : 512 x 512 resolution - 50 Hz 625 line interlaced scanning
FMAT = CK : 416 x 512 resolution - 60 Hz 525 line interlaced scanning.

EXAMPLE OF A COLOR APPLICATION : 208 x 512 or 256 x 512

Eight colours may be obtained from the three basic colours red (R), green (G), blue (B)

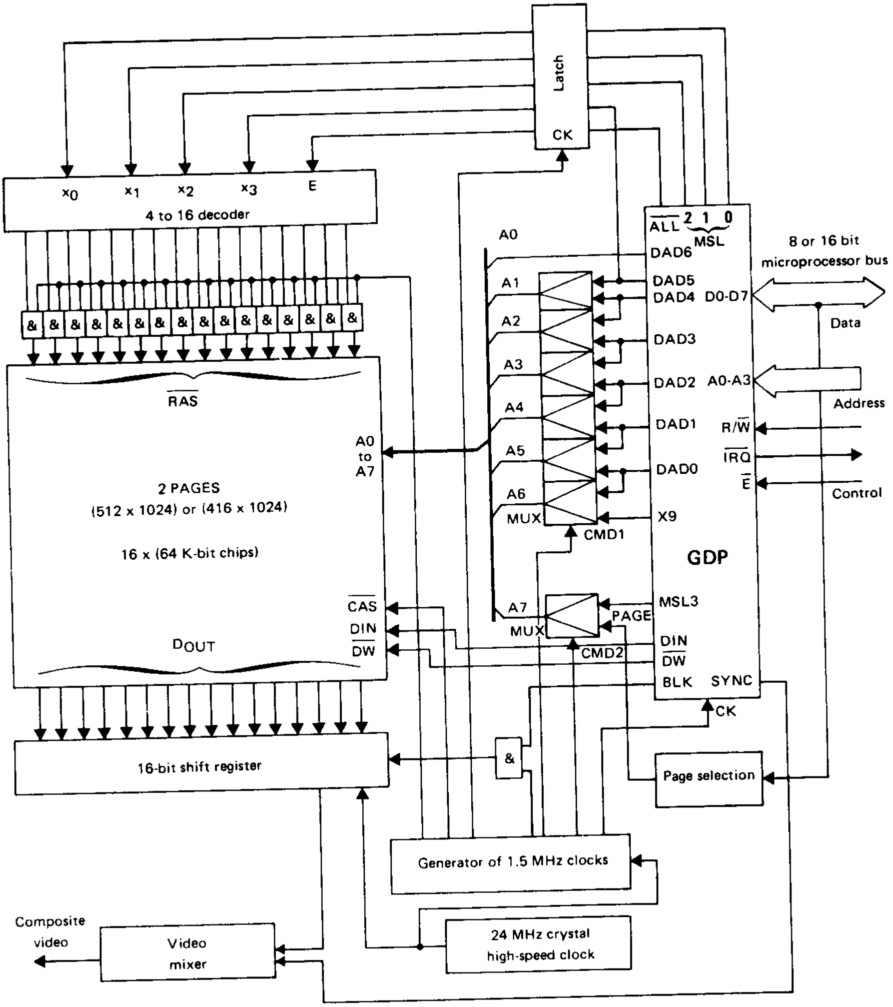


Note : FMAT = V_{SS} : 256 x 512 resolution - 50 Hz 625 line non interlaced scanning

FMAT = $\overline{CK}$: 208 x 512 resolution - 60 Hz 525 line non interlaced scanning.

EXAMPLE OF A MONOCHROME, MULTIPAGE APPLICATION : 512 x 1024 or 416 x 1024

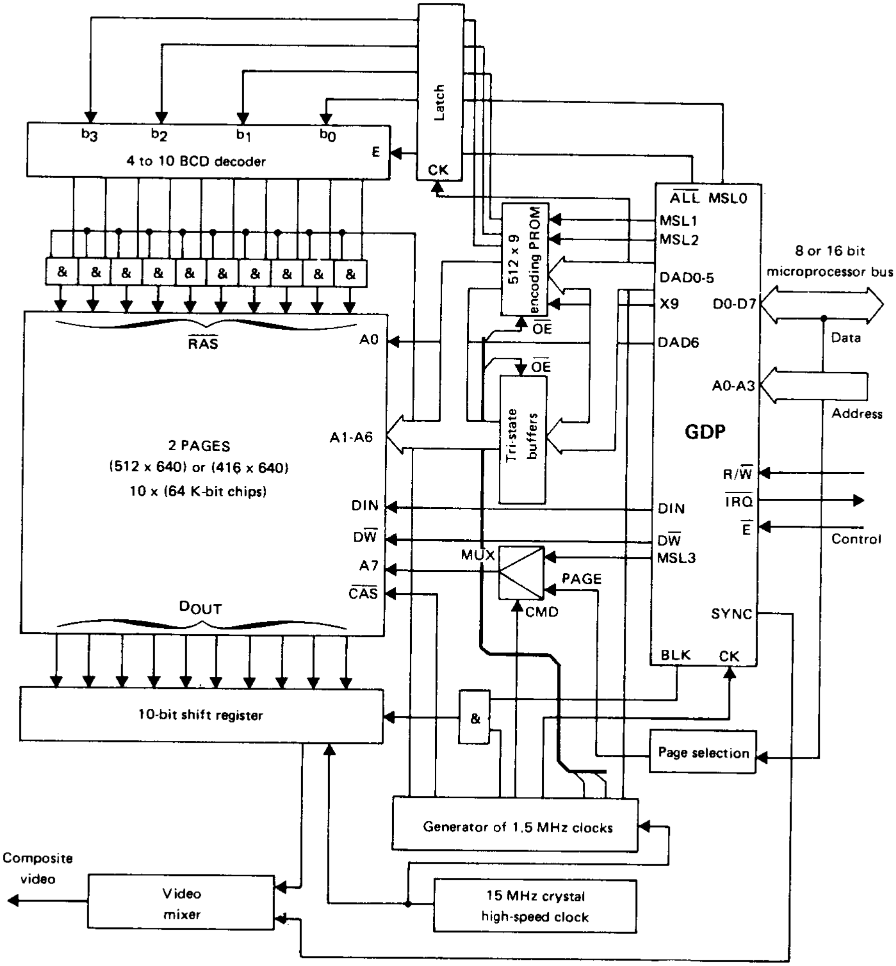
(See page 30 for MUX command law)



Note : FMAT = V_{CC} : 512 x 1024 resolution - 50 Hz 625 line interlaced scanning
FMAT = CK : 416 x 1024 resolution - 60 Hz 525 line interlaced scanning.

EXAMPLE OF A MONOCHROME, MULTIPAGE APPLICATION : 512 x 640 or 416 x 640

(See page 30 for PROM encoding)



Note : FMAT = V_{CC} : 512 x 640 resolution - 50 Hz 625 line interlaced scanning.
FMAT = CK : 416 x 640 resolution - 60 Hz 525 line interlaced scanning.

MUX COMMAND LAW

Following table indicates MUX command principles.

Selected MUX input				Output	Comment
Read cycles		Write cycles		Address bit	
$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}$		
DAD6	DAD6	DAD6	DAD6	A_0	No MUX
DAD5(h_0)	DAD5	DAD4(X_4)	DAD5	A_1	These six MUX are driven identically by CMD1
DAD4(h_1)	DAD4	DAD3(X_5)	DAD4	A_2	
DAD3(h_2)	DAD3	DAD2(X_6)	DAD3	A_3	
DAD2(h_3)	DAD2	DAD1(X_7)	DAD2	A_4	
DAD1(h_4)	DAD1	DAD0(X_8)	DAD1	A_5	
DAD0(h_5)	DAD0	X_9	DAD0	A_6	
MSL3	PAGE	MSL3	PAGE	A_7	Driven by CMD2

PROM CODING PRINCIPLES

The PROM coding consists in the use of the 10 horizontal address bits (X_0, - - - -, X_9) to access the 640 pixels (organized in 64 segments of 10 pixels each).

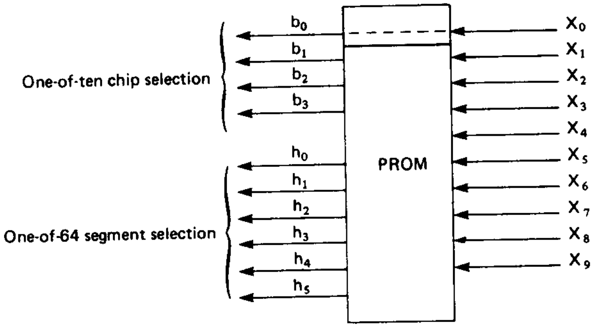
The 4 bits (b_0, b_1, b_2, b_3) are coding decimal numbers. Parity is maintained by BCD coding ; X_0 signal is therefore not coded inside the PROM and provides directly b_0.

Example : Considering the pixel with decimal abscissa X = 378 (17A in hexadecimal). This pixel is inside the 38th segment (h = 37 dec. or 25 hex.) with an abscissa x = 8.

The binary number 0101111010 (17A hex.) must be encoded into 1001011000 (258 hex.).

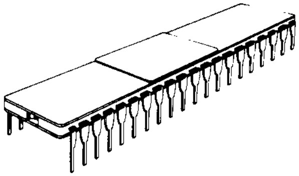
This principle allows transcoding of all horizontal address values. Transcoding must only be active (PROM selection) during write cycles ($\overline{ALL}$ = 1) when horizontal addresses are output ($\overline{RAS}$).

Note : This transcoding system may be adapted to other horizontal resolutions as 320, 384, 768. Horizontal resolutions are multiples of 64.

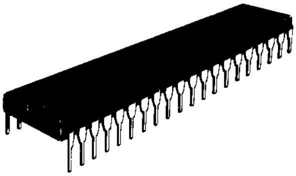


PHYSICAL DIMENSIONS

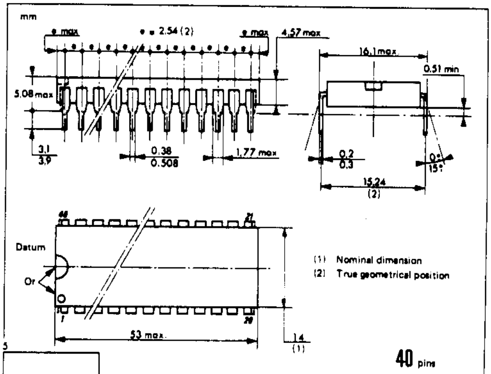
CB-182



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



DIN				
A51F CEI	D.A.T.A.	JEDEC	F.119 SITELESC	CB-182