

Overview

The DSP56374 is a high density CMOS device with 3.3 V inputs and outputs.

NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Finalized specifications may be published after further characterization and device qualifications are completed.

The DSP56374 supports digital audio applications requiring sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56374 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Freescale Semiconductor, Inc. (formerly Motorola) Symphony™ DSP family, as shown in [Figure 1](#). Significant architectural enhancements include a barrel shifter, 24-bit addressing, and direct memory access (DMA). The DSP56374 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock.

Table of Contents

Section	Page
1 Features	2
2 Documentation	4
3 Signal Groupings	4
4 Maximum Ratings	24
5 Power Requirements	25
6 Thermal Characteristics	26
7 DC Electrical Characteristics	26
8 AC Electrical Characteristics	27
9 Internal Clocks	27
10 External Clock Operation	29
11 Reset, Stop, Mode Select, and Interrupt Timing	30
12 Serial Host Interface SPI Protocol Timing	34
13 Serial Host Interface (SHI) I2C Protocol Timing	40
14 Programming the Serial Clock ..	42
15 Enhanced Serial Audio Interface Timing	43
16 Timer Timing	48
17 GPIO Timing	48
18 JTAG Timing	50
19 Watchdog Timer Timing	52
Appendix A Package Information ..	53
Appendix B IBIS Model	63

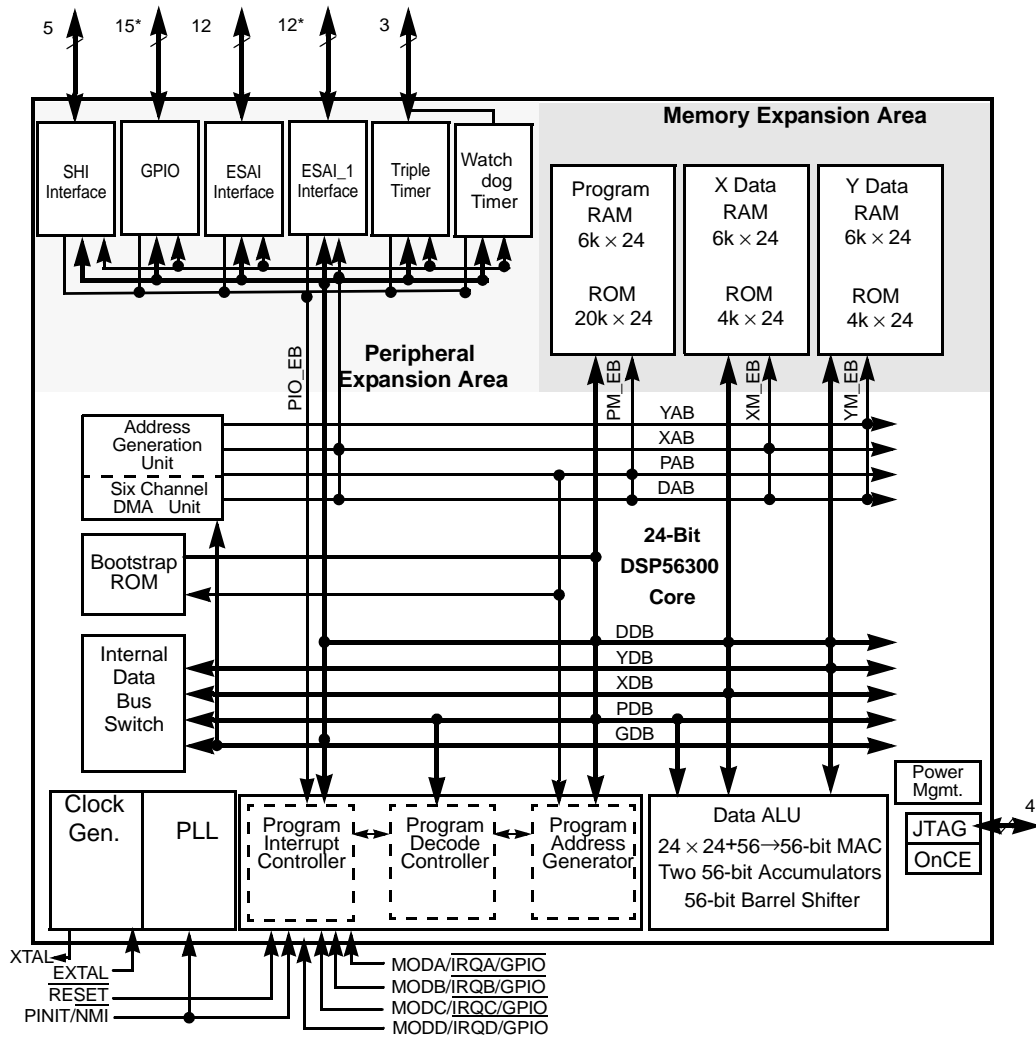
Data Sheet Conventions

This data sheet uses the following conventions:

- OVERBAR** Used to indicate a signal that is active when pulled low (For example, the **RESET** pin is active when low.)
- “asserted” Means that a high true (active high) signal is high or that a low true (active low) signal is low
- “deasserted” Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage*
	$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
	PIN	True	Asserted	V_{IH} / V_{OH}
	PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL} , V_{OL} , V_{IH} , and V_{OH} are defined by individual product specifications.



* ESAI_1 and dedicated GPIO pins are not available in the 52-pin package.

Figure 1. DSP56374 Block Diagram

1 Features

1.1 DSP56300 Modular Chassis

- 150 Million Instructions Per Second (MIPS) with a 150 MHz clock at an internal logic supply (QVDDL) of 1.25 V.
- Object Code Compatible with the 56K core.
- Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter; 16 bit arithmetic support.
- Program Control with position independent code support.
- Six-channel DMA controller.
- Provides a wide range of frequency multiplications (1 to 255), predivider factors (1 to 31), PLL feedback multiplier (2 or 4), Output divide factor (1, 2 or 4) and a power-saving clock divider (2^i ; $i = 0$ to 7) to reduce clock noise
- Internal address tracing support and OnCE for Hardware/Software debugging.
- JTAG port, supporting boundary scan, compliant to IEEE 1149.1.
- Very low-power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low-power standby modes.

1.2 On-chip Memory Configuration

- 6Kx24 Bit Y-Data RAM and 4Kx24 Bit Y-Data ROM.
- 6Kx24 Bit X-Data RAM and 4Kx24 Bit X-Data ROM.
- 20Kx24 Bit Program and Bootstrap ROM including a PROM patching mechanism.
- 6Kx24 Bit Program RAM.
- Various memory switches are available. See memory table below.

Table 1. DSP56374 Memory Switch Configurations

Bit Settings			Memory Sizes (24-bit words)					
MSW1	MSW0	MS	Prog RAM	X Data RAM	Y Data RAM	Prog ROM	X Data ROM	Y Data ROM
X	X	0	6K	6K	6K	20K	4K	4K
0	0	1	2K	10K	6K	20K	4K	4K
0	1	1	4K	8K	6K	20K	4K	4K
1	0	1	8K	4K	6K	20K	4K	4K
1	1	1	10K	4K	4K	20K	4K	4K

1.3 Peripheral modules

- Enhanced Serial Audio Interface (ESAI): up to 4 receiver pins and up to 6 transmitter pins, master or slave. I²S, Sony, AC97, network and other programmable protocols.
- Enhanced Serial Audio Interface I (ESAI_1): up to 4 receiver pins and up to 6 transmitter pins, master or slave. I²S, Sony, AC97, network and other programmable protocols. *Note: Available in the 80 pin package only*
- Serial Host Interface (SHI): SPI and I²C protocols, 10-word receive FIFO, support for 8, 16 and 24-bit words. Three noise reduction filter modes.
- Triple Timer module (TEC).
- Most pins of unused peripherals may be programmed as GPIO pins. Up to 47 pins can be configured as GPIO on the 80 pin package and 20 pins on the 52 pin package.
- Hardware Watchdog Timer

1.4 Packages

- 80-pin and 52-pin plastic LQFP packages.

2 Documentation

Table 2 lists the documents that provide a complete description of the DSP56374 and are required to design properly with the part. Documentation is available from a local Freescale Semiconductor, Inc. (formerly Motorola) distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 2. DSP56374 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56374 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56374UM/D
DSP56374 Technical Data Sheet	Electrical and timing specifications; pin and package descriptions	DSP56374
DSP56374 Product Brief	Brief description of the chip	DSP56374PB/D

3 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 3..

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 3. DSP56374 Functional Signal Groupings

Functional Group	Number of Signals ¹	Detailed Description	
Power (V_{DD})	11	Table 15.	
Ground (GND)	9	Table 5.	
Scan Pins	1	Table 6.	
Clock and PLL	3	Table 7.	
Interrupt and mode control	Port H ²	5	Table 8.
SHI	Port H ²	5	Table 9.
ESAI	Port C ⁴	12	Table 10.
ESAI_1	Port E ⁵	12	Table 11.
Dedicated GPIO	Port G ³	15	Table 12.
Timer		3	Table 13.
JTAG/OnCE Port		4	Table 14.
Note: <ol style="list-style-type: none"> 1. Pins are not 5 V. tolerant unless noted. 2. Port H signals are the GPIO port signals which are multiplexed with the MOD and \overline{HREQ} signals. 3. Port G signals are the dedicated GPIO port signals. 4. Port C signals are the GPIO port signals which are multiplexed with the ESAI signals. 5. Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals. 			

3.1 Power

Table 4. Power Inputs

Power Name	Description
PLLA_VDD (1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V _{DD} power rail. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND. PLLA_VDD requires a filter as shown in Figure 21 and Figure 22 below. See the DSP56374 technical data sheet for additional details.
PLLP_VDD(1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V _{DD} power rail. The user must provide adequate external decoupling capacitors between PLLP_VDD and PLLP_GND.
PLLD_VDD (1)	PLL Power— The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V _{DD} power rail. The user must provide adequate external decoupling capacitors between PLLD_VDD and PLLD_GND.
CORE_VDD (4)	Core Power—The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V _{DD} power rail. The user must provide adequate external decoupling capacitors.
IO_VDD (80-pin 4) (52-pin 3)	SHI, ESAI, ESAI_1, WDT and Timer I/O Power —The voltage (3.3 V) should be well-regulated, and the input should be provided with an extremely low impedance path to the 3.3 V _{DD} power rail. This is an isolated power for the SHI, ESAI, ESAI_1, WDT and Timer I/O. The user must provide adequate external decoupling capacitors.

3.2 Ground

Table 5. Grounds

Ground Name	Description
PLLA_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND.
PLLP_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLP_VDD and PLLP_GND.
PLLD_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLD_VDD and PLLD_GND.
CORE_GND(4)	Core Ground—The Core ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
IO_GND(2)	SHI, ESAI, ESAI_1, WDT and Timer I/O Ground—IO_GND is the ground for the SHI, ESAI, ESAI_1, WDT and Timer I/O. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

3.3 SCAN

Table 6. SCAN signals

Signal Name	Type	State during Reset	Signal Description
SCAN	Input	Input	SCAN—Manufacturing test pin. This pin must be connected to ground.

3.4 Clock and PLL

Table 7. Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	External Clock / Crystal Input—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL.
XTAL	Output	Chip Driven	Crystal Output—Connects the internal Crystal Oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.
PINIT/ $\overline{\text{NMI}}$	Input	Input	<p>PLL Initial/Nonmaskable Interrupt—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de-assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to the internal system clock.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>

3.5 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is de-asserted, these inputs are hardware interrupt request lines.

Table 8. Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/ $\overline{\text{IRQA}}$	Input	MODA Input	<p>Mode Select A/External Interrupt Request A—MODA/$\overline{\text{IRQA}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/$\overline{\text{IRQA}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is de-asserted. If the processor is in the stop standby state and the MODA/$\overline{\text{IRQA}}$ pin is pulled to GND, the processor will exit the stop state.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>

Table 8. Interrupt and Mode Control (Continued)

Signal Name	Type	State during Reset	Signal Description
PH0	Input, output, or disconnected		Port H0—When the MODA/IRQA is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODB/ $\overline{\text{IRQB}}$	Input	MODB Input	<p>Mode Select B/External Interrupt Request B—MODB/$\overline{\text{IRQB}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/$\overline{\text{IRQB}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is de-asserted.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>
PH1	Input, output, or disconnected		Port H1—When the MODB/IRQB is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODC/ $\overline{\text{IRQC}}$	Input	MODC Input	<p>Mode Select C/External Interrupt Request C—MODC/$\overline{\text{IRQC}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/$\overline{\text{IRQC}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is de-asserted.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>
PH2	Input, output, or disconnected		Port H2—When the MODC/IRQC is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODD/ $\overline{\text{IRQD}}$	Input	MODD Input	<p>Mode Select D/External Interrupt Request D—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is de-asserted.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>
PH3	Input, output, or disconnected		Port H3—When the MODD/IRQD is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.

Table 8. Interrupt and Mode Control (Continued)

Signal Name	Type	State during Reset	Signal Description
RESET	Input	Input	<p>Reset—$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is de-asserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>

3.6 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I²C mode.

Table 9. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	<p>SPI Serial Clock—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{\text{SS}}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.</p>
SCL	Input or output		<p>I²C Serial Clock—SCL carries the clock for I²C bus transactions in the I²C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{DD} through an external pull-up resistor according to the I²C specifications.</p> <p>This signal is tri-stated during hardware, software, and individual reset.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>

Table 9. Serial Host Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MISO	Input or output	Tri-stated	SPI Master-In-Slave-Out—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when \overline{SS} is de-asserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output		<p>I²C Data and Acknowledge—In I²C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{DD} through a pull-up resistor. SDA carries the data for I²C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event.</p> <p>This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>
MOSI	Input or output	Tri-stated	SPI Master-Out-Slave-In—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		<p>I²C Slave Address 0—This signal uses a Schmitt-trigger input when configured for the I²C mode. When configured for I²C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I²C master mode.</p> <p>This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>
SS	Input	Ignored Input	SPI Slave Select—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept de-asserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If \overline{SS} is de-asserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		<p>I²C Slave Address 2—This signal uses a Schmitt-trigger input when configured for the I²C mode. When configured for the I²C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I²C master mode.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>

Table 9. Serial Host Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
HREQ	Input or Output	Tri-stated	<p>Host Request—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode.</p> <p>When configured for the slave mode, $\overline{\text{HREQ}}$ is asserted to indicate that the SHI is ready for the next data word transfer and de-asserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{\text{HREQ}}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{\text{HREQ}}$ to proceed to the next transfer. This pin can also be programmed as GPIO.</p> <p>Port H4—When $\overline{\text{HREQ}}$ is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>This pin has an internal pull up resistor.</p> <p>This input is 5 V tolerant.</p>
PH4	Input, output, or disconnected		

3.7 Enhanced Serial Audio Interface

Table 10. Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or output	GPIO disconnected	<p>High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.</p>
PC2	Input, output, or disconnected		<p>Port C2—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This pin has an internal pull up resistor.</p> <p>This input is 5 V tolerant.</p>

Table 10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
HCKT	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, output, or disconnected	GPIO disconnected	<p>Port C5—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>This pin has an internal pull up resistor. This input is 5 V tolerant.</p>
FSR	Input or output	GPIO disconnected	<p>Frame Sync for Receiver—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1).</p> <p>When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.</p>
PC1	Input, output, or disconnected	GPIO disconnected	<p>Port C1—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant.</p>

Table 10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
FST	Input or output	GPIO disconnected	Frame Sync for Transmitter—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, output, or disconnected	GPIO disconnected	<p>Port C4—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant.</p>
SCKR	Input or output	GPIO disconnected	<p>Receiver Serial Clock—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1).</p> <p>When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.</p>
PC0	Input, output, or disconnected	GPIO disconnected	<p>Port C0—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant.</p>
SCKT	Input or output	GPIO disconnected	<p>Transmitter Serial Clock—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.</p>
PC3	Input, output, or disconnected	GPIO disconnected	<p>Port C3—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant.</p>

Table 10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5	Output	GPIO disconnected	Serial Data Output 5—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		Serial Data Input 0—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, output, or disconnected		Port C6—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO4	Output	GPIO disconnected	Serial Data Output 4—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		Serial Data Input 1—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected		Port C7—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3	Output	GPIO disconnected	Serial Data Output 3 —When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register.
SDI2	Input		Serial Data Input 2 —When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register.
PC8	Input, output, or disconnected		Port C8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		Serial Data Input 3—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		Port C9—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1	Output	GPIO disconnected	Serial Data Output 1—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		Port C10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0	Output	GPIO disconnected	Serial Data Output 0—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		Port C11—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

3.8 Enhanced Serial Audio Interface_1

Table 11. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR_1	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PE2	Input, output, or disconnected		<p>Port E2—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant.</p>
HCKT_1	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PE5	Input, output, or disconnected		<p>Port E5—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant.</p>

Table 11. Enhanced Serial Audio Interface_1 Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	<p>Frame Sync for Receiver_1—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR_1 pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1).</p> <p>When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR_1 register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR_1 register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.</p>
PE1	Input, output, or disconnected	GPIO disconnected	<p>Port E1—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant</p>
FST_1	Input or output	GPIO disconnected	<p>Frame Sync for Transmitter_1—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST_1 is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI_1 transmit clock control register (TCCR_1).</p>
PE4	Input, output, or disconnected	GPIO disconnected	<p>Port E4—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.</p> <p>The default state after reset is GPIO disconnected.</p> <p>Internal Pull down resistor. This input is 5 V tolerant.</p>

Table 11. Enhanced Serial Audio Interface_1 Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR_1	Input or output	GPIO disconnected	Receiver Serial Clock_1—SCKR_1 provides the receiver serial bit clock for the ESAI_1. The SCKR_1 operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR_1 register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR_1 register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE0	Input, output, or disconnected	GPIO disconnected	Port E0—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
SCKT_1	Input or output	GPIO disconnected	Transmitter Serial Clock_1—This signal provides the serial bit rate clock for the ESAI_1. SCKT_1 is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected	GPIO disconnected	Port E3—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 11. Enhanced Serial Audio Interface_1 Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5_1	Output	GPIO disconnected	Serial Data Output 5_1—When programmed as a transmitter, SDO5_1 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		Serial Data Input 0_1—When programmed as a receiver, SDI0_1 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected		Port E6—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
SDO4_1	Output	GPIO disconnected	Serial Data Output 4_1—When programmed as a transmitter, SDO4_1 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		Serial Data Input 1_1—When programmed as a receiver, SDI1_1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected		Port E7—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3_1	Output	GPIO disconnected	Serial Data Output 3 —When programmed as a transmitter, SDO3_1 is used to transmit data from the TX3 serial transmit shift register.
SDI2_1	Input		Serial Data Input 2 —When programmed as a receiver, SDI2_1 is used to receive serial data into the RX2 serial receive shift register.
PE8	Input, output, or disconnected		Port E8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2_1	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2_1 is used to transmit data from the TX2 serial transmit shift register.
SDI3_1	Input		Serial Data Input 3—When programmed as a receiver, SDI3_1 is used to receive serial data into the RX3 serial receive shift register.
PE9	Input, output, or disconnected		Port E9—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1_1	Output	GPIO disconnected	Serial Data Output 1—SDO1_1 is used to transmit data from the TX1 serial transmit shift register.
PE10	Input, output, or disconnected		Port E10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0_1	Output	GPIO disconnected	Serial Data Output 0—SDO0_1 is used to transmit data from the TX0 serial transmit shift register.
PE11	Input, output, or disconnected		Port E11—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

3.9 Dedicated GPIO - Port G

Table 12. Dedicated GPIO - Port G Signals

Signal Name	Type	State During Reset	Signal Description
PG0	Input, output, or disconnected	GPIO disconnected	Port G0—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 12. Dedicated GPIO - Port G Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
PG1	Input, output, or disconnected	GPIO disconnected	Port G1—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG2	Input, output, or disconnected	GPIO disconnected	Port G2—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG3	Input, output, or disconnected	GPIO disconnected	Port G3—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG4	Input, output, or disconnected	GPIO disconnected	Port G4—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG5	Input, output, or disconnected	GPIO disconnected	Port G5—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG6	Input, output, or disconnected	GPIO disconnected	Port G6—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG7	Input, output, or disconnected	GPIO disconnected	Port G7—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG8	Input, output, or disconnected	GPIO disconnected	Port G8—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 12. Dedicated GPIO - Port G Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
PG9	Input, output, or disconnected	GPIO disconnected	Port G9—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG10	Input, output, or disconnected	GPIO disconnected	Port G10—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG11	Input, output, or disconnected	GPIO disconnected	Port G11—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG12	Input, output, or disconnected	GPIO disconnected	Port G12—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG13	Input, output, or disconnected	GPIO disconnected	Port G13—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG14	Input, output, or disconnected	GPIO disconnected	Port G14—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

3.10 Timer

Table 13. Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	GPIO Input	<p>Timer 0 Schmitt-Trigger Input/Output—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output.</p> <p>The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input.</p> <p>Internal Pull down resistor. This input is 5 V tolerant</p>
TIO1	Input or Output	Watchdog Timer Output	<p>Timer 1 Schmitt-Trigger Input/Output—When timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output.</p> <p>The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 1 control/status register (TCSR1). If TIO1 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input.</p>
WDT	Output		<p>WDT—When this pin is configured as a hardware watchdog timer pin, this signal is asserted low when the hardware watchdog timer counts down to zero.</p> <p>Internal Pull down resistor. This input is 5 V tolerant</p>
TIO2	Input or Output	PLOCK Output	<p>Timer 2 Schmitt-Trigger Input/Output—When timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output.</p> <p>The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer control/status register (TCSR2). If TIO2 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input .</p>

Table 13. Timer Signal (Continued)

Signal Name	Type	State during Reset	Signal Description
PLOCK	Output		<p>PLOCK—When this pin is configured as a PLL lock pin, this signal is asserted high when the on-chip PLL enabled and locked and de-asserted when the PLL enabled and unlocked. This pin is also asserted high when the PLL is disabled.</p> <p>Internal Pull down resistor. This input is 5 V tolerant</p>

3.11 JTAG/OnCE Interface

Table 14. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	<p>Test Clock—TCK is a test clock input signal used to synchronize the JTAG test logic.</p> <p>Internal Pull up resistor. This input is 5 V tolerant.</p>
TDI	Input	Input	<p>Test Data Input—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK.</p> <p>Internal Pull up resistor. This input is 5 V tolerant.</p>
TDO	Output	Tri-stated	<p>Test Data Output—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.</p>
TMS	Input	Input	<p>Test Mode Select—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK.</p> <p>Internal Pull up resistor. This input is 5 V tolerant.</p>

4 Maximum Ratings

Caution

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{DD}). The suggested value for a pullup or pulldown resistor is 10 k Ω .

NOTE

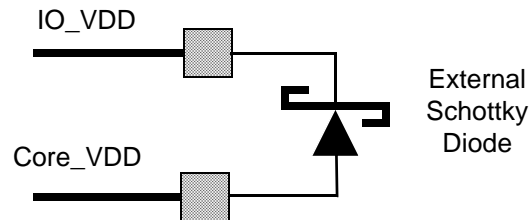
In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 15. Maximum Ratings

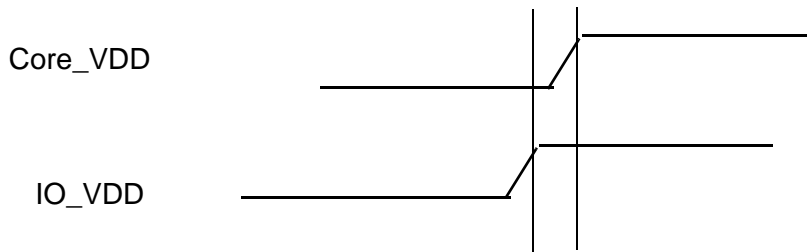
Rating ¹	Symbol	Value ^{1, 2}	Unit
Supply Voltage	V_{CORE_VDD} , V_{PLLD_VDD}	−0.3 to + 1.6	V
	V_{PLL_VDD} , V_{IO_VDD} , V_{PLLA_VDD}	−0.3 to + 4.0	V
Maximum CORE_VDD power supply ramp time ⁴	T_r	10	ms
All “5.0V tolerant” input voltages	V_{IN}	GND – 0.3 to 6V	V
Current drain per pin excluding V_{DD} and GND(Except for pads listed below)	I	12	mA
SCK_SCL	I_{SCK}	16	mA
TDO	I_{JTAG}	24	ma
Operating temperature range ³	T_J	80 LQFP = 90 52 LQFP = 95	°C
Storage temperature	T_{STG}	−55 to +125	°C
ESD protected voltage (Human Body Model)		1250	V
ESD protected voltage (Machine Model)		75	V
Note: <ol style="list-style-type: none"> 1. GND = 0 V, $T_J = 0^\circ\text{C}$ to 95°C (52 LQFP) / 0°C to 90°C (80 LQFP), CL = 50pF 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device. 3. Operating temperature qualified for consumer applications. $T_J = T_A + \theta_{JA} \times \text{Power}$. 4. If the power supply ramp to full supply time is longer than 10 ms, the POR circuitry will not operate correctly, causing erroneous operation. 			

5 Power Requirements

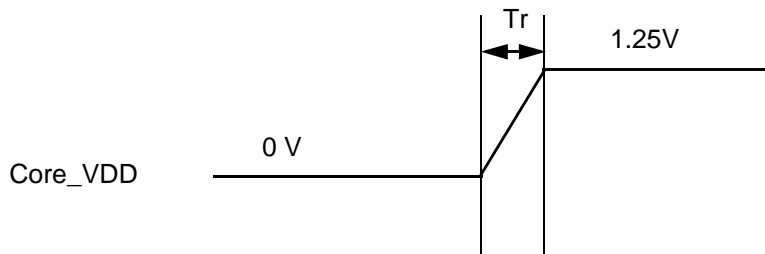
To prevent high current conditions due to possible improper sequencing of the power supplies, the connection shown below is recommended to be made between the DSP56374 IO_VDD and Core_VDD power pins.



To prevent a high current condition upon power up, the IO_VDD must be applied ahead of the Core_VDD as shown below if the external Schottky is not used.



For correct operation of the internal power on reset logic, the Core_VDD ramp rate (T_r) to full supply must be less than 10 ms. This is shown below.



6 Thermal Characteristics

Table 16. Thermal Characteristics

Characteristic	Symbol	LQFP Values	Unit
Natural Convection, Junction-to-ambient thermal resistance ^{1,2}	$R_{\theta JA}$ or θ_{JA}	68 (52 LQFP) 50 (80 LQFP)	$^{\circ}\text{C}/\text{W}$
Junction-to-case thermal resistance ³	$R_{\theta JC}$ or θ_{JC}	17 (52 LQFP) 11 (80 LQFP)	$^{\circ}\text{C}/\text{W}$
Note: <ol style="list-style-type: none"> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). 			

7 DC Electrical Characteristics

Table 17. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltages <ul style="list-style-type: none"> Core (Core_VDD) PLL (PLLD_VDD) 	V_{DD}	1.2	1.25	1.3	V
Supply voltages <ul style="list-style-type: none"> VIO_VDD PLL (PLL_P_VDD) PLL (PLLA_VDD) 	V_{DDIO}	3.14	3.3	3.46	V
Input high voltage <ul style="list-style-type: none"> All pins 	V_{IH}	2.0	—	$V_{IO_VDD}+2\text{V}$	V
Note: All 3.3 volt supplies must rise prior to the rise of the 1.25 volt supplies to avoid a high current condition and possible system damage.					
Input low voltage <ul style="list-style-type: none"> All pins 	V_{IL}	-0.3	—	0.8	V
Input leakage current	I_{IN}	—	—	± 84	μA
Clock pin Input Capacitance (EXTAL)	C_{IN}		4.7		pF
High impedance (off-state) input current (@ 3.46V)	I_{TSI}	-10	—	84	μA
Output high voltage $I_{OH} = -5 \text{ mA}$. XTAL Pin $I_{OH} = -10 \text{ mA}$	V_{OH}	2.4	—	—	V
Output low voltage $I_{OH} = 5 \text{ mA}$. XTAL Pin $I_{OH} = 10 \text{ mA}$	V_{OL}	—	—	0.4	V

Table 17. DC Electrical Characteristics (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
Internal supply current ¹ (core only) at internal clock of 150MHz					
• In Normal mode	I _{CCI}	—	65	100	mA
• In Wait mode	I _{CCW}	—	16	40	mA
• In Stop mode ²	I _{CCS}	—	1.2	15	mA
Supply current ¹ (I/O only) at internal clock of 150MHz					
• In Normal mode	I _{CCI}	—	35	60	mA
• In Wait mode	I _{CCW}	—	36	50	mA
• In Stop mode ²	I _{CCS}	—	1.2	20	uA
Input capacitance	C _{IN}	—	—	10	pF
Note:					
1. The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V _{CORE_VDD} = 1.25V, V _{DD_IO} = 3.3V at T _J = 25°C. Maximum internal supply current is measured with V _{CORE_VDD} = 1.30V, V _{IO_VDD} = 3.46V at T _J = 115°C.					
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).					

8 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56374 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 1.0V and 1.8V, respectively.

9 Internal Clocks

Table 18. INTERNAL CLOCKS²

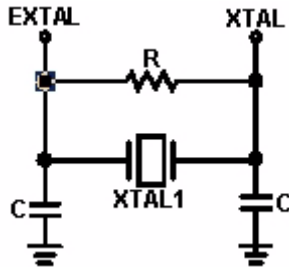
No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition	
1	Comparison Frequency	Fref	5	—	20	MHz	Fref = FIN/NR	
2	Input Clock Frequency	FIN	Fref*NR					NR is input divider value
3	Output clock Frequency (with PLL enabled ^[1])	FOUT	75	(Ef × MF × FM) / (PDF × DF × OD)	150	MHz	FOUT = FVCO/NO where NO is output divider value	
4	Output clock Frequency (with PLL disabled ^[1])	FOUT	—	Ef	150	MHz	—	
5	Duty Cycle	—	40	50	60	%	FVCO = 300MHz ~ 600MHz	

Table 18. INTERNAL CLOCKS² (Continued)

No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Note: 1.	DF = Division Factor Ef = External frequency MF = Multiplication Factor PDF = Predivision Factor FM= Frequency Multiplier OD = Output Divider 2. For details of internal clock operation, see Chapter 5 of Users Guide.						

10 External Clock Operation

The DSP56374 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; an example is shown below.



Suggested component values:

$$f_{osc} = 24.576 \text{ MHz}$$

$$R = 1 \text{ M} \pm 10\%$$

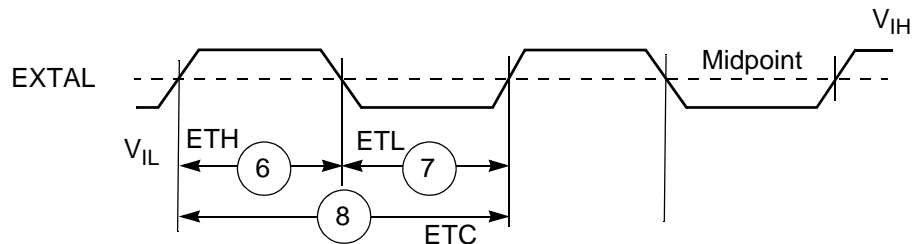
$$C (\text{EXTAL}) = 18 \text{ pF}$$

$$C (\text{XTAL}) = 47 \text{ pF}$$

Calculations are for a 12 - 49 MHz crystal with the following parameters:

- shunt capacitance (C_0) of 10 pF - 12 pF
- series resistance 40 Ohm
- drive level of 10 μW

If the DSP56374 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 2). When the external square wave source connects to EXTAL, the XTAL pin is not used.



Note: The midpoint is $0.5 (V_{IH} + V_{IL})$.

Figure 2. External Clock Timing

Table 19. Clock Operation

No.	Characteristics	Symbol	Min	Max	Units
6	EXTAL input high ¹ (40% to 60% duty cycle)	Eth	3.33	50	ns
7	EXTAL input low ¹ (40% to 60% duty cycle)	Etl	3.33	50	ns
8	EXTAL cycle time <ul style="list-style-type: none"> • With PLL disabled • With PLL enabled 	Etc	6.67 50	inf 200	ns

Table 19. Clock Operation (Continued)

No.	Characteristics	Symbol	Min	Max	Units
9	Instruction cycle time= $I_{CYC} = T_C^4$ <ul style="list-style-type: none"> • With PLL disabled • With PLL enabled 	lcyc	6.67 6.67	inf 13.33	ns
Note: <ol style="list-style-type: none"> 1. Measured at 50% of the input transition. 2. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met. 					

11 Reset, Stop, Mode Select, and Interrupt Timing

Table 20. Reset, Stop, Mode Select, and Interrupt Timing

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value ³	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration ⁴ <ul style="list-style-type: none"> • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled 	$2 \times T_C$	13.4	—	ns
		$2 \times T_C$	13.4	—	ns
13	Syn reset deassert delay time <ul style="list-style-type: none"> • Minimum • Maximum (PLL enabled) 	$2 \times T_C$	13.4	—	ns
		$(2 \times T_C) + T_{\text{LOCK}}$	5.0	—	ms
14	Mode select setup time		10.0	—	ns
15	Mode select hold time		10.0	—	ns
16	Minimum edge-triggered interrupt request assertion width	$2 \times T_C$	13.4	—	ns
17	Minimum edge-triggered interrupt request deassertion width	$2 \times T_C$	13.4	—	ns
18	Delay from interrupt trigger to interrupt code execution	$10 \times T_C + 5$	72	—	ns

Table 20. Reset, Stop, Mode Select, and Interrupt Timing (Continued)

No.	Characteristics	Expression	Min	Max	Unit
19	Duration of level sensitive \overline{IRQA} assertion to ensure interrupt service (when exiting Stop) ^{1, 2, 3}				
	• PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$9+(128 \times T_C)$	854	—	μs
	• PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$25 \times T_C$	165	—	ns
	• PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$9+(128 \times T_C) + T_{\text{LOCK}}$	5.7		ms
	• PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$(25 \times T_C) + T_{\text{LOCK}}$	5		ms
20	• Delay from \overline{IRQA} , \overline{IRQB} , \overline{IRQC} , \overline{IRQD} , \overline{NMI} assertion to general-purpose transfer output valid caused by first interrupt instruction execution ¹	$10 \times T_C + 3.0$		69.0	ns
21	Interrupt Requests Rate ¹				
	• ESAI, ESAI_1, SHI, Timer	$12 \times T_C$	—	80.0	ns
	• DMA	$8 \times T_C$	—	53.0	ns
	• \overline{IRQ} , \overline{NMI} (edge trigger)	$8 \times T_C$	—	53.0	ns
	• \overline{IRQ} (level trigger)	$12 \times T_C$	—	80.0	ns
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, SHI	$6 \times T_C$	—	40.0	ns
	• Data write to ESAI, ESAI_1, SHI	$7 \times T_C$	—	46.7	ns
	• Timer	$2 \times T_C$	—	13.4	ns
	• \overline{IRQ} , \overline{NMI} (edge trigger)	$3 \times T_C$	—	20.0	ns
Note:					
1. When using fast interrupts and \overline{IRQA} , \overline{IRQB} , \overline{IRQC} , and \overline{IRQD} are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.					
2. For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.					
For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0.5 ms.					
3. Periodically sampled and not 100% tested.					
4. \overline{RESET} duration is measured during the time in which \overline{RESET} is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When the V_{DD} is valid, but the other "required \overline{RESET} duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.					

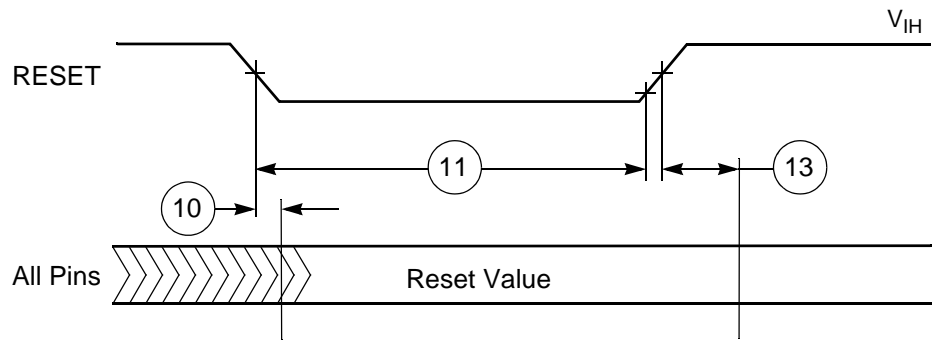
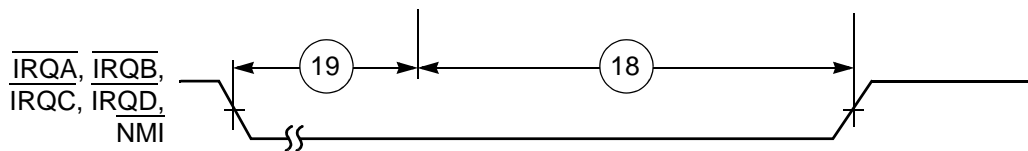
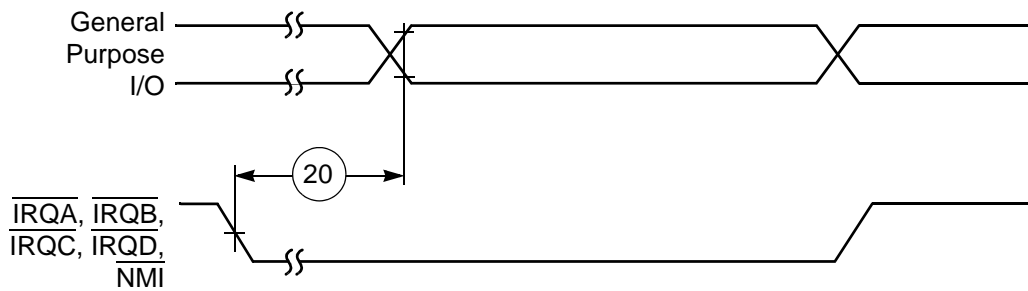


Figure 3. Reset Timing



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 4. External Fast Interrupt Timing

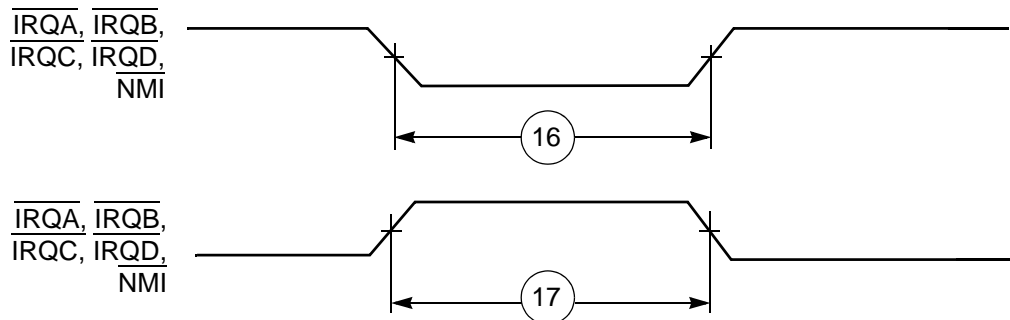


Figure 5. External Interrupt Timing (Negative Edge-Triggered)

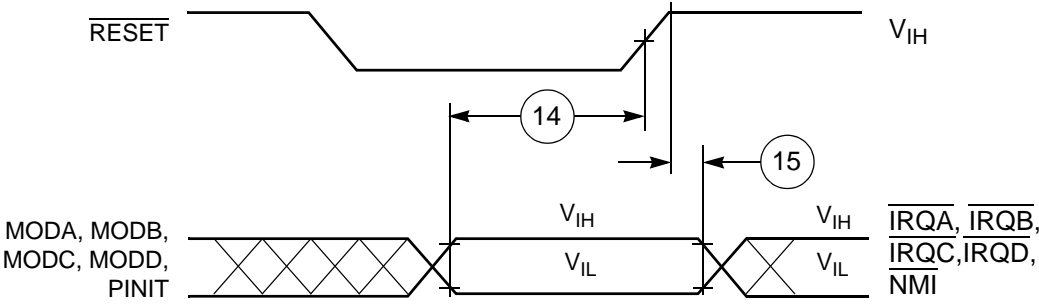


Figure 6. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

12 Serial Host Interface SPI Protocol Timing

Table 21. Serial Host Interface SPI Protocol Timing

No.	Characteristics ^{1,3,4}	Mode	Filter Mode	Min	Max	Unit
23	Minimum serial clock cycle = $t_{SPICC}(\text{min})$	Master	Bypassed	76.0	—	ns
			Very Narrow	76.0	—	ns
			Narrow	200.0	—	ns
			Wide	400.0	—	ns
XX	Tolerable Spike width on data or clock in.	—	Bypassed	—	0	ns
			Very Narrow	—	10	ns
			Narrow	—	50	ns
			Wide	—	100	ns
24	Serial clock high period	Master	Bypassed	38.0	—	ns
			Very Narrow	38.0	—	ns
			Narrow	100.0	—	ns
			Wide	200.0	—	ns
		Slave	Bypassed	33.0	—	ns
			Very Narrow	33.0	—	ns
			Narrow	100.0	—	ns
			Wide	200.0	—	ns
25	Serial clock low period	Master	Bypassed	38.0	—	ns
			Very Narrow	38.0	—	ns
			Narrow	100.0	—	ns
			Wide	200.0	—	ns
		Slave	Bypassed	33.0	—	ns
			Very Narrow	33.0	—	ns
			Narrow	100.0	—	ns
			Wide	200.0	—	ns
26	Serial clock rise/fall time	Master	—	—	—	ns
		Slave	—	—	5	ns

Table 21. Serial Host Interface SPI Protocol Timing (Continued)

No.	Characteristics ^{1,3,4}	Mode	Filter Mode	Min	Max	Unit
27	\overline{SS} assertion to first SCK edge CPHA = 0	Slave	Bypassed	38.4	—	ns
			Very Narrow	28.4	—	ns
			Narrow	0	—	ns
			Wide	0	—	ns
	CPHA = 1	Slave	Bypassed	10	—	ns
			Very Narrow	0	—	ns
			Narrow	0	—	ns
			Wide	0	—	ns
28	Last SCK edge to \overline{SS} not asserted	Slave	Bypassed	12	—	ns
			Very Narrow	22	—	ns
			Narrow	100	—	ns
			Wide	200	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	0	—	ns
			Very Narrow	0	—	ns
			Narrow	0	—	ns
			Wide	0	—	ns
30	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	23.2	—	ns
			Very Narrow	43.2	—	ns
			Narrow	73.2	—	ns
			Wide	100.0	—	ns
31	\overline{SS} assertion to data out active	Slave	—	5	—	ns
32	\overline{SS} deassertion to data high impedance ²	Slave	—	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	—	210	ns
			Very Narrow	—	270	ns
			Narrow	—	376	ns
			Wide	—	521	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	5	—	ns
			Very Narrow	15	—	ns
			Narrow	55	—	ns
			Wide	105	—	ns
35	\overline{SS} assertion to data out valid (CPHA = 0)	Slave	—	—	15.0	ns

Table 21. Serial Host Interface SPI Protocol Timing (Continued)

No.	Characteristics ^{1,3,4}	Mode	Filter Mode	Min	Max	Unit
36	First SCK sampling edge to $\overline{\text{HREQ}}$ output deassertion	Slave	Bypassed	50	—	ns
			Very Narrow	60	—	ns
			Narrow	100	—	ns
			Wide	150	—	ns
37	Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 1)	Slave	Bypassed	57.0	—	ns
			Very Narrow	67.0	—	ns
			Narrow	107.0	—	ns
			Wide	157.0	—	ns
38	$\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 0)	Slave	—	50.0	—	ns
39	$\overline{\text{SS}}$ deassertion pulse width (CPHA = 0)	Slave	—	12.7	—	ns
40	$\overline{\text{HREQ}}$ in assertion to first SCK edge	Master	—	63.0	—	ns
41	$\overline{\text{HREQ}}$ in deassertion to last SCK sampling edge ($\overline{\text{HREQ}}$ in set-up time) (CPHA = 1)	Master	—	0	—	ns
42	First SCK edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time)	Master	—	0	—	ns
43	$\overline{\text{HREQ}}$ assertion width	Master	—	20	—	ns
Note: <ol style="list-style-type: none"> $V_{\text{CORE_VDD}} = 1.25 \pm 0.05 \text{ V}$; $T_{\text{J}} = 0^{\circ}\text{C}$ to 95°C (52 LQFP) / 0°C to 90°C (80 LQFP), $C_{\text{L}} = 50 \text{ pF}$ Periodically sampled, not 100% tested All times assume noise free inputs. All times assume internal clock frequency of 150 MHz. 						

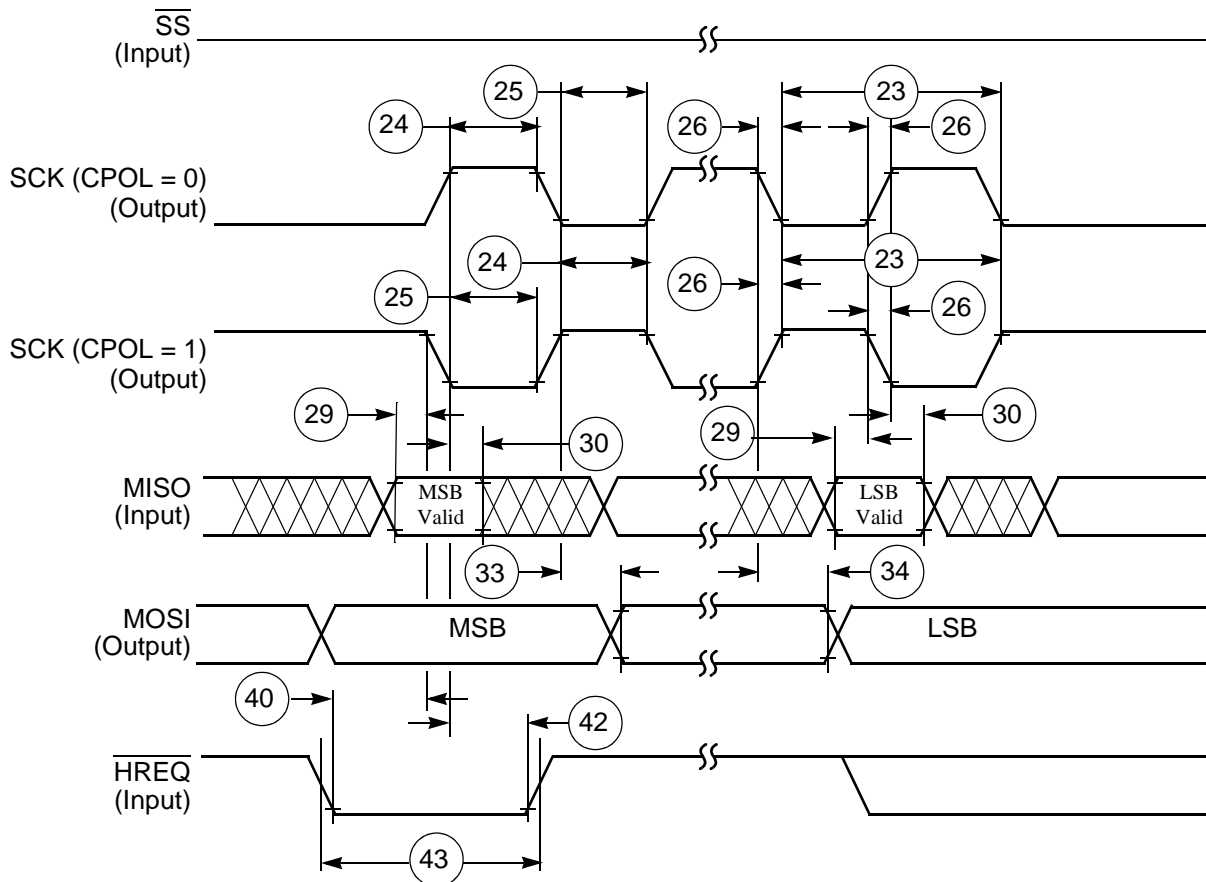


Figure 7. SPI Master Timing (CPHA = 0)

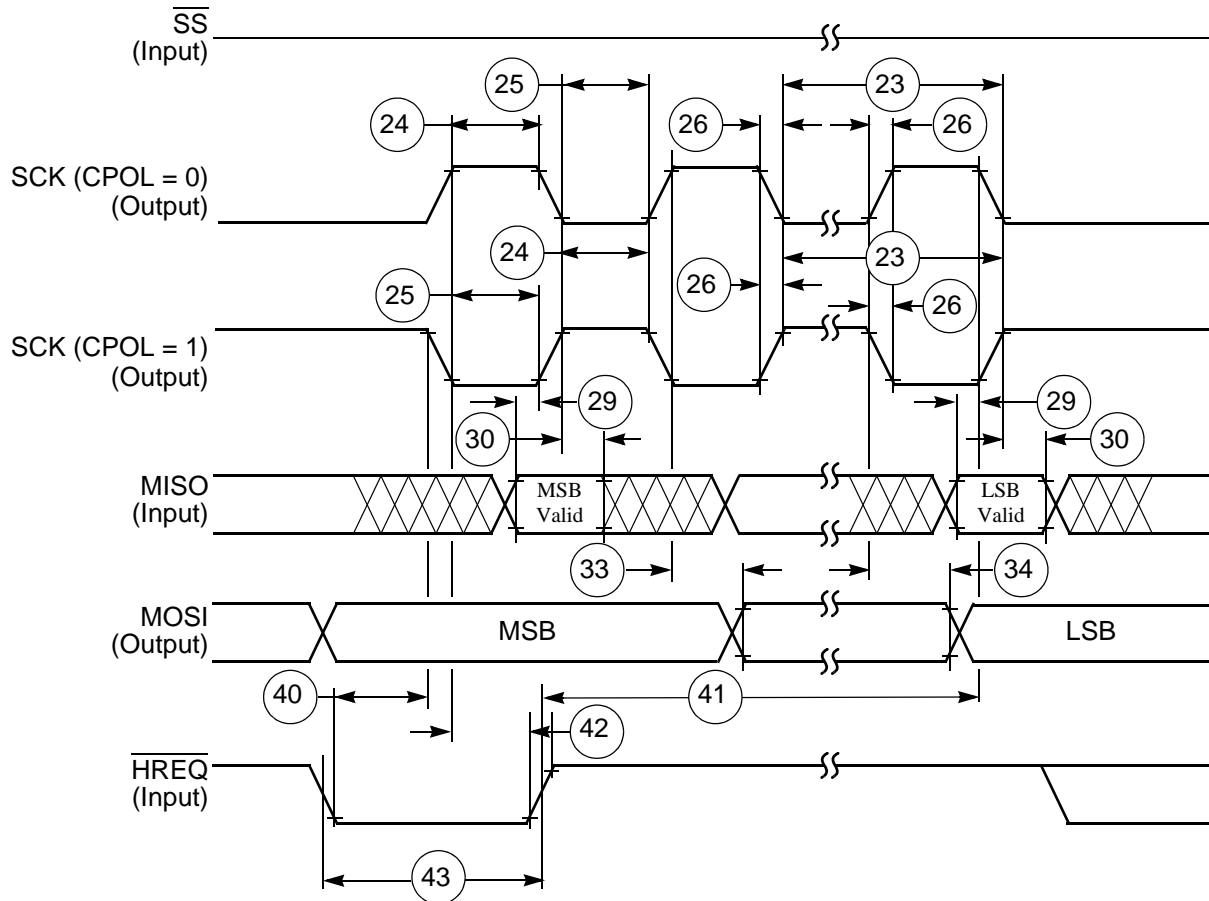


Figure 8. SPI Master Timing (CPHA = 1)

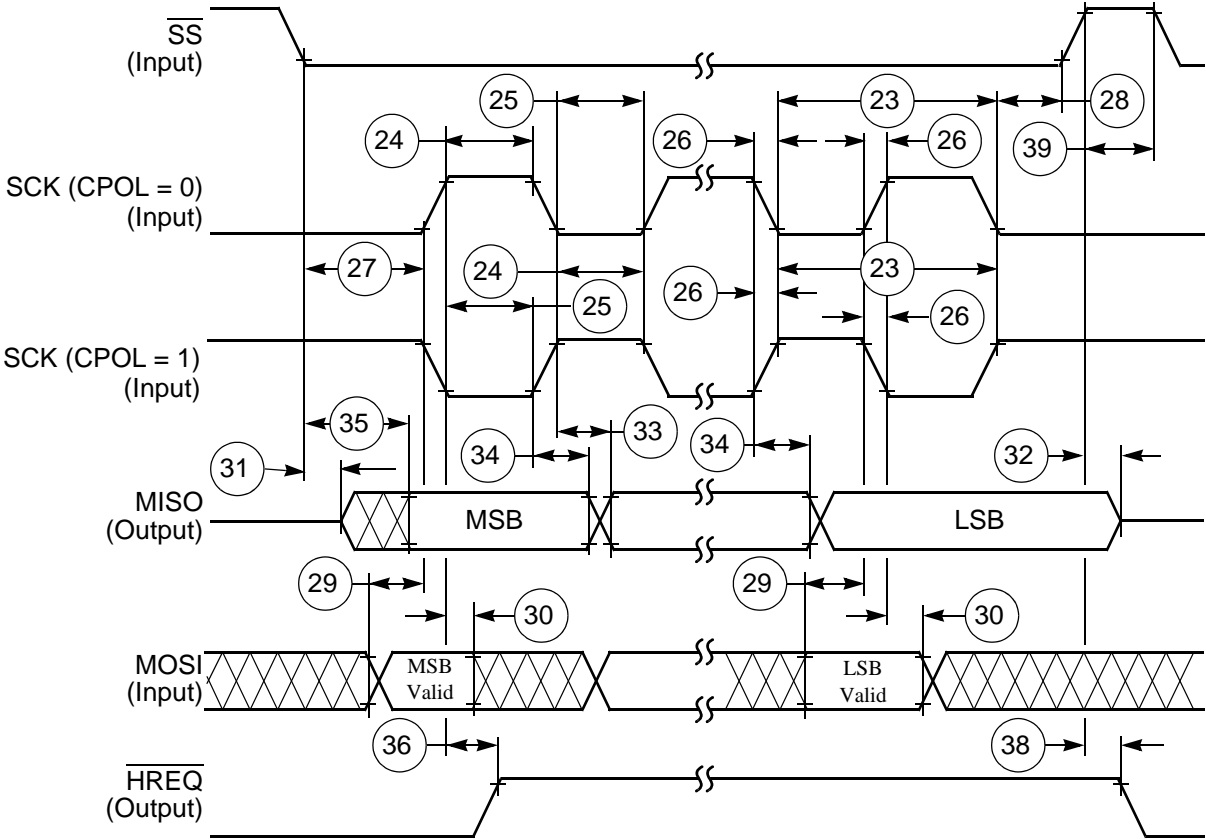


Figure 9. SPI Slave Timing (CPHA = 0)

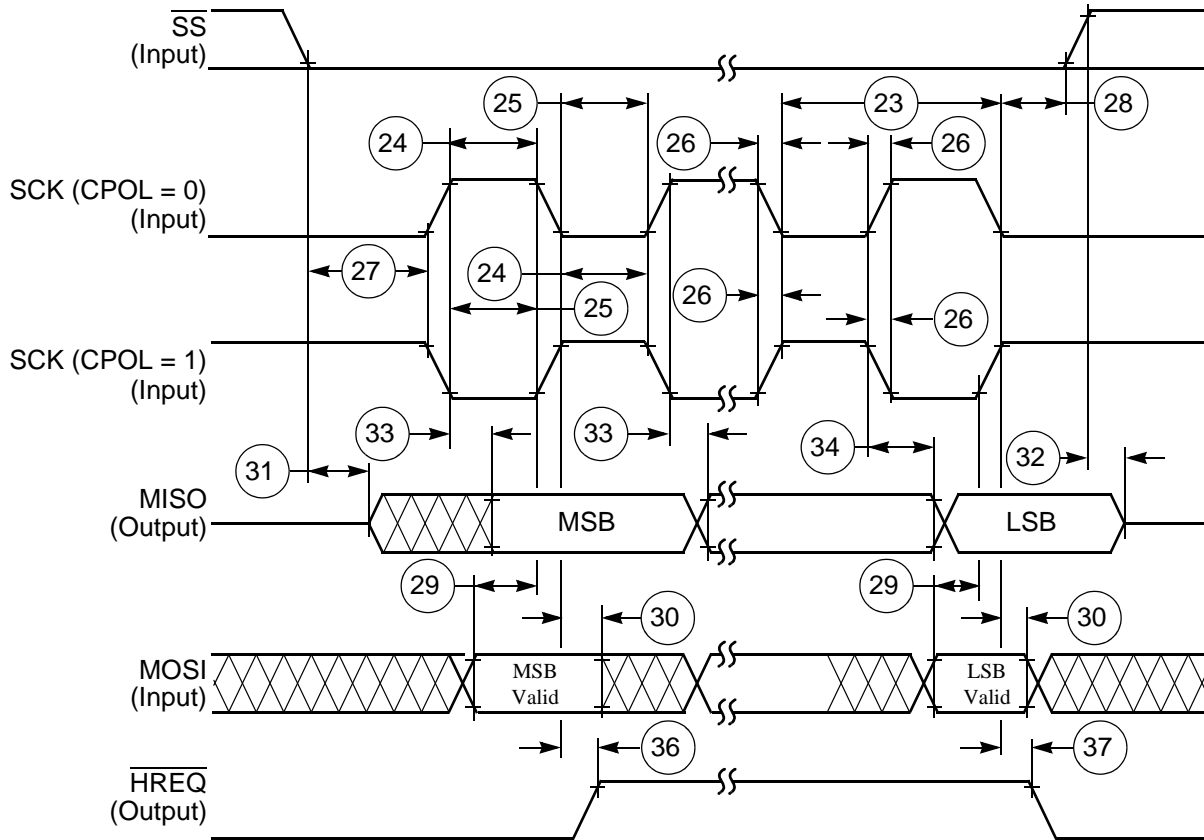


Figure 10. SPI Slave Timing (CPHA = 1)

13 Serial Host Interface (SHI) I²C Protocol Timing

Table 22. SHI I²C Protocol Timing

Standard I ² C							
No.	Characteristics ^{1,2,3,4,5}	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
XX	Tolerable Spike Width on SCL or SDA Filters Bypassed Very Narrow Filters enabled Narrow Filters enabled Wide Fileters enabled.	—	—	0	—	0	ns
44	SCL clock frequency	F _{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T _{SCL}	10	—	2.5	—	μs
45	Bus free time	T _{BUF}	4.7	—	1.3	—	μs
46	Start condition set-up time	T _{SUSTA}	4.7	—	0.6	—	μs

Table 22. SHI I²C Protocol Timing (Continued)

Standard I ² C								
No.	Characteristics ^{1,2,3,4,5}	Symbol/ Expression	Standard		Fast-Mode		Unit	
			Min	Max	Min	Max		
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	μs	
48	SCL low period	T_{LOW}	4.7	—	1.3	—	μs	
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	μs	
50	SCL and SDA rise time	T_R	—	5.0	—	5.0	ns	
51	SCL and SDA fall time	T_F	—	5.0	—	5.0	ns	
52	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns	
53	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	μs	
54	DSP clock frequency <ul style="list-style-type: none"> • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled 	F_{OSC}	10.6	—	28.5	—	MHz	
			10.6	—	28.5	—	MHz	
			11.8	—	39.7	—	MHz	
			13.1	—	61.0	—	MHz	
55	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	μs	
56	Stop condition setup time	$T_{SU;STO}$	4.0	—	0.6	—	μs	
57	\overline{HREQ} in deassertion to last SCL edge (\overline{HREQ} in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns	
58	First SCL sampling edge to \overline{HREQ} output deassertion ² <ul style="list-style-type: none"> • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled 	$T_{NG;RQO}$	$4 \times T_C + 30$	—	57.0	—	57.0	ns
			$4 \times T_C + 50$	—	77.0	—	67.0	ns
			$4 \times T_C + 130$	—	157.0	—	157.0	ns
			$4 \times T_C + 230$	—	257.0	—	257.0	ns
59	Last SCL edge to \overline{HREQ} output not deasserted ² <ul style="list-style-type: none"> • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled 	$T_{AS;RQO}$	$2 \times T_C + 30$	44	—	44	—	ns
			$2 \times T_C + 40$	54	—	54	—	ns
			$2 \times T_C + 80$	94	—	94	—	ns
			$2 \times T_C + 130$	144	—	144	—	ns
60	\overline{HREQ} in assertion to first SCL edge <ul style="list-style-type: none"> • Filters bypassed • Very Narrow filters enabled • Narrow filters enabled • Wide filters enabled 	$T_{AS;RQI}$	4327	—	927	—	ns	
			4317	—	917	—	ns	
			4282	—	877	—	ns	
			4227	—	827	—	ns	
61	First SCL edge to \overline{HREQ} is not asserted (\overline{HREQ} in hold time.)	$t_{HO;RQI}$	0.0	—	0.0	—	ns	

Note:

1. $V_{CORE_VDD} = 1.25 \pm 0.05$ V; $T_J = 0^\circ\text{C}$ to 95°C (52 LQFP) / 0°C to 90°C (80 LQFP), $C_L = 50$ pF
2. Pull-up resistor: R_P (min) = 1.5 kOhm
3. Capacitive load: C_b (max) = 50 pF
4. All times assume noise free inputs
5. All times assume internal clock frequency of 150MHz

14 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP} , is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

where

- HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.
- HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = \$00 to \$FF) may be selected.

In I²C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \quad (\text{if } HDM[7:0] = \$02 \text{ and } HRS = 1)$$

to

$$4096 \times T_C \quad (\text{if } HDM[7:0] = \$FF \text{ and } HRS = 0)$$

The programmed serial clock cycle (T_{I^2CCP}) should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Table 23.

Table 23. SCL Serial Clock Cycle (T_{SCL}) Generated as Master

Nominal	$T_{I^2CCP} + 3 \times T_C + 45ns + T_R$
---------	--

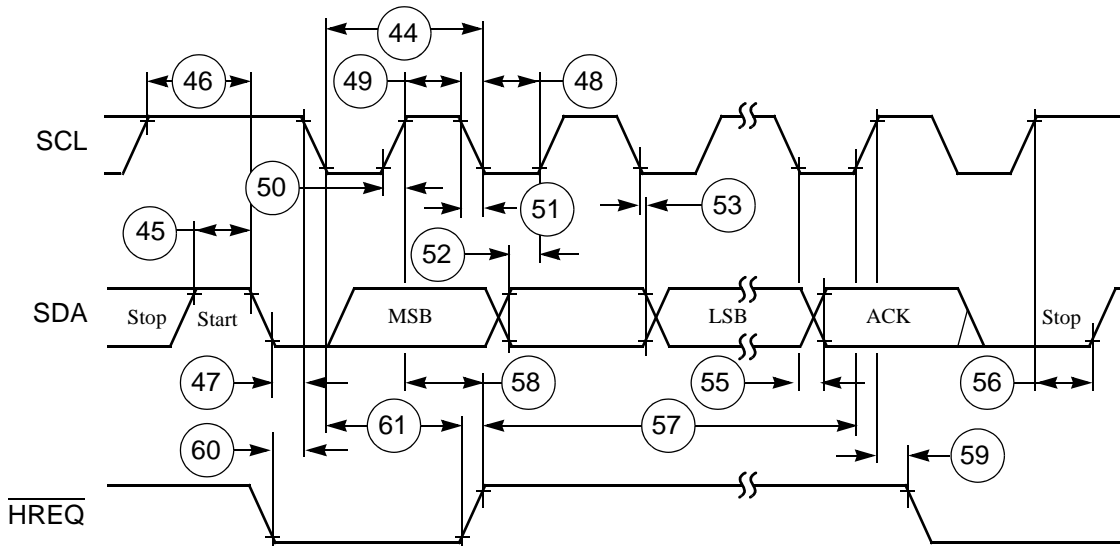


Figure 11. I²C Timing

15 Enhanced Serial Audio Interface Timing

Table 24. Enhanced Serial Audio Interface Timing

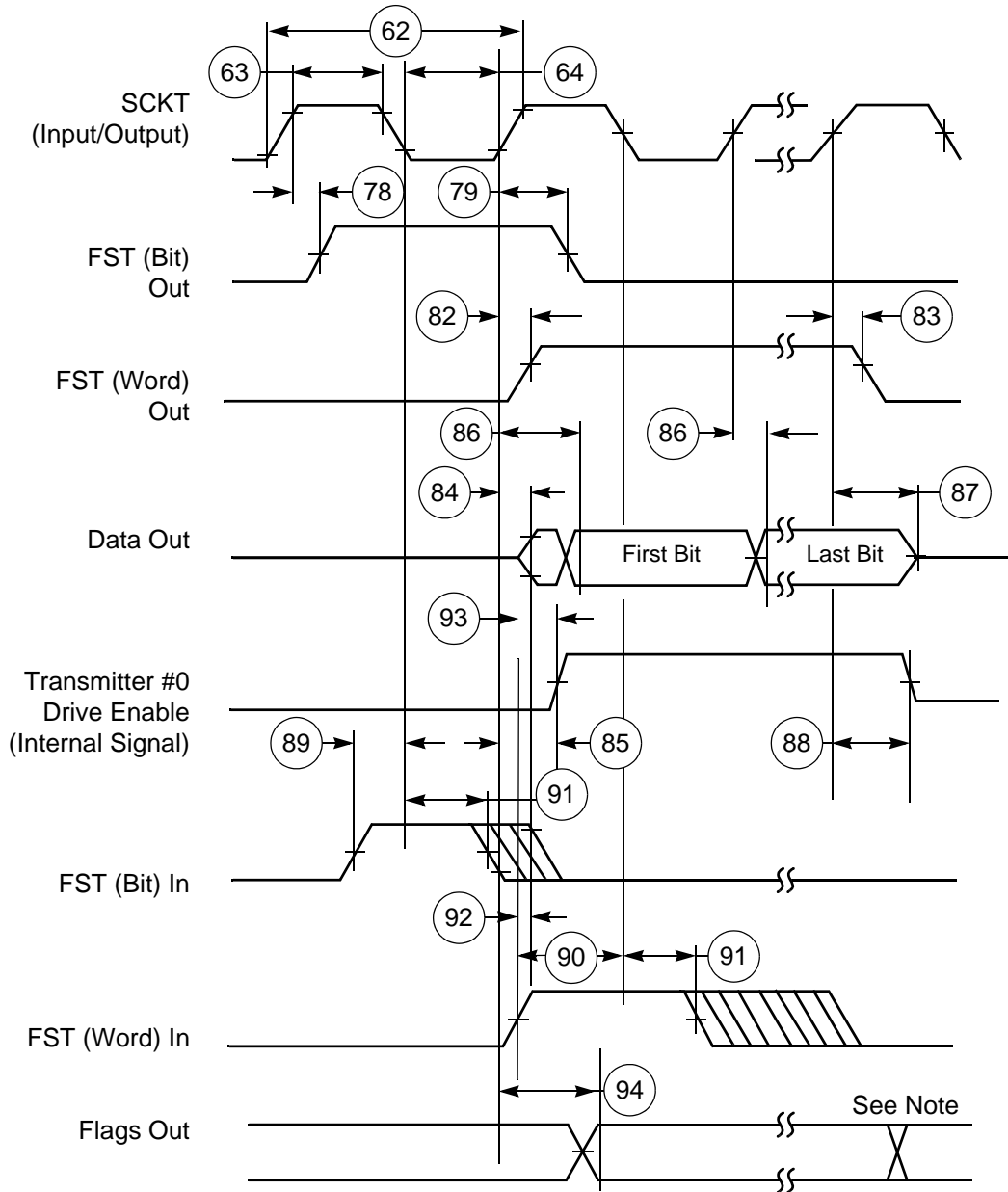
No.	Characteristics ^{1, 2, 3}	Symbol	Expression ³	Min	Max	Condition ⁴	Unit
62	Clock cycle ⁵	t_{SSICC}	$4 \times T_C$	26.4	—	i ck	ns
			$4 \times T_C$	26.4	—	i ck	
63	Clock high period <ul style="list-style-type: none"> • For internal clock • For external clock 	—	$2 \times T_C - 10.0$	3.4	—		ns
			$2 \times T_C$	13.4	—		
64	Clock low period <ul style="list-style-type: none"> • For internal clock • For external clock 	—	$2 \times T_C - 10.0$	3.4	—		ns
			$2 \times T_C$	13.4	—		
65	SCKR rising edge to FSR out (bl) high	—	—	—	37.0	x ck	ns
				—	22.0	i ck a	
66	SCKR rising edge to FSR out (bl) low	—	—	—	37.0	x ck	ns
				—	22.0	i ck a	
67	SCKR rising edge to FSR out (wr) high ⁶	—	—	—	39.0	x ck	ns
				—	24.0	i ck a	
68	SCKR rising edge to FSR out (wr) low ⁶	—	—	—	39.0	x ck	ns
				—	24.0	i ck a	
69	SCKR rising edge to FSR out (wl) high	—	—	—	36.0	x ck	ns
				—	21.0	i ck a	
70	SCKR rising edge to FSR out (wl) low	—	—	—	37.0	x ck	ns
				—	22.0	i ck a	
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	0.0	—	x ck	ns
				19.0	—	i ck	
72	Data in hold time after SCKR falling edge	—	—	5.0	—	x ck	ns
				3.0	—	i ck	
73	FSR input (bl, wr) high before SCKR falling edge ⁶	—	—	23.0	—	x ck	ns
				1.0	—	i ck a	
74	FSR input (wl) high before SCKR falling edge	—	—	23.0	—	x ck	ns
				1.0	—	i ck a	
75	FSR input hold time after SCKR falling edge	—	—	3.0	—	x ck	ns
				0.0	—	i ck a	
76	Flags input setup before SCKR falling edge	—	—	0.0	—	x ck	ns
				19.0	—	i ck s	
77	Flags input hold time after SCKR falling edge	—	—	6.0	—	x ck	ns
				0.0	—	i ck s	
78	SCKT rising edge to FST out (bl) high	—	—	—	29.0	x ck	ns
				—	15.0	i ck	

Table 24. Enhanced Serial Audio Interface Timing (Continued)

No.	Characteristics ^{1, 2, 3}	Symbol	Expression ³	Min	Max	Condition ⁴	Unit
79	SCKT rising edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high ⁶	—	—	— —	31.0 17.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low ⁶	—	—	— —	33.0 19.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
86	SCKT rising edge to data out valid	—	—	— —	26.5 21.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance ⁷	—	—	— —	31.0 16.0	x ck i ck	ns
88	SCKT rising edge to transmitter #0 drive enable deassertion ⁷	—	—	— —	34.0 20.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge ⁶	—	—	2.0 21.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	—	—	2.0 21.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	—	—	4.0 0.0	— —	x ck i ck	ns
92	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	ns
93	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	31.0	—	ns
94	Flag output valid after SCKT rising edge	—	—	— —	32.0 18.0	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	$2 \times T_C$	13.4	—		ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0		ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0		ns

Table 24. Enhanced Serial Audio Interface Timing (Continued)

No.	Characteristics ^{1, 2, 3}	Symbol	Expression ³	Min	Max	Condition ⁴	Unit
Note:	<p>1. $V_{\text{CORE_VDD}} = 1.25 \pm 0.05 \text{ V}$; $T_{\text{J}} = 0^{\circ}\text{C}$ to 95°C (52 LQFP) / 0°C to 90°C (80 LQFP), $C_{\text{L}} = 50 \text{ pF}$</p> <p>2. i ck = internal clock x ck = external clock i ck a = internal clock, asynchronous mode (asynchronous implies that SCKT and SCKR are two different clocks) i ck s = internal clock, synchronous mode (synchronous implies that SCKT and SCKR are the same clock)</p> <p>3. bl = bit length wl = word length wr = word length relative</p> <p>4. SCKT(SCKT pin) = transmit clock SCKR(SCKR pin) = receive clock FST(FST pin) = transmit frame sync FSR(FSR pin) = receive frame sync HCKT(HCKT pin) = transmit high frequency clock HCKR(HCKR pin) = receive high frequency clock</p> <p>5. For the internal clock, the external clock cycle is defined by t_{cyc} and the ESAI control register.</p> <p>6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.</p> <p>7. Periodically sampled and not 100% tested.</p> <p>8. ESAI_1 specs match those of ESAI.</p>						



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 12. ESAI Transmitter Timing

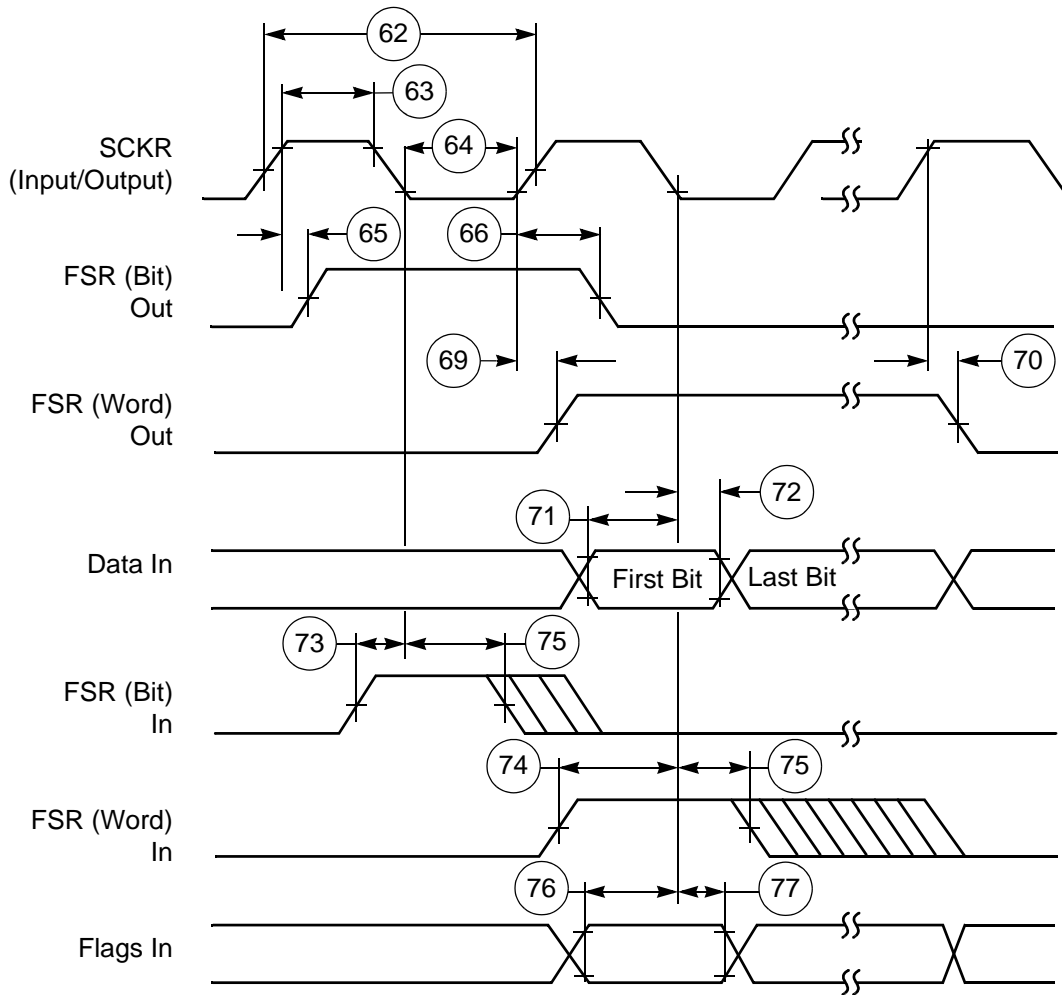


Figure 13. ESAI Receiver Timing

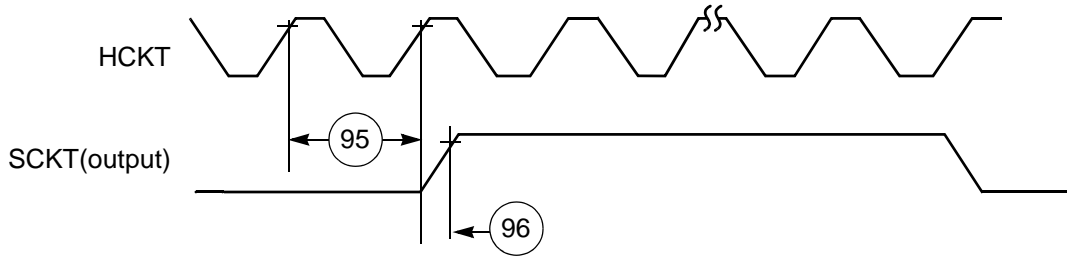


Figure 14. ESAI HCKT Timing

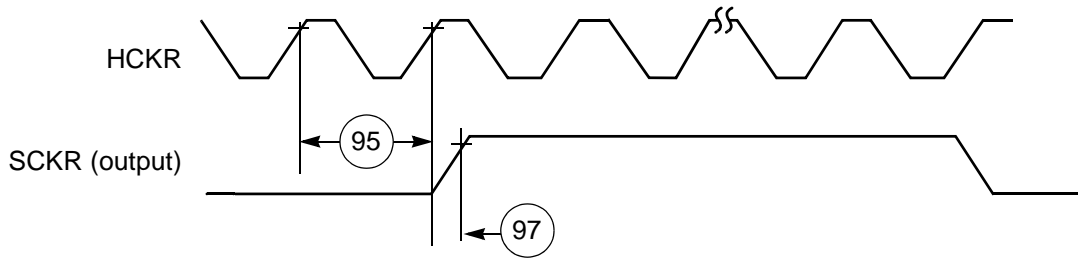


Figure 15. ESAI HCKR Timing

16 Timer Timing

Table 25. Timer Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	15.4	—	ns
99	TIO High	$2 \times T_C + 2.0$	15.4	—	ns

Note: $V_{CORE_VDD} = 1.25 \text{ V} \pm 0.05 \text{ V}$; $T_J = 0^\circ\text{C}$ to 95°C (52 LQFP) / 0°C to 90°C (80 LQFP), $C_L = 50 \text{ pF}$

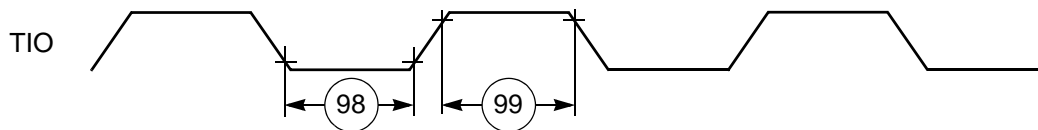


Figure 16. TIO Timer Event Input Restrictions

17 GPIO Timing

Table 26. GPIO Timing

No.	Characteristics ¹	Expression	Min	Max	Unit
100	FOSC edge to GPIO out valid (GPIO out delay time) ²		—	7	ns
101	FOSC edge to GPIO out not valid (GPIO out hold time) ²		—	7	ns
102	FOSC In valid to EXTAL edge (GPIO in set-up time) ²		2	—	ns
103	FOSC edge to GPIO in not valid (GPIO in hold time) ²		0	—	ns
104	Minimum GPIO pulse high width	2 x TC	13.4	—	ns
105	Minimum GPIO pulse low width	2 x TC	13.4	—	ns
106	GPIO out rise time	—	—	13.0	ns
107	GPIO out fall time	—	—	13.0	ns

Note:

- $V_{\text{CORE_VDD}} = 1.25 \text{ V} \pm 0.05 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+115^\circ\text{C}$, $C_L = 50 \text{ pF}$
- Simulation numbers-subject to change.

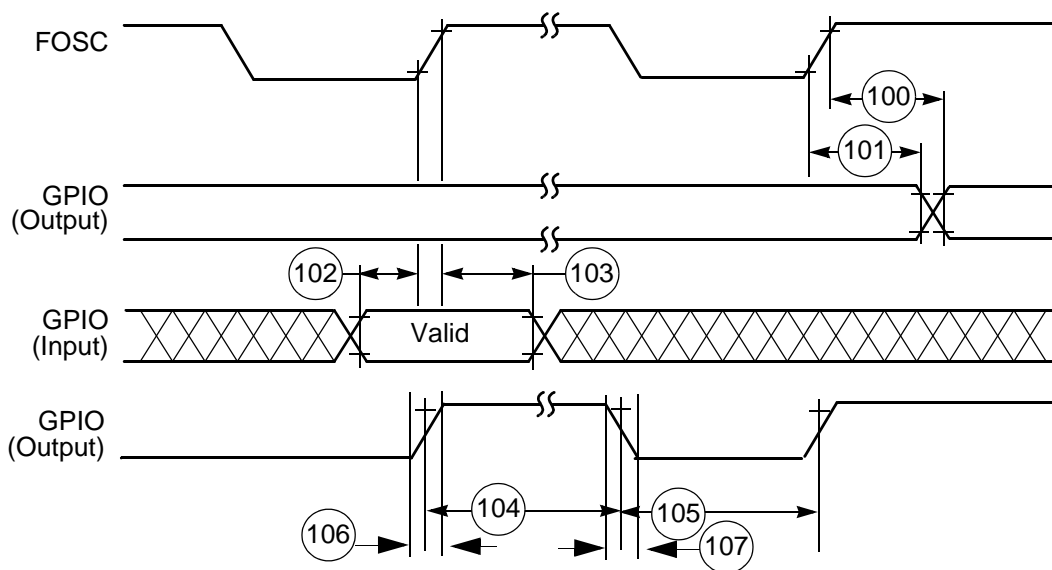


Figure 17. GPIO Timing

18 JTAG Timing

Table 27. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
108	TCK frequency of operation ($1/(T_C \times 3)$; maximum 10 MHz)	—	10.0	MHz
109	TCK cycle time in Crystal mode	100.0	—	ns
110	TCK clock pulse width measured at 1.65 V	50.0	—	ns
111	TCK rise and fall times	—	3.0	ns
112	Boundary scan input data setup time	15.0	—	ns
113	Boundary scan input data hold time	24.0	—	ns
114	TCK low to output data valid	—	40.0	ns
115	TCK low to output high impedance	—	40.0	ns
116	TMS, TDI data setup time	5.0	—	ns
117	TMS, TDI data hold time	25.0	—	ns
118	TCK low to TDO data valid	—	44.0	ns
119	TCK low to TDO high impedance	—	44.0	ns

Note:

- $V_{CORE_VDD} = 1.25 V \pm 0.05 V$; $T_J = -40^\circ C$ to $+95^\circ C$, $C_L = 50 pF$
- All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

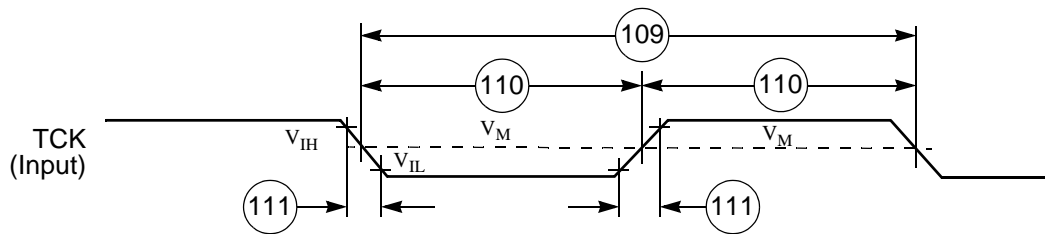


Figure 18. Test Clock Input Timing Diagram

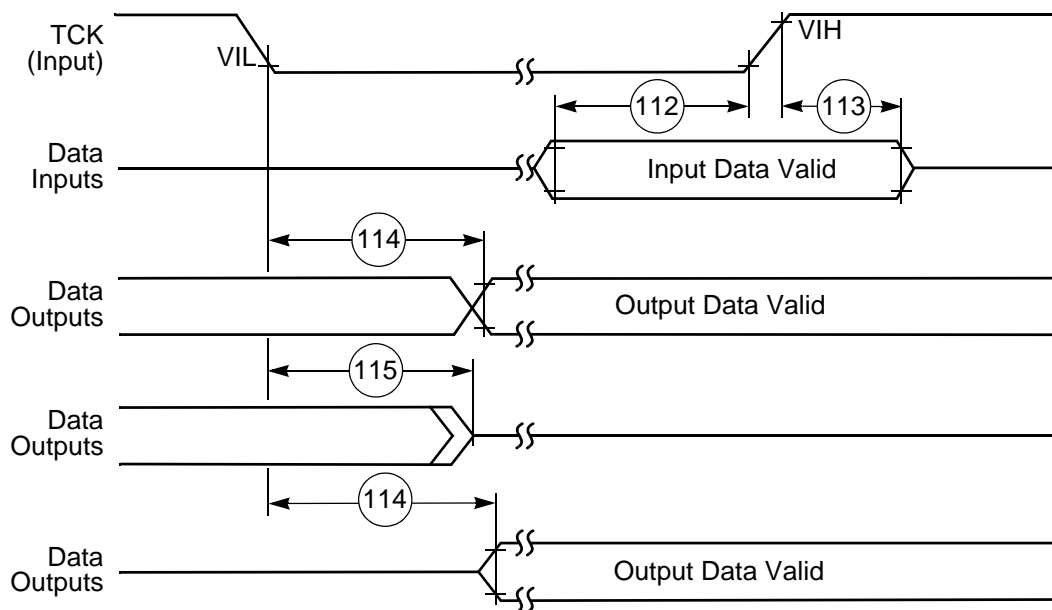


Figure 19. Debugger Port Timing Diagram

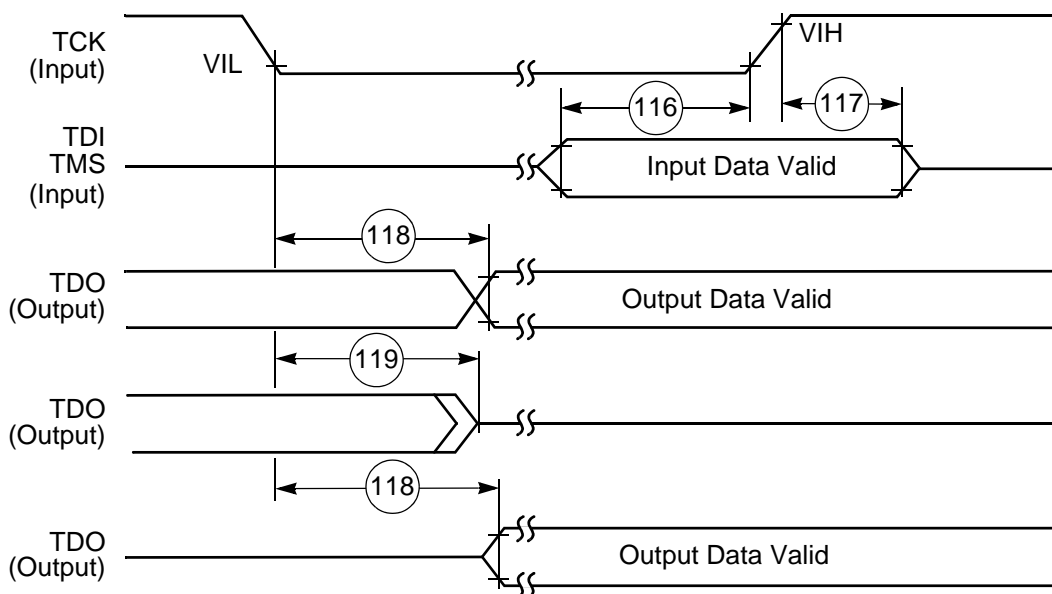


Figure 20. Test Access Port Timing Diagram

19 Watchdog Timer Timing

Table 28. Watchdog Timer Timing

No.	Characteristics	Expression	Min	Max	Unit
120	Delay from time-out to fall of TIO1	$2 \times T_C$	13.4	—	ns
121	Delay from timer clear to rise of TIO1	$2 \times T_C$	13.4	—	ns

Appendix A Package Information

DSP56374 Pinout

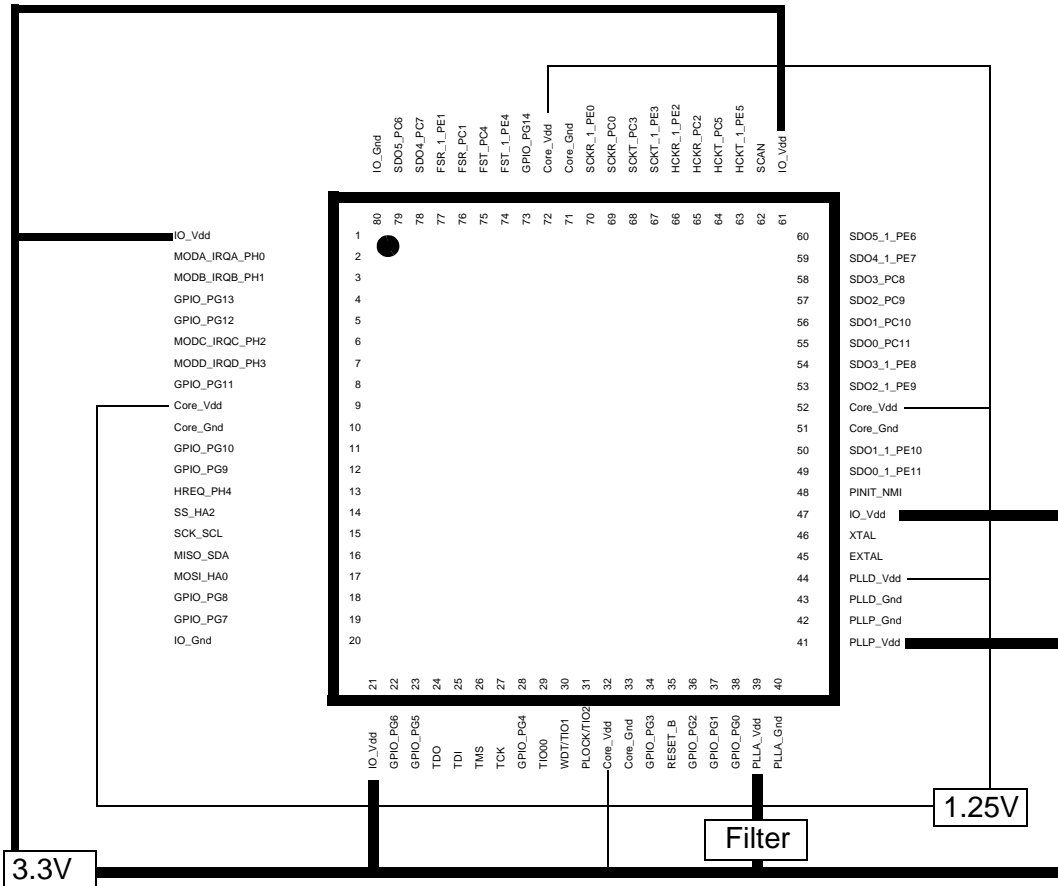


Figure 21. 80-pin Vdd Connections

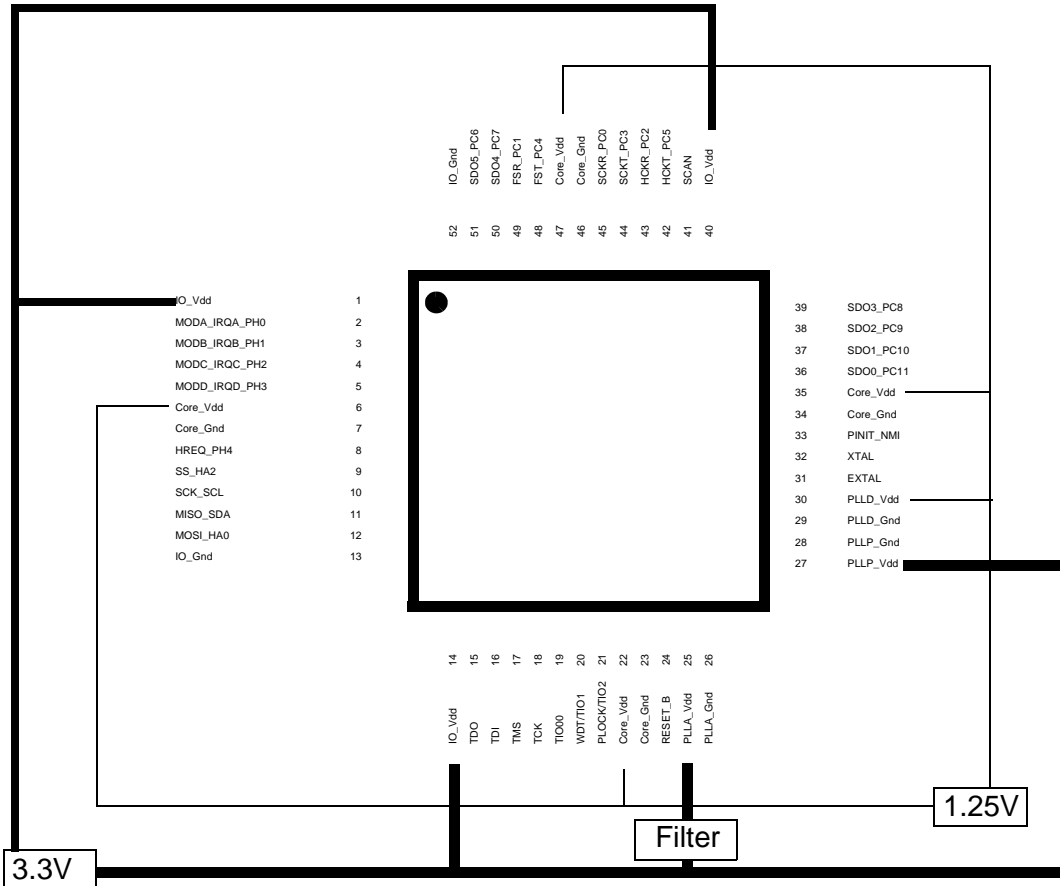
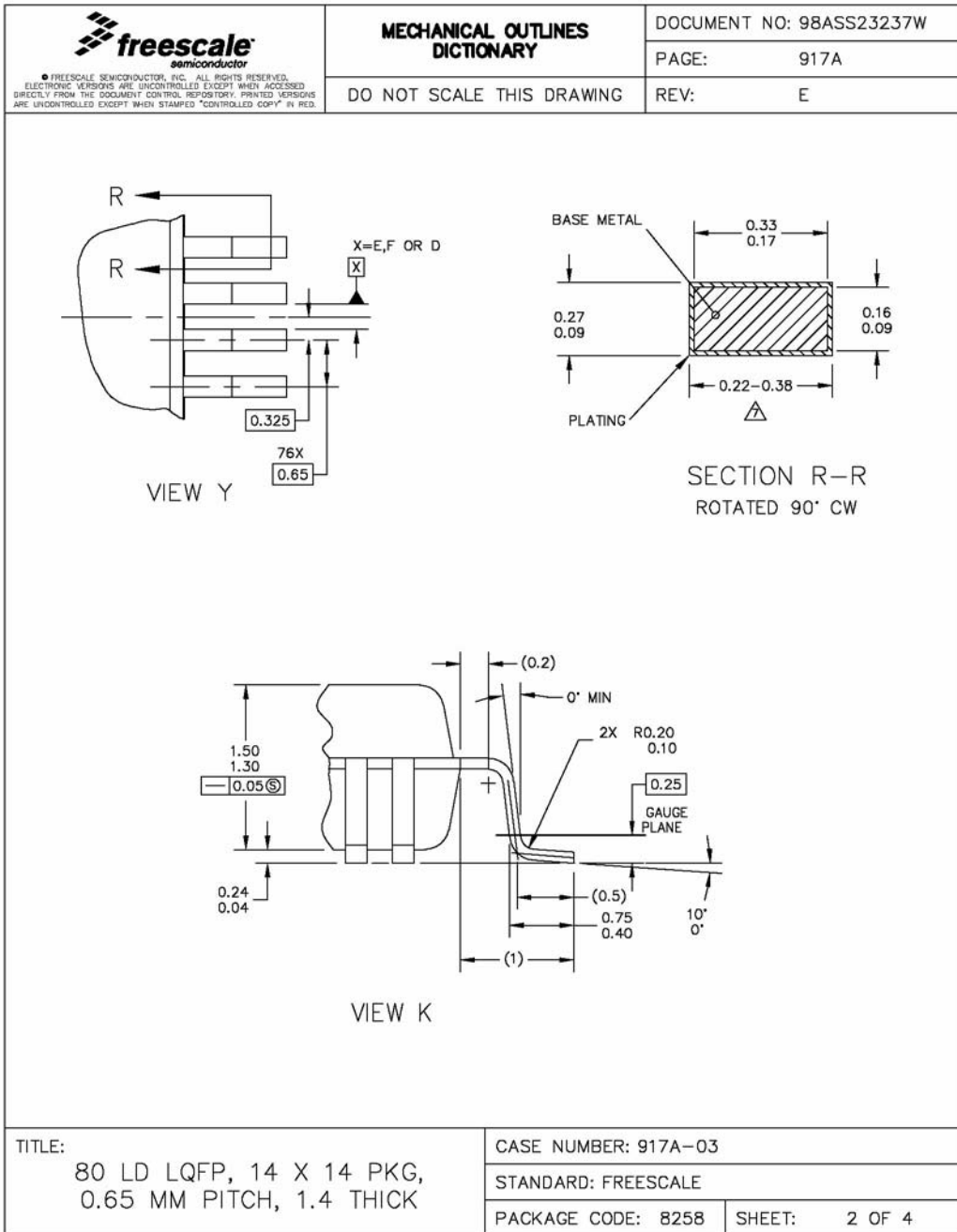




Figure 22. 52-pin Vdd Connections

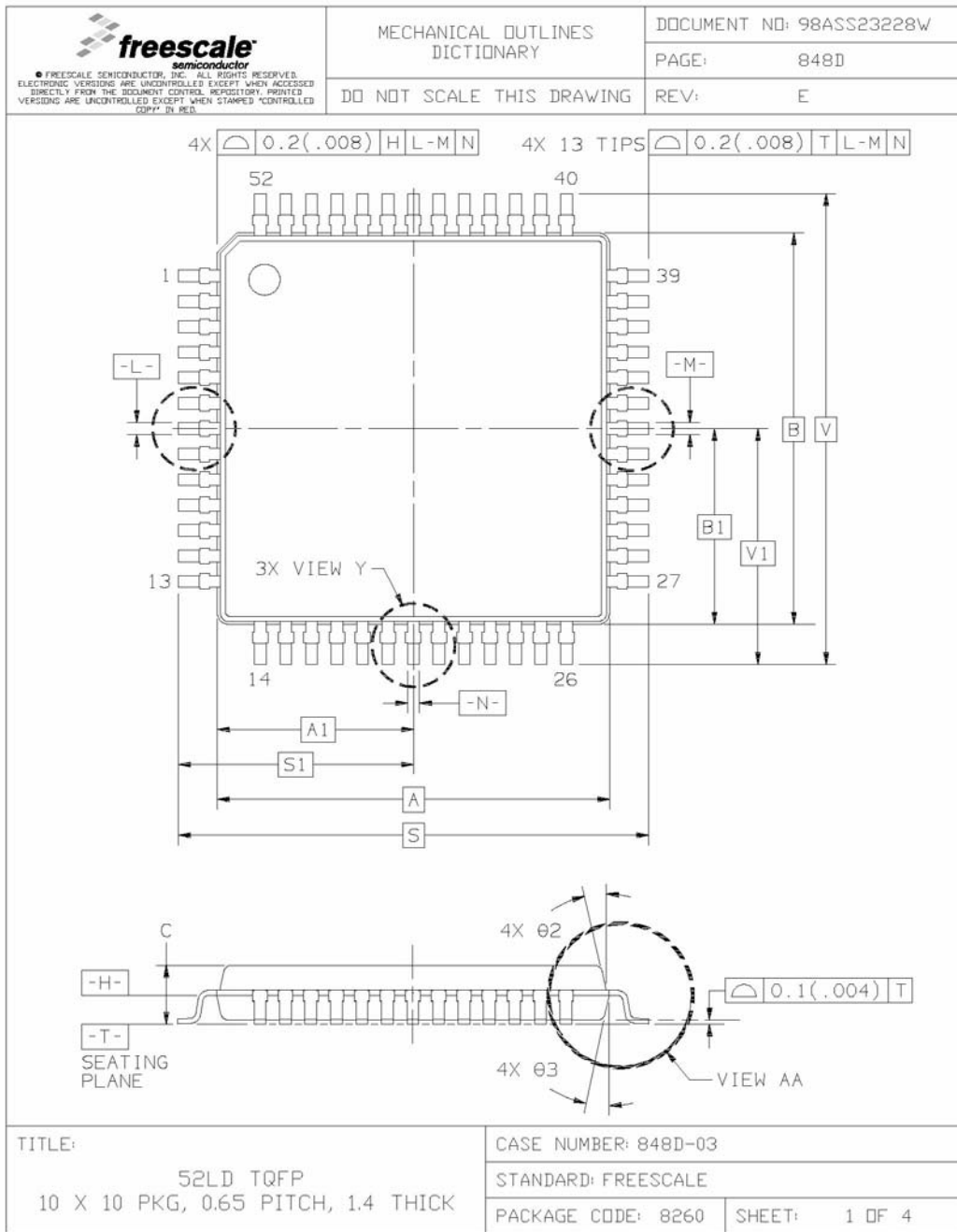
19.1 Signal Identification by Pin Number

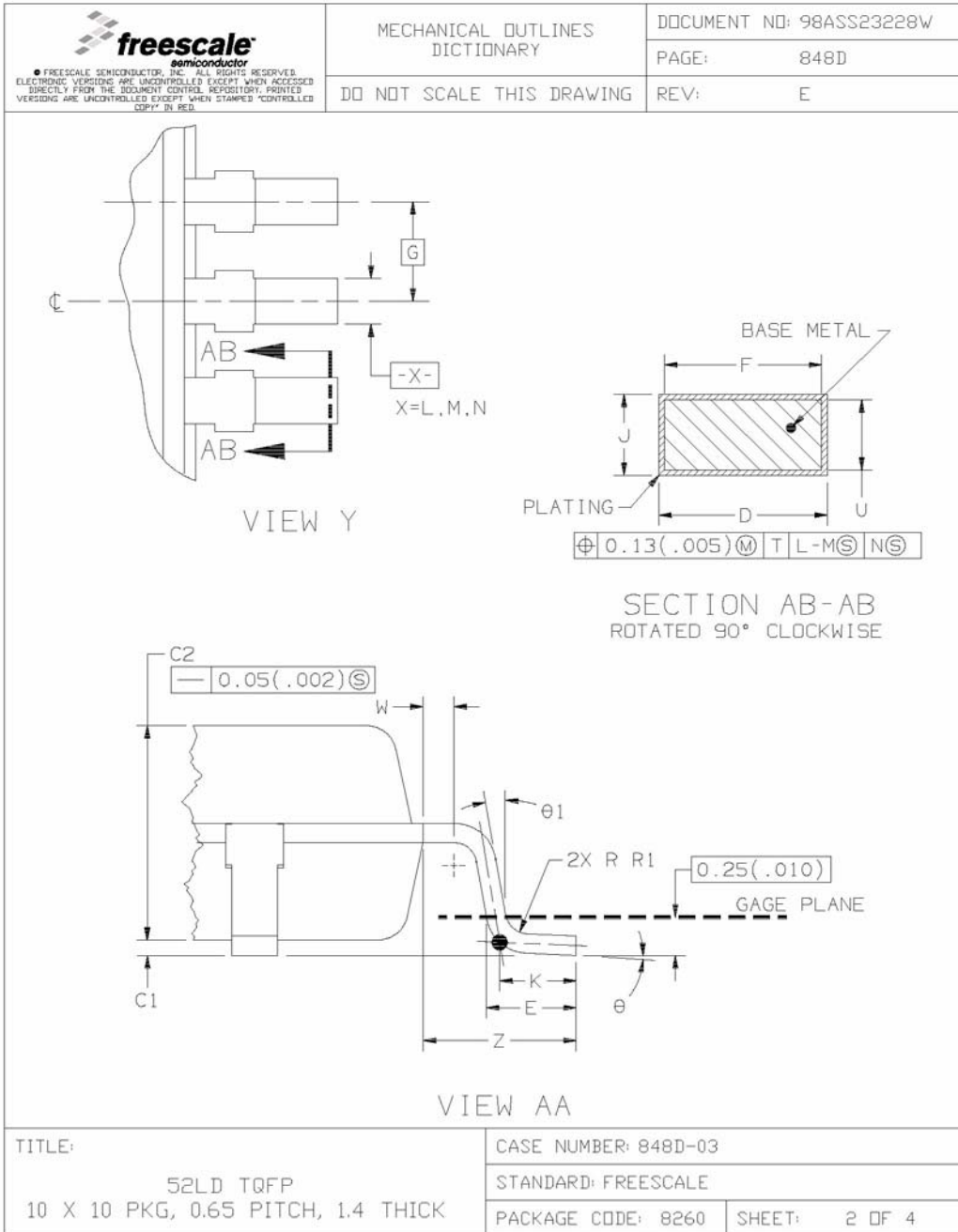



 <small> ● FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED. </small>	MECHANICAL OUTLINES DICTIONARY		DOCUMENT NO: 98ASS23237W	
	DO NOT SCALE THIS DRAWING		PAGE: 917A	REV: E
<p>NOTES:</p> <ol style="list-style-type: none"> 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. 2. CONTROLLING DIMENSION : MILIMETER. 3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. 4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H. <p>△ DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.</p> <p>△ DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.</p> <p>△ DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.</p>				
TITLE:		CASE NUMBER: 917A-03		
80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK		STANDARD: FREESCALE		
		PACKAGE CODE: 8258	SHEET:	3 OF 4


 <small>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACSESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.</small>		<h2 style="margin: 0;">REVISION HISTORY</h2>		DOCUMENT NO: 98ASS23237W	
				PAGE: 917A	
				REV: E	
LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE	
O	-----	RELEASED FOR PRODUCTION	-----	-----	
A	-----	-----	-----	-----	
B	-----	-----	-----	-----	
C	-----	-----	-----	-----	
D	GARY JOHNSON	REFORMAT DOCUMENT, DELETED DUAL DIMENSIONS (INCH), CHANGED DOCUMENT TITLE FROM TQFP TO LQFP.	AZHAR A.	11 MAR 2004	
E	PATRICE L.	UPDATED DRAWNGS PER FREESCALE FORMAT.	KL CHIN	7 OCT 2004	
TITLE: 80 LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK			CASE NUMBER: 917A-03		
			STANDARD: FREESCALE		
			PACKAGE CODE: 8258	SHEET: 4 OF 4	

52 pin package





 <small>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" BY PED.</small>		MECHANICAL OUTLINES DICTIONARY		DOCUMENT NO: 98ASS23228W					
		DO NOT SCALE THIS DRAWING		REV: E	PAGE: 848D				
<p>NOTES</p> <ol style="list-style-type: none"> DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25(.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46(.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07(.003). 									
	MILLIMETERS		INCHES			MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	10.00	BSC	0.394	BSC					
A1	5.00	BSC	0.197	BSC					
B	10.00	BSC	0.394	BSC					
B1	5.00	BSC	0.197	BSC					
C	---	1.70	---	0.067					
C1	0.05	0.20	0.002	0.008					
C2	1.30	1.50	0.051	0.059					
D	0.20	0.40	0.008	0.016					
E	0.45	0.75	0.018	0.030					
F	0.22	0.35	0.009	0.014					
G	0.65	BSC	0.026	BSC					
J	0.07	0.20	0.003	0.008					
K	0.50	REF	0.020	REF					
R1	0.08	0.20	0.003	0.008					
S	12.00	BSC	0.472	BSC					
S1	6.00	BSC	0.236	BSC					
U	0.09	0.16	0.004	0.006					
V	12.00	BSC	0.472	BSC					
V1	6.00	BSC	0.236	BSC					
W	0.20	REF	0.008	REF					
Z	1.00	REF	0.039	REF					
θ	0°	7°	0°	7°					
θ1	0°	---	0°	---					
θ2	12°	REF	12°	REF					
θ3	12°	REF	12°	REF					
TITLE:					CASE NUMBER: 848D-03				
52LD TQFP					STANDARD: FREESCALE				
10 X 10 PKG, 0.65 PITCH, 1.4 THICK					PACKAGE CODE: 8260		SHEET: 3 OF 4		

 <small>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.</small>		<h2>REVISION HISTORY</h2>		DOCUMENT NO: 98ASS23228W	
				PAGE: 848D	
				REV: E	
LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE	
O	-----	RELEASED FOR PRODUCTION	-----	-----	
A	-----	-----	-----	-----	
B	-----	-----	-----	-----	
C	-----	-----	-----	-----	
D	-----	-----	-----	-----	
E	PATRICE L.	UPDATED DRAWINGS PER FREESCALE FORMAT. ADDED REVISION HISTORY PAGE.	KL CHIN	7 OCT 2004	
TITLE:			CASE NUMBER: 848D-03		
52LD TQFP			STANDARD: FREESCALE		
10 X 10 PKG, 0.65 PITCH, 1.4 THICK			PACKAGE CODE: 8260	SHEET: 4 OF 4	

Appendix B IBIS Model

```
[IBIS ver]      2.1
[File name]    tpz013g3.ibs
[File Rev]     1.0
[Date]         07/30/2002
[Source]       Made By 0.13uu HSPIICE model.
[Disclaimer]    This information is for modeling purposes only and is not
                guaranteed.
[Copyright]    Copyright 2002, Design Service, tsmc, All Rights Reserved.
```

```
|
|*****
|
|                               Component tpz013g3
|*****
```

(Pin)	signal_name	model_name
1	IO_VDD	PVDD2DGZ/PVDD2POC
2	MODA_IRQA_PH0	PDU12SDGZ
3	MODB_IRQB_PH1	PDU12SDGZ
4	GPIO_PG13	PRD12DGZ
5	GPIO_PG12	PRD12DGZ
6	MODC_IRQC_PH2	PDU12SDGZ
7	MODD_IRQD_PH3	PDU12SDGZ
8	GPIO_PG11	PRD12DGZ
9	CORE_VDD	PVDD1DGZ
10	CORE_GND	PVSS3DGZ
11	GPIO_PG10	PRD12DGZ
12	GPIO_PG9	PRD12DGZ
13	HREQ_PH4	PDU12SDGZ
14	SS_HA2	PDUSDGZ
15	SCK_SCL	PDU12SDGZ
16	MISO_SDA	PDU16SDGZ
17	MOSI_HA0	PDU12SDGZ
18	GPIO_PG8	PRD12DGZ
19	GPIO_PG7	PRD12DGZ
20	IO_GND	PVSS3DGZ
21	IO_VDD	PVDD2DGZ
22	GPIO_PG6	PRD12DGZ
23	GPIO_PG5	PRD12DGZ
24	TDO	PRT24DGZ
25	TDI	PDUDGZ
26	TCK	PDUDGZ
27	TMS	PDUDGZ
28	GPIO_PG4	PRD12DGZ

Appendix B IBIS Model

29	TIO0_PB0		PRD12DGZ
30	WDT_TIO1_PB1		PRD12DGZ
31	PLOCK_TIO1_PB2		PRD12DGZ
32	CORE_VDD		PVDD1DGZ
33	CORE_GND		PVSS3DGZ
34	GPIO_PG3		PRD12DGZ
35	RESET_B		PDUSDGZ
36	GPIO_PG2		PRD12DGZ
37	GPIO_PG1		PRD12DGZ
38	GPIO_PG0		PRD12DGZ
39	PLLA_VDD		PVDD1P
40	PLLA_GND		PVSS1P
41	PLLP_VDD		PVDD2DGZ
42	PLLP_GND		PVSS2P
43	PLLD_GND		PVSS1P
44	PLLD_VDD		PVDD1PC
45	EXTAL	1/2	PDX03DGZ
46	XTAL	1/2	PDX03DGZ
47	IO_VDD		PVDD2DGZ
48	PINIT_NMI		PDUSDGZ
49	SDO0_1_PE11		PRD12DGZ
50	SDO1_1_PE10		PRD12DGZ
51	CORE_GND		PVSS3DGZ
52	CORE_VDD		PVDD1DGZ
53	SDO2_1_PE9		PRD12DGZ
54	SDO3_1_PE8		PRD12DGZ
55	SDO0_PC11		PRD12DGZ
56	SDO1_PC10		PRD12DGZ
57	SDO2_SDI3_PC9		PRD12DGZ
58	SDO3_SDI2_PC8		PRD12DGZ
59	SDO4_1_PE7		PRD12DGZ
60	SDO5_1_PC6		PRD12DGZ
61	IO_VDD		PVDD2DGZ
62	SCAN		PDDDGZ
63	HCKT_1_PE5		PRD12DGZ
64	HCKT_PC5		PRD12DGZ
65	HCKR_PC2		PRD12DGZ
66	HCKR_1_PE2		PRD12DGZ
67	SCKT_1_PE3		PRD12DGZ
68	SCKT_PC3		PRD12DGZ
69	SCKR_PC0		PRD12DGZ
70	SCKR_1_PE0		PRD12DGZ
71	CORE_GND		PVSS3DGZ
72	CORE_VDD		PVDD1DGZ


```

73      GPIO_PG14          PRD12DGZ
74      FST_1_PE4         PRD12DGZ
75      FST_PC4           PRD12DGZ
76      FSR_PC1           PRD12DGZ
77      FSR_1_PE1         PRD12DGZ
78      SDO4_SDI1_PC7     PRD12DGZ

```

```

|*****
|
|                               Model prd12dgz
|*****
|

```

```

[Model]          prd12dgz
Model_type       I/O
Polarity         Non-Inverting
Enable           Active-Low
Vinl =          0.80V
Vinh =          2.00V
Vmeas =         1.50V
Cref =          50.00pF
Rref =          1.00M
Vref =          0.000V

```

```

C_comp           4.17pF           3.75pF           4.58pF

```

```

[Temperature Range]      25.00           0.12k           0.000
[Pullup Reference]       3.30V           3.00V           3.60V
[ Pulldown Reference]    0.000V          0.000V          0.000V
[POWER Clamp Reference]  5.00V           4.50V           5.50V
[GND Clamp Reference]    0.000V          0.000V          0.000V

```

```

[Pulldown]

```

voltage	I(typ)	I(min)	I(max)
-3.30	0.000A	0.000A	0.000A
-3.10	0.000A	0.000A	-10.00mA
-2.90	0.000A	0.000A	0.000A
-2.70	0.000A	0.000A	0.000A
-2.50	0.000A	-10.00mA	0.000A
-2.30	-10.00mA	0.000A	-10.00mA
-2.10	0.000A	-10.00mA	0.000A
-1.90	0.000A	0.000A	-10.00mA
-1.70	0.000A	0.000A	-10.00mA
-1.50	-10.00mA	0.000A	-10.00mA
-1.00	-11.00mA	-5.00mA	-13.00mA
-0.90	-12.00mA	-5.00mA	-15.00mA
-0.80	-24.00mA	-7.00mA	-32.51mA

Appendix B IBIS Model

-0.70	-29.14mA	-8.00mA	-32.35mA
-0.60	-26.47mA	-13.80mA	-29.35mA
-0.50	-22.61mA	-14.54mA	-25.54mA
-0.40	-18.32mA	-12.17mA	-20.93mA
-0.30	-13.87mA	-9.16mA	-15.91mA
-0.20	-9.33mA	-6.10mA	-10.74mA
-0.10	-4.70mA	-3.05mA	-5.43mA
-0.00	2.86nA	7.25nA	11.72nA
0.10	4.61mA	2.94mA	5.36mA
0.20	8.96mA	5.69mA	10.49mA
0.30	13.07mA	8.26mA	15.36mA
0.40	16.92mA	10.65mA	20.00mA
0.50	20.53mA	12.86mA	24.40mA
0.60	23.91mA	14.90mA	28.55mA
0.70	27.04mA	16.76mA	32.48mA
0.80	29.95mA	18.46mA	36.18mA
0.90	32.61mA	19.99mA	39.64mA
1.00	35.06mA	21.37mA	42.87mA
1.10	37.27mA	22.58mA	45.87mA
1.20	39.27mA	23.64mA	48.64mA
1.30	41.04mA	24.55mA	51.19mA
1.40	42.60mA	25.32mA	53.50mA
1.50	43.95mA	25.95mA	55.60mA
1.60	45.08mA	26.44mA	57.46mA
1.70	46.00mA	26.80mA	59.11mA
1.80	46.70mA	27.07mA	60.53mA
1.90	47.20mA	27.26mA	61.71mA
2.00	47.55mA	27.41mA	62.63mA
2.10	47.81mA	27.53mA	63.31mA
2.20	48.01mA	27.63mA	63.79mA
2.30	48.17mA	27.71mA	64.15mA
2.40	48.31mA	27.78mA	64.43mA
2.50	48.42mA	27.85mA	64.65mA
2.60	48.53mA	27.90mA	64.84mA
2.70	48.62mA	27.96mA	65.00mA
2.80	48.70mA	28.01mA	65.14mA
2.90	48.78mA	28.05mA	65.27mA
3.00	48.85mA	28.09mA	65.38mA
3.10	48.92mA	28.14mA	65.49mA
3.20	48.99mA	28.18mA	65.59mA
3.30	49.05mA	28.23mA	65.68mA
3.40	49.12mA	28.42mA	65.77mA
3.50	49.20mA	28.97mA	65.86mA
3.60	49.24mA	29.74mA	65.95mA

3.70	49.31mA	30.57mA	66.04mA
3.80	49.40mA	31.13mA	66.12mA
3.90	49.61mA	28.60mA	66.22mA
4.00	50.41mA	28.66mA	66.33mA
4.10	51.65mA	28.72mA	66.49mA
4.20	52.87mA	28.80mA	66.72mA
4.30	50.78mA	28.89mA	67.28mA
4.50	50.67mA	29.12mA	70.40mA
4.70	51.17mA	29.42mA	73.03mA
4.90	51.85mA	29.83mA	69.12mA
5.10	52.75mA	30.37mA	70.18mA
5.30	53.86mA	31.02mA	71.45mA
5.50	55.21mA	31.82mA	73.05mA
5.70	56.82mA	32.77mA	74.98mA
5.90	58.68mA	33.86mA	77.25mA
6.10	60.78mA	35.10mA	79.83mA
6.60	66.91mA	38.73mA	87.50mA
[Pullup]			
voltage	I (typ)	I (min)	I (max)
-3.30	0.11A	82.01mA	0.13A
-3.10	0.11A	79.25mA	0.13A
-2.90	0.10A	76.07mA	0.12A
-2.70	97.60mA	72.55mA	0.11A
-2.50	92.41mA	68.70mA	0.11A
-2.30	87.04mA	64.55mA	0.10A
-2.10	81.44mA	60.13mA	94.69mA
-1.90	75.56mA	55.45mA	87.72mA
-1.70	69.36mA	50.52mA	80.48mA
-1.50	62.83mA	45.36mA	73.03mA
-1.00	48.46mA	31.37mA	56.75mA
-0.90	43.82mA	28.63mA	50.74mA
-0.80	38.59mA	28.69mA	44.61mA
-0.70	33.28mA	24.97mA	38.60mA
-0.60	28.26mA	21.04mA	33.20mA
-0.50	23.64mA	17.11mA	27.91mA
-0.40	19.01mA	13.34mA	22.52mA
-0.30	14.32mA	9.87mA	17.03mA
-0.20	9.58mA	6.53mA	11.45mA
-0.10	4.80mA	3.23mA	5.78mA
0.00	34.08uA	11.20uA	71.92uA
0.10	-4.58mA	-3.08mA	-5.50mA
0.20	-8.94mA	-5.98mA	-10.80mA

Appendix B IBIS Model

0.30	-13.04mA	-8.72mA	-15.82mA
0.40	-16.89mA	-11.27mA	-20.56mA
0.50	-20.50mA	-13.66mA	-25.04mA
0.60	-23.86mA	-15.87mA	-29.25mA
0.70	-26.98mA	-17.92mA	-33.21mA
0.80	-29.87mA	-19.80mA	-36.91mA
0.90	-32.53mA	-21.51mA	-40.36mA
1.00	-34.96mA	-23.06mA	-43.56mA
1.10	-37.16mA	-24.45mA	-46.52mA
1.20	-39.15mA	-25.68mA	-49.24mA
1.30	-40.92mA	-26.75mA	-51.73mA
1.40	-42.48mA	-27.66mA	-53.98mA
1.50	-43.83mA	-28.43mA	-56.01mA
1.60	-44.98mA	-29.05mA	-57.81mA
1.70	-45.94mA	-29.53mA	-59.40mA
1.80	-46.72mA	-29.90mA	-60.77mA
1.90	-47.35mA	-30.20mA	-61.93mA
2.00	-47.86mA	-30.45mA	-62.90mA
2.10	-48.29mA	-30.66mA	-63.70mA
2.20	-48.65mA	-30.85mA	-64.37mA
2.30	-48.97mA	-31.02mA	-64.93mA
2.40	-49.25mA	-31.17mA	-65.40mA
2.50	-49.50mA	-31.31mA	-65.82mA
2.60	-49.72mA	-31.44mA	-66.18mA
2.70	-49.92mA	-31.56mA	-66.50mA
2.80	-50.11mA	-31.67mA	-66.79mA
2.90	-50.28mA	-31.78mA	-67.05mA
3.00	-50.44mA	-31.88mA	-67.29mA
3.10	-50.59mA	-31.98mA	-67.51mA
3.20	-50.74mA	-32.08mA	-67.72mA
3.30	-50.88mA	-32.20mA	-67.92mA
3.40	-51.01mA	-32.75mA	-68.11mA
3.50	-51.14mA	-40.35mA	-68.29mA
3.60	-51.27mA	-0.14A	-68.47mA
3.70	-51.42mA	-0.94A	-68.64mA
3.80	-51.84mA	-2.69A	-68.80mA
3.90	-53.78mA	-4.48A	-68.97mA
4.00	-64.80mA	-6.27A	-69.30mA
4.10	-0.29A	-8.06A	-70.82mA
4.20	-1.85A	-9.85A	-75.29mA
4.30	-3.90A	-11.63A	-83.12mA
4.50	-8.00A	-15.21A	-1.14A
4.70	-12.10A	-18.79A	-5.39A
4.90	-16.20A	-22.36A	-9.64A

5.10	-20.30A	-25.94A	-13.89A
5.30	-24.40A	-29.51A	-18.15A
5.50	-28.50A	-33.09A	-22.41A
5.70	-32.60A	-36.67A	-26.66A
5.90	-36.70A	-40.24A	-30.92A
6.10	-40.80A	-43.82A	-35.17A
6.60	-51.05A	-52.76A	-45.81A

[GND_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	-85.83A	-77.78A	-88.32A
-4.80	-81.73A	-74.20A	-84.06A
-4.60	-77.63A	-70.62A	-79.80A
-4.40	-73.53A	-67.04A	-75.54A
-4.20	-69.43A	-63.46A	-71.28A
-4.00	-65.33A	-59.88A	-67.02A
-3.80	-61.23A	-56.30A	-62.76A
-3.60	-57.13A	-52.72A	-58.50A
-3.40	-53.03A	-49.14A	-54.24A
-3.20	-48.93A	-45.56A	-49.98A
-3.00	-44.84A	-41.99A	-45.73A
-2.80	-40.74A	-38.42A	-41.48A
-2.60	-36.64A	-34.84A	-37.22A
-2.40	-32.54A	-31.27A	-32.97A
-2.20	-28.45A	-27.69A	-28.72A
-2.00	-24.35A	-24.12A	-24.46A
-1.80	-20.25A	-20.54A	-20.21A
-1.60	-16.15A	-16.97A	-15.95A
-1.40	-12.05A	-13.39A	-11.70A
-1.20	-7.95A	-9.82A	-7.44A
-1.00	-3.85A	-6.24A	-3.19A
-0.80	-0.23A	-2.66A	-70.99mA
-0.60	-2.25mA	-0.10A	-5.98mA
-0.40	-89.81uA	-0.52mA	-0.26mA
-0.20	-27.92uA	-14.70uA	-42.92uA
-0.00	-87.63nA	-89.05nA	-0.10uA
0.20	18.71uA	7.31uA	32.27uA
0.40	29.19uA	10.25uA	54.12uA
0.60	32.49uA	10.67uA	65.78uA
0.80	33.07uA	10.78uA	69.33uA
1.00	33.30uA	10.86uA	70.17uA
1.20	33.45uA	10.92uA	70.55uA
1.40	33.57uA	10.97uA	70.80uA

Appendix B IBIS Model

1.60	33.68uA	11.02uA	70.99uA
1.80	33.77uA	11.07uA	71.16uA
2.00	33.87uA	11.11uA	71.32uA
2.20	33.96uA	11.14uA	71.46uA
2.40	34.01uA	11.15uA	71.61uA
2.60	34.03uA	11.16uA	71.76uA
2.80	34.05uA	11.17uA	71.84uA
3.00	34.06uA	11.19uA	71.86uA
3.20	34.07uA	11.51uA	71.88uA
3.40	34.07uA	10.95uA	71.90uA
3.60	34.07uA	10.39uA	71.92uA
3.80	34.07uA	9.83uA	71.94uA
4.00	34.07uA	9.27uA	71.96uA
4.20	34.07uA	8.71uA	71.98uA
4.40	34.07uA	8.15uA	72.00uA
4.60	34.07uA	7.59uA	72.02uA
4.80	34.07uA	7.03uA	72.04uA
5.00	34.07uA	6.47uA	72.06uA

[POWER_clamp]

voltage	I (typ)	I (min)	I (max)
-5.00	48.57uA	16.33uA	95.57uA
-4.90	48.24uA	16.21uA	95.07uA
-4.80	47.91uA	16.09uA	94.57uA
-4.70	47.58uA	15.97uA	94.07uA
-4.60	47.25uA	15.85uA	93.57uA
-4.50	46.92uA	15.73uA	93.07uA
-4.40	46.59uA	15.61uA	92.57uA
-4.30	46.26uA	15.49uA	92.07uA
-4.20	45.93uA	15.37uA	91.57uA
-4.10	45.60uA	15.25uA	91.07uA
-4.00	45.27uA	15.13uA	90.57uA
-3.90	44.94uA	15.01uA	90.07uA
-3.80	44.61uA	14.89uA	89.57uA
-3.70	44.28uA	14.77uA	89.07uA
-3.60	43.95uA	14.65uA	88.57uA
-3.50	43.62uA	14.53uA	88.07uA
-3.40	43.29uA	14.41uA	87.57uA
-3.30	42.96uA	14.29uA	87.07uA
-3.20	42.63uA	14.17uA	86.57uA
-3.10	42.30uA	14.05uA	86.07uA
-3.00	41.97uA	13.93uA	85.57uA
-2.90	41.64uA	13.81uA	85.07uA

-2.80	41.31uA	13.69uA	84.57uA
-2.70	40.98uA	13.57uA	84.07uA
-2.60	40.65uA	13.45uA	83.57uA
-2.50	40.32uA	13.33uA	83.07uA
-2.40	39.99uA	13.21uA	82.57uA
-2.30	39.66uA	13.09uA	82.07uA
-2.20	39.33uA	12.97uA	81.57uA
-2.10	39.00uA	12.85uA	81.07uA
-2.00	38.67uA	12.73uA	80.57uA
-1.90	38.34uA	12.61uA	80.07uA
-1.80	38.01uA	12.49uA	79.57uA
-1.70	37.68uA	12.37uA	79.07uA
-1.60	37.35uA	12.25uA	78.57uA
-1.50	37.02uA	12.15uA	78.07uA
-1.40	36.71uA	12.05uA	77.57uA
-1.30	36.42uA	11.95uA	77.07uA
-1.20	36.15uA	11.87uA	76.57uA
-1.10	35.89uA	11.79uA	76.07uA
-1.00	35.66uA	11.72uA	75.57uA
-0.90	35.45uA	11.66uA	75.10uA
-0.80	35.26uA	11.60uA	74.67uA
-0.70	35.09uA	11.55uA	74.28uA
-0.60	34.93uA	11.51uA	73.93uA
-0.50	34.80uA	11.47uA	73.61uA
-0.40	34.68uA	11.43uA	73.34uA
-0.30	34.59uA	11.41uA	73.10uA
-0.20	34.50uA	11.38uA	72.89uA
-0.10	34.43uA	11.36uA	72.72uA
0.00	34.37uA	11.34uA	72.57uA

|

[Ramp]

variable	typ	min	max
dV/dt_r	1.21/2.06n	0.85/2.62n	1.45/1.82n
dV/dt_f	1.22/2.51n	0.78/3.11n	1.45/2.14n

R_load = 50.00

|

[Rising Waveform]

R_fixture = 50.00

V_fixture = 0.000

V_fixture_min = 0.000

V_fixture_max = 0.000

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
------	--------	--------	--------

Appendix B IBIS Model

0.000S	1.26uV	1.62uV	1.22uV
0.20nS	1.04uV	1.45uV	0.74uV
0.40nS	-5.64uV	-1.36uV	11.59uV
0.60nS	-0.29mV	-5.13uV	-3.27mV
0.80nS	-3.54mV	25.94uV	-9.17mV
1.00nS	-3.50mV	-4.79uV	56.24mV
1.20nS	33.86mV	-0.86mV	0.13V
1.40nS	79.34mV	-3.75mV	0.19V
1.60nS	0.14V	-8.09mV	0.27V
1.80nS	0.20V	3.52mV	0.36V
2.00nS	0.28V	38.97mV	0.47V
2.20nS	0.36V	82.84mV	0.59V
2.40nS	0.47V	0.13V	0.74V
2.60nS	0.60V	0.18V	0.90V
2.80nS	0.77V	0.27V	1.12V
3.00nS	0.92V	0.34V	1.32V
3.20nS	1.03V	0.40V	1.46V
3.40nS	1.16V	0.50V	1.63V
3.60nS	1.29V	0.59V	1.78V
3.80nS	1.39V	0.67V	1.91V
4.00nS	1.49V	0.75V	2.01V
4.20nS	1.58V	0.84V	2.11V
4.40nS	1.65V	0.91V	2.18V
4.60nS	1.69V	0.95V	2.21V
4.80nS	1.72V	0.99V	2.23V
5.00nS	1.76V	1.03V	2.27V
5.20nS	1.80V	1.07V	2.29V
5.40nS	1.83V	1.12V	2.31V
5.60nS	1.86V	1.16V	2.33V
5.80nS	1.88V	1.18V	2.34V
6.00nS	1.89V	1.20V	2.34V
6.20nS	1.91V	1.23V	2.35V
6.40nS	1.92V	1.25V	2.36V
6.60nS	1.93V	1.27V	2.37V
6.80nS	1.94V	1.28V	2.38V
7.00nS	1.95V	1.30V	2.38V
7.20nS	1.96V	1.31V	2.39V
7.40nS	1.97V	1.33V	2.39V
7.60nS	1.98V	1.34V	2.39V
7.80nS	1.98V	1.35V	2.40V
8.00nS	1.98V	1.36V	2.40V
8.20nS	1.99V	1.37V	2.40V
8.40nS	1.99V	1.37V	2.40V

8.60nS	1.99V	1.38V	2.41V
8.80nS	2.00V	1.39V	2.41V
9.00nS	2.00V	1.39V	2.41V
9.20nS	2.00V	1.40V	2.41V
9.40nS	2.01V	1.40V	2.41V
9.60nS	2.01V	1.41V	2.42V
9.80nS	2.01V	1.41V	2.42V
10.00nS	2.01V	1.41V	2.42V

```

|
[Rising Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

```

time	V(typ)	V(min)	V(max)
0.000S	1.27V	1.66V	1.18V
0.20nS	1.27V	1.66V	1.18V
0.40nS	1.27V	1.66V	1.18V
0.60nS	1.27V	1.66V	1.19V
0.80nS	1.28V	1.66V	1.24V
1.00nS	1.40V	1.66V	1.47V
1.20nS	1.60V	1.67V	1.71V
1.40nS	1.77V	1.69V	1.88V
1.60nS	1.99V	1.80V	2.12V
1.80nS	2.24V	1.95V	2.41V
2.00nS	2.50V	2.13V	2.70V
2.20nS	2.74V	2.32V	2.99V
2.40nS	2.94V	2.49V	3.21V
2.60nS	3.09V	2.63V	3.34V
2.80nS	3.18V	2.79V	3.44V
3.00nS	3.24V	2.87V	3.49V
3.20nS	3.26V	2.91V	3.52V
3.40nS	3.27V	2.96V	3.55V
3.60nS	3.29V	2.98V	3.57V
3.80nS	3.29V	2.99V	3.59V
4.00nS	3.30V	2.99V	3.59V
4.20nS	3.30V	3.00V	3.60V
4.40nS	3.30V	3.00V	3.60V
4.60nS	3.30V	3.00V	3.60V
4.80nS	3.30V	3.00V	3.60V
5.00nS	3.30V	3.00V	3.60V

Appendix B IBIS Model

5.20nS	3.30V	3.00V	3.60V
5.40nS	3.30V	3.00V	3.60V
5.60nS	3.30V	3.00V	3.60V
5.80nS	3.30V	3.00V	3.60V
6.00nS	3.30V	3.00V	3.60V
6.20nS	3.30V	3.00V	3.60V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V
7.00nS	3.30V	3.00V	3.60V
7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V
8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V
9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

|
[Falling Waveform]

R_fixture = 50.00

V_fixture = 0.000

V_fixture_min = 0.000

V_fixture_max = 0.000

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	2.02V	1.44V	2.43V
0.20nS	2.02V	1.44V	2.43V
0.40nS	2.02V	1.44V	2.43V
0.60nS	2.02V	1.44V	2.38V
0.80nS	1.97V	1.44V	2.13V
1.00nS	1.73V	1.44V	1.82V
1.20nS	1.45V	1.42V	1.49V
1.40nS	1.24V	1.38V	1.24V
1.60nS	0.96V	1.29V	0.92V

1.80nS	0.70V	1.12V	0.67V
2.00nS	0.50V	0.92V	0.50V
2.20nS	0.36V	0.73V	0.38V
2.40nS	0.27V	0.55V	0.30V
2.60nS	0.20V	0.40V	0.24V
2.80nS	0.14V	0.27V	0.17V
3.00nS	99.16mV	0.20V	0.13V
3.20nS	79.41mV	0.16V	0.11V
3.40nS	53.08mV	0.11V	78.74mV
3.60nS	36.21mV	75.26mV	59.16mV
3.80nS	23.36mV	51.00mV	39.59mV
4.00nS	12.42mV	31.87mV	27.31mV
4.20nS	6.73mV	18.57mV	15.01mV
4.40nS	2.10mV	8.15mV	7.54mV
4.60nS	1.57mV	5.93mV	4.99mV
4.80nS	1.14mV	3.71mV	2.45mV
5.00nS	0.68mV	1.71mV	1.29mV
5.20nS	0.62mV	1.31mV	0.88mV
5.40nS	0.54mV	0.89mV	0.54mV
5.60nS	0.46mV	0.73mV	0.46mV
5.80nS	0.41mV	0.65mV	0.42mV
6.00nS	0.37mV	0.59mV	0.38mV
6.20nS	0.34mV	0.53mV	0.34mV
6.40nS	0.32mV	0.48mV	0.29mV
6.60nS	0.27mV	0.43mV	0.26mV
6.80nS	0.22mV	0.38mV	0.22mV
7.00nS	0.18mV	0.34mV	0.20mV
7.20nS	0.18mV	0.30mV	0.18mV
7.40nS	0.18mV	0.26mV	0.15mV
7.60nS	0.15mV	0.23mV	0.13mV
7.80nS	0.12mV	0.22mV	0.12mV
8.00nS	0.11mV	0.20mV	0.11mV
8.20nS	0.11mV	0.18mV	0.10mV
8.40nS	0.12mV	0.17mV	92.36uV
8.60nS	97.87uV	0.16mV	78.53uV
8.80nS	59.73uV	0.15mV	64.71uV
9.00nS	36.18uV	0.14mV	61.02uV
9.20nS	61.23uV	0.12mV	60.74uV
9.40nS	87.87uV	0.10mV	58.12uV
9.60nS	67.13uV	0.10mV	46.02uV
9.80nS	29.42uV	0.10mV	39.81uV
10.00nS	71.42uV	84.83uV	50.29uV

[Falling Waveform]

Appendix B IBIS Model

R_fixture = 50.00

V_fixture = 3.30

V_fixture_min = 3.00

V_fixture_max = 3.60

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	3.30V	3.00V	3.60V
0.20nS	3.30V	3.00V	3.60V
0.40nS	3.30V	3.00V	3.60V
0.60nS	3.30V	3.00V	3.59V
0.80nS	3.30V	3.00V	3.48V
1.00nS	3.22V	3.00V	3.36V
1.20nS	3.12V	3.00V	3.25V
1.40nS	3.06V	3.00V	3.16V
1.60nS	2.96V	3.00V	3.04V
1.80nS	2.86V	2.95V	2.90V
2.00nS	2.75V	2.89V	2.76V
2.20nS	2.64V	2.83V	2.61V
2.40nS	2.52V	2.77V	2.48V
2.60nS	2.40V	2.70V	2.34V
2.80nS	2.26V	2.61V	2.18V
3.00nS	2.16V	2.54V	2.04V
3.20nS	2.10V	2.48V	1.93V
3.40nS	2.01V	2.41V	1.79V
3.60nS	1.93V	2.35V	1.68V
3.80nS	1.86V	2.30V	1.57V
4.00nS	1.78V	2.25V	1.49V
4.20nS	1.68V	2.19V	1.41V
4.40nS	1.58V	2.13V	1.34V
4.60nS	1.53V	2.10V	1.31V
4.80nS	1.49V	2.08V	1.29V
5.00nS	1.43V	2.04V	1.26V
5.20nS	1.39V	2.01V	1.24V
5.40nS	1.35V	1.98V	1.22V
5.60nS	1.32V	1.95V	1.21V
5.80nS	1.31V	1.94V	1.20V
6.00nS	1.30V	1.93V	1.20V
6.20nS	1.29V	1.91V	1.19V
6.40nS	1.29V	1.90V	1.19V
6.60nS	1.29V	1.88V	1.19V
6.80nS	1.28V	1.87V	1.19V
7.00nS	1.28V	1.85V	1.19V

7.20nS	1.28V	1.84V	1.19V
7.40nS	1.28V	1.83V	1.19V
7.60nS	1.28V	1.82V	1.19V
7.80nS	1.28V	1.81V	1.19V
8.00nS	1.28V	1.81V	1.19V
8.20nS	1.28V	1.80V	1.19V
8.40nS	1.27V	1.79V	1.19V
8.60nS	1.27V	1.79V	1.19V
8.80nS	1.27V	1.78V	1.19V
9.00nS	1.27V	1.77V	1.19V
9.20nS	1.27V	1.76V	1.19V
9.40nS	1.27V	1.75V	1.19V
9.60nS	1.27V	1.73V	1.18V
9.80nS	1.27V	1.72V	1.18V
10.00nS	1.27V	1.71V	1.18V

|
| End [Model] prd12dgz
|

| *****

| Model prd16dgz

| *****

|
[Model] prd16dgz
Model_type I/O
Polarity Non-Inverting
Enable Active-Low
Vinl = 0.80V
Vinh = 2.00V
Vmeas = 1.50V
Cref = 50.00pF
Rref = 1.00M
Vref = 0.000V

C_comp 3.86pF 3.48pF 4.25pF

|
|
[Temperature Range] 25.00 0.12k 0.000
[Pullup Reference] 3.30V 3.00V 3.60V
[Pulldown Reference] 0.000V 0.000V 0.000V
[POWER Clamp Reference] 5.00V 4.50V 5.50V
[GND Clamp Reference] 0.000V 0.000V 0.000V

[Pulldown]

voltage	I(typ)	I(min)	I(max)
-3.30	-10.00mA	0.000A	0.000A

Appendix B IBIS Model

-3.10	0.000A	0.000A	0.000A
-2.90	0.000A	0.000A	0.000A
-2.70	0.000A	0.000A	0.000A
-2.50	0.000A	0.000A	0.000A
-2.30	0.000A	0.000A	0.000A
-2.10	-10.00mA	0.000A	0.000A
-1.90	0.000A	0.000A	-10.00mA
-1.70	-10.00mA	0.000A	-10.00mA
-1.50	-10.00mA	0.000A	-20.00mA
-1.00	-16.00mA	-6.00mA	-18.00mA
-0.90	-16.00mA	-8.00mA	-21.00mA
-0.80	-32.00mA	-8.00mA	-43.34mA
-0.70	-38.86mA	-10.60mA	-43.13mA
-0.60	-35.29mA	-18.40mA	-39.13mA
-0.50	-30.14mA	-19.39mA	-34.05mA
-0.40	-24.42mA	-16.22mA	-27.89mA
-0.30	-18.49mA	-12.22mA	-21.21mA
-0.20	-12.44mA	-8.14mA	-14.32mA
-0.10	-6.27mA	-4.06mA	-7.24mA
-0.00	4.09nA	6.98nA	10.67nA
0.10	6.14mA	3.92mA	7.15mA
0.20	11.95mA	7.59mA	13.98mA
0.30	17.42mA	11.01mA	20.48mA
0.40	22.56mA	14.20mA	26.67mA
0.50	27.38mA	17.14mA	32.53mA
0.60	31.88mA	19.86mA	38.07mA
0.70	36.06mA	22.35mA	43.31mA
0.80	39.93mA	24.61mA	48.24mA
0.90	43.49mA	26.66mA	52.85mA
1.00	46.74mA	28.49mA	57.16mA
1.10	49.69mA	30.11mA	61.16mA
1.20	52.35mA	31.52mA	64.86mA
1.30	54.72mA	32.74mA	68.25mA
1.40	56.80mA	33.76mA	71.34mA
1.50	58.59mA	34.59mA	74.13mA
1.60	60.11mA	35.25mA	76.62mA
1.70	61.33mA	35.74mA	78.81mA
1.80	62.26mA	36.09mA	80.70mA
1.90	62.93mA	36.35mA	82.27mA
2.00	63.40mA	36.55mA	83.51mA
2.10	63.75mA	36.71mA	84.41mA
2.20	64.01mA	36.84mA	85.06mA
2.30	64.23mA	36.95mA	85.54mA
2.40	64.41mA	37.04mA	85.91mA

2.50	64.56mA	37.13mA	86.20mA
2.60	64.70mA	37.21mA	86.45mA
2.70	64.82mA	37.28mA	86.66mA
2.80	64.94mA	37.34mA	86.85mA
2.90	65.04mA	37.40mA	87.02mA
3.00	65.14mA	37.46mA	87.17mA
3.10	65.23mA	37.51mA	87.32mA
3.20	65.32mA	37.57mA	87.45mA
3.30	65.40mA	37.63mA	87.58mA
3.40	65.49mA	37.81mA	87.70mA
3.50	65.59mA	38.34mA	87.82mA
3.60	65.66mA	39.10mA	87.93mA
3.70	65.75mA	39.94mA	88.05mA
3.80	65.86mA	40.42mA	88.16mA
3.90	66.08mA	38.09mA	88.29mA
4.00	66.86mA	38.16mA	88.44mA
4.10	68.11mA	38.25mA	88.63mA
4.20	69.36mA	38.35mA	88.90mA
4.30	67.34mA	38.47mA	89.46mA
4.50	67.43mA	38.78mA	92.67mA
4.70	68.10mA	39.19mA	95.47mA
4.90	69.00mA	39.73mA	91.91mA
5.10	70.20mA	40.44mA	93.29mA
5.30	71.67mA	41.32mA	95.00mA
5.50	73.47mA	42.38mA	97.12mA
5.70	75.61mA	43.64mA	99.69mA
5.90	78.09mA	45.10mA	0.10A
6.10	80.89mA	46.75mA	0.11A
6.60	89.06mA	51.59mA	0.12A
[Pullup]			
voltage	I (typ)	I (min)	I (max)
-3.30	0.16A	0.12A	0.19A
-3.10	0.16A	0.12A	0.18A
-2.90	0.15A	0.11A	0.17A
-2.70	0.14A	0.11A	0.16A
-2.50	0.14A	0.10A	0.16A
-2.30	0.13A	96.26mA	0.15A
-2.10	0.12A	89.72mA	0.14A
-1.90	0.11A	82.79mA	0.13A
-1.70	0.10A	75.47mA	0.12A
-1.50	93.76mA	67.80mA	0.11A
-1.00	70.54mA	46.98mA	82.43mA

Appendix B IBIS Model

-0.90	63.97mA	42.83mA	74.23mA
-0.80	56.74mA	41.47mA	65.83mA
-0.70	49.39mA	36.27mA	57.50mA
-0.60	42.27mA	30.78mA	49.67mA
-0.50	35.43mA	25.27mA	41.79mA
-0.40	28.50mA	19.90mA	33.74mA
-0.30	21.47mA	14.79mA	25.52mA
-0.20	14.35mA	9.79mA	17.14mA
-0.10	7.19mA	4.85mA	8.64mA
0.00	34.08uA	11.19uA	71.92uA
0.10	-6.89mA	-4.62mA	-8.29mA
0.20	-13.43mA	-8.98mA	-16.24mA
0.30	-19.58mA	-13.08mA	-23.77mA
0.40	-25.36mA	-16.92mA	-30.88mA
0.50	-30.77mA	-20.50mA	-37.60mA
0.60	-35.81mA	-23.82mA	-43.93mA
0.70	-40.49mA	-26.89mA	-49.86mA
0.80	-44.83mA	-29.70mA	-55.41mA
0.90	-48.81mA	-32.27mA	-60.59mA
1.00	-52.46mA	-34.60mA	-65.39mA
1.10	-55.77mA	-36.68mA	-69.83mA
1.20	-58.75mA	-38.52mA	-73.91mA
1.30	-61.41mA	-40.13mA	-77.64mA
1.40	-63.75mA	-41.50mA	-81.02mA
1.50	-65.77mA	-42.65mA	-84.06mA
1.60	-67.50mA	-43.58mA	-86.77mA
1.70	-68.93mA	-44.31mA	-89.14mA
1.80	-70.10mA	-44.87mA	-91.20mA
1.90	-71.04mA	-45.31mA	-92.94mA
2.00	-71.82mA	-45.68mA	-94.40mA
2.10	-72.46mA	-46.00mA	-95.60mA
2.20	-73.01mA	-46.28mA	-96.60mA
2.30	-73.48mA	-46.53mA	-97.44mA
2.40	-73.90mA	-46.76mA	-98.15mA
2.50	-74.27mA	-46.97mA	-98.77mA
2.60	-74.60mA	-47.17mA	-99.31mA
2.70	-74.91mA	-47.35mA	-99.80mA
2.80	-75.18mA	-47.52mA	-0.10A
2.90	-75.44mA	-47.68mA	-0.10A
3.00	-75.68mA	-47.83mA	-0.10A
3.10	-75.90mA	-47.97mA	-0.10A
3.20	-76.12mA	-48.11mA	-0.10A
3.30	-76.32mA	-48.27mA	-0.10A
3.40	-76.52mA	-48.87mA	-0.10A

3.50	-76.71mA	-56.48mA	-0.10A
3.60	-76.89mA	-0.15A	-0.10A
3.70	-77.09mA	-0.95A	-0.10A
3.80	-77.56mA	-2.71A	-0.10A
3.90	-79.54mA	-4.50A	-0.10A
4.00	-90.56mA	-6.29A	-0.10A
4.10	-0.31A	-8.09A	-0.11A
4.20	-1.88A	-9.88A	-0.11A
4.30	-3.93A	-11.66A	-0.12A
4.50	-8.04A	-15.24A	-1.17A
4.70	-12.14A	-18.83A	-5.43A
4.90	-16.25A	-22.41A	-9.69A
5.10	-20.36A	-25.99A	-13.95A
5.30	-24.46A	-29.57A	-18.21A
5.50	-28.57A	-33.15A	-22.48A
5.70	-32.68A	-36.73A	-26.74A
5.90	-36.78A	-40.31A	-31.00A
6.10	-40.89A	-43.89A	-35.27A
6.60	-51.16A	-52.84A	-45.93A
[GND_clamp]			
voltage			
	I (typ)	I (min)	I (max)
-5.00	-85.90A	-77.84A	-88.40A
-4.80	-81.80A	-74.26A	-84.14A
-4.60	-77.70A	-70.68A	-79.88A
-4.40	-73.60A	-67.10A	-75.62A
-4.20	-69.50A	-63.52A	-71.36A
-4.00	-65.40A	-59.94A	-67.10A
-3.80	-61.30A	-56.36A	-62.84A
-3.60	-57.20A	-52.78A	-58.58A
-3.40	-53.10A	-49.20A	-54.32A
-3.20	-49.00A	-45.62A	-50.06A
-3.00	-44.90A	-42.04A	-45.80A
-2.80	-40.80A	-38.46A	-41.54A
-2.60	-36.69A	-34.89A	-37.28A
-2.40	-32.59A	-31.31A	-33.02A
-2.20	-28.49A	-27.73A	-28.76A
-2.00	-24.38A	-24.15A	-24.50A
-1.80	-20.28A	-20.57A	-20.24A
-1.60	-16.17A	-16.99A	-15.97A
-1.40	-12.06A	-13.40A	-11.71A
-1.20	-7.96A	-9.83A	-7.45A
-1.00	-3.86A	-6.25A	-3.19A

Appendix B IBIS Model

-0.80	-0.23A	-2.66A	-70.76mA
-0.60	-2.22mA	-0.10A	-5.90mA
-0.40	-89.20uA	-0.52mA	-0.26mA
-0.20	-27.89uA	-14.67uA	-42.88uA
-0.00	-62.88nA	-63.80nA	-74.38nA
0.20	18.73uA	7.33uA	32.30uA
0.40	29.21uA	10.27uA	54.14uA
0.60	32.51uA	10.69uA	65.81uA
0.80	33.09uA	10.80uA	69.35uA
1.00	33.31uA	10.87uA	70.19uA
1.20	33.46uA	10.93uA	70.56uA
1.40	33.58uA	10.98uA	70.81uA
1.60	33.69uA	11.03uA	71.00uA
1.80	33.78uA	11.08uA	71.17uA
2.00	33.87uA	11.12uA	71.33uA
2.20	33.96uA	11.14uA	71.47uA
2.40	34.01uA	11.15uA	71.62uA
2.60	34.03uA	11.16uA	71.76uA
2.80	34.04uA	11.17uA	71.84uA
3.00	34.05uA	11.18uA	71.86uA
3.20	34.06uA	11.57uA	71.88uA
3.40	34.08uA	10.87uA	71.90uA
3.60	34.10uA	10.17uA	71.92uA
3.80	34.12uA	9.47uA	71.94uA
4.00	34.14uA	8.77uA	71.96uA
4.20	34.16uA	8.07uA	71.98uA
4.40	34.18uA	7.37uA	72.00uA
4.60	34.20uA	6.67uA	72.02uA
4.80	34.22uA	5.97uA	72.04uA
5.00	34.24uA	5.27uA	72.06uA

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	48.54uA	16.29uA	95.93uA
-4.90	48.21uA	16.17uA	95.42uA
-4.80	47.88uA	16.05uA	94.91uA
-4.70	47.55uA	15.93uA	94.40uA
-4.60	47.22uA	15.81uA	93.89uA
-4.50	46.89uA	15.69uA	93.38uA
-4.40	46.56uA	15.57uA	92.87uA
-4.30	46.23uA	15.45uA	92.36uA
-4.20	45.90uA	15.33uA	91.85uA
-4.10	45.57uA	15.21uA	91.34uA

-4.00	45.24uA	15.09uA	90.83uA
-3.90	44.91uA	14.97uA	90.32uA
-3.80	44.58uA	14.85uA	89.81uA
-3.70	44.25uA	14.73uA	89.30uA
-3.60	43.92uA	14.61uA	88.79uA
-3.50	43.59uA	14.49uA	88.28uA
-3.40	43.26uA	14.37uA	87.77uA
-3.30	42.93uA	14.25uA	87.26uA
-3.20	42.60uA	14.13uA	86.75uA
-3.10	42.27uA	14.01uA	86.24uA
-3.00	41.94uA	13.89uA	85.73uA
-2.90	41.61uA	13.77uA	85.22uA
-2.80	41.28uA	13.65uA	84.71uA
-2.70	40.95uA	13.53uA	84.20uA
-2.60	40.62uA	13.41uA	83.69uA
-2.50	40.29uA	13.29uA	83.18uA
-2.40	39.96uA	13.17uA	82.67uA
-2.30	39.63uA	13.05uA	82.16uA
-2.20	39.30uA	12.93uA	81.65uA
-2.10	38.97uA	12.81uA	81.14uA
-2.00	38.64uA	12.69uA	80.63uA
-1.90	38.31uA	12.57uA	80.12uA
-1.80	37.98uA	12.45uA	79.61uA
-1.70	37.65uA	12.33uA	79.10uA
-1.60	37.32uA	12.22uA	78.59uA
-1.50	36.99uA	12.11uA	78.08uA
-1.40	36.68uA	12.02uA	77.57uA
-1.30	36.39uA	11.92uA	77.06uA
-1.20	36.12uA	11.84uA	76.55uA
-1.10	35.87uA	11.76uA	76.04uA
-1.00	35.63uA	11.69uA	75.53uA
-0.90	35.42uA	11.63uA	75.06uA
-0.80	35.23uA	11.58uA	74.64uA
-0.70	35.06uA	11.53uA	74.25uA
-0.60	34.91uA	11.48uA	73.90uA
-0.50	34.78uA	11.44uA	73.58uA
-0.40	34.66uA	11.41uA	73.31uA
-0.30	34.56uA	11.38uA	73.07uA
-0.20	34.48uA	11.36uA	72.87uA
-0.10	34.41uA	11.34uA	72.69uA
0.00	34.35uA	11.32uA	72.55uA

|

[Ramp]

| variable

typ

min

max

Appendix B IBIS Model

```

dV/dt_r          1.43/2.06n          1.08/2.82n          1.66/1.86n
dV/dt_f          1.39/2.80n          0.98/4.41n          1.61/2.52n
R_load = 50.00
|
[Rising Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F
| time            V(typ)            V(min)            V(max)
|
0.000S           0.71uV            0.94uV            0.68uV
0.20nS           0.48uV            0.81uV            0.000V
0.40nS           -6.07uV           -1.89uV           12.38uV
0.60nS           -0.29mV           -5.66uV           -3.13mV
0.80nS           -3.39mV           26.90uV           -6.39mV
1.00nS           -4.34mV           -5.17uV           43.34mV
1.20nS           25.79mV           -0.87mV           0.11V
1.40nS           62.40mV           -3.65mV           0.15V
1.60nS           0.11V             -7.89mV           0.21V
1.80nS           0.16V             0.71mV            0.28V
2.00nS           0.22V             29.71mV           0.37V
2.20nS           0.28V             65.63mV           0.46V
2.40nS           0.37V             0.10V             0.59V
2.60nS           0.48V             0.15V             0.71V
2.80nS           0.63V             0.22V             0.92V
3.00nS           0.79V             0.28V             1.12V
3.20nS           0.90V             0.34V             1.28V
3.40nS           1.07V             0.43V             1.49V
3.60nS           1.24V             0.53V             1.70V
3.80nS           1.39V             0.63V             1.89V
4.00nS           1.55V             0.74V             2.07V
4.20nS           1.71V             0.86V             2.24V
4.40nS           1.84V             0.97V             2.37V
4.60nS           1.90V             1.03V             2.44V
4.80nS           1.96V             1.09V             2.50V
5.00nS           2.03V             1.16V             2.54V
5.20nS           2.08V             1.22V             2.59V
5.40nS           2.13V             1.29V             2.62V
5.60nS           2.18V             1.36V             2.65V
5.80nS           2.20V             1.39V             2.66V
6.00nS           2.22V             1.43V             2.67V

```

6.20nS	2.24V	1.47V	2.68V
6.40nS	2.26V	1.51V	2.69V
6.60nS	2.27V	1.54V	2.70V
6.80nS	2.29V	1.57V	2.71V
7.00nS	2.30V	1.60V	2.72V
7.20nS	2.31V	1.63V	2.72V
7.40nS	2.32V	1.66V	2.73V
7.60nS	2.33V	1.68V	2.74V
7.80nS	2.34V	1.69V	2.74V
8.00nS	2.34V	1.70V	2.74V
8.20nS	2.35V	1.72V	2.75V
8.40nS	2.35V	1.73V	2.75V
8.60nS	2.36V	1.74V	2.75V
8.80nS	2.36V	1.75V	2.76V
9.00nS	2.36V	1.76V	2.76V
9.20nS	2.37V	1.77V	2.76V
9.40nS	2.37V	1.78V	2.76V
9.60nS	2.38V	1.79V	2.77V
9.80nS	2.38V	1.80V	2.77V
10.00nS	2.38V	1.80V	2.77V

|
[Rising Waveform]

R_fixture = 50.00

V_fixture = 3.30

V_fixture_min = 3.00

V_fixture_max = 3.60

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.98V	1.34V	0.92V
0.20nS	0.98V	1.34V	0.92V
0.40nS	0.98V	1.34V	0.92V
0.60nS	0.98V	1.34V	0.92V
0.80nS	0.99V	1.34V	0.94V
1.00nS	1.05V	1.34V	1.07V
1.20nS	1.18V	1.34V	1.24V
1.40nS	1.31V	1.36V	1.37V
1.60nS	1.49V	1.44V	1.55V
1.80nS	1.69V	1.57V	1.76V
2.00nS	1.92V	1.73V	2.02V
2.20nS	2.18V	1.92V	2.33V
2.40nS	2.46V	2.11V	2.62V
2.60nS	2.73V	2.32V	2.91V

Appendix B IBIS Model

2.80nS	2.97V	2.55V	3.20V
3.00nS	3.09V	2.69V	3.33V
3.20nS	3.15V	2.76V	3.39V
3.40nS	3.20V	2.86V	3.44V
3.60nS	3.24V	2.92V	3.50V
3.80nS	3.26V	2.95V	3.53V
4.00nS	3.28V	2.98V	3.55V
4.20nS	3.29V	2.99V	3.57V
4.40nS	3.29V	2.99V	3.59V
4.60nS	3.30V	3.00V	3.59V
4.80nS	3.30V	3.00V	3.59V
5.00nS	3.30V	3.00V	3.60V
5.20nS	3.30V	3.00V	3.60V
5.40nS	3.30V	3.00V	3.60V
5.60nS	3.30V	3.00V	3.60V
5.80nS	3.30V	3.00V	3.60V
6.00nS	3.30V	3.00V	3.60V
6.20nS	3.30V	3.00V	3.60V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V
7.00nS	3.30V	3.00V	3.60V
7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V
8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V
9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

```
|  
[Falling Waveform]  
R_fixture = 50.00  
V_fixture = 0.000  
V_fixture_min = 0.000  
V_fixture_max = 0.000  
L_fixture = 0.000H
```

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	2.41V	1.87V	2.79V
0.20nS	2.41V	1.87V	2.79V
0.40nS	2.41V	1.87V	2.79V
0.60nS	2.41V	1.87V	2.76V
0.80nS	2.37V	1.87V	2.62V
1.00nS	2.24V	1.86V	2.44V
1.20nS	2.07V	1.85V	2.25V
1.40nS	1.94V	1.82V	2.10V
1.60nS	1.76V	1.75V	1.85V
1.80nS	1.54V	1.65V	1.55V
2.00nS	1.28V	1.51V	1.23V
2.20nS	1.01V	1.36V	0.96V
2.40nS	0.78V	1.18V	0.77V
2.60nS	0.61V	0.99V	0.63V
2.80nS	0.46V	0.76V	0.51V
3.00nS	0.37V	0.59V	0.43V
3.20nS	0.33V	0.49V	0.37V
3.40nS	0.26V	0.39V	0.32V
3.60nS	0.21V	0.31V	0.27V
3.80nS	0.17V	0.25V	0.22V
4.00nS	0.14V	0.19V	0.19V
4.20nS	0.10V	0.15V	0.14V
4.40nS	73.29mV	0.10V	0.11V
4.60nS	60.19mV	87.46mV	93.57mV
4.80nS	48.89mV	70.67mV	78.29mV
5.00nS	34.23mV	50.83mV	61.98mV
5.20nS	24.65mV	38.23mV	46.06mV
5.40nS	14.47mV	23.57mV	32.51mV
5.60nS	8.10mV	14.65mV	20.47mV
5.80nS	5.49mV	9.93mV	15.65mV
6.00nS	3.06mV	6.30mV	11.70mV
6.20nS	1.82mV	4.27mV	6.64mV
6.40nS	1.09mV	2.24mV	4.15mV
6.60nS	0.61mV	1.46mV	2.31mV
6.80nS	0.54mV	1.08mV	1.05mV
7.00nS	0.47mV	0.78mV	0.76mV
7.20nS	0.42mV	0.69mV	0.48mV
7.40nS	0.35mV	0.59mV	0.37mV
7.60nS	0.31mV	0.52mV	0.31mV
7.80nS	0.29mV	0.48mV	0.29mV
8.00nS	0.27mV	0.45mV	0.26mV

Appendix B IBIS Model

8.20nS	0.24mV	0.40mV	0.24mV
8.40nS	0.20mV	0.35mV	0.21mV
8.60nS	0.18mV	0.32mV	0.18mV
8.80nS	0.18mV	0.31mV	0.16mV
9.00nS	0.17mV	0.28mV	0.16mV
9.20nS	0.15mV	0.24mV	0.15mV
9.40nS	0.12mV	0.20mV	0.12mV
9.60nS	0.10mV	0.19mV	93.74uV
9.80nS	0.11mV	0.20mV	90.71uV
10.00nS	0.11mV	0.17mV	97.83uV

|
[Falling Waveform]

R_fixture = 50.00

V_fixture = 3.30

V_fixture_min = 3.00

V_fixture_max = 3.60

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	3.30V	3.00V	3.60V
0.20nS	3.30V	3.00V	3.60V
0.40nS	3.30V	3.00V	3.60V
0.60nS	3.30V	3.00V	3.59V
0.80nS	3.30V	3.00V	3.52V
1.00nS	3.25V	3.00V	3.43V
1.20nS	3.17V	3.00V	3.34V
1.40nS	3.12V	3.00V	3.27V
1.60nS	3.05V	3.00V	3.17V
1.80nS	2.97V	2.97V	3.06V
2.00nS	2.87V	2.92V	2.95V
2.20nS	2.78V	2.87V	2.83V
2.40nS	2.68V	2.82V	2.70V
2.60nS	2.58V	2.76V	2.58V
2.80nS	2.45V	2.69V	2.43V
3.00nS	2.34V	2.62V	2.30V
3.20nS	2.26V	2.57V	2.21V
3.40nS	2.17V	2.50V	2.07V
3.60nS	2.07V	2.44V	1.91V
3.80nS	1.98V	2.38V	1.76V
4.00nS	1.89V	2.32V	1.62V
4.20nS	1.76V	2.25V	1.49V
4.40nS	1.63V	2.18V	1.37V
4.60nS	1.55V	2.15V	1.32V

4.80nS	1.48V	2.11V	1.27V
5.00nS	1.40V	2.06V	1.21V
5.20nS	1.32V	2.01V	1.16V
5.40nS	1.25V	1.96V	1.10V
5.60nS	1.19V	1.92V	1.06V
5.80nS	1.15V	1.89V	1.04V
6.00nS	1.13V	1.87V	1.02V
6.20nS	1.10V	1.84V	1.00V
6.40nS	1.07V	1.81V	0.98V
6.60nS	1.05V	1.78V	0.96V
6.80nS	1.03V	1.75V	0.95V
7.00nS	1.02V	1.72V	0.94V
7.20nS	1.01V	1.70V	0.93V
7.40nS	1.00V	1.67V	0.93V
7.60nS	1.00V	1.64V	0.92V
7.80nS	1.00V	1.62V	0.92V
8.00nS	1.00V	1.60V	0.92V
8.20nS	0.99V	1.57V	0.92V
8.40nS	0.99V	1.53V	0.92V
8.60nS	0.99V	1.50V	0.92V
8.80nS	0.99V	1.47V	0.92V
9.00nS	0.99V	1.44V	0.92V
9.20nS	0.99V	1.42V	0.92V
9.40nS	0.99V	1.40V	0.92V
9.60nS	0.99V	1.38V	0.92V
9.80nS	0.99V	1.37V	0.92V
10.00nS	0.99V	1.36V	0.92V

|
| End [Model] prd16dgz
|

| *****

| Model prd24dgz

| *****

|
[Model] prd24dgz
Model_type I/O
Polarity Non-Inverting
Enable Active-Low
Vinl = 0.80V
Vinh = 2.00V
Vmeas = 1.50V
Cref = 50.00pF
Rref = 1.00M
Vref = 0.000V

Appendix B IBIS Model

C_comp	4.15pF	3.73pF	4.56pF
[Temperature Range]	25.00	0.12k	0.000
[Pullup Reference]	3.30V	3.00V	3.60V
[Pulldown Reference]	0.000V	0.000V	0.000V
[POWER Clamp Reference]	5.00V	4.50V	5.50V
[GND Clamp Reference]	0.000V	0.000V	0.000V
[Pulldown]			
voltage	I(typ)	I(min)	I(max)
-3.30	-10.00mA	0.000A	0.000A
-3.10	0.000A	0.000A	-10.00mA
-2.90	0.000A	0.000A	0.000A
-2.70	0.000A	0.000A	0.000A
-2.50	0.000A	0.000A	0.000A
-2.30	0.000A	0.000A	-10.00mA
-2.10	-10.00mA	0.000A	-10.00mA
-1.90	-10.00mA	0.000A	-10.00mA
-1.70	-10.00mA	-10.00mA	-10.00mA
-1.50	-10.00mA	-10.00mA	-20.00mA
-1.00	-19.00mA	-10.00mA	-23.00mA
-0.90	-21.00mA	-10.00mA	-26.00mA
-0.80	-41.70mA	-11.00mA	-55.33mA
-0.70	-50.61mA	-14.60mA	-55.12mA
-0.60	-46.07mA	-25.10mA	-50.21mA
-0.50	-39.45mA	-26.37mA	-43.90mA
-0.40	-32.03mA	-22.06mA	-36.08mA
-0.30	-24.29mA	-16.63mA	-27.48mA
-0.20	-16.36mA	-11.11mA	-18.57mA
-0.10	-8.26mA	-5.55mA	-9.40mA
-0.00	3.80nA	7.33nA	12.06nA
0.10	8.11mA	5.36mA	9.30mA
0.20	15.76mA	10.37mA	18.18mA
0.30	22.98mA	15.05mA	26.64mA
0.40	29.76mA	19.40mA	34.69mA
0.50	36.11mA	23.42mA	42.32mA
0.60	42.04mA	27.12mA	49.54mA
0.70	47.55mA	30.50mA	56.36mA
0.80	52.66mA	33.58mA	62.78mA
0.90	57.35mA	36.36mA	68.80mA
1.00	61.65mA	38.84mA	74.42mA
1.10	65.55mA	41.04mA	79.65mA
1.20	69.06mA	42.96mA	84.48mA

1.30	72.19mA	44.61mA	88.92mA
1.40	74.94mA	45.99mA	92.97mA
1.50	77.32mA	47.12mA	96.63mA
1.60	79.33mA	48.01mA	99.91mA
1.70	80.95mA	48.68mA	0.10A
1.80	82.19mA	49.17mA	0.11A
1.90	83.09mA	49.54mA	0.11A
2.00	83.74mA	49.83mA	0.11A
2.10	84.23mA	50.06mA	0.11A
2.20	84.62mA	50.25mA	0.11A
2.30	84.93mA	50.42mA	0.11A
2.40	85.20mA	50.57mA	0.11A
2.50	85.44mA	50.70mA	0.11A
2.60	85.65mA	50.82mA	0.11A
2.70	85.84mA	50.93mA	0.11A
2.80	86.01mA	51.03mA	0.11A
2.90	86.18mA	51.13mA	0.11A
3.00	86.33mA	51.22mA	0.11A
3.10	86.48mA	51.31mA	0.11A
3.20	86.62mA	51.40mA	0.11A
3.30	86.75mA	51.50mA	0.11A
3.40	86.89mA	51.73mA	0.12A
3.50	87.06mA	52.32mA	0.12A
3.60	87.16mA	53.14mA	0.12A
3.70	87.30mA	54.02mA	0.12A
3.80	87.47mA	54.48mA	0.12A
3.90	87.77mA	52.16mA	0.12A
4.00	88.66mA	52.28mA	0.12A
4.10	90.00mA	52.42mA	0.12A
4.20	91.34mA	52.58mA	0.12A
4.30	89.39mA	52.77mA	0.12A
4.50	89.66mA	53.24mA	0.12A
4.70	90.64mA	53.86mA	0.12A
4.90	91.94mA	54.68mA	0.12A
5.10	93.66mA	55.73mA	0.12A
5.30	95.77mA	57.03mA	0.13A
5.50	98.33mA	58.59mA	0.13A
5.70	0.10A	60.44mA	0.13A
5.90	0.10A	62.55mA	0.14A
6.10	0.11A	64.93mA	0.14A
6.60	0.12A	71.83mA	0.15A
[Pullup]			
voltage	I(typ)	I(min)	I(max)

Appendix B IBIS Model

-3.30	0.22A	0.16A	0.25A
-3.10	0.21A	0.16A	0.24A
-2.90	0.20A	0.15A	0.23A
-2.70	0.19A	0.14A	0.22A
-2.50	0.18A	0.14A	0.21A
-2.30	0.17A	0.13A	0.20A
-2.10	0.16A	0.12A	0.19A
-1.90	0.15A	0.11A	0.17A
-1.70	0.14A	0.10A	0.16A
-1.50	0.12A	90.15mA	0.14A
-1.00	92.80mA	62.50mA	0.11A
-0.90	84.30mA	57.02mA	97.94mA
-0.80	75.06mA	54.41mA	87.24mA
-0.70	65.63mA	47.70mA	76.50mA
-0.60	56.31mA	40.65mA	66.14mA
-0.50	47.22mA	33.53mA	55.68mA
-0.40	38.00mA	26.51mA	44.96mA
-0.30	28.62mA	19.71mA	34.00mA
-0.20	19.12mA	13.04mA	22.83mA
-0.10	9.57mA	6.46mA	11.50mA
0.00	34.08uA	11.19uA	71.92uA
0.10	-9.20mA	-6.16mA	-11.08mA
0.20	-17.92mA	-11.98mA	-21.68mA
0.30	-26.12mA	-17.45mA	-31.71mA
0.40	-33.83mA	-22.56mA	-41.21mA
0.50	-41.04mA	-27.33mA	-50.17mA
0.60	-47.76mA	-31.76mA	-58.60mA
0.70	-54.01mA	-35.85mA	-66.51mA
0.80	-59.78mA	-39.61mA	-73.91mA
0.90	-65.10mA	-43.04mA	-80.81mA
1.00	-69.96mA	-46.14mA	-87.22mA
1.10	-74.37mA	-48.91mA	-93.14mA
1.20	-78.35mA	-51.37mA	-98.58mA
1.30	-81.89mA	-53.51mA	-0.10A
1.40	-85.01mA	-55.34mA	-0.11A
1.50	-87.72mA	-56.87mA	-0.11A
1.60	-90.01mA	-58.11mA	-0.12A
1.70	-91.93mA	-59.08mA	-0.12A
1.80	-93.48mA	-59.83mA	-0.12A
1.90	-94.74mA	-60.42mA	-0.12A
2.00	-95.77mA	-60.91mA	-0.13A
2.10	-96.63mA	-61.34mA	-0.13A
2.20	-97.36mA	-61.71mA	-0.13A

2.30	-97.99mA	-62.05mA	-0.13A
2.40	-98.55mA	-62.36mA	-0.13A
2.50	-99.04mA	-62.64mA	-0.13A
2.60	-99.49mA	-62.90mA	-0.13A
2.70	-99.89mA	-63.14mA	-0.13A
2.80	-0.10A	-63.36mA	-0.13A
2.90	-0.10A	-63.57mA	-0.13A
3.00	-0.10A	-63.78mA	-0.13A
3.10	-0.10A	-63.97mA	-0.14A
3.20	-0.10A	-64.15mA	-0.14A
3.30	-0.10A	-64.35mA	-0.14A
3.40	-0.10A	-64.99mA	-0.14A
3.50	-0.10A	-72.69mA	-0.14A
3.60	-0.10A	-0.17A	-0.14A
3.70	-0.10A	-0.97A	-0.14A
3.80	-0.10A	-2.72A	-0.14A
3.90	-0.11A	-4.50A	-0.14A
4.00	-0.12A	-6.28A	-0.14A
4.10	-0.34A	-8.06A	-0.14A
4.20	-1.90A	-9.85A	-0.14A
4.30	-3.94A	-11.62A	-0.15A
4.50	-8.02A	-15.19A	-1.21A
4.70	-12.10A	-18.75A	-5.43A
4.90	-16.18A	-22.31A	-9.67A
5.10	-20.27A	-25.88A	-13.90A
5.30	-24.35A	-29.44A	-18.14A
5.50	-28.43A	-33.00A	-22.38A
5.70	-32.51A	-36.56A	-26.62A
5.90	-36.60A	-40.13A	-30.86A
6.10	-40.68A	-43.69A	-35.09A
6.60	-50.89A	-52.59A	-45.69A

[GND_clamp]			
voltage	I(typ)	I(min)	I(max)
-5.00	-85.26A	-77.43A	-87.91A
-4.80	-81.20A	-73.87A	-83.67A
-4.60	-77.14A	-70.31A	-79.43A
-4.40	-73.08A	-66.75A	-75.19A
-4.20	-69.02A	-63.19A	-70.95A
-4.00	-64.96A	-59.63A	-66.71A
-3.80	-60.90A	-56.07A	-62.47A
-3.60	-56.84A	-52.51A	-58.23A
-3.40	-52.78A	-48.95A	-53.99A

Appendix B IBIS Model

-3.20	-48.72A	-45.39A	-49.75A
-3.00	-44.64A	-41.83A	-45.52A
-2.80	-40.56A	-38.27A	-41.29A
-2.60	-36.48A	-34.71A	-37.05A
-2.40	-32.40A	-31.15A	-32.82A
-2.20	-28.32A	-27.59A	-28.58A
-2.00	-24.24A	-24.03A	-24.35A
-1.80	-20.16A	-20.47A	-20.11A
-1.60	-16.08A	-16.90A	-15.88A
-1.40	-12.00A	-13.34A	-11.64A
-1.20	-7.92A	-9.78A	-7.41A
-1.00	-3.84A	-6.22A	-3.18A
-0.80	-0.23A	-2.66A	-71.67mA
-0.60	-2.33mA	-0.10A	-6.23mA
-0.40	-91.55uA	-0.52mA	-0.28mA
-0.20	-27.91uA	-14.70uA	-42.94uA
-0.00	-75.80nA	-77.03nA	-90.19nA
0.20	18.72uA	7.32uA	32.29uA
0.40	29.20uA	10.26uA	54.13uA
0.60	32.50uA	10.68uA	65.79uA
0.80	33.08uA	10.79uA	69.34uA
1.00	33.30uA	10.86uA	70.18uA
1.20	33.45uA	10.92uA	70.55uA
1.40	33.57uA	10.98uA	70.80uA
1.60	33.68uA	11.03uA	71.00uA
1.80	33.78uA	11.07uA	71.16uA
2.00	33.87uA	11.11uA	71.32uA
2.20	33.96uA	11.14uA	71.47uA
2.40	34.01uA	11.15uA	71.61uA
2.60	34.03uA	11.16uA	71.76uA
2.80	34.04uA	11.17uA	71.84uA
3.00	34.05uA	11.18uA	71.86uA
3.20	34.06uA	11.75uA	71.88uA
3.40	34.08uA	10.69uA	71.90uA
3.60	34.10uA	9.63uA	71.92uA
3.80	34.12uA	8.57uA	71.94uA
4.00	34.14uA	7.51uA	71.96uA
4.20	34.16uA	6.45uA	71.98uA
4.40	34.18uA	5.39uA	72.00uA
4.60	34.20uA	4.33uA	72.02uA
4.80	34.22uA	3.27uA	72.04uA
5.00	34.24uA	2.21uA	72.06uA

|
[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	48.55uA	16.31uA	95.55uA
-4.90	48.22uA	16.19uA	95.05uA
-4.80	47.89uA	16.07uA	94.55uA
-4.70	47.56uA	15.95uA	94.05uA
-4.60	47.23uA	15.83uA	93.55uA
-4.50	46.90uA	15.71uA	93.05uA
-4.40	46.57uA	15.59uA	92.55uA
-4.30	46.24uA	15.47uA	92.05uA
-4.20	45.91uA	15.35uA	91.55uA
-4.10	45.58uA	15.23uA	91.05uA
-4.00	45.25uA	15.11uA	90.55uA
-3.90	44.92uA	14.99uA	90.05uA
-3.80	44.59uA	14.87uA	89.55uA
-3.70	44.26uA	14.75uA	89.05uA
-3.60	43.93uA	14.63uA	88.55uA
-3.50	43.60uA	14.51uA	88.05uA
-3.40	43.27uA	14.39uA	87.55uA
-3.30	42.94uA	14.27uA	87.05uA
-3.20	42.61uA	14.15uA	86.55uA
-3.10	42.28uA	14.03uA	86.05uA
-3.00	41.95uA	13.91uA	85.55uA
-2.90	41.62uA	13.79uA	85.05uA
-2.80	41.29uA	13.67uA	84.55uA
-2.70	40.96uA	13.55uA	84.05uA
-2.60	40.63uA	13.43uA	83.55uA
-2.50	40.30uA	13.31uA	83.05uA
-2.40	39.97uA	13.19uA	82.55uA
-2.30	39.64uA	13.07uA	82.05uA
-2.20	39.31uA	12.95uA	81.55uA
-2.10	38.98uA	12.83uA	81.05uA
-2.00	38.65uA	12.71uA	80.55uA
-1.90	38.32uA	12.59uA	80.05uA
-1.80	37.99uA	12.47uA	79.55uA
-1.70	37.66uA	12.35uA	79.05uA
-1.60	37.33uA	12.23uA	78.55uA
-1.50	37.00uA	12.13uA	78.05uA
-1.40	36.69uA	12.03uA	77.55uA
-1.30	36.40uA	11.94uA	77.05uA
-1.20	36.13uA	11.85uA	76.55uA
-1.10	35.88uA	11.78uA	76.05uA
-1.00	35.64uA	11.71uA	75.55uA
-0.90	35.43uA	11.64uA	75.08uA

Appendix B IBIS Model

-0.80	35.24uA	11.59uA	74.65uA
-0.70	35.07uA	11.54uA	74.26uA
-0.60	34.92uA	11.49uA	73.91uA
-0.50	34.79uA	11.45uA	73.60uA
-0.40	34.67uA	11.42uA	73.32uA
-0.30	34.57uA	11.39uA	73.08uA
-0.20	34.49uA	11.37uA	72.88uA
-0.10	34.42uA	11.35uA	72.70uA
0.00	34.36uA	11.33uA	72.56uA

|

[Ramp]

variable	typ	min	max
dV/dt_r	1.54/2.22n	1.20/2.88n	1.77/2.15n
dV/dt_f	1.52/3.16n	1.15/4.46n	1.73/3.00n

R_load = 50.00

|

[Rising Waveform]

R_fixture = 50.00

V_fixture = 0.000

V_fixture_min = 0.000

V_fixture_max = 0.000

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.70uV	0.92uV	0.68uV
0.20nS	0.45uV	0.77uV	0.000V
0.40nS	-5.49uV	-1.76uV	16.07uV
0.60nS	-0.25mV	-4.97uV	-2.66mV
0.80nS	-2.88mV	24.27uV	-5.55mV
1.00nS	-3.85mV	-5.54uV	32.40mV
1.20nS	18.80mV	-0.76mV	80.52mV
1.40nS	45.63mV	-3.09mV	0.11V
1.60nS	80.05mV	-6.58mV	0.16V
1.80nS	0.11V	-0.18mV	0.21V
2.00nS	0.16V	21.52mV	0.27V
2.20nS	0.20V	48.21mV	0.33V
2.40nS	0.26V	76.15mV	0.41V
2.60nS	0.32V	0.11V	0.48V
2.80nS	0.41V	0.16V	0.61V
3.00nS	0.51V	0.19V	0.73V
3.20nS	0.58V	0.24V	0.82V
3.40nS	0.71V	0.30V	0.97V
3.60nS	0.85V	0.36V	1.16V

3.80nS	1.00V	0.45V	1.35V
4.00nS	1.17V	0.54V	1.55V
4.20nS	1.38V	0.67V	1.80V
4.40nS	1.57V	0.80V	2.03V
4.60nS	1.68V	0.88V	2.15V
4.80nS	1.78V	0.96V	2.26V
5.00nS	1.91V	1.06V	2.39V
5.20nS	2.01V	1.15V	2.51V
5.40nS	2.13V	1.25V	2.61V
5.60nS	2.22V	1.34V	2.70V
5.80nS	2.27V	1.40V	2.74V
6.00nS	2.31V	1.44V	2.77V
6.20nS	2.35V	1.50V	2.80V
6.40nS	2.38V	1.56V	2.82V
6.60nS	2.41V	1.61V	2.84V
6.80nS	2.43V	1.66V	2.86V
7.00nS	2.45V	1.70V	2.87V
7.20nS	2.46V	1.74V	2.88V
7.40nS	2.48V	1.78V	2.89V
7.60nS	2.49V	1.82V	2.90V
7.80nS	2.50V	1.84V	2.91V
8.00nS	2.51V	1.86V	2.91V
8.20nS	2.52V	1.88V	2.92V
8.40nS	2.52V	1.90V	2.92V
8.60nS	2.53V	1.92V	2.92V
8.80nS	2.54V	1.93V	2.93V
9.00nS	2.54V	1.95V	2.93V
9.20nS	2.55V	1.96V	2.94V
9.40nS	2.55V	1.97V	2.94V
9.60nS	2.56V	1.98V	2.94V
9.80nS	2.56V	2.00V	2.95V
10.00nS	2.57V	2.00V	2.95V

```

|
[Rising Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F
| time          V(typ)          V(min)          V(max)
|
0.000S          0.76V          1.03V          0.72V
0.20nS          0.76V          1.03V          0.72V

```

Appendix B IBIS Model

0.40nS	0.76V	1.03V	0.72V
0.60nS	0.76V	1.03V	0.72V
0.80nS	0.77V	1.03V	0.73V
1.00nS	0.81V	1.03V	0.82V
1.20nS	0.90V	1.03V	0.93V
1.40nS	0.98V	1.04V	1.01V
1.60nS	1.09V	1.11V	1.13V
1.80nS	1.22V	1.20V	1.26V
2.00nS	1.35V	1.32V	1.42V
2.20nS	1.51V	1.45V	1.58V
2.40nS	1.69V	1.59V	1.78V
2.60nS	1.91V	1.74V	2.02V
2.80nS	2.22V	1.96V	2.36V
3.00nS	2.47V	2.16V	2.63V
3.20nS	2.65V	2.31V	2.82V
3.40nS	2.85V	2.49V	3.03V
3.60nS	2.97V	2.62V	3.17V
3.80nS	3.08V	2.73V	3.30V
4.00nS	3.14V	2.83V	3.36V
4.20nS	3.19V	2.89V	3.42V
4.40nS	3.23V	2.94V	3.47V
4.60nS	3.25V	2.95V	3.50V
4.80nS	3.27V	2.97V	3.52V
5.00nS	3.28V	2.98V	3.54V
5.20nS	3.29V	2.99V	3.56V
5.40nS	3.29V	2.99V	3.57V
5.60nS	3.30V	3.00V	3.58V
5.80nS	3.30V	3.00V	3.59V
6.00nS	3.30V	3.00V	3.59V
6.20nS	3.30V	3.00V	3.59V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V
7.00nS	3.30V	3.00V	3.60V
7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V
8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V

9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

|
[Falling Waveform]

R_fixture = 50.00

V_fixture = 0.000

V_fixture_min = 0.000

V_fixture_max = 0.000

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	2.62V	2.12V	2.99V
0.20nS	2.62V	2.12V	2.99V
0.40nS	2.62V	2.12V	2.99V
0.60nS	2.62V	2.12V	2.96V
0.80nS	2.60V	2.12V	2.85V
1.00nS	2.50V	2.12V	2.72V
1.20nS	2.38V	2.11V	2.59V
1.40nS	2.29V	2.09V	2.50V
1.60nS	2.17V	2.04V	2.36V
1.80nS	2.04V	1.96V	2.20V
2.00nS	1.89V	1.85V	2.00V
2.20nS	1.71V	1.74V	1.76V
2.40nS	1.51V	1.63V	1.49V
2.60nS	1.27V	1.50V	1.23V
2.80nS	0.99V	1.33V	0.98V
3.00nS	0.81V	1.17V	0.83V
3.20nS	0.71V	1.04V	0.75V
3.40nS	0.59V	0.87V	0.66V
3.60nS	0.51V	0.72V	0.57V
3.80nS	0.44V	0.59V	0.50V
4.00nS	0.37V	0.49V	0.45V
4.20nS	0.31V	0.40V	0.38V
4.40nS	0.26V	0.33V	0.32V
4.60nS	0.23V	0.28V	0.29V
4.80nS	0.20V	0.25V	0.26V
5.00nS	0.17V	0.21V	0.23V
5.20nS	0.15V	0.18V	0.20V
5.40nS	0.12V	0.14V	0.17V
5.60nS	92.71mV	0.11V	0.14V

Appendix B IBIS Model

5.80nS	79.46mV	96.17mV	0.12V
6.00nS	67.17mV	83.01mV	0.11V
6.20nS	54.74mV	65.86mV	89.82mV
6.40nS	42.77mV	53.06mV	75.55mV
6.60nS	33.26mV	41.31mV	61.63mV
6.80nS	25.46mV	31.29mV	50.25mV
7.00nS	18.21mV	23.99mV	40.51mV
7.20nS	13.43mV	16.92mV	31.37mV
7.40nS	8.06mV	11.32mV	23.11mV
7.60nS	4.81mV	6.46mV	15.54mV
7.80nS	3.27mV	4.82mV	12.49mV
8.00nS	1.98mV	3.62mV	9.63mV
8.20nS	1.32mV	2.10mV	6.17mV
8.40nS	0.78mV	1.45mV	4.24mV
8.60nS	0.50mV	1.01mV	2.46mV
8.80nS	0.42mV	0.70mV	1.45mV
9.00nS	0.34mV	0.61mV	0.94mV
9.20nS	0.30mV	0.51mV	0.50mV
9.40nS	0.27mV	0.45mV	0.38mV
9.60nS	0.24mV	0.40mV	0.28mV
9.80nS	0.21mV	0.35mV	0.23mV
10.00nS	0.22mV	0.32mV	0.21mV

|
[Falling Waveform]

R_fixture = 50.00

V_fixture = 3.30

V_fixture_min = 3.00

V_fixture_max = 3.60

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	3.30V	3.00V	3.60V
0.20nS	3.30V	3.00V	3.60V
0.40nS	3.30V	3.00V	3.60V
0.60nS	3.30V	3.00V	3.59V
0.80nS	3.30V	3.00V	3.52V
1.00nS	3.25V	3.00V	3.44V
1.20nS	3.18V	3.00V	3.37V
1.40nS	3.14V	3.00V	3.32V
1.60nS	3.09V	3.00V	3.24V
1.80nS	3.03V	2.97V	3.16V
2.00nS	2.96V	2.92V	3.07V
2.20nS	2.88V	2.88V	2.98V

2.40nS	2.80V	2.84V	2.88V
2.60nS	2.72V	2.80V	2.78V
2.80nS	2.61V	2.74V	2.65V
3.00nS	2.51V	2.68V	2.55V
3.20nS	2.44V	2.64V	2.47V
3.40nS	2.34V	2.58V	2.35V
3.60nS	2.25V	2.52V	2.23V
3.80nS	2.15V	2.46V	2.09V
4.00nS	2.06V	2.39V	1.93V
4.20nS	1.93V	2.32V	1.75V
4.40nS	1.81V	2.24V	1.58V
4.60nS	1.73V	2.20V	1.50V
4.80nS	1.65V	2.15V	1.43V
5.00nS	1.54V	2.09V	1.34V
5.20nS	1.44V	2.04V	1.26V
5.40nS	1.32V	1.97V	1.18V
5.60nS	1.23V	1.91V	1.11V
5.80nS	1.18V	1.87V	1.07V
6.00nS	1.13V	1.84V	1.04V
6.20nS	1.08V	1.79V	1.00V
6.40nS	1.04V	1.75V	0.96V
6.60nS	1.00V	1.71V	0.92V
6.80nS	0.96V	1.67V	0.89V
7.00nS	0.93V	1.63V	0.87V
7.20nS	0.90V	1.59V	0.84V
7.40nS	0.87V	1.54V	0.82V
7.60nS	0.85V	1.48V	0.80V
7.80nS	0.83V	1.44V	0.78V
8.00nS	0.82V	1.40V	0.78V
8.20nS	0.81V	1.35V	0.76V
8.40nS	0.80V	1.31V	0.75V
8.60nS	0.79V	1.27V	0.75V
8.80nS	0.78V	1.23V	0.74V
9.00nS	0.78V	1.20V	0.73V
9.20nS	0.78V	1.17V	0.73V
9.40nS	0.77V	1.15V	0.73V
9.60nS	0.77V	1.12V	0.72V
9.80nS	0.77V	1.10V	0.72V
10.00nS	0.77V	1.09V	0.72V

|
| End [Model] prd24dgz
|

|*****

| Model prt24dgz

Appendix B IBIS Model

```

| *****
|
[Model]          prt24dgz
Model_type      3-state
Polarity        Non-Inverting
Enable          Active-Low
Vmeas =        1.50V
Cref =          50.00pF
Rref =          1.00M
Vref =          0.000V
C_comp          4.09pF          3.68pF          4.50pF
|
|
[Temperature Range]      25.00          0.12k          0.000
[Pullup Reference]      3.30V          3.00V          3.60V
[Pulldown Reference]    0.000V          0.000V          0.000V
[POWER Clamp Reference] 5.00V          4.50V          5.50V
[GND Clamp Reference]   0.000V          0.000V          0.000V
[Pulldown]
| voltage      I(typ)          I(min)          I(max)
|
-3.30      -10.00mA          0.000A          0.000A
-3.10      0.000A          0.000A          -10.00mA
-2.90      0.000A          0.000A          0.000A
-2.70      0.000A          0.000A          0.000A
-2.50      0.000A          0.000A          0.000A
-2.30      0.000A          0.000A          -10.00mA
-2.10      -10.00mA          0.000A          -10.00mA
-1.90      -10.00mA          0.000A          -10.00mA
-1.70      -10.00mA          -10.00mA          -10.00mA
-1.50      -10.00mA          -10.00mA          -20.00mA
-1.00      -20.00mA          -10.00mA          -23.00mA
-0.90      -21.00mA          -10.00mA          -26.00mA
-0.80      -41.70mA          -12.00mA          -55.37mA
-0.70      -50.60mA          -14.60mA          -55.11mA
-0.60      -46.07mA          -25.10mA          -50.21mA
-0.50      -39.45mA          -26.38mA          -43.90mA
-0.40      -32.03mA          -22.06mA          -36.09mA
-0.30      -24.30mA          -16.63mA          -27.49mA
-0.20      -16.36mA          -11.10mA          -18.57mA
-0.10      -8.26mA          -5.55mA          -9.40mA
-0.00      3.97nA          7.41nA          12.45nA
0.10      8.11mA          5.36mA          9.30mA
0.20      15.76mA          10.38mA          18.18mA

```

0.30	22.98mA	15.05mA	26.64mA
0.40	29.76mA	19.40mA	34.68mA
0.50	36.11mA	23.42mA	42.32mA
0.60	42.04mA	27.11mA	49.54mA
0.70	47.55mA	30.50mA	56.36mA
0.80	52.65mA	33.58mA	62.78mA
0.90	57.35mA	36.36mA	68.80mA
1.00	61.64mA	38.84mA	74.42mA
1.10	65.54mA	41.04mA	79.65mA
1.20	69.06mA	42.96mA	84.48mA
1.30	72.18mA	44.61mA	88.92mA
1.40	74.93mA	45.99mA	92.97mA
1.50	77.31mA	47.12mA	96.63mA
1.60	79.32mA	48.01mA	99.91mA
1.70	80.95mA	48.68mA	0.10A
1.80	82.19mA	49.17mA	0.11A
1.90	83.08mA	49.54mA	0.11A
2.00	83.74mA	49.82mA	0.11A
2.10	84.23mA	50.06mA	0.11A
2.20	84.61mA	50.25mA	0.11A
2.30	84.93mA	50.42mA	0.11A
2.40	85.20mA	50.57mA	0.11A
2.50	85.43mA	50.70mA	0.11A
2.60	85.64mA	50.82mA	0.11A
2.70	85.83mA	50.93mA	0.11A
2.80	86.01mA	51.03mA	0.11A
2.90	86.17mA	51.13mA	0.11A
3.00	86.32mA	51.22mA	0.11A
3.10	86.47mA	51.31mA	0.11A
3.20	86.61mA	51.40mA	0.11A
3.30	86.75mA	51.50mA	0.11A
3.40	86.88mA	51.73mA	0.12A
3.50	87.01mA	52.32mA	0.12A
3.60	87.15mA	53.14mA	0.12A
3.70	87.30mA	54.01mA	0.12A
3.80	87.47mA	54.42mA	0.12A
3.90	87.77mA	52.16mA	0.12A
4.00	88.66mA	52.28mA	0.12A
4.10	90.00mA	52.42mA	0.12A
4.20	91.29mA	52.58mA	0.12A
4.30	89.03mA	52.77mA	0.12A
4.50	89.65mA	53.24mA	0.12A
4.70	90.63mA	53.86mA	0.12A
4.90	91.94mA	54.68mA	0.12A

Appendix B IBIS Model

5.10	93.62mA	55.72mA	0.12A
5.30	95.73mA	57.02mA	0.13A
5.50	98.29mA	58.58mA	0.13A
5.70	0.10A	60.42mA	0.13A
5.90	0.10A	62.54mA	0.14A
6.10	0.11A	64.92mA	0.14A
6.60	0.12A	71.81mA	0.15A

[Pullup]

voltage	I (typ)	I (min)	I (max)
-3.30	0.22A	0.16A	0.25A
-3.10	0.21A	0.16A	0.24A
-2.90	0.20A	0.15A	0.23A
-2.70	0.19A	0.14A	0.22A
-2.50	0.18A	0.14A	0.21A
-2.30	0.17A	0.13A	0.20A
-2.10	0.16A	0.12A	0.18A
-1.90	0.15A	0.11A	0.17A
-1.70	0.14A	0.10A	0.16A
-1.50	0.12A	90.13mA	0.14A
-1.00	92.59mA	62.48mA	0.11A
-0.90	84.26mA	56.95mA	97.88mA
-0.80	75.03mA	54.36mA	87.19mA
-0.70	65.60mA	47.69mA	76.45mA
-0.60	56.28mA	40.63mA	66.08mA
-0.50	47.19mA	33.52mA	55.62mA
-0.40	37.96mA	26.49mA	44.89mA
-0.30	28.58mA	19.70mA	33.93mA
-0.20	19.09mA	13.03mA	22.76mA
-0.10	9.54mA	6.45mA	11.43mA
0.00	0.17uA	0.16uA	0.19uA
0.10	-9.23mA	-6.17mA	-11.15mA
0.20	-17.95mA	-11.99mA	-21.75mA
0.30	-26.16mA	-17.46mA	-31.79mA
0.40	-33.86mA	-22.57mA	-41.28mA
0.50	-41.07mA	-27.35mA	-50.24mA
0.60	-47.79mA	-31.77mA	-58.67mA
0.70	-54.04mA	-35.86mA	-66.58mA
0.80	-59.82mA	-39.62mA	-73.98mA
0.90	-65.13mA	-43.05mA	-80.88mA
1.00	-69.99mA	-46.15mA	-87.29mA
1.10	-74.41mA	-48.92mA	-93.21mA
1.20	-78.38mA	-51.38mA	-98.65mA

1.30	-81.93mA	-53.52mA	-0.10A
1.40	-85.05mA	-55.36mA	-0.11A
1.50	-87.75mA	-56.88mA	-0.11A
1.60	-90.05mA	-58.12mA	-0.12A
1.70	-91.96mA	-59.09mA	-0.12A
1.80	-93.52mA	-59.84mA	-0.12A
1.90	-94.78mA	-60.43mA	-0.12A
2.00	-95.80mA	-60.92mA	-0.13A
2.10	-96.66mA	-61.35mA	-0.13A
2.20	-97.39mA	-61.72mA	-0.13A
2.30	-98.03mA	-62.06mA	-0.13A
2.40	-98.58mA	-62.37mA	-0.13A
2.50	-99.08mA	-62.65mA	-0.13A
2.60	-99.52mA	-62.91mA	-0.13A
2.70	-99.92mA	-63.15mA	-0.13A
2.80	-0.10A	-63.37mA	-0.13A
2.90	-0.10A	-63.58mA	-0.13A
3.00	-0.10A	-63.78mA	-0.13A
3.10	-0.10A	-63.96mA	-0.14A
3.20	-0.10A	-64.14mA	-0.14A
3.30	-0.10A	-64.33mA	-0.14A
3.40	-0.10A	-64.95mA	-0.14A
3.50	-0.10A	-72.61mA	-0.14A
3.60	-0.10A	-0.17A	-0.14A
3.70	-0.10A	-0.97A	-0.14A
3.80	-0.10A	-2.72A	-0.14A
3.90	-0.11A	-4.50A	-0.14A
4.00	-0.12A	-6.28A	-0.14A
4.10	-0.34A	-8.06A	-0.14A
4.20	-1.90A	-9.85A	-0.14A
4.30	-3.94A	-11.62A	-0.15A
4.50	-8.02A	-15.19A	-1.20A
4.70	-12.10A	-18.75A	-5.43A
4.90	-16.18A	-22.31A	-9.67A
5.10	-20.27A	-25.88A	-13.90A
5.30	-24.35A	-29.44A	-18.14A
5.50	-28.43A	-33.00A	-22.38A
5.70	-32.51A	-36.56A	-26.62A
5.90	-36.60A	-40.13A	-30.86A
6.10	-40.68A	-43.69A	-35.09A
6.60	-50.89A	-52.59A	-45.69A

|
[GND_clamp]
| voltage I(typ) I(min) I(max)

Appendix B IBIS Model

-3.30	-50.75A	-47.17A	-51.87A
-3.20	-48.72A	-45.39A	-49.75A
-3.10	-46.68A	-43.61A	-47.63A
-3.00	-44.64A	-41.83A	-45.52A
-2.90	-42.60A	-40.05A	-43.40A
-2.80	-40.56A	-38.27A	-41.29A
-2.70	-38.52A	-36.49A	-39.17A
-2.60	-36.48A	-34.71A	-37.05A
-2.50	-34.44A	-32.93A	-34.94A
-2.40	-32.40A	-31.15A	-32.82A
-2.30	-30.36A	-29.37A	-30.70A
-2.20	-28.32A	-27.59A	-28.58A
-2.10	-26.28A	-25.81A	-26.47A
-2.00	-24.24A	-24.03A	-24.35A
-1.90	-22.20A	-22.25A	-22.23A
-1.80	-20.16A	-20.47A	-20.11A
-1.70	-18.12A	-18.68A	-18.00A
-1.60	-16.08A	-16.90A	-15.88A
-1.50	-14.04A	-15.12A	-13.76A
-1.40	-12.00A	-13.34A	-11.64A
-1.30	-9.96A	-11.56A	-9.53A
-1.20	-7.92A	-9.78A	-7.41A
-1.10	-5.88A	-8.00A	-5.29A
-1.00	-3.84A	-6.22A	-3.18A
-0.90	-1.80A	-4.44A	-1.07A
-0.80	-0.23A	-2.65A	-71.53mA
-0.70	-13.26mA	-0.90A	-13.93mA
-0.60	-2.23mA	-0.10A	-6.08mA
-0.50	-0.34mA	-7.99mA	-1.62mA
-0.40	-28.68uA	-0.48mA	-0.18mA
-0.30	-1.65uA	-27.22uA	-10.18uA
-0.20	-0.15uA	-1.61uA	-0.42uA
-0.10	-86.50nA	-0.17uA	-0.11uA
-0.00	-76.61nA	-77.36nA	-91.73nA
0.10	-68.52nA	-64.82nA	-83.30nA
0.20	-60.47nA	-56.49nA	-75.01nA
0.30	-52.43nA	-48.39nA	-66.73nA
0.40	-44.39nA	-40.30nA	-58.46nA
0.50	-36.35nA	-32.21nA	-50.19nA
0.60	-28.31nA	-24.12nA	-41.93nA
0.70	-20.27nA	-16.03nA	-33.68nA
0.80	-12.24nA	-7.94nA	-25.42nA
0.90	-4.20nA	0.15nA	-17.17nA

1.00	3.83nA	8.23nA	-8.92nA
1.10	11.86nA	16.32nA	-0.67nA
1.20	19.89nA	24.41nA	7.58nA
1.30	27.92nA	32.50nA	15.84nA
1.40	35.95nA	40.59nA	24.10nA
1.50	43.98nA	48.68nA	32.36nA
1.60	52.00nA	56.77nA	40.64nA
1.70	60.02nA	64.85nA	48.92nA
1.80	68.04nA	72.94nA	57.21nA
1.90	76.05nA	81.03nA	65.52nA
2.00	84.05nA	89.12nA	73.85nA
2.10	92.04nA	97.20nA	82.20nA
2.20	100.00nA	0.11uA	90.59nA
2.30	0.11uA	0.11uA	99.01nA
2.40	0.12uA	0.12uA	0.11uA
2.50	0.12uA	0.12uA	0.12uA
2.60	0.13uA	0.13uA	0.12uA
2.70	0.13uA	0.13uA	0.13uA
2.80	0.14uA	0.13uA	0.14uA
2.90	0.14uA	0.14uA	0.15uA
3.00	0.15uA	0.15uA	0.15uA
3.10	0.15uA	0.17uA	0.16uA
3.20	0.15uA	0.56uA	0.16uA
3.30	0.16uA	0.19uA	0.17uA

|
[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-3.30	0.37uA	0.37uA	0.40uA
-3.20	0.37uA	0.36uA	0.39uA
-3.10	0.36uA	0.36uA	0.39uA
-3.00	0.35uA	0.35uA	0.38uA
-2.90	0.35uA	0.34uA	0.37uA
-2.80	0.34uA	0.34uA	0.37uA
-2.70	0.33uA	0.33uA	0.36uA
-2.60	0.33uA	0.33uA	0.36uA
-2.50	0.32uA	0.32uA	0.35uA
-2.40	0.32uA	0.31uA	0.34uA
-2.30	0.31uA	0.31uA	0.34uA
-2.20	0.30uA	0.30uA	0.33uA
-2.10	0.30uA	0.29uA	0.32uA
-2.00	0.29uA	0.29uA	0.32uA
-1.90	0.28uA	0.28uA	0.31uA
-1.80	0.28uA	0.28uA	0.30uA

Appendix B IBIS Model

-1.70	0.27uA	0.27uA	0.30uA
-1.60	0.27uA	0.26uA	0.29uA
-1.50	0.26uA	0.26uA	0.29uA
-1.40	0.25uA	0.25uA	0.28uA
-1.30	0.25uA	0.25uA	0.27uA
-1.20	0.24uA	0.24uA	0.27uA
-1.10	0.24uA	0.23uA	0.26uA
-1.00	0.23uA	0.23uA	0.25uA
-0.90	0.22uA	0.22uA	0.25uA
-0.80	0.22uA	0.22uA	0.24uA
-0.70	0.21uA	0.21uA	0.24uA
-0.60	0.21uA	0.20uA	0.23uA
-0.50	0.20uA	0.20uA	0.22uA
-0.40	0.20uA	0.19uA	0.22uA
-0.30	0.19uA	0.19uA	0.21uA
-0.20	0.48mA	0.56uA	0.72uA
-0.10	0.16uA	0.17uA	0.18uA
0.00	0.16uA	0.15uA	0.18uA

[Ramp]			
variable	typ	min	max
dV/dt_r	1.54/2.19n	1.20/2.87n	1.77/2.14n
dV/dt_f	1.52/3.15n	1.15/4.45n	1.73/3.01n

R_load = 50.00

[Rising Waveform]

R_fixture = 50.00

V_fixture = 0.000

V_fixture_min = 0.000

V_fixture_max = 0.000

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.70uV	0.93uV	0.69uV
0.20nS	0.46uV	0.77uV	0.000V
0.40nS	-5.77uV	-1.75uV	11.67uV
0.60nS	-0.27mV	-5.10uV	-2.79mV
0.80nS	-2.96mV	26.03uV	-6.12mV
1.00nS	-3.62mV	-5.61uV	32.64mV
1.20nS	19.35mV	-0.80mV	81.12mV
1.40nS	46.31mV	-3.19mV	0.11V
1.60nS	79.98mV	-6.88mV	0.16V

1.80nS	0.12V	-0.22mV	0.21V
2.00nS	0.16V	21.89mV	0.27V
2.20nS	0.20V	48.68mV	0.33V
2.40nS	0.26V	76.62mV	0.41V
2.60nS	0.32V	0.11V	0.49V
2.80nS	0.42V	0.16V	0.61V
3.00nS	0.51V	0.20V	0.73V
3.20nS	0.58V	0.24V	0.82V
3.40nS	0.71V	0.30V	0.99V
3.60nS	0.85V	0.36V	1.17V
3.80nS	1.01V	0.45V	1.36V
4.00nS	1.18V	0.54V	1.56V
4.20nS	1.38V	0.67V	1.81V
4.40nS	1.57V	0.81V	2.03V
4.60nS	1.69V	0.89V	2.16V
4.80nS	1.79V	0.96V	2.27V
5.00nS	1.91V	1.06V	2.40V
5.20nS	2.03V	1.15V	2.52V
5.40nS	2.14V	1.26V	2.61V
5.60nS	2.24V	1.35V	2.70V
5.80nS	2.28V	1.40V	2.74V
6.00nS	2.31V	1.45V	2.77V
6.20nS	2.36V	1.51V	2.80V
6.40nS	2.39V	1.56V	2.83V
6.60nS	2.41V	1.61V	2.85V
6.80nS	2.43V	1.66V	2.86V
7.00nS	2.45V	1.70V	2.87V
7.20nS	2.46V	1.74V	2.88V
7.40nS	2.48V	1.78V	2.89V
7.60nS	2.49V	1.82V	2.90V
7.80nS	2.50V	1.84V	2.91V
8.00nS	2.51V	1.86V	2.91V
8.20nS	2.52V	1.88V	2.92V
8.40nS	2.52V	1.90V	2.92V
8.60nS	2.53V	1.92V	2.93V
8.80nS	2.54V	1.93V	2.93V
9.00nS	2.54V	1.95V	2.93V
9.20nS	2.55V	1.96V	2.94V
9.40nS	2.55V	1.97V	2.94V
9.60nS	2.56V	1.99V	2.94V
9.80nS	2.56V	2.00V	2.95V
10.00nS	2.57V	2.00V	2.95V

|
[Rising Waveform]

Appendix B IBIS Model

R_fixture = 50.00

V_fixture = 3.30

V_fixture_min = 3.00

V_fixture_max = 3.60

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.76V	1.03V	0.72V
0.20nS	0.76V	1.03V	0.72V
0.40nS	0.76V	1.03V	0.72V
0.60nS	0.76V	1.03V	0.72V
0.80nS	0.77V	1.03V	0.73V
1.00nS	0.81V	1.03V	0.82V
1.20nS	0.90V	1.03V	0.93V
1.40nS	0.98V	1.04V	1.02V
1.60nS	1.10V	1.11V	1.13V
1.80nS	1.22V	1.21V	1.26V
2.00nS	1.36V	1.33V	1.42V
2.20nS	1.53V	1.46V	1.58V
2.40nS	1.72V	1.60V	1.80V
2.60nS	1.93V	1.75V	2.04V
2.80nS	2.23V	1.97V	2.36V
3.00nS	2.48V	2.16V	2.62V
3.20nS	2.66V	2.30V	2.82V
3.40nS	2.85V	2.49V	3.04V
3.60nS	2.97V	2.63V	3.19V
3.80nS	3.09V	2.73V	3.29V
4.00nS	3.14V	2.83V	3.36V
4.20nS	3.19V	2.89V	3.42V
4.40nS	3.23V	2.94V	3.47V
4.60nS	3.25V	2.96V	3.50V
4.80nS	3.27V	2.97V	3.52V
5.00nS	3.28V	2.98V	3.54V
5.20nS	3.29V	2.99V	3.56V
5.40nS	3.29V	2.99V	3.57V
5.60nS	3.30V	3.00V	3.58V
5.80nS	3.30V	3.00V	3.59V
6.00nS	3.30V	3.00V	3.59V
6.20nS	3.30V	3.00V	3.60V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V
7.00nS	3.30V	3.00V	3.60V

7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V
8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V
9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

|
[Falling Waveform]

R_fixture = 50.00

V_fixture = 0.000

V_fixture_min = 0.000

V_fixture_max = 0.000

L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	2.62V	2.12V	2.99V
0.20nS	2.62V	2.12V	2.99V
0.40nS	2.62V	2.12V	2.99V
0.60nS	2.62V	2.12V	2.96V
0.80nS	2.60V	2.12V	2.85V
1.00nS	2.50V	2.12V	2.72V
1.20nS	2.37V	2.11V	2.59V
1.40nS	2.29V	2.09V	2.50V
1.60nS	2.17V	2.04V	2.36V
1.80nS	2.04V	1.96V	2.20V
2.00nS	1.89V	1.85V	2.00V
2.20nS	1.71V	1.74V	1.75V
2.40nS	1.50V	1.63V	1.48V
2.60nS	1.28V	1.50V	1.24V
2.80nS	1.01V	1.33V	1.01V
3.00nS	0.82V	1.17V	0.82V
3.20nS	0.72V	1.04V	0.75V
3.40nS	0.61V	0.87V	0.65V
3.60nS	0.51V	0.72V	0.57V

Appendix B IBIS Model

3.80nS	0.44V	0.60V	0.50V
4.00nS	0.38V	0.49V	0.44V
4.20nS	0.32V	0.40V	0.38V
4.40nS	0.26V	0.32V	0.32V
4.60nS	0.23V	0.28V	0.29V
4.80nS	0.21V	0.25V	0.26V
5.00nS	0.17V	0.21V	0.23V
5.20nS	0.15V	0.18V	0.20V
5.40nS	0.12V	0.14V	0.17V
5.60nS	93.14mV	0.11V	0.14V
5.80nS	80.86mV	94.78mV	0.12V
6.00nS	68.57mV	80.67mV	0.11V
6.20nS	55.24mV	65.96mV	90.13mV
6.40nS	43.92mV	51.39mV	74.96mV
6.60nS	33.33mV	40.71mV	61.03mV
6.80nS	25.91mV	31.19mV	50.31mV
7.00nS	18.81mV	22.83mV	39.65mV
7.20nS	13.52mV	17.13mV	31.61mV
7.40nS	8.40mV	10.61mV	22.62mV
7.60nS	4.73mV	6.73mV	15.75mV
7.80nS	3.46mV	4.67mV	12.43mV
8.00nS	2.19mV	3.16mV	9.14mV
8.20nS	1.26mV	2.23mV	6.37mV
8.40nS	0.84mV	1.32mV	4.12mV
8.60nS	0.49mV	0.95mV	2.29mV
8.80nS	0.41mV	0.74mV	1.55mV
9.00nS	0.35mV	0.58mV	0.81mV
9.20nS	0.31mV	0.51mV	0.53mV
9.40nS	0.28mV	0.45mV	0.39mV
9.60nS	0.24mV	0.40mV	0.27mV
9.80nS	0.22mV	0.36mV	0.24mV
10.00nS	0.20mV	0.32mV	0.21mV

```

|
[Falling Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F
| time          V(typ)          V(min)          V(max)
|
0.000S          3.30V          3.00V          3.60V
0.20nS          3.30V          3.00V          3.60V

```


0.40nS	3.30V	3.00V	3.60V
0.60nS	3.30V	3.00V	3.59V
0.80nS	3.30V	3.00V	3.52V
1.00nS	3.25V	3.00V	3.44V
1.20nS	3.18V	3.00V	3.37V
1.40nS	3.14V	3.00V	3.32V
1.60nS	3.09V	3.00V	3.24V
1.80nS	3.03V	2.97V	3.16V
2.00nS	2.96V	2.92V	3.07V
2.20nS	2.88V	2.88V	2.98V
2.40nS	2.80V	2.84V	2.88V
2.60nS	2.72V	2.80V	2.77V
2.80nS	2.60V	2.74V	2.64V
3.00nS	2.51V	2.68V	2.54V
3.20nS	2.44V	2.64V	2.46V
3.40nS	2.34V	2.58V	2.34V
3.60nS	2.25V	2.52V	2.22V
3.80nS	2.15V	2.46V	2.08V
4.00nS	2.05V	2.39V	1.92V
4.20nS	1.93V	2.32V	1.74V
4.40nS	1.81V	2.24V	1.58V
4.60nS	1.73V	2.19V	1.50V
4.80nS	1.65V	2.15V	1.42V
5.00nS	1.53V	2.09V	1.34V
5.20nS	1.43V	2.04V	1.26V
5.40nS	1.32V	1.97V	1.18V
5.60nS	1.22V	1.91V	1.11V
5.80nS	1.18V	1.87V	1.07V
6.00nS	1.13V	1.84V	1.03V
6.20nS	1.08V	1.79V	0.99V
6.40nS	1.03V	1.75V	0.95V
6.60nS	0.99V	1.70V	0.92V
6.80nS	0.96V	1.66V	0.89V
7.00nS	0.93V	1.63V	0.87V
7.20nS	0.90V	1.59V	0.84V
7.40nS	0.87V	1.53V	0.82V
7.60nS	0.84V	1.47V	0.80V
7.80nS	0.83V	1.44V	0.78V
8.00nS	0.82V	1.40V	0.78V
8.20nS	0.81V	1.35V	0.76V
8.40nS	0.80V	1.30V	0.75V
8.60nS	0.79V	1.26V	0.75V
8.80nS	0.78V	1.23V	0.74V
9.00nS	0.78V	1.19V	0.73V

Appendix B IBIS Model

9.20nS	0.78V	1.17V	0.73V
9.40nS	0.77V	1.14V	0.73V
9.60nS	0.77V	1.12V	0.72V
9.80nS	0.77V	1.10V	0.72V
10.00nS	0.77V	1.08V	0.72V

| End [Model] prt24dgz

| *****
| Model pdusdgz

[Model] pdusdgz
Model_type Input
Polarity Non-Inverting

Vinl = 0.000V

Vinh = 3.30V

C_comp 5.00pF 5.00pF 5.00pF

[Temperature Range] 25.00 0.12k 0.000
[Pullup Reference] 3.30V 3.00V 3.60V
[Pulldown Reference] 0.000V 0.000V 0.000V
[POWER Clamp Reference] 5.00V 4.50V 5.50V
[GND Clamp Reference] 0.000V 0.000V 0.000V

[GND_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	-64.63A	-59.13A	-66.41A
-4.80	-61.55A	-56.41A	-63.21A
-4.60	-58.47A	-53.69A	-60.01A
-4.40	-55.39A	-50.97A	-56.81A
-4.20	-52.31A	-48.25A	-53.61A
-4.00	-49.23A	-45.53A	-50.41A
-3.80	-46.15A	-42.81A	-47.21A
-3.60	-43.07A	-40.09A	-44.01A
-3.40	-39.99A	-37.37A	-40.81A
-3.20	-36.91A	-34.65A	-37.61A
-3.00	-33.82A	-31.94A	-34.41A
-2.80	-30.73A	-29.22A	-31.22A
-2.60	-27.64A	-26.51A	-28.02A
-2.40	-24.56A	-23.79A	-24.82A
-2.20	-21.47A	-21.08A	-21.62A
-2.00	-18.38A	-18.36A	-18.42A

-1.80	-15.29A	-15.64A	-15.22A
-1.60	-12.20A	-12.93A	-12.03A
-1.40	-9.12A	-10.21A	-8.83A
-1.20	-6.03A	-7.50A	-5.63A
-1.00	-2.94A	-4.78A	-2.43A
-0.80	-0.20A	-2.07A	-64.17mA
-0.60	-1.85mA	-96.40mA	-4.85mA
-0.40	-83.24uA	-0.50mA	-0.23mA
-0.20	-60.52uA	-36.82uA	-86.29uA
-0.00	-60.40uA	-35.33uA	-85.95uA
0.20	-60.32uA	-35.27uA	-85.85uA
0.40	-60.23uA	-35.20uA	-85.73uA
0.60	-60.11uA	-35.13uA	-85.57uA
0.80	-59.96uA	-35.03uA	-85.37uA
1.00	-59.74uA	-34.91uA	-85.08uA
1.20	-59.32uA	-34.50uA	-84.56uA
1.40	-58.35uA	-33.59uA	-83.44uA
1.60	-56.47uA	-31.92uA	-81.36uA
1.80	-53.57uA	-29.25uA	-78.20uA
2.00	-49.55uA	-7.60uA	-73.89uA
2.20	-43.70uA	-16.78nA	-68.43uA
2.40	-3.73uA	0.10uA	-61.70uA
2.60	0.10uA	0.11uA	-51.99uA
2.80	0.12uA	0.12uA	-2.43uA
3.00	0.13uA	0.13uA	0.13uA
3.20	0.14uA	0.20uA	0.14uA
3.40	0.15uA	0.15uA	0.15uA
3.60	0.16uA	96.30nA	0.16uA
3.80	0.17uA	43.50nA	0.17uA
4.00	0.18uA	-9.30nA	0.18uA
4.20	0.18uA	-62.10nA	0.19uA
4.40	0.19uA	-0.11uA	0.20uA
4.60	0.20uA	-0.17uA	0.21uA
4.80	0.21uA	-0.22uA	0.22uA
5.00	0.22uA	-0.27uA	0.23uA

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	0.61uA	0.59uA	0.65uA
-4.90	0.60uA	0.58uA	0.65uA
-4.80	0.59uA	0.58uA	0.64uA
-4.70	0.59uA	0.57uA	0.63uA
-4.60	0.58uA	0.56uA	0.63uA

Appendix B IBIS Model

-4.50	0.57uA	0.56uA	0.62uA
-4.40	0.56uA	0.55uA	0.61uA
-4.30	0.56uA	0.54uA	0.60uA
-4.20	0.55uA	0.54uA	0.60uA
-4.10	0.54uA	0.53uA	0.59uA
-4.00	0.54uA	0.52uA	0.58uA
-3.90	0.53uA	0.52uA	0.58uA
-3.80	0.52uA	0.51uA	0.57uA
-3.70	0.52uA	0.50uA	0.56uA
-3.60	0.51uA	0.50uA	0.56uA
-3.50	0.50uA	0.49uA	0.55uA
-3.40	0.50uA	0.48uA	0.54uA
-3.30	0.49uA	0.48uA	0.53uA
-3.20	0.48uA	0.47uA	0.53uA
-3.10	0.48uA	0.46uA	0.52uA
-3.00	0.47uA	0.46uA	0.51uA
-2.90	0.46uA	0.45uA	0.51uA
-2.80	0.46uA	0.44uA	0.50uA
-2.70	0.45uA	0.44uA	0.49uA
-2.60	0.44uA	0.43uA	0.49uA
-2.50	0.44uA	0.42uA	0.48uA
-2.40	0.43uA	0.41uA	0.47uA
-2.30	0.42uA	0.41uA	0.46uA
-2.20	0.42uA	0.40uA	0.46uA
-2.10	0.41uA	0.39uA	0.45uA
-2.00	0.40uA	0.39uA	0.44uA
-1.90	0.39uA	0.38uA	0.44uA
-1.80	0.39uA	0.37uA	0.43uA
-1.70	0.38uA	0.37uA	0.42uA
-1.60	0.37uA	0.36uA	0.42uA
-1.50	0.37uA	0.35uA	0.41uA
-1.40	0.36uA	0.35uA	0.40uA
-1.30	0.35uA	0.34uA	0.39uA
-1.20	0.35uA	0.33uA	0.39uA
-1.10	0.34uA	0.33uA	0.38uA
-1.00	0.33uA	0.32uA	0.37uA
-0.90	0.33uA	0.31uA	0.37uA
-0.80	0.32uA	0.31uA	0.36uA
-0.70	0.31uA	0.30uA	0.35uA
-0.60	0.31uA	0.29uA	0.35uA
-0.50	0.30uA	0.29uA	0.34uA
-0.40	0.29uA	0.28uA	0.33uA
-0.30	0.29uA	0.27uA	0.32uA
-0.20	0.28uA	0.27uA	0.32uA

```

-0.10      0.27uA      0.26uA      0.31uA
 0.00      0.27uA      0.25uA      0.30uA
|
| End [Model] pdusdgz
|
|*****
|
|                               Model pdddgz
|*****
|
[Model]          pdddgz
Model_type      Input
Polarity        Non-Inverting
Vinl = 0.000V
Vinh = 3.30V
C_comp          5.00pF          5.00pF          5.00pF
|
|
[Temperature Range]      25.00          0.12k          0.000
[Pullup Reference]      3.30V          3.00V          3.60V
[Pulldown Reference]    0.000V          0.000V          0.000V
[POWER Clamp Reference] 5.00V          4.50V          5.50V
[GND Clamp Reference]   0.000V          0.000V          0.000V
[GND_clamp]
| voltage      I(typ)          I(min)          I(max)
|
-5.00      -64.63A      -59.13A      -66.41A
-4.80      -61.55A      -56.41A      -63.21A
-4.60      -58.47A      -53.69A      -60.01A
-4.40      -55.39A      -50.97A      -56.81A
-4.20      -52.31A      -48.25A      -53.61A
-4.00      -49.23A      -45.53A      -50.41A
-3.80      -46.15A      -42.81A      -47.21A
-3.60      -43.07A      -40.09A      -44.01A
-3.40      -39.99A      -37.37A      -40.81A
-3.20      -36.91A      -34.65A      -37.61A
-3.00      -33.82A      -31.94A      -34.41A
-2.80      -30.73A      -29.22A      -31.22A
-2.60      -27.64A      -26.51A      -28.02A
-2.40      -24.56A      -23.79A      -24.82A
-2.20      -21.47A      -21.08A      -21.62A
-2.00      -18.38A      -18.36A      -18.42A
-1.80      -15.29A      -15.64A      -15.22A
-1.60      -12.20A      -12.93A      -12.03A
-1.40      -9.12A       -10.21A      -8.83A

```

Appendix B IBIS Model

-1.20	-6.03A	-7.50A	-5.63A
-1.00	-2.94A	-4.78A	-2.43A
-0.80	-0.20A	-2.07A	-64.21mA
-0.60	-1.89mA	-96.41mA	-4.91mA
-0.40	-85.69uA	-0.50mA	-0.24mA
-0.20	-27.91uA	-14.61uA	-42.88uA
-0.00	-87.50nA	-88.83nA	-0.10uA
0.20	18.71uA	7.31uA	32.27uA
0.40	29.18uA	10.24uA	54.12uA
0.60	32.49uA	10.66uA	65.78uA
0.80	33.06uA	10.78uA	69.33uA
1.00	33.29uA	10.85uA	70.16uA
1.20	33.44uA	10.91uA	70.54uA
1.40	33.56uA	10.96uA	70.78uA
1.60	33.66uA	11.01uA	70.98uA
1.80	33.76uA	11.06uA	71.15uA
2.00	33.85uA	11.10uA	71.30uA
2.20	33.94uA	11.12uA	71.44uA
2.40	33.99uA	11.13uA	71.59uA
2.60	34.01uA	11.14uA	71.74uA
2.80	34.02uA	11.15uA	71.82uA
3.00	34.03uA	11.16uA	71.84uA
3.20	34.04uA	11.25uA	71.85uA
3.40	34.06uA	11.17uA	71.87uA
3.60	34.08uA	11.09uA	71.89uA
3.80	34.10uA	11.01uA	71.91uA
4.00	34.12uA	10.93uA	71.93uA
4.20	34.14uA	10.85uA	71.95uA
4.40	34.16uA	10.77uA	71.97uA
4.60	34.18uA	10.69uA	71.99uA
4.80	34.20uA	10.61uA	72.01uA
5.00	34.22uA	10.53uA	72.03uA
[POWER_clamp]			
voltage			
	I (typ)	I (min)	I (max)
-5.00	48.19uA	16.29uA	95.53uA
-4.90	47.87uA	16.17uA	95.03uA
-4.80	47.55uA	16.05uA	94.53uA
-4.70	47.23uA	15.93uA	94.03uA
-4.60	46.91uA	15.81uA	93.53uA
-4.50	46.59uA	15.69uA	93.03uA
-4.40	46.27uA	15.57uA	92.53uA
-4.30	45.95uA	15.45uA	92.03uA

-4.20	45.63uA	15.33uA	91.53uA
-4.10	45.31uA	15.21uA	91.03uA
-4.00	44.99uA	15.09uA	90.53uA
-3.90	44.67uA	14.97uA	90.03uA
-3.80	44.35uA	14.85uA	89.53uA
-3.70	44.03uA	14.73uA	89.03uA
-3.60	43.71uA	14.61uA	88.53uA
-3.50	43.39uA	14.49uA	88.03uA
-3.40	43.07uA	14.37uA	87.53uA
-3.30	42.75uA	14.25uA	87.03uA
-3.20	42.43uA	14.13uA	86.53uA
-3.10	42.11uA	14.01uA	86.03uA
-3.00	41.79uA	13.89uA	85.53uA
-2.90	41.47uA	13.77uA	85.03uA
-2.80	41.15uA	13.65uA	84.53uA
-2.70	40.83uA	13.53uA	84.03uA
-2.60	40.51uA	13.41uA	83.53uA
-2.50	40.19uA	13.29uA	83.03uA
-2.40	39.87uA	13.17uA	82.53uA
-2.30	39.55uA	13.05uA	82.03uA
-2.20	39.23uA	12.93uA	81.53uA
-2.10	38.91uA	12.81uA	81.03uA
-2.00	38.59uA	12.69uA	80.53uA
-1.90	38.27uA	12.57uA	80.03uA
-1.80	37.95uA	12.45uA	79.53uA
-1.70	37.63uA	12.33uA	79.03uA
-1.60	37.31uA	12.22uA	78.53uA
-1.50	36.99uA	12.11uA	78.03uA
-1.40	36.68uA	12.01uA	77.53uA
-1.30	36.38uA	11.92uA	77.03uA
-1.20	36.11uA	11.84uA	76.53uA
-1.10	35.86uA	11.76uA	76.03uA
-1.00	35.63uA	11.69uA	75.53uA
-0.90	35.41uA	11.63uA	75.06uA
-0.80	35.22uA	11.57uA	74.63uA
-0.70	35.05uA	11.52uA	74.24uA
-0.60	34.90uA	11.48uA	73.89uA
-0.50	34.77uA	11.44uA	73.58uA
-0.40	34.65uA	11.41uA	73.30uA
-0.30	34.55uA	11.38uA	73.06uA
-0.20	34.47uA	11.35uA	72.86uA
-0.10	34.40uA	11.33uA	72.68uA
0.00	34.34uA	11.31uA	72.54uA

Appendix B IBIS Model

```

| End [Model] pdddgz
|
| *****
|                                     Model pdudgz
| *****
|
[Model]          pdudgz
Model_type       Input
Polarity         Non-Inverting
Vinl = 0.000V
Vinh = 3.30V
C_comp          5.00pF          5.00pF          5.00pF
|
|
[Temperature Range]    25.00          0.12k          0.000
[Pullup Reference]    3.30V          3.00V          3.60V
[Pulldown Reference]  0.000V          0.000V          0.000V
[POWER Clamp Reference] 5.00V          4.50V          5.50V
[GND Clamp Reference]  0.000V          0.000V          0.000V
[GND_clamp]
| voltage      I(typ)          I(min)          I(max)
|
-5.00         -64.63A          -59.13A          -66.41A
-4.80         -61.55A          -56.41A          -63.21A
-4.60         -58.47A          -53.69A          -60.01A
-4.40         -55.39A          -50.97A          -56.81A
-4.20         -52.31A          -48.25A          -53.61A
-4.00         -49.23A          -45.53A          -50.41A
-3.80         -46.15A          -42.81A          -47.21A
-3.60         -43.07A          -40.09A          -44.01A
-3.40         -39.99A          -37.37A          -40.81A
-3.20         -36.91A          -34.65A          -37.61A
-3.00         -33.82A          -31.94A          -34.41A
-2.80         -30.73A          -29.22A          -31.22A
-2.60         -27.64A          -26.51A          -28.02A
-2.40         -24.56A          -23.79A          -24.82A
-2.20         -21.47A          -21.08A          -21.62A
-2.00         -18.38A          -18.36A          -18.42A
-1.80         -15.29A          -15.64A          -15.22A
-1.60         -12.20A          -12.93A          -12.03A
-1.40         -9.12A           -10.21A          -8.83A
-1.20         -6.03A           -7.50A           -5.63A
-1.00         -2.94A           -4.78A           -2.43A
-0.80         -0.20A           -2.07A           -64.17mA

```


-0.60	-1.85mA	-96.40mA	-4.85mA
-0.40	-83.24uA	-0.50mA	-0.23mA
-0.20	-60.52uA	-36.82uA	-86.29uA
-0.00	-60.40uA	-35.33uA	-85.95uA
0.20	-60.32uA	-35.27uA	-85.85uA
0.40	-60.23uA	-35.20uA	-85.73uA
0.60	-60.11uA	-35.13uA	-85.57uA
0.80	-59.96uA	-35.03uA	-85.37uA
1.00	-59.74uA	-34.87uA	-85.08uA
1.20	-59.32uA	-34.50uA	-84.56uA
1.40	-58.35uA	-33.59uA	-83.44uA
1.60	-56.47uA	-31.92uA	-81.36uA
1.80	-53.57uA	-29.25uA	-78.20uA
2.00	-49.55uA	-7.60uA	-73.89uA
2.20	-43.70uA	-16.78nA	-68.43uA
2.40	-3.73uA	0.10uA	-61.70uA
2.60	0.10uA	0.11uA	-51.99uA
2.80	0.12uA	0.12uA	-2.43uA
3.00	0.13uA	0.13uA	0.13uA
3.20	0.14uA	0.20uA	0.14uA
3.40	0.15uA	0.15uA	0.15uA
3.60	0.16uA	96.30nA	0.16uA
3.80	0.17uA	43.50nA	0.17uA
4.00	0.18uA	-9.30nA	0.18uA
4.20	0.18uA	-62.10nA	0.19uA
4.40	0.19uA	-0.11uA	0.20uA
4.60	0.20uA	-0.17uA	0.21uA
4.80	0.21uA	-0.22uA	0.22uA
5.00	0.22uA	-0.27uA	0.23uA

[POWER_clamp]			
voltage	I (typ)	I (min)	I (max)
-5.00	0.61uA	0.59uA	0.65uA
-4.90	0.60uA	0.58uA	0.65uA
-4.80	0.59uA	0.58uA	0.64uA
-4.70	0.59uA	0.57uA	0.63uA
-4.60	0.58uA	0.56uA	0.63uA
-4.50	0.57uA	0.56uA	0.62uA
-4.40	0.56uA	0.55uA	0.61uA
-4.30	0.56uA	0.54uA	0.60uA
-4.20	0.55uA	0.54uA	0.60uA
-4.10	0.54uA	0.53uA	0.59uA
-4.00	0.54uA	0.52uA	0.58uA

Appendix B IBIS Model

-3.90	0.53uA	0.52uA	0.58uA
-3.80	0.52uA	0.51uA	0.57uA
-3.70	0.52uA	0.50uA	0.56uA
-3.60	0.51uA	0.50uA	0.56uA
-3.50	0.50uA	0.49uA	0.55uA
-3.40	0.50uA	0.48uA	0.54uA
-3.30	0.49uA	0.48uA	0.53uA
-3.20	0.48uA	0.47uA	0.53uA
-3.10	0.48uA	0.46uA	0.52uA
-3.00	0.47uA	0.46uA	0.51uA
-2.90	0.46uA	0.45uA	0.51uA
-2.80	0.46uA	0.44uA	0.50uA
-2.70	0.45uA	0.44uA	0.49uA
-2.60	0.44uA	0.43uA	0.49uA
-2.50	0.44uA	0.42uA	0.48uA
-2.40	0.43uA	0.41uA	0.47uA
-2.30	0.42uA	0.41uA	0.46uA
-2.20	0.42uA	0.40uA	0.46uA
-2.10	0.41uA	0.39uA	0.45uA
-2.00	0.40uA	0.39uA	0.44uA
-1.90	0.39uA	0.38uA	0.44uA
-1.80	0.39uA	0.37uA	0.43uA
-1.70	0.38uA	0.37uA	0.42uA
-1.60	0.37uA	0.36uA	0.42uA
-1.50	0.37uA	0.35uA	0.41uA
-1.40	0.36uA	0.35uA	0.40uA
-1.30	0.35uA	0.34uA	0.39uA
-1.20	0.35uA	0.33uA	0.39uA
-1.10	0.34uA	0.33uA	0.38uA
-1.00	0.33uA	0.32uA	0.37uA
-0.90	0.33uA	0.31uA	0.37uA
-0.80	0.32uA	0.31uA	0.36uA
-0.70	0.31uA	0.30uA	0.35uA
-0.60	0.31uA	0.29uA	0.35uA
-0.50	0.30uA	0.29uA	0.34uA
-0.40	0.29uA	0.28uA	0.33uA
-0.30	0.29uA	0.27uA	0.32uA
-0.20	0.28uA	0.27uA	0.32uA
-0.10	0.27uA	0.26uA	0.31uA
0.00	0.27uA	0.25uA	0.30uA

| End [Model] pdudgz

|*****

```

|                                     Model pdidgz
|*****
|
[Model]          pdidgz
Model_type      Input
Polarity        Non-Inverting
Vinl = 0.000V
Vinh = 3.30V
C_comp          5.00pF          5.00pF          5.00pF
|
|
[Temperature Range]      25.00          0.12k          0.000
[Pullup Reference]      3.30V          3.00V          3.60V
[ Pulldown Reference]   0.000V          0.000V          0.000V
[POWER Clamp Reference] 5.00V          4.50V          5.50V
[GND Clamp Reference]   0.000V          0.000V          0.000V
[GND_clamp]
| voltage      I(typ)          I(min)          I(max)
|
-5.00      -64.63A          -59.13A          -66.41A
-4.80      -61.55A          -56.41A          -63.21A
-4.60      -58.47A          -53.69A          -60.01A
-4.40      -55.39A          -50.97A          -56.81A
-4.20      -52.31A          -48.25A          -53.61A
-4.00      -49.23A          -45.53A          -50.41A
-3.80      -46.15A          -42.81A          -47.21A
-3.60      -43.07A          -40.09A          -44.01A
-3.40      -39.99A          -37.37A          -40.81A
-3.20      -36.91A          -34.65A          -37.61A
-3.00      -33.82A          -31.94A          -34.41A
-2.80      -30.73A          -29.22A          -31.22A
-2.60      -27.64A          -26.51A          -28.02A
-2.40      -24.56A          -23.79A          -24.82A
-2.20      -21.47A          -21.08A          -21.62A
-2.00      -18.38A          -18.36A          -18.42A
-1.80      -15.29A          -15.64A          -15.22A
-1.60      -12.20A          -12.93A          -12.03A
-1.40      -9.12A          -10.21A          -8.83A
-1.20      -6.03A          -7.50A          -5.63A
-1.00      -2.94A          -4.78A          -2.43A
-0.80      -0.20A          -2.07A          -64.14mA
-0.60      -1.79mA          -96.39mA          -4.77mA
-0.40      -22.83uA          -0.47mA          -0.14mA
-0.20      -0.15uA          -1.56uA          -0.37uA

```

Appendix B IBIS Model

-0.00	-88.71nA	-89.34nA	-0.11uA
0.20	-72.38nA	-68.50nA	-88.30nA
0.40	-56.11nA	-52.12nA	-71.55nA
0.60	-39.84nA	-35.76nA	-54.82nA
0.80	-23.57nA	-19.40nA	-38.12nA
1.00	-7.31nA	-3.04nA	-21.42nA
1.20	8.94nA	13.32nA	-4.73nA
1.40	25.19nA	29.68nA	11.97nA
1.60	41.42nA	46.03nA	28.68nA
1.80	57.64nA	62.39nA	45.42nA
2.00	73.83nA	78.74nA	62.20nA
2.20	89.95nA	94.86nA	79.06nA
2.40	0.11uA	0.11uA	96.02nA
2.60	0.12uA	0.12uA	0.11uA
2.80	0.13uA	0.13uA	0.13uA
3.00	0.14uA	0.14uA	0.14uA
3.20	0.15uA	0.21uA	0.15uA
3.40	0.15uA	0.15uA	0.16uA
3.60	0.16uA	0.10uA	0.17uA
3.80	0.17uA	47.20nA	0.18uA
4.00	0.18uA	-5.80nA	0.18uA
4.20	0.19uA	-58.80nA	0.19uA
4.40	0.20uA	-0.11uA	0.20uA
4.60	0.20uA	-0.16uA	0.21uA
4.80	0.21uA	-0.22uA	0.22uA
5.00	0.22uA	-0.27uA	0.23uA

|

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	0.60uA	0.59uA	0.65uA
-4.90	0.60uA	0.58uA	0.64uA
-4.80	0.59uA	0.58uA	0.64uA
-4.70	0.58uA	0.57uA	0.63uA
-4.60	0.58uA	0.56uA	0.62uA
-4.50	0.57uA	0.56uA	0.62uA
-4.40	0.56uA	0.55uA	0.61uA
-4.30	0.56uA	0.54uA	0.60uA
-4.20	0.55uA	0.54uA	0.59uA
-4.10	0.54uA	0.53uA	0.59uA
-4.00	0.54uA	0.52uA	0.58uA
-3.90	0.53uA	0.52uA	0.57uA
-3.80	0.52uA	0.51uA	0.57uA
-3.70	0.52uA	0.50uA	0.56uA

-3.60	0.51uA	0.50uA	0.55uA
-3.50	0.50uA	0.49uA	0.55uA
-3.40	0.49uA	0.48uA	0.54uA
-3.30	0.49uA	0.48uA	0.53uA
-3.20	0.48uA	0.47uA	0.53uA
-3.10	0.47uA	0.46uA	0.52uA
-3.00	0.47uA	0.46uA	0.51uA
-2.90	0.46uA	0.45uA	0.51uA
-2.80	0.45uA	0.44uA	0.50uA
-2.70	0.45uA	0.43uA	0.49uA
-2.60	0.44uA	0.43uA	0.48uA
-2.50	0.43uA	0.42uA	0.48uA
-2.40	0.43uA	0.41uA	0.47uA
-2.30	0.42uA	0.41uA	0.46uA
-2.20	0.41uA	0.40uA	0.46uA
-2.10	0.41uA	0.39uA	0.45uA
-2.00	0.40uA	0.39uA	0.44uA
-1.90	0.39uA	0.38uA	0.44uA
-1.80	0.39uA	0.37uA	0.43uA
-1.70	0.38uA	0.37uA	0.42uA
-1.60	0.37uA	0.36uA	0.42uA
-1.50	0.37uA	0.35uA	0.41uA
-1.40	0.36uA	0.35uA	0.40uA
-1.30	0.35uA	0.34uA	0.39uA
-1.20	0.35uA	0.33uA	0.39uA
-1.10	0.34uA	0.33uA	0.38uA
-1.00	0.33uA	0.32uA	0.37uA
-0.90	0.33uA	0.31uA	0.37uA
-0.80	0.32uA	0.31uA	0.36uA
-0.70	0.31uA	0.30uA	0.35uA
-0.60	0.31uA	0.29uA	0.35uA
-0.50	0.30uA	0.29uA	0.34uA
-0.40	0.29uA	0.28uA	0.33uA
-0.30	0.29uA	0.27uA	0.33uA
-0.20	0.28uA	0.27uA	0.32uA
-0.10	0.28uA	0.26uA	0.31uA
0.00	0.27uA	0.26uA	0.31uA

|

| End [Model] pdidgz

Revision History

Revision	Date	Description
0.0	27 April 2004	Initial release

NOTES

How to Reach Us:

Home Page:

www.freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
1-800-521-6274 or 480-768-2130

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0063
Japan
0120 191014 or +81 3 5437 9125
support-japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
852-26668334

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2004. All rights reserved.