DENSE-PAC
MICROSYSTEMS

1 Megabit High Speed CMOS SRAM

DPS128M8CnY/BnY, DPS128X8CA3/BA3

DESCRIPTION:

The DPS128M8CnY/BnY, DPS128X8CA3/BA3 High Speed SRAM devices are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, ''J'' leaded or gullwing leaded packages, or mounted on a 50-pin PGA co-fired ceramic substrate. These devices pack 1-Megabits of low-power CMOS static RAM in an area as small as 0.463 in^2, while maintaining a total height as low as 0.082 inches.

The SLCC devices contain an individual 128K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

The DPS128M8BnY/DPS128X8BA3 has one active low Chip Enable ($\overline{CE}$) while the DPS128M8CnY/DPS128X8CA3 has an active low Chip Enable ($\overline{CE}$) and an active high Select Line (SEL).

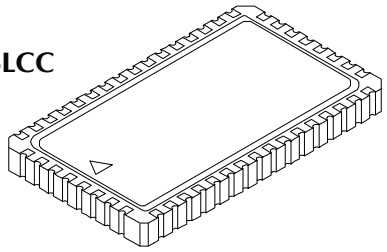
By using SLCCs, the ''Stack'' family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

FEATURES:

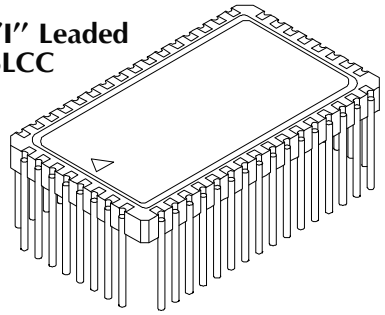
- Organization Available: 128Kx8
- Access Times: 20*, 25, 30, 35, 45ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:
  - 48 - Pin SLCC
  - 48 - Pin Straight Leaded SLCC
  - 48 - Pin ''J'' Leaded SLCC
  - 48 - Pin Gullwing Leaded SLCC
  - 50 - Pin PGA Dense-Stack

* Commercial only.

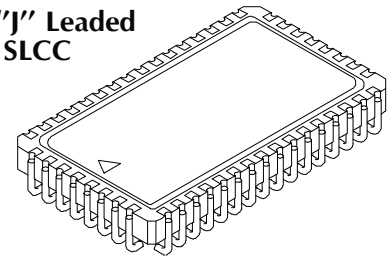
SLCC



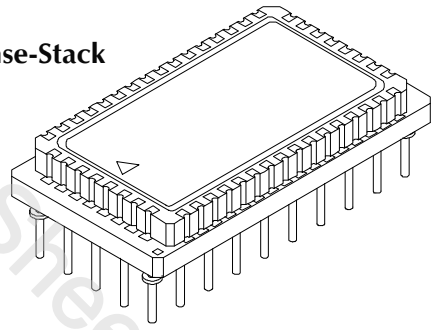
''I'' Leaded SLCC



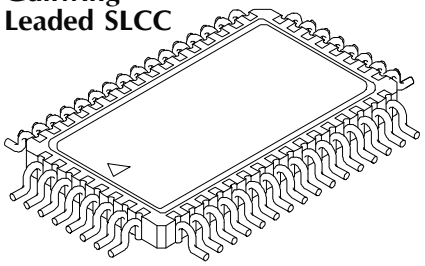
''J'' Leaded SLCC



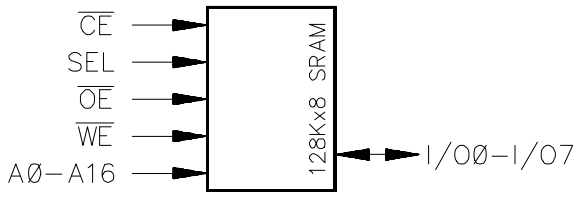
Dense-Stack



Gullwing Leaded SLCC



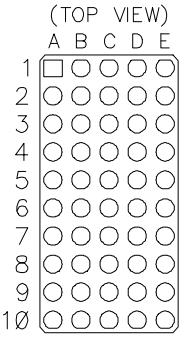
FUNCTIONAL BLOCK DIAGRAM



NOTE: SEL apply to DPS128M8CnY/DPS128X8CA3 versions only.

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O7	Data Input/Output
$\overline{CE}$	Low Chip Enable
SEL	High Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

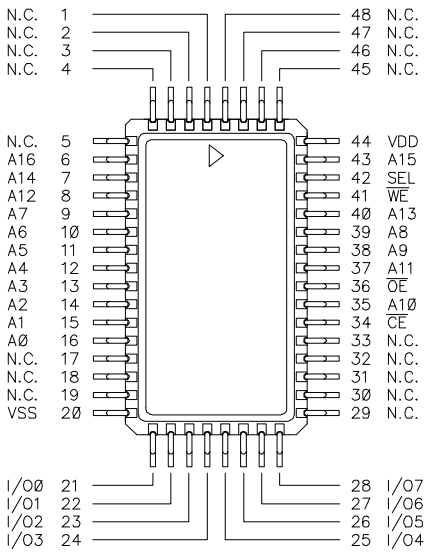
PIN-OUT DIAGRAM



50 - PIN PGA
DENSE-STACK

	A	B	C	D	E
1	N.C.	N.C.	N.C.	N.C.	N.C.
2	VSS	N.C.	N.C.	N.C.	VDD
3	N.C.	A16	$\overline{WE}$	SEL	A15
4	A14	A12	A7	A8	A13
5	A6	A5	$\overline{OE}$	A11	A9
6	A4	A3	A2	$\overline{CE}$	A1Ø
7	A1	AØ	N.C.	N.C.	N.C.
8	N.C.	N.C.	N.C.	N.C.	N.C.
9	VSS	I/O1	I/O3	I/O5	VDD
1Ø	I/OØ	I/O2	I/O4	I/O6	I/O7

48 - PIN LEADLESS STACK
48 - PIN STRAIGHT LEADED STACK
48 - PIN "J" LEADED STACK
48 - PIN GULLWING LEADED STACK



NOTE: SEL apply to DPS128M8CnY/DPS128X8CA3 versions only, No Connect for DPS128M8BnY/DPS128X8BA3 versions.

RECOMMENDED OPERATING RANGE [3]						
Symbol	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Unit**
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		$V_{DD}+0.3$	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

TRUTH TABLE						
Mode	**SEL**	**$\overline{CE}$**	**$\overline{WE}$**	**$\overline{OE}$**	**I/O Pin**	**Supply Current**
Not Selected	L	X	X	X	High-Z	Standby
Not Selected	X	H	X	X	High-Z	Standby
D_{OUT} Disable	H	L	H	H	High-Z	Active
Read	H	L	H	L	D_{OUT}	Active
Write	H	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care
NOTE: SEL applies to DPS128M8CnY/DPS128X8CA3 version only.

DC OUTPUT CHARACTERISTICS					
Symbol	**Parameter**	**Conditions**	**Min.**	**Max.**	**Unit**
V_{OH}	HIGH Voltage	I_{OH} = -4.0mA	2.4		V
V_{OL}	LOW Voltage	I_{OL} = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	**Parameter**	**Value**	**Unit**
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD}+0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	**Parameter**	**Max.**	**Unit**	**Condition**
C_{ADR}	Address Input	10	pF	V_{IN}[2] = 0V
C_{CE}	Chip Enable	10		
C_{SEL}	Active High Chip Select	10		
C_{WE}	Write Enable	10		
C_{OE}	Output Enable	10		
$C_{I/O}$	Data Input/Output	14		

NOTE: C_{SEL} applies to DPS128M8CnY/DPS128X8CA3 version only.

DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	**Characteristics**	**Test Conditions**	**Typ. (†)**	**C**		**I**		**M/B**		**Unit**
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-	-5	+5	-5	+5	-5	+5	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-	-10	+10	-10	+10	-10	+10	µA
I_{CC}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	100		140		140		160	mA
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V	0.4		5		5		10	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}	25		30		35		35	mA
I_{DR3}	Data Retention Supply Current (3.0V)	V_{DR} = 3.0V, $\overline{CE} \geq V_{DR}$ -0.2V, (or SEL ≤ 0.2V, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq$ +0.2V)	70		400		600		2000	µA
I_{DR2}	Data Retention Supply Current (2.0V)	V_{DR} = 2.0V, $\overline{CE} \geq V_{DR}$ -0.2V, (or SEL ≤ 0.2V, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq$ +0.2V)	35		250		400		1800	µA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA	-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA	-	2.4		2.4		2.4		V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.
NOTE: Test Conditions in parenthesis apply to DPS128M8CnY/DPS128X8CA3 version only.

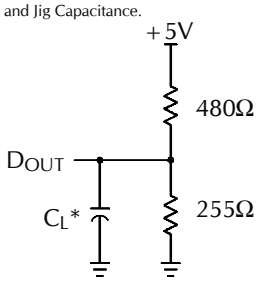
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	100pF	except t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5pF	t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

NOTE: t_{LZ2} and t_{HZ2} apply to DPS128M8CnY/DPS128X8CA3 version only.

Figure 1. Output Load

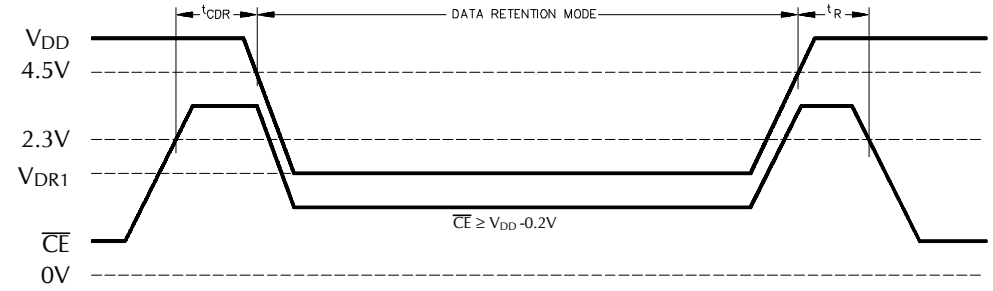
* Including Probe and Jig Capacitance.



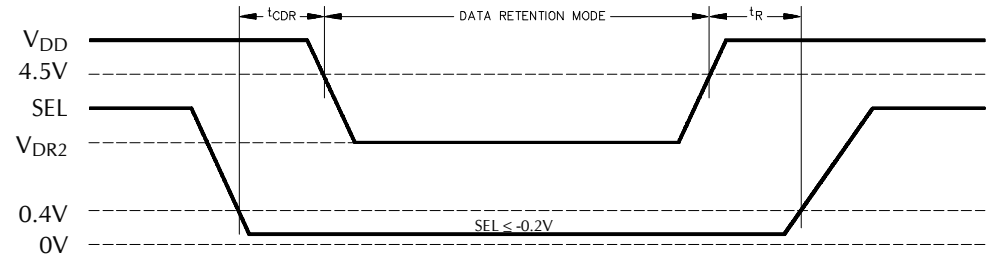
Data Retention AC Characteristics [8]						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{DR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DR}$ -0.2V, (SEL $\geq V_{DR}$ -0.2V, or $V_{IN} \leq V_{DR}$ -0.2V or $V_{IN} \leq$ 0.2V)	2.0	-	-	V
V_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

NOTE: Test Conditions in parenthesis apply to DPS128M8CnY/DPS128X8CA3 version only.

DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



DATA RETENTION WAVEFORM: SEL Controlled. (Applies to DPS128M8CnY/DPS128X8CA3 only)

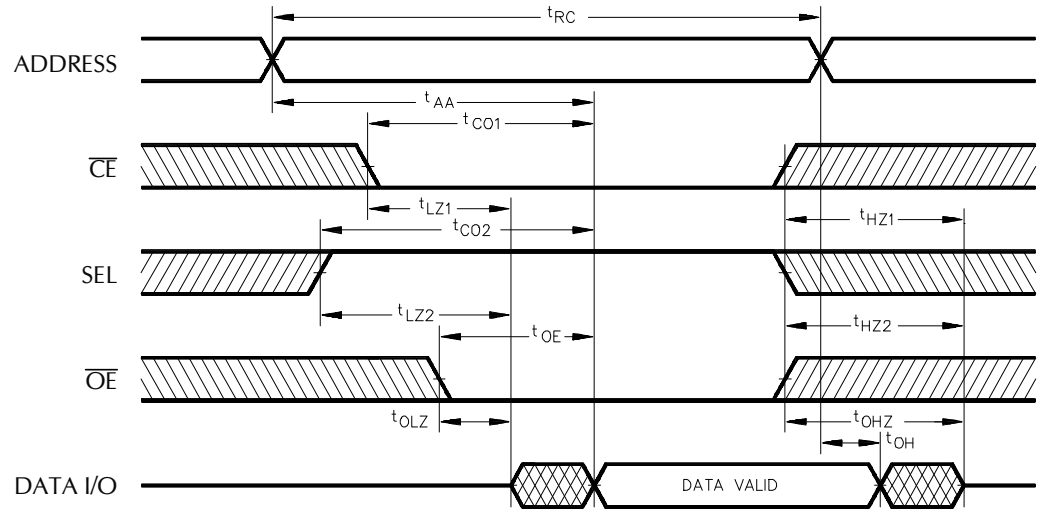


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	20		25		30		35		45		ns
2	t_{AA}	Address Access Time		20		25		30		35		45	ns
3	t_{CO1}	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t_{CO2}	SEL to Output Valid		20		25		30		35		45	ns
5	t_{OE}	Output Enable to Output Valid		8		10		15		20		25	ns
6	t_{LZ1}	$\overline{CE}$ to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
7	t_{LZ2}	SEL to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
8	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	0		0		0		0		0		ns
9	t_{HZ1}	$\overline{CE}$ to Output in HIGH-Z [4, 5]		10		12		15		20		25	ns
10	t_{HZ2}	SEL to Output in HIGH-Z [4, 5]		10		12		15		20		25	ns
11	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		8		10		15		20		25	ns
12	t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns

* Available in Commercial Only.
NOTE: t_{CO2}, t_{LZ2} and t_{HZ2} apply to DPS128M8CnY/DPS128X8CA3 version only.

READ CYCLE



NOTE: SEL, t_{CO2}, t_{LZ2} and t_{HZ2} apply to DPS128M8CnY/DPS128X8CA3 version only.

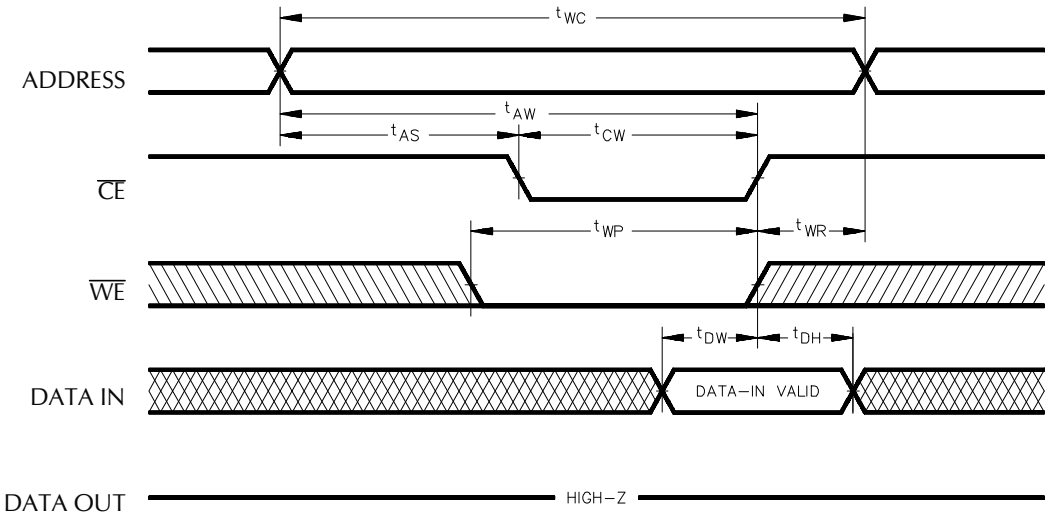
WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6, 7]: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	20		25		30		35		45		ns
14	t_{AW}	Address Valid to End of Write	15		20		25		30		40		ns
15	t_{CW}	Chip Enable to End of Write	15		20		25		30		40		ns
16	t_{AS}	Address Set-Up Time **	0		0		0		0		0		ns
17	t_{WP}	Write Pulse Width	15		20		25		30		35		ns
18	t_{WR}	Write Recovery Time	0		0		0		0		0		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		8		10		12		15		20	ns
20	t_{DW}	Data to Write Time Overlap	12		15		15		20		25		ns
21	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
22	t_{OW}	Output Active from End of Write	3		3		3		3		3		ns

* Available in Commercial Only.
** Valid for both Read and Write Cycles.

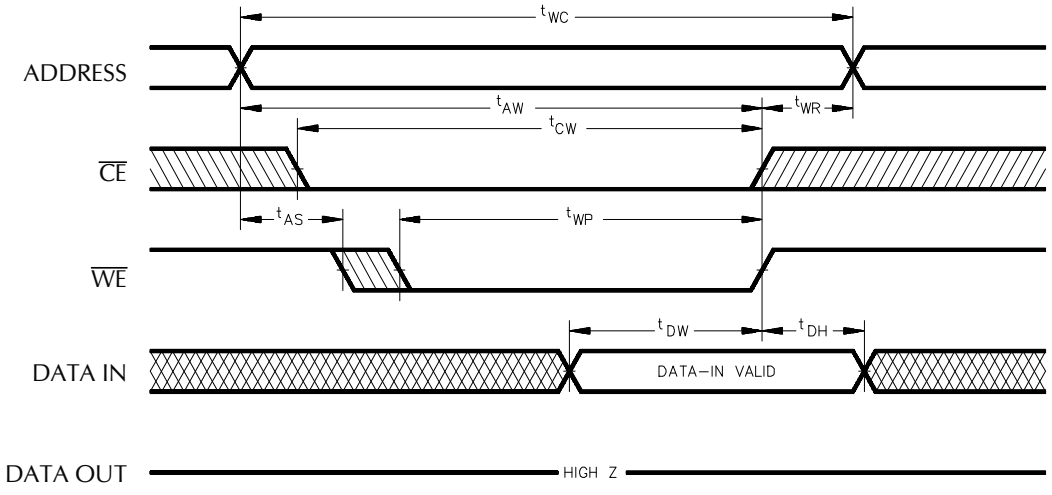
WRITE CYCLE 1: $\overline{CE}$ Controlled. [8]



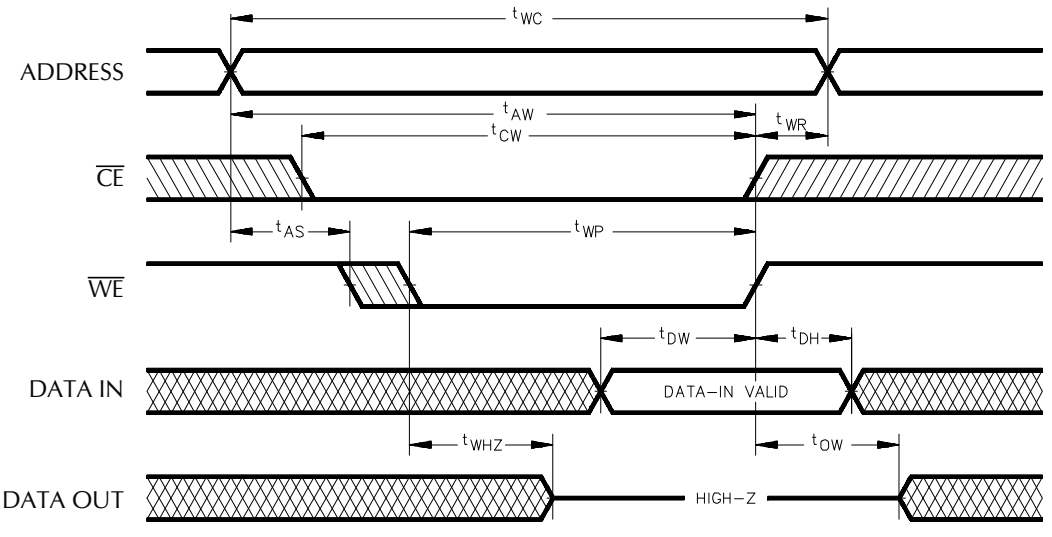
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. SEL timing is the same as $\overline{CE}$ timing (Valid for DPS128M8CnY/DPS128CA3 only). The Waveform is inverted.
9. Chip Enable and Write Enable can initiate and terminate WRITE Cycle.

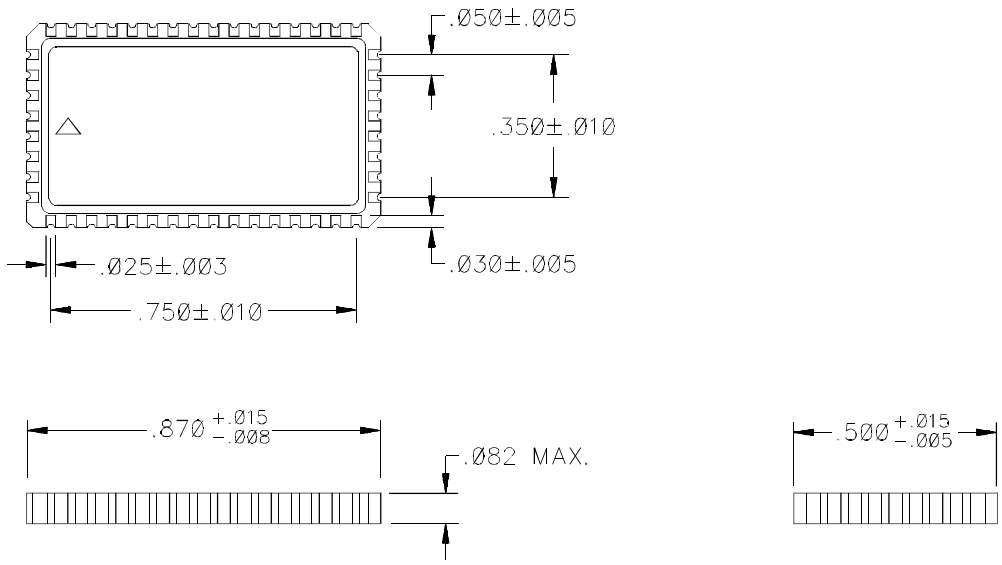
WRITE CYCLE 2: $\overline{WE}$ Controlled. $\overline{OE}$ is HIGH. [8, 9]



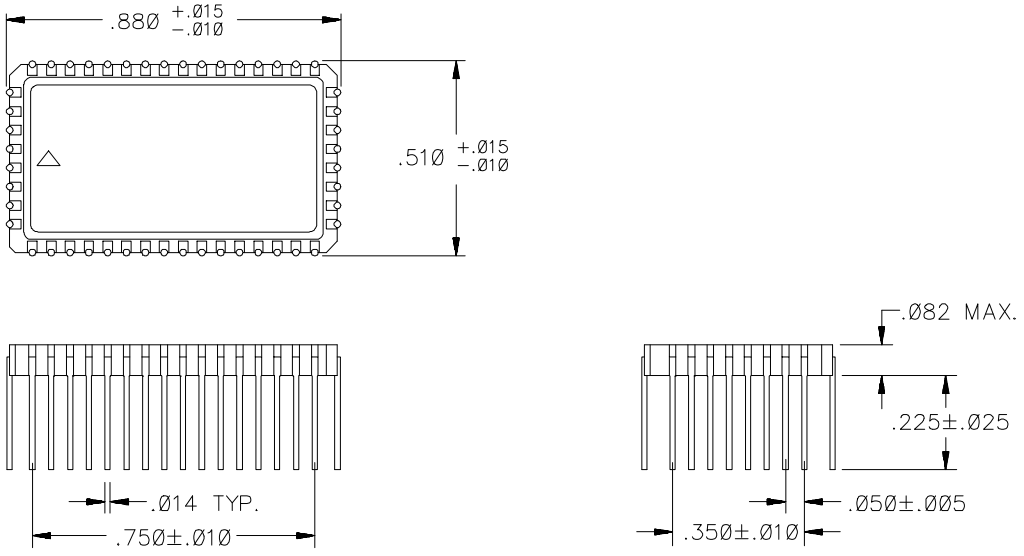
WRITE CYCLE 3: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW. [8, 9]



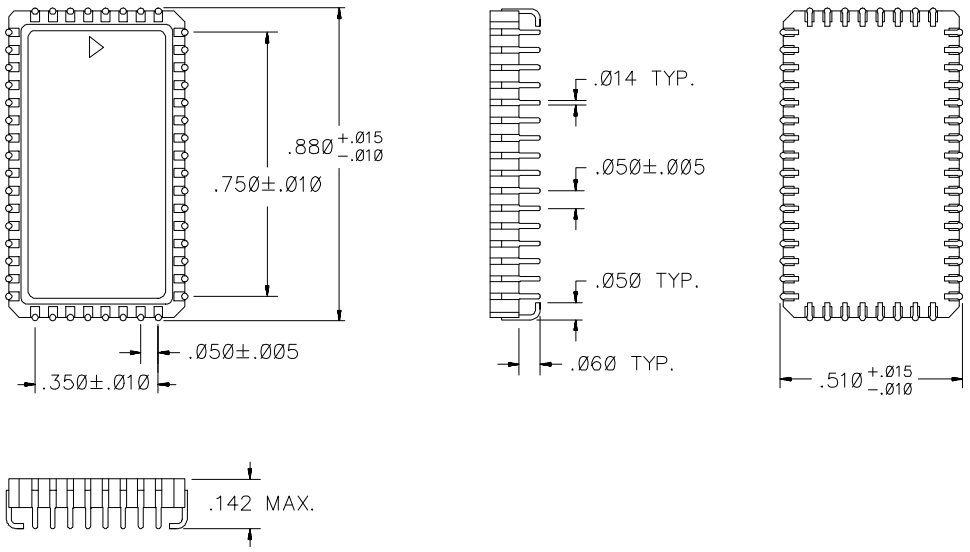
(48 - PIN LEADLESS SLCC) MECHANICAL DRAWING



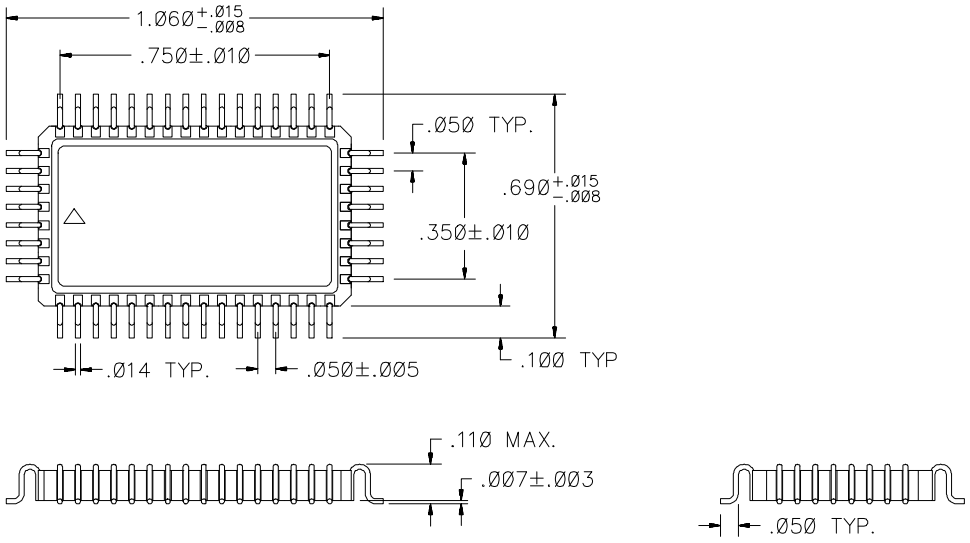
(48 - PIN STRAIGHT LEADED SLCC) MECHANICAL DRAWING



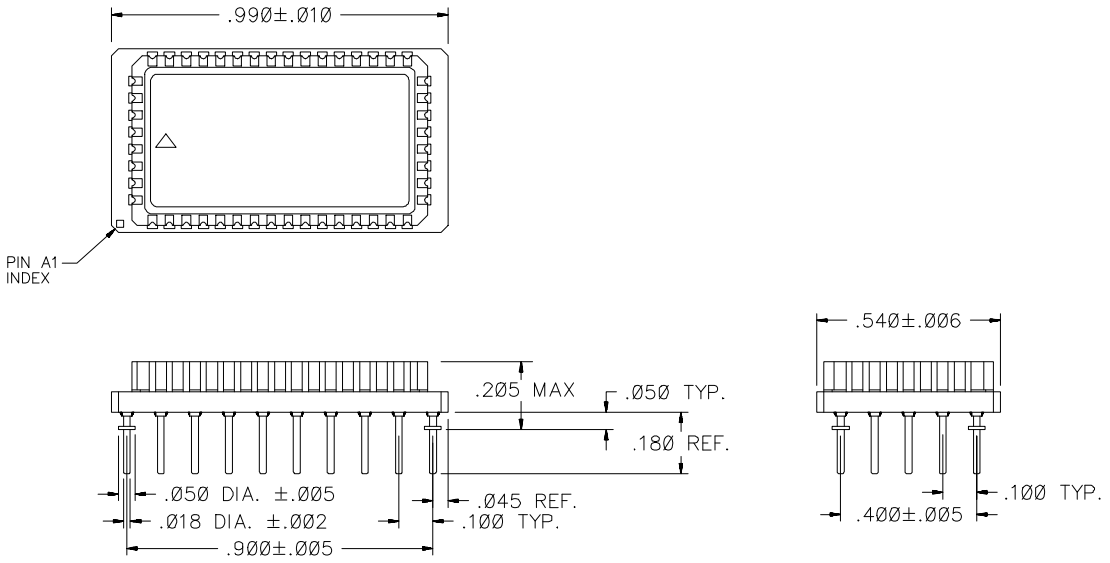
(48 - PIN "J" LEADED SLCC) MECHANICAL DRAWING



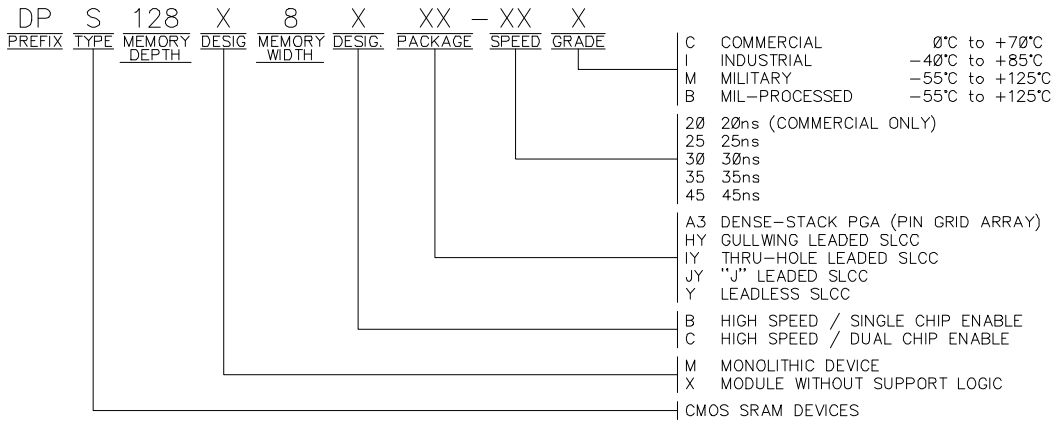
(48 - PIN GULLWING LEADED SLCC) MECHANICAL DRAWING



(50 - PIN PGA) MECHANICAL DRAWING



ORDERING INFORMATION



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