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MA9000 Series

SILICON-ON-SAPPHIRE RADIATION HARD GATE ARRAYS

The logic building block for the GPS double level metal CMOS/SOS gate arrays is a four transistor 'cell-unit' equivalent in size to a 2 input NAND gate. Back to back cell-units as illustrated, organised in rows, form the core of the array

The interconnection patterns that cause groups of cell units within a row, to become defined logic cells, and the models which are used to simulate these cells, are stored as software in LIBRARIES. Cells up to the complexity of, say, multiple bit shift registers are treated in this way.

Higher complexity functions are described by MACROS as the interconnection of defined cells. Macros are 'hard', 'soft', or 'firm' according to the constraints that are applied to the distribution of the component cells within the array and whether the full function is simulated by a model or by the additive effects of the component cells.

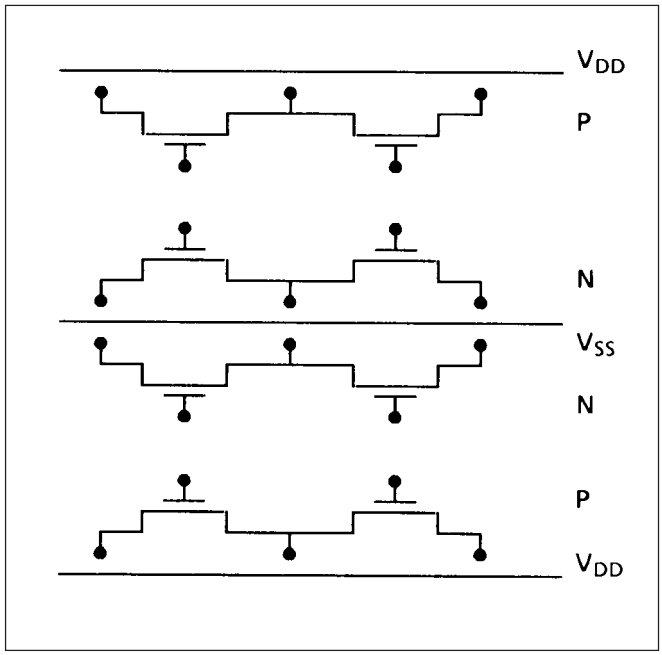

Figure 1: Cell Unit

FEATURES

- Radiation Hard to 1MRad(Si)
- High SEU Immunity, Latch-Up Free
- Double-Level-Metal CMOS/SOS Technology
- 2.5 Micron Design Rules
- Typical Gate Delay 1.2nS With 2 Loads, 60MHz Toggle Speeds
- Comprehensive Library of Logic Cells and Logic Function Building Macros
- 100% Automatic Place and Route for Typically 70% Utilisation

ARRAY OPTIONS

Array Type	Cell Units	Bonding Pads		
		I/O	Power	Total
MA9007	748	46	2	48
MA9024	2484	80	4	84
MA9040	4048	102	4	106

Each cell-unit is equivalent to a 2 input NAND gate.

Any I/O site may be configured as a power pad to give flexible bonding options, but to standardise testing, preferred positions exist.

CHARACTERISITICS & RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	˚C
T_S	Storage temperature	-65	150	˚C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification. is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	V
V_{IH2}	CMOS input high voltage	-	80	-	-	$\%V_{DD}$
V_{IL2}	CMOS input low voltage	-	-	-	20	$\%V_{DD}$
V_{OH1}	TTL output high voltage	I_{OH} = -2mA	2.4	-	-	V
V_{OL1}	TTL output low voltage	I_{OL} = 5mA	-	-	0.4	V
V_{OH2}	CMOS output high voltage	I_{OH} = -4mA	90	-	-	$\%V_{DD}$
V_{OL2}	CMOS output low voltage	I_{OL} = 4mA	-	-	10	$\%V_{DD}$
I_L	Input leakage current	-	-	-	10	µA
I_{OZ}	Output leakage current	Tristate Output	-	-	30	µA
I_{DD}	Power supply current	-	-	0.1	*	mA

V_{DD} = 5V ±10%, over full operating temperature.

* Dependent on array type.

Table 2: Electrical Characteristics

AC CHARACTERISTICS

Cell Name	Function	O/P Edge	Inherent Delay	Per 1pF Load*	Units
NOP	Push/Pull Output Buffer	Rising	0.5	0.4	ns
		Falling	0.3	0.2	
NOR2	2 Input NOR	Rising	1.6	13.6	ns
		Falling	0.8	5.0	
RDT	Reset D Type	Rising CK - QB	4.6	13.7	ns
		Falling CK - QB	7.8	13.6	
		Data Set-up time	7.1	-	
		Data Hold time	4.4	-	

* 1pF is equivalent to fanout of 5 standard gates

Table 3: Electrical Characteristics

PROPAGATION DELAY

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 60% of those listed.

Use the following normalised graphs to obtain converstion factors to predict delays at any other working temperature or voltage:

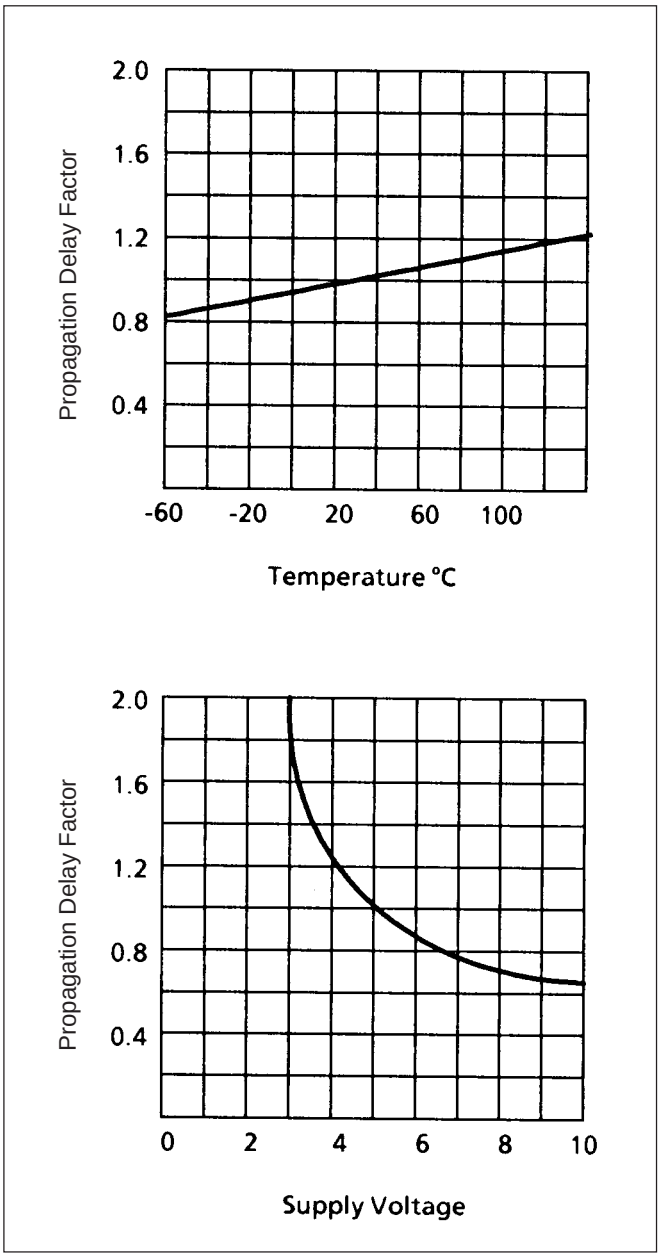

Figure 2: Propogation Delay vs Temperature & Propogation Delay vs Supply Voltage

PACKAGE OPTIONS

	MA9007 196 x 129	**MA9024** 247 x 240	**MA9040** 301 x 302
DIL14	X		
DIL16	X		
DIL20	X		
DIL24	X	X	
DIL28	X	X	
DIL40	X	X	
DIL48		X	X
DIL64		X	X
LCC28	X		
LCC40	X	X	
LCC44	X		
LCC48		X	X
LCC68		X	X
LCC84		X	X
FPK16	X		
FPK20	X		
FPK24	X		
FPK28	X	X	
FPK64		X	X
FPK68		X	X
FPK84		X	X
PGA68		X	X
PGA84		X	X
PGA120		X	X
PGA144		X	X

DIL = Dual in line
LCC = Leadless chip carrier
FPK = Leaded flatpack
PGA = Pin grid array

These are standard packages. If your package requirement is not shown above, discuss other options with an applications engineer.

RADIATION TOLERANCE

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GPS can provide radiation testing compliant with MIL-STD-883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request
** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 4: Radiation Hardness Parameters

CELL LIBRARY QUICK GUIDE

Cell Name	Function	Cell Units
COMBINATIONAL GATES		
INV	Inverter	1
DUALINV	Dual inverter	1
INVB	Fast inverter	1
INVC	Super fast inverter	2
BUFF	Non-inverting buffer	1
BUFFB	Fast non-inverting buffer	2
BUFFC	Super fast non-inverting buffer	3
NAND2	2 input NAND	1
NAND2B	Fast 2 input NAND	2
NAND3	3 input NAND	2
NAND4	4 input NAND	2
NAND8	8 input NAND	6
NAND12	12 input NAND	8
NAND16	16 input NAND	11
AND2	2 input AND	2
AND3	3 input AND	2
AND4	4 input AND	3
NOR2	2 input NOR	1
NOR2B	Fast 2 input NOR	2
NOR3	3 input NOR	2
NOR4	4 input NOR	2
NOR8	8 input NOR	6
NOR12	12 input NOR	8
NOR16	16 input NOR	11
OR2	2 input OR	2
OR3	3 input OR	2
OR4	4 Input OR	3
ANDNOR	2 + 2 input AND/NOR	2
ANDOR	2 + 2 input AND/OR	3
ORNAND	2 + 2 OR/NAND	2
ORAND	2 + 2 OR/AND	3
A2N01	2 + 1 Input AND/NOR	2
A201	2 + 1 input AND/OR	2
02NA1	2 + 1 input OR/NAND	2
02A1	2 + 1 input OR/AND	2
EXNOR	Exclusive NOR	3
EXORN	Exclusive OR	3
SEL21NV	Select 1 of 2 (inverting)	3
SEL2	Select 1 of 2	3
SEL41NV	4 bit data selector (inverting)	6
SEL4	4 bit data selector	7

Cell Name	Function	Cell Units
DECODERS		
DEC2T4	2 to 4 line decoder	6
DEC3T8	3 to 8 line decoder	11
DEC4T16	4 to 16 line decider	40
ARITHMETIC		
HAD	Half adder	5
FAD	Full adder	8
FLAD	Fast look ahead adder	6
LAH2	2 bit look ahead unit	10
LAH3	3 bit look ahead unit	14
LAH4	4 bit look ahead unit	24
ADD4	4 bit look ahead adder	50
ADD8	8 bit look ahead adder	106
SIMPLE LATCHES		
NASR	NAND set reset-latch	3
NOSR	NOR set-reset latch	3
TRANSPARENT LATCHES		
DL	D-latch (Active low)	4
DLH	D-latch(Actlve high)	4
SDL	Set D-latch	4
RDL	Reset D-latch	4
SRDL	Set/reset D-latch	5
EDGE TRIGGERED LATCHES		
RETS	Latch with reset	7
SRETS	Latch with reset and set	8
MASTER-SLAVE FLIP-FLOPS		
DT	D-type	6
D2T	Dual input D-type	8
SDT	Set D-type	7
RDT	Reset D-type	7
SRDT	Set/reset D-type	8
JK	JK flip-flop	10
SDK	JK flip-flopwith set	11
RJK	JK flip-flop with reset	11
SRJK	JK flip-flop with reset and set	12
TOGGLE FLIP-FLOPS		
STT	Set T-type	7
RTT	Reset T-type	7
SRTT	Set/reset T-type	8
SYNCHRONOUS COUNTER		
SYNC	Synchronous counter stage	10

Cell Name	Function	Cell Units
REGISTERS / SHIFT REGISTERS		
SHRx	Multibit (x = 2-8) serial register	16-46
RSHRx	Multibit (x = 2-8) serial reg. with reset	18-54
DREGx	Multibit parallel register (x = 2-8)	8-22
DREGTx	Multibit parallel register (x = 2-8) with tri-state outputs	12-36
HPLSx	Half parallel loading shift registers (x = 2-8)	22-64
INVERTING TRI-STATE BUFFERS		
TRIBUFF	Tristate buffer (enable high)	2
TRIBUFFL	Tristate buffer (enable low)	2
TRINV	Tristate inv buffer (enable high)	2
TRINVL	Tristate inv. buffer (enable low)	2
INPUT OUTPUT AND PERIPHERAL CELLS		
DIP	Direct input (protection cicuit only)	
PUP	Pull up (approx 30 Kohms)	
PDO	Pull down (approx 40 Kohms)	
TSCHMITT	TTL compatible Schmitt	6
CSCHMITT	CMOS compatible Schmitt	6
CMOSIN	CMOS buffer (non-inverting)	1
TTLIN	TTL buffer (non-inverting)	3
NOP	Push/pull output buffer (inverting)	
WNOP	Multiple NOP	
BOP	Push/pull output buffer (non inverting)	
ZOP	Tri-state output buffer	
ODN	Open drain output pull down	
ODP	Open drain output pull up	
TRIOP	Tristate I/O buffer	4
BUSINT	Bus interface	6
STEPUP	Output Buffer	6
POWER SUPPLY PADS		
VDD	V_{DD} pad	
VSS	V_{SS} pad	

MACROS

The following Macros are included in the MA9000 library. GPS are constantly adding new Macros to the library, please contact our nearest office for information on the latest additions.

Macro name	Macro name
ACOUNTn	Asynchronous counters
ALU4	ALU
GCOUNTn	Gray counters
JCOUNTn	Johnson counters
LADDn	Lookahead adders
MCOMPn	Magnitude comparators
PARITYn	Parity detectors
RADDn	Ripple carry adders
SEL8	Select 1 of 8
SEL16	Select 1 of 16
M2901	4 bit slice microprocessor
M2909	4 bit microprogram controller
M2902	Look ahead carry unit
M2910	12 bit microprogram sequencer
M2918	Pipeline register

DEVELOPMENT INTERFACES

Circuit design, captive and simulation activities are carried out by the customer. Schematic capture and simulation libraries for Dazix and Mentor Graphics CAE systems are provided by GPS. GPS will accept a simulated design and perform layout, verification checks and PG. GPS will then procure masks and fabricate and test parts prior to prototype delivery. The MA9000 arrays fall within the ESA capability domain.

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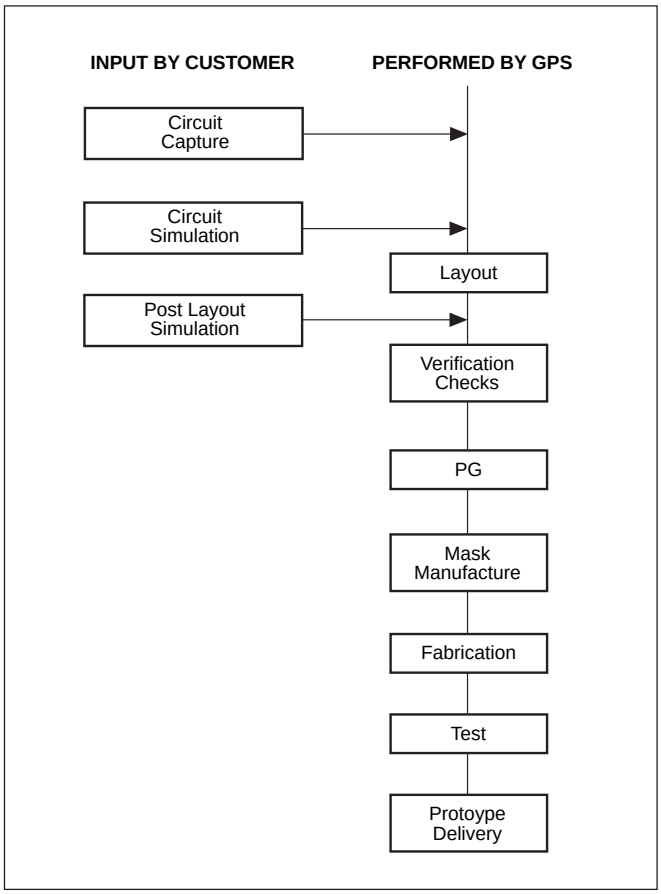
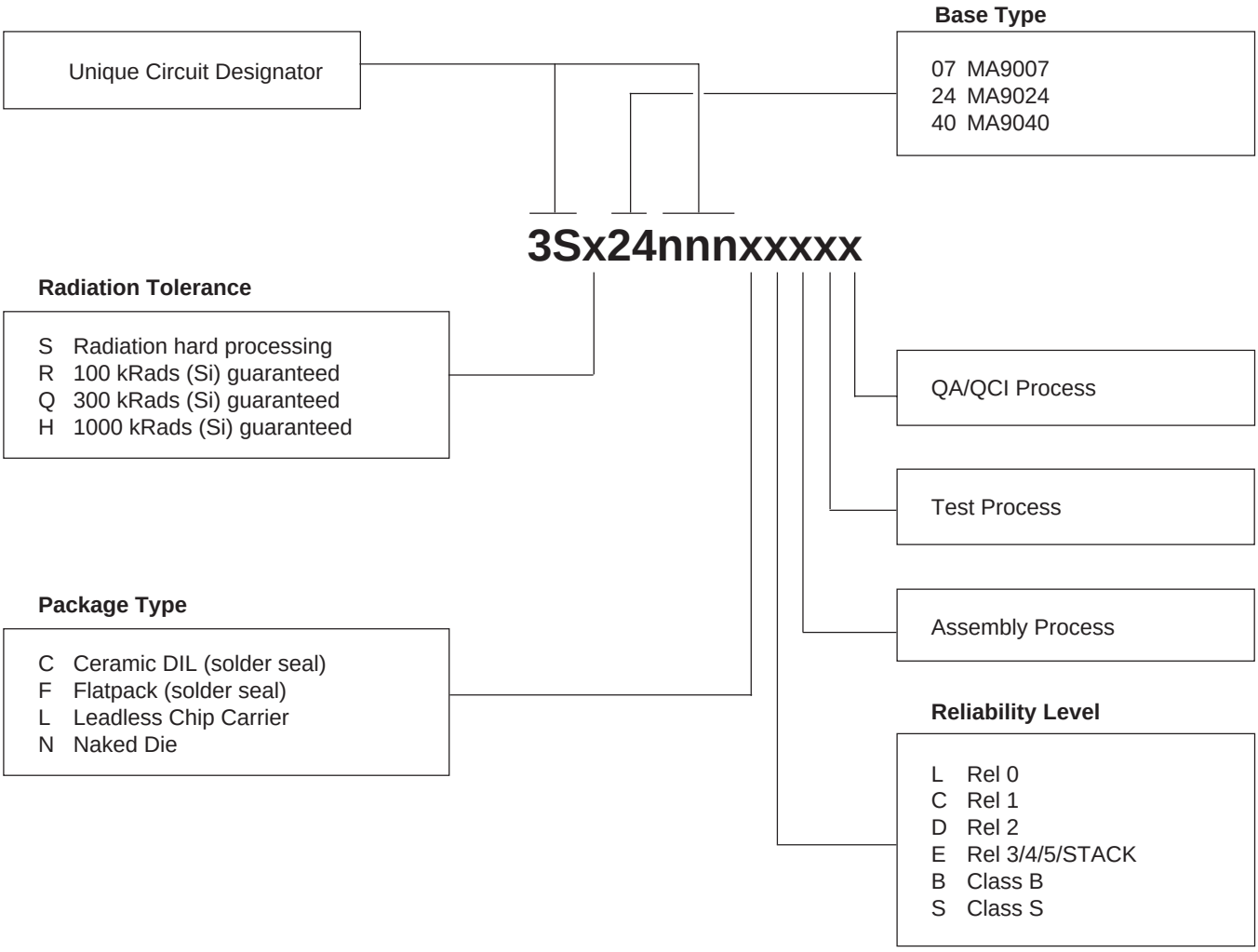


Figure 3: Development Interfaces

ORDERING INFORMATION

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards'.



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 Publication No. DS3598-3.4 May 1995

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