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SSI 32H6210
Servo Demodulator

Preliminary Data

February 1992

DESCRIPTION

The SSI 32H6210 Servo Demodulator is a bipolar device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H101 or SSI 32H116, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H6210 and its companion devices, the SSI 32H6220 Servo Controller and SSI 32H6230 Servo Motor Driver.

The SSI 32H6210 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse area detectors to recover the position information. External components are used to set the operating characteristics of the SSI 32H6210, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 400 kHz.

FEATURES

- **Servo signal demodulation for dedicated surface head positioning systems**
- **Supports industry standard di-bit quadrature servo pattern with frame rates up to 400 kHz**
- **N, Q outputs convey track crossing and position error information**
- **PLL for timing recovery and synchronization**
- **Adjustable sync separator threshold**
- **Auto-zeroing AGC input amplifier**
- **AGC reference level adjustment**
- **Precision bandgap voltage reference output**
- **Advanced bipolar process dissipates less than 900 mW (5V, 12V)**
- **Available in 28-pin PLCC, DIP, SO packages**

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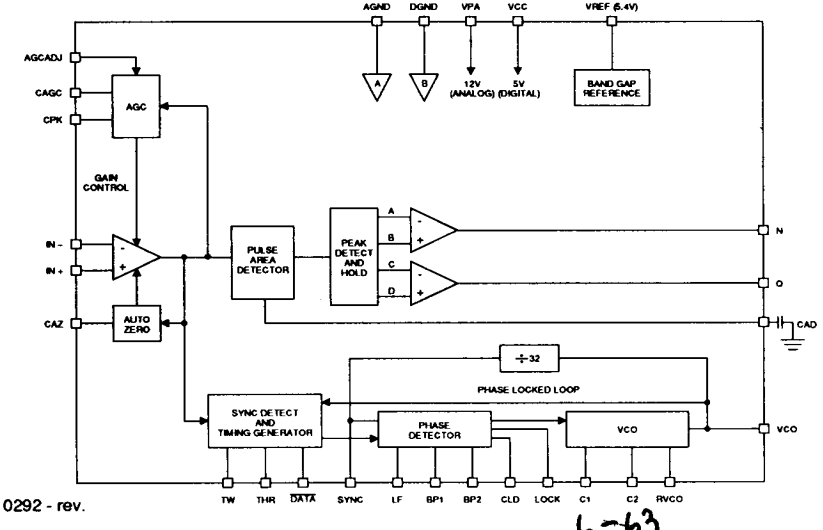
BLOCK DIAGRAM



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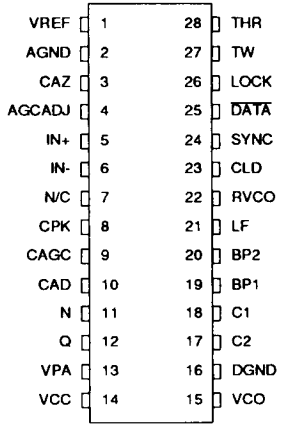
PIN DIAGRAM



28-PIN
DIP, SO

FUNCTIONAL DESCRIPTION

(Refer to block diagram, and typical application, Fig.2)

The SSI 32H6210 processes servo position information which is read from a dedicated surface by a pre-amplifier. The servo information must conform to the 'di-bit quadrature' pattern which is illustrated in Figure 4. Servo frames, consisting of data and sync pulses followed by four information pulses (A, B, C, D) are prerecorded along each track of the servo surface. All the servo frames on an individual track are identical, but in the radial direction four different frame types are encountered, with every fourth track being identical. The N signal generated by the SSI 32H6210 is proportional to the difference in sizes of pulses A and B, while the Q signal is proportional to the difference between pulses C and D. When the read head is off track, the read signal is effectively a linear interpolation between the prerecorded information of two adjacent tracks, making it possible to sense the head displacement exactly.

The SSI 32H6210 has a differential input amplifier which incorporates offset voltage cancellation and automatic gain control. An external read preamplifier must provide a differential input signal of 23 to 400 mV peak to peak from the servo read head. This signal is applied to a pulse detector whose output is proportional to the area under the input pulse.

An AGC circuit adjusts the input gain so that the maximum pulse detector output is 2V peak. The AGC circuit incorporates a peak detector which stores the maximum pulse area signal on the external capacitor C_{PK}. This signal is compared to an internal amplitude reference and the input amplifier gain is adjusted until they are equal. The capacitor C_{AGC} determines the response time of the gain control circuit. An offset cancellation circuit , whose response is set with the external capacitor C_{AZ}, ensures that the average level at the differential amplifier output is zero.

An AGC adjust (AGCADJ) pin allows the user to adjust the AGC reference level. AGCADJ can be driven with a potentiometer or a D/A (a simple Pulse Width Modulated signal is usually sufficient.) This pin is left open if no AGC adjustment is required.

All internal analog signals are referenced to a 5.4V bandgap reference voltage. This level is available at the VREF output, which is capable of supplying 10 mA to the rest of the servo path electronics.

In a standard servo frame, the data and sync pulses are more closely spaced than the information pulses (A-D). This allows the sync detect circuit to recover the SYNC pulses. A threshold, which is defined as percentage of the peak signal at the output of the AGC amplifier, is set externally with R_{TH}. Pulses which exceed this threshold are defined as valid pulses. As illustrated in Figure 6, at the end of the positive going half of a valid pulse, a window, whose width is set by Rw and Cw, is opened. If a second valid pulse occurs within this window, it is recognized as a SYNC pulse. This pulse becomes the input signal to a phase locked loop whose VCO clock frequency is 32 times the SYNC frequency (servo frame rate). The $\overline{DATA}$ output rises after a missing data pulse. The example illustrated in Figure 6 includes the case of a missing DATA pulse. The SYNC clock output, which marks the start of a new servo frame, is derived from the VCO output so that the clock continues to run when a data pulse is missing. Absolute positioning information such as track 0 and guardband flags may be encoded on the servo surface by the omission of data pulses.

To generate the servo pattern shown in the timing diagram, Figure 5, the DATA and SYNC pulses must be written to overlap as shown in Figure 7.

The phase detector compares the detected sync pulses with the SYNC output. A current pulse proportional to the phase error is applied to an external loop filter network connected to the LF pin, to generate the VCO control voltage. If improved power supply rejection is required, bypassing may be provided at pins BP1 and BP2. The VCO center frequency is determined by the external components R_{VCO} and C_{VCO}.

A lock detect circuit measures the phase difference between the detected sync pulses and the sync output. When this difference exceeds half of a VCO clock cycle, a pulse of discharge current is applied to CLD. Otherwise a pulse of charging current is applied to CLD.

A clamp circuit limits the swing of the CLD pin and also insures that a small amount of hysteresis is present. When the voltage on CLD falls below the upper clamp level by more than the "lock margin," the open collector LOCK output transistor is turned on. Likewise, when the voltage on CLD rises above the lower clamp level by more than the "unlock margin," the LOCK output transistor is turned off.

FUNCTIONAL DESCRIPTION (Continued)

Internal timing windows are generated from the recovered SYNC pulse and VCO clock. These windows, WA, WB, WC, and WD, in Figure 5, enable the four peak detectors to capture the A, B, C and D information pulses. The N and Q analog outputs are formed by differencing adjacent pulses. These outputs change during a servo frame and only become valid after the D pulse has been detected. N and Q should be sampled by the servo controller on the next falling edge of the SYNC output clock.

An example of an entire servo path implemented with the SSI 32H6210 and its companion devices, the SSI 32H6220 and SSI 32H6230, is shown in Figure 9.

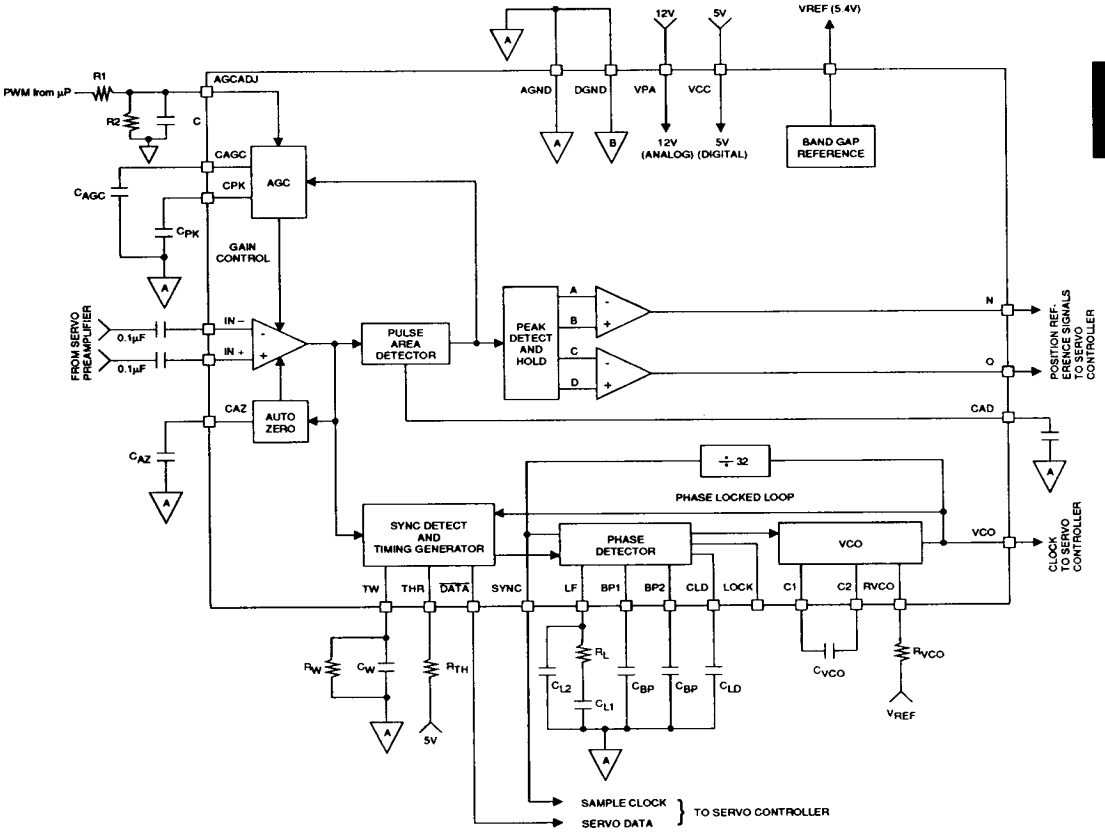


FIGURE 2: Typical Application

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VREF	O	REFERENCE VOLTAGE - 5.4V output. All analog signals are referenced to this voltage.
AGND	-	ANALOG GROUND
VPA	-	ANALOG SUPPLY - 12V power supply.
VCC	-	DIGITAL SUPPLY - 5V power supply.
DGND	-	DIGITAL GROUND

INPUT AMPLIFIER

NAME	TYPE	DESCRIPTION
CAZ	-	AUTOZERO CAPACITOR - A capacitor which sets the response of the input amplifier offset cancellation circuit should be connected between this pin and analog ground.
IN +	I	NON-INVERTING INPUT - AGC input amplifier connection. The non-inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
IN -	I	INVERTING INPUT - AGC input amplifier connection. The inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
CPK	-	PEAK HOLD CAPACITOR - A capacitor which is used by the peak detector of the AGC circuitry must be connected between this pin and analog ground.
CAGC	-	AGC CAPACITOR - A capacitor which sets the AGC attack and decay times must be connected between this pin and analog ground.
AGCADJ	I	AGC Adjust - This pin allows for AGC reference level adjustment. It is driven by a potentiometer or D/A. Normally this pin is left open.

TIMING RECOVERY

NAME	TYPE	DESCRIPTION
VCO	O	VCO OUTPUT - TTL compatible digital clock which is 32 times the sync frequency (servo frame rate).
C2,C1	-	VCO CAPACITOR - Connection points for a capacitor which sets the VCO center frequency in conjunction with an external resistor connected to RVCO.
BP1,BP2	-	PLL BYPASS - Bypass capacitors may be connected between these pins and analog ground to provide additional power supply rejection in the phase locked loop.

TIMING RECOVERY (Continued)

NAME	TYPE	DESCRIPTION
LF	-	PHASE LOCKED LOOP FILTER - An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
RVCO	-	VCO RESISTOR - Connection for a resistor which sets the VCO center frequency, in conjunction with the capacitor between pins C1 and C2. The resistor must be connected between this pin and the VREF output.
SYNC	O	SYNC OUTPUT - TTL compatible digital clock whose falling edge indicates the presence of valid analog signals on the N and Q outputs. There is one SYNC cycle per servo frame.
$\overline{\text{DATA}}$	O	DATA OUTPUT - Active low TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the SYNC output.
TW	-	TIMING WINDOW - A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses.
THR	-	PULSE THRESHOLD - A resistor which sets a threshold for SYNC and $\overline{\text{DATA}}$ pulse detection must be connected between this pin and VCC (digital 5V supply).
CLD	-	LOCK DETECT CAPACITOR - The value of this capacitor determines how quickly the LOCK output responds (1000 pF).
LOCK	O	LOCK OUTPUT - An open collector output that indicates the lock status of the PLL.

POSITION INFORMATION

NAME	TYPE	DESCRIPTION
CAD	-	AREA DETECTOR CAPACITOR - A capacitor, which forms an integrator to sense the pulse area of the servo position signals, must be connected between this point and analog ground.
N	O	N OUTPUT - This sampled analog signal is the normal position reference output. N is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks.
Q	O	Q OUTPUT - This sampled analog signal is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks. It is 90 degrees out of phase with N.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC voltage		0		8	V
VPA voltage		0		16	V
Voltage on PLL inputs		-0.5		VCC+0.5	V
Voltage on other inputs		0		14	V
Storage Temp.		-45		160	°C
Solder Temp.	10 sec. duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VPA, analog supply		10.8	12	13.2	V
Supply noise	F<1 MHz			0.1	Vpp
VCC, digital supply		4.75	5	5.25	V
Ta, ambient temperature		0		70	°C
VCO operating range				12.8	MHz
Load resistance	To VREF	10			kΩ
Load capacitance				50	pF

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IPA, VPA current				50	mA
ICC, VCC current				60	mA
VOH, digital output high	|IOH|<40 µA	2.4			V
VOL, digital output low	|IOL|<1.6 mA			0.5	V
IREF, VREF output current capacity		10			mA
VREF output voltage	|IREF|<10 mA	5.1	5.4	5.7	V

ELECTRICAL SPECIFICATIONS (Continued)

AC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VREF output impedance	IOUT = 0-10 mA 1 µF bypass to AGND Frequency<15MHz			12	Ω
N, Q outputs					
Output impedance	F = 1 MHz			100	Ω
Voltage per track	Referenced to VREF 23-400 mVpp differential AGCADJ open	1.8	2	2.2	V
Offset voltage				20	mV
Output noise	10 Hz<F<1 kHz		-55		dBV
Input amplifier					
Input resistance		5			kΩ
Input resistance mismatch				1	%
Input capacitance				20	pF
PSRR	F<0.5MHz	35			dB
AGC headroom		2			dB
AGC bandwidth	Open loop unity gain C_{AGC}=0.04 µF C_{PK}=1500 pF	5		15	kHz
Autozero pole	C_{AZ} in µF		220/C_{AZ}		Hz
AGCADJ					
Open circuit voltage		0.7	0.76	0.82	V
Gain		-1.6	-1.4	-1.2	V/V
Volts per track adj range		1.0		2.6	V
Input impedance, R_{AGC}	Ta = 25°C	4	5.5	7	kΩ
	Temp. coefficient		2600		ppm/°C
SYNC detector					
Timing window	Rw in Ω, Cw in pF		$0.4(Rw \cdot Cw) + 43 \cdot 10^{-9}$		s
Valid pulse threshold	R_{TH} in kΩ (% of full scale)		0.37/R_{TH}		%

ELECTRICAL SPECIFICATIONS (Continued)

AC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOCK Detector					
CLD up current	RVCO = 11K ± 1%	0.7		3	µA
CLD down current	RVCO = 11K ± 1%	3		10	µA
CLD lock margin		0.5		1.3	V
CLD unlock margin		0.5		1.3	V
CLD hysteresis		75		400	mV
Phase locked loop					
Capture range	Centered on selected f_{NOM}	±5			%
VCO phase shift	Missing DATA pulse			0.005	rad/frame
VCO phase delay	Relative to sync pulse zero crossing			70	ns
VCO gain	fvco in Hz		10.47 fvco		rad/s/V
Phase detector gain			32		uA/rad

TIMING CHARACTERISTICS
(Digital output load capacitance Cl<15 pF, VCO frequency f_{VCO} <12.8 MHz, timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TDD, data delay				30	ns
TW, sync pulse width		40			ns
TSKW, SYNC to VCO skew		0		40	ns
SYNC fall time				20	ns
TADS, N or Q output settling time				260	ns
TADH, N or Q output hold time		0			ns

APPLICATIONS INFORMATION

A typical SSI 32H6210 application is shown in Figure 2. The selection criteria for the external components shown are discussed below.

INPUT AMPLIFIER

The autozero circuit is effectively a high pass filter, whose pole frequency is given by:

$$f_{AZ} = \frac{220}{C_{AZ}(\mu F)} Hz$$

With a value of 10 µF for C_{AZ}, the autozero circuit's corner frequency will be 22 Hz. This is sufficient for DC offset rejection and it will not interfere with the servo signal.

The AGC response may be characterized in terms of the open loop unity gain bandwidth of its control loop. The nominal value for this loop is set by C_{AGC} as follows:

$$f_{BW} = \frac{390}{C_{AGC}(\mu F)} Hz$$

For a nominal bandwidth of 10 kHz, C_{AGC} should be 0.039 µF. With a 1% capacitor, the variation in actual bandwidth will be +/- 50% due to the tolerance of internal components. The AGC peak detector capacitor should always be set to 1500 pF. This represents a reasonable tradeoff between leakage current tolerance and storage aperture time.

The pulse area detector storage capacitor must be chosen to keep the AGC circuit operating within its linear range. Its value is related to the VCO frequency as follows:

$C_{AD} = \frac{620}{fvco(MHz)}$ pF, where fvco is the VCO freq.

Larger values for CAD are required with lower VCO frequencies in order to maintain constant signal levels within the device, since the integration time is increased.

$$K = 2\frac{V_{AGCADJ}(typ)}{VCC(min)} \qquad dv = \frac{\Delta V}{AGCADJGain(max)}$$

$$R1 = \frac{R_{AGC}(min)}{K}\left(\frac{V_{AGCADJ}(min)}{dv} - 1\right)$$

$$R2 = \frac{K}{1-K}(R1)$$

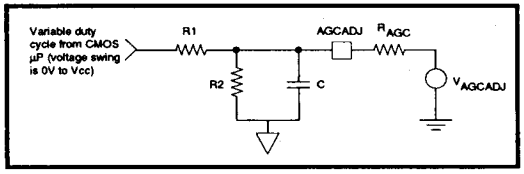


FIGURE 3: AGCADJ Input

for example if: $\Delta V = 0.4V$, $VCC = 5V \pm 5\%$, $Ta = 0\text{-}70°C$
$VREF = 5.4V \pm 6\%$

then: $K = .318$, $dv = 0.26V$, $R1 = 20.4k$,
$R2 = 9.5k$

The amplitude of N & Q signals can be adjusted using the AGCADJ input. If it is desired to adjust the N & Q amplitude by $\pm \Delta V$ volts, the values of R1 and R2 can be calculated from K and dv as shown in figure 3.

When R1 & R2 are calculated, a filter capacitor C is calculated from the replication rate of the µP duty cycle output. The parallel combination of R1, R2, R_{AGC} minimizes the ripple of V_{AGC}, and yet still provides sufficient response time to changes in duty cycle.

SYNC DETECTOR

Two sync detector parameters may be adjusted with external components. The first is the valid pulse threshold. The threshold is expressed as a percentage of a full scale pulse (since the sync detector follows the AGC and input amplitude variations are removed). The threshold is determined with resistor R_{TH} as follows:

$$Threshold = \frac{0.44}{R_{TH}(k\Omega)} \cdot 100(\%)$$

For example, a value of R_{TH} = 1.0 kΩ sets the valid pulse threshold at 44% of full scale. This prevents false triggering on noisy signals, but does not unduly shorten the sync pulse.

A timing window is used to detect sync pulses, since the sync and data pulses are more closely spaced than any other pulses in a valid servo signal. The delay from the zero crossing of the data pulse to the leading edge of the sync pulse is 1.5 cycles of the VCO clock. The next most closely spaced pulses (which must be rejected by the sync detect circuit) are separated by 3

APPLICATIONS INFORMATION (Continued)

SYNC DETECTOR (Continued)

VCO cycles. Thus the timing window should be set for 2 cycles of the VCO clock, to allow reliable detection of the sync pulse while suppressing false syncs. The timing window is determined as follows:

$$0.4\,(R_W \cdot C_W) + 43 \cdot 10^{-9}$$

The resistor Rw should always be set to 5.6 kΩ, which means that for a 2 cycle window, Cw is given by:

$$Cw = \frac{900}{fvco(MHz)} - 19pF$$

For a 12.8 MHz clock, Cw should be chosen as 51 pF.

LOCK DETECTOR

The LOCK detector behavior is controlled by the value of C_{LD}. A value too small will be prone to unlock prematurely and give false warnings to the system. A typical value for C_{LD} is 0.001µF.

PHASE LOCKED LOOP

The VCO center frequency is determined by Rvco and Cvco. Rvco should always be set to 11 kΩ ± 1%. Cvco may then be chosen by:

$$Cvco = \frac{830}{f_{vco}} - 10.6\,pF,$$

where fvco is the desired center frequency in MHz.

For fvco = 12.8 MHz, Cvco = 54 pF and for fvco = 4 MHz, Cvco = 200 pF. If 1% tolerance external components are used, the VCO absolute frequency accuracy will be 15%. The VCO output frequency is related to the control voltage at the loop filter pin, V_{LF}, as follows:

$$fo/fvco = 1 + 1.667(V_{LF} - V_{BPI})$$

This means that the VCO gain, K_0, is given by:

$$K_0 = 2 \cdot \pi \cdot fvco(Hz) \cdot 1.667\ rads/s/V$$

The phase detector is a digitally controlled charge pump, which injects a current into the loop filter whose average value is proportional to the phase error. The detector gain, K_d, is fixed at 32 µA/rad. If a loop filter consisting of a series resistor and capacitor is used, as shown in Figure 2, the phase locked loop becomes a second order system with the following transfer function:

$$\frac{\text{phase error}}{\text{input phase}}(s) = \frac{(s/\omega n)^2}{1 + 2 \cdot \zeta \cdot s/\omega n + (s/\omega n)^2}$$

where:

$$\omega n\,(\text{natural freq.}) = \sqrt{((K_d \cdot K_0/(32 \cdot C_{L1}))}\ rad/s$$

$$\zeta(\text{damping factor}) = 0.5 \cdot R_L \cdot C_{L1} \cdot \omega n$$

As an example, the values for Cvco, R_L and C_L are

$$fvco = 12.8\,MHz,\ \omega n/(2 \cdot \pi) = 4600\,Hz,\ \zeta = 0.68$$

$$Cvco = \frac{830}{fvco} - 10.6 = 54pF$$

$$C_{L1} = \frac{K_d K_0}{32 \cdot \omega n^2} = \frac{(32 \cdot 10e-6)(10.47 \cdot f_{VCO})}{32(2 \cdot \pi \cdot 4600)^2} = .2\mu F$$

$$R_L = \frac{2 \cdot z}{C_{L1} \cdot \omega n} = 470\,\Omega$$

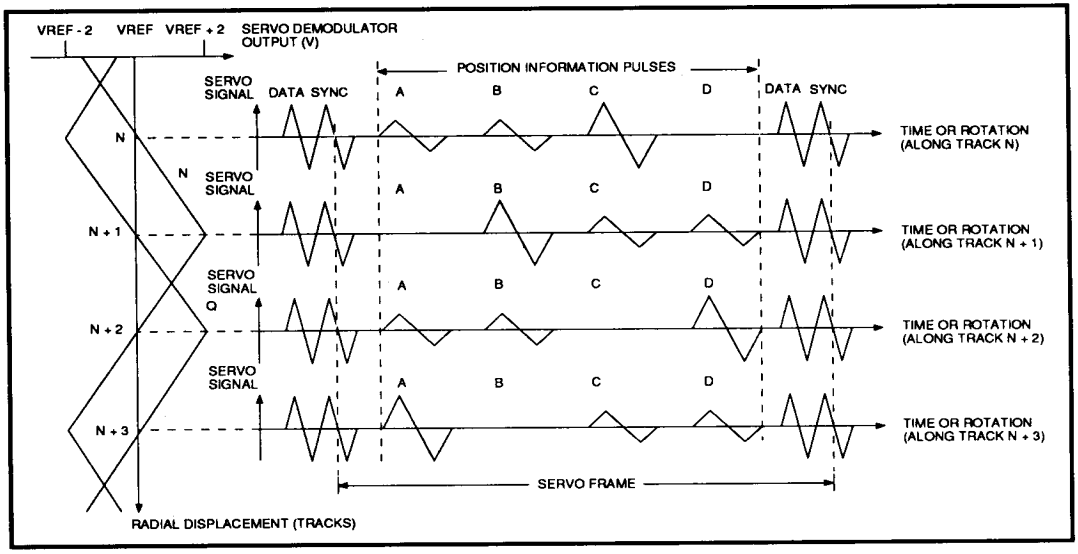


FIGURE 4: Pre-recorded Servo Signal and Servo Demodulator Output vs. Radial Displacement

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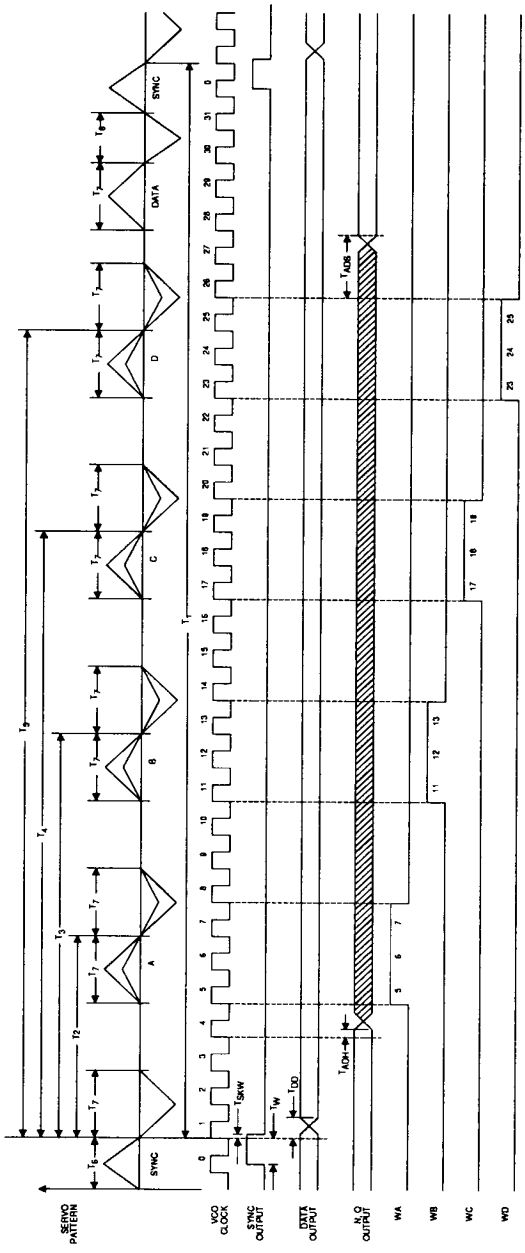


FIGURE 5: Timing Diagram

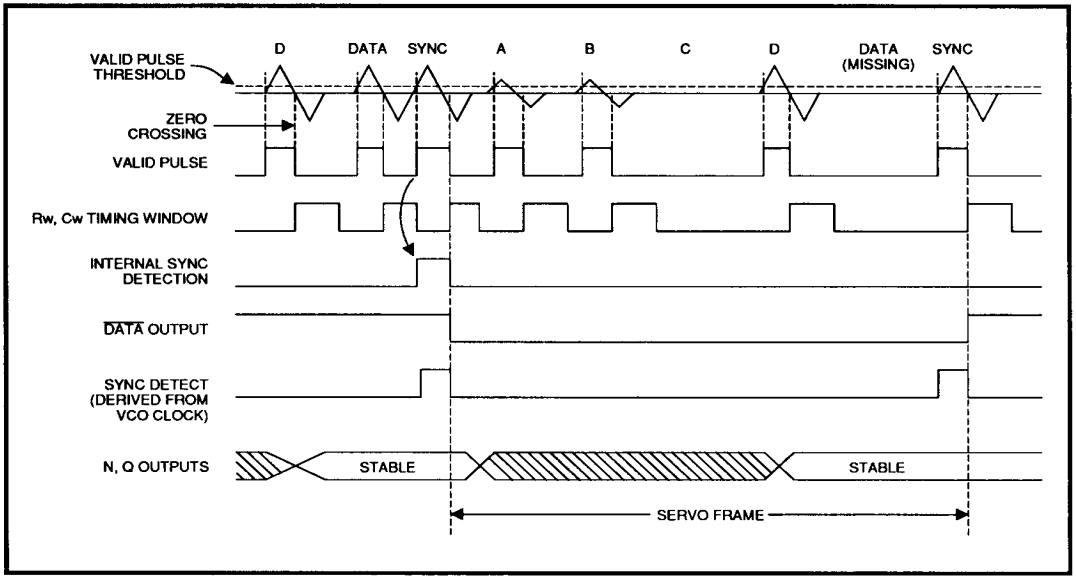


FIGURE 6 : Sync and $\overline{\text{DATA}}$ Pulse Detection

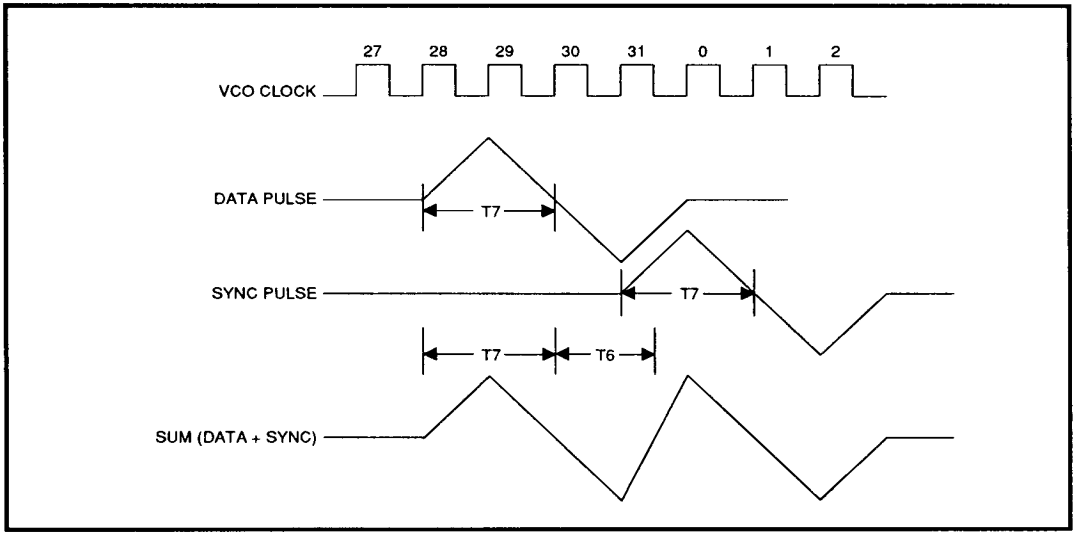


FIGURE 7 : Servo Writer Data-Sync Pulse Generation

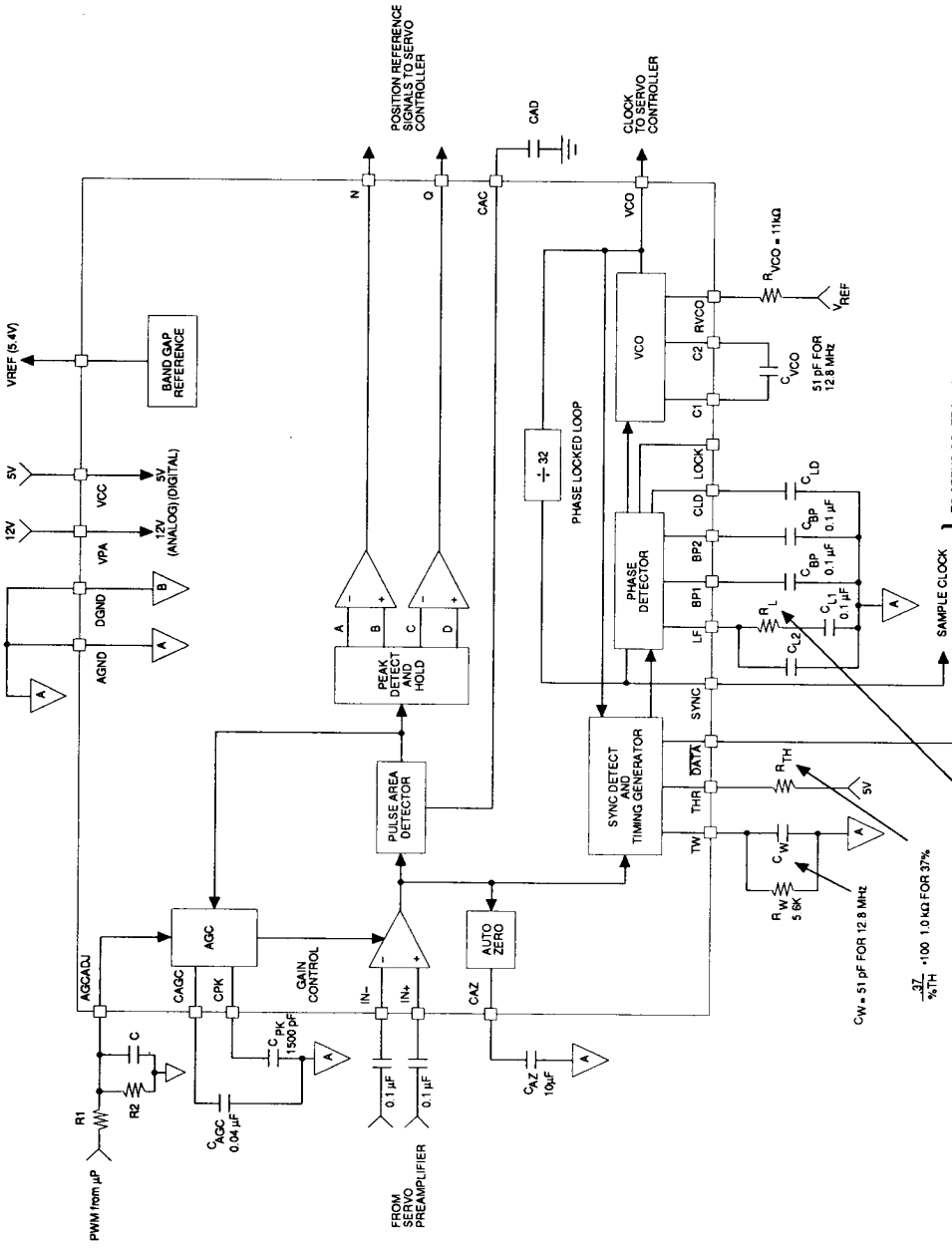


FIGURE 8: Design Example for 400 kHz Frame Rate

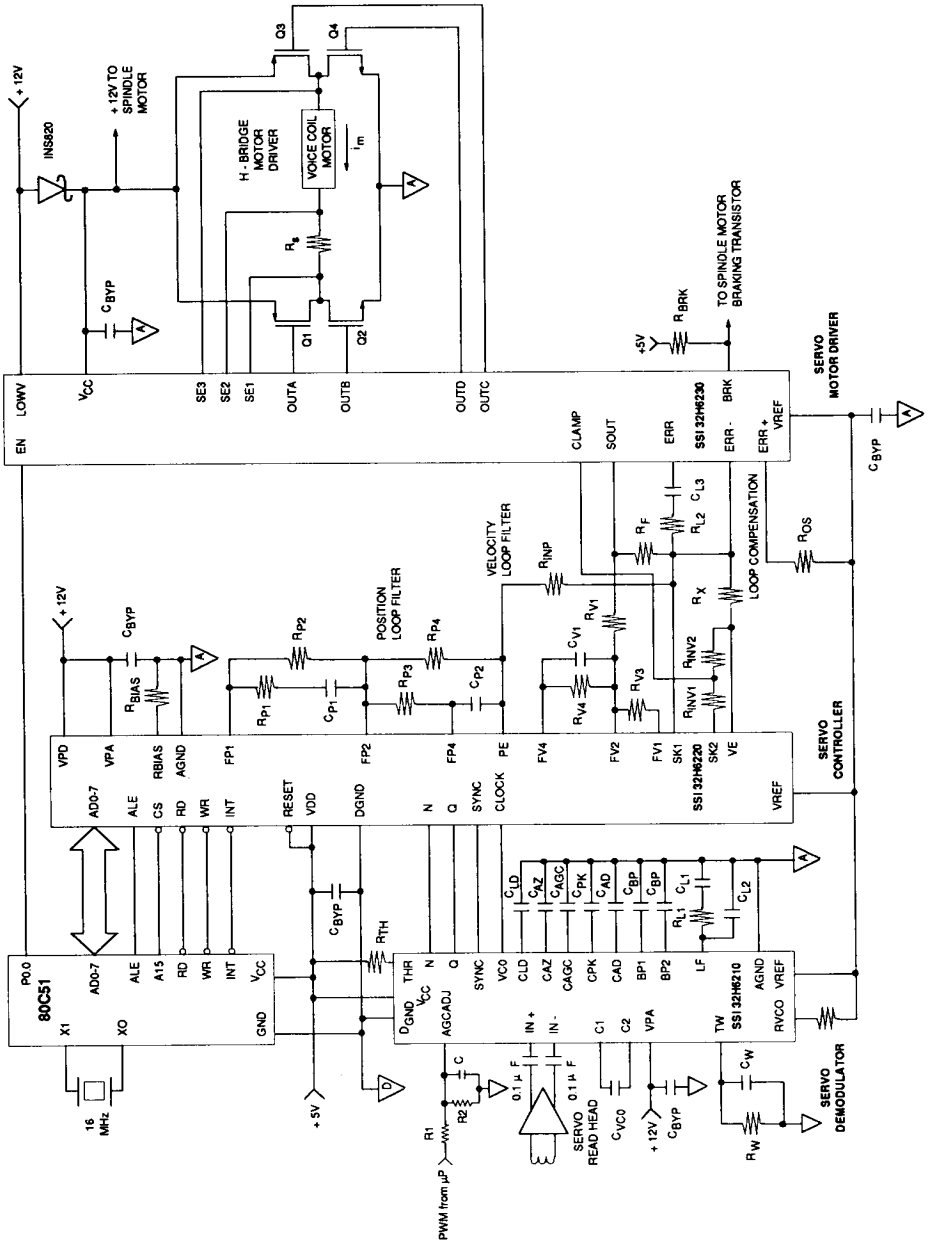
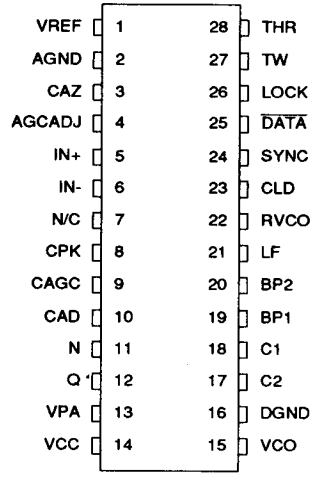


FIGURE 9: Complete Example of Servo Path Electronics Using SSI 32H6210/6220/6230 Chip Set

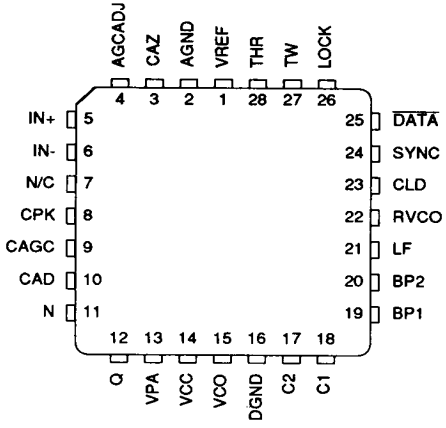
PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP,SOL



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H6210		
28-Pin DIP	32H6210-CP	32H6210-CP
28-Lead SOL	32H6210-CL	32H6210-CL
28-Lead PLCC	32H6210-CH	32H6210-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914