
HB56UW873E-A Series

64MB Buffered EDO DRAM DIMM
8-Mword $\times$ 72-bit, 4k Refresh, 1 Bank Module
(9 pcs of 8M $\times$ 8 components)

HITACHI

ADE-203-821B (Z)

Rev. 2.0

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Description

The HB56UW873E-A belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56UW873E-A is a 8M $\times$ 72 dynamic RAM module, mounted 9 pieces of 64-Mbit DRAM (HM5165805A) sealed in TSOP package and 2 pieces of 16-bit BiCMOS line driver sealed in TSSOP package. The HB56UW873E-A offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56UW873E-A is 168-pin socket type package (dual lead out). Therefore, the HB56UW873E-A makes high density mounting possible without surface mount technology. The HB56UW873E-A provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the its module board.

Features

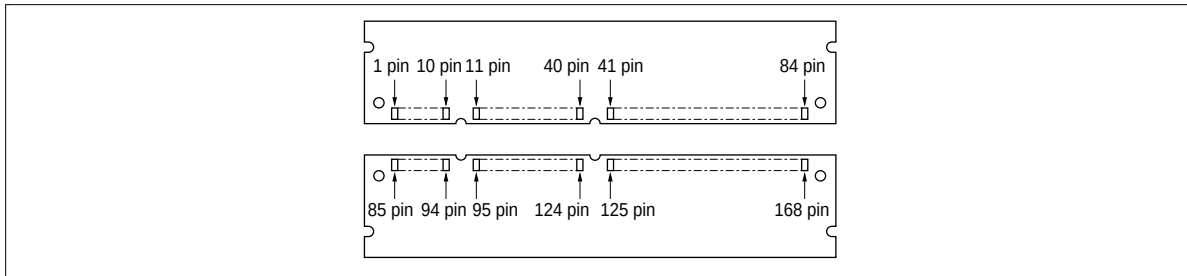
- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 3.3 V supply: 3.3 V $\pm$ 0.3 V / -0.15 V (HB56UW873E-5AR)
3.3 V $\pm$ 0.3 V (HB56UW873E-6A/7A)
- High speed
 - Access time: t_{RAC} = 50 ns / 60 ns / 70 ns (max)
 - Access time: t_{CAC} = 18 ns / 20 ns / 23 ns (max)
- Low power dissipation
 - Active mode: 6.32 mW / 5.38 W / 4.73 W (max)
 - Standby mode (TTL): 100 mW (max)
- Buffered input except $\overline{RAS}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- EDO page mode capability
- 4,096 refresh cycle: 64 ms
- 2 variations of refresh
 - $\overline{RAS}$ -only refresh
 - $\overline{CAS}$ -before- $\overline{RAS}$ refresh

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Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW873E-5AR	50 ns	168-pin dual lead out socket type	Gold
HB56UW873E-6A	60 ns		
HB56UW873E-7A	70 ns		

Pin Arrangement



Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ36	128	NC
3	DQ1	45	$\overline{\text{RE2}}$	87	DQ37	129	NC
4	DQ2	46	$\overline{\text{CE4}}$	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	V _{CC}	48	$\overline{\text{WE2}}$	90	V _{CC}	132	$\overline{\text{PDE}}$
7	DQ4	49	V _{CC}	91	DQ40	133	V _{CC}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56

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Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V _{CC}	101	DQ49	143	V _{CC}
18	V _{CC}	60	DQ24	102	V _{CC}	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	V _{SS}	65	DQ25	107	V _{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	$\overline{\text{WE0}}$	69	DQ28	111	NC	153	DQ64
28	$\overline{\text{CE0}}$	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	$\overline{\text{RE0}}$	72	DQ31	114	NC	156	DQ67
31	$\overline{\text{OE0}}$	73	V _{CC}	115	NC	157	V _{CC}
32	V _{SS}	74	DQ32	116	V _{SS}	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	V _{CC}	82	PD7	124	V _{CC}	166	PD8
41	NC	83	ID0 (V _{SS})	125	NC	167	ID1 (V _{SS})
42	NC	84	V _{CC}	126	B0	168	V _{CC}

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Pin Description

Pin name	Function
A0 to A11, B0	Address input (D0 to D8) : A0 to A11, B0 Row address (D0 to D8) : A0 to A11, B0 Column address (D0 to D8) : A0 to A10, B0 Refresh address (D0 to D8) : A0 to A11, B0
DQ0 to DQ71	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$, $\overline{CE4}$	Column address strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/Write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence detect enable
NC	Non connection

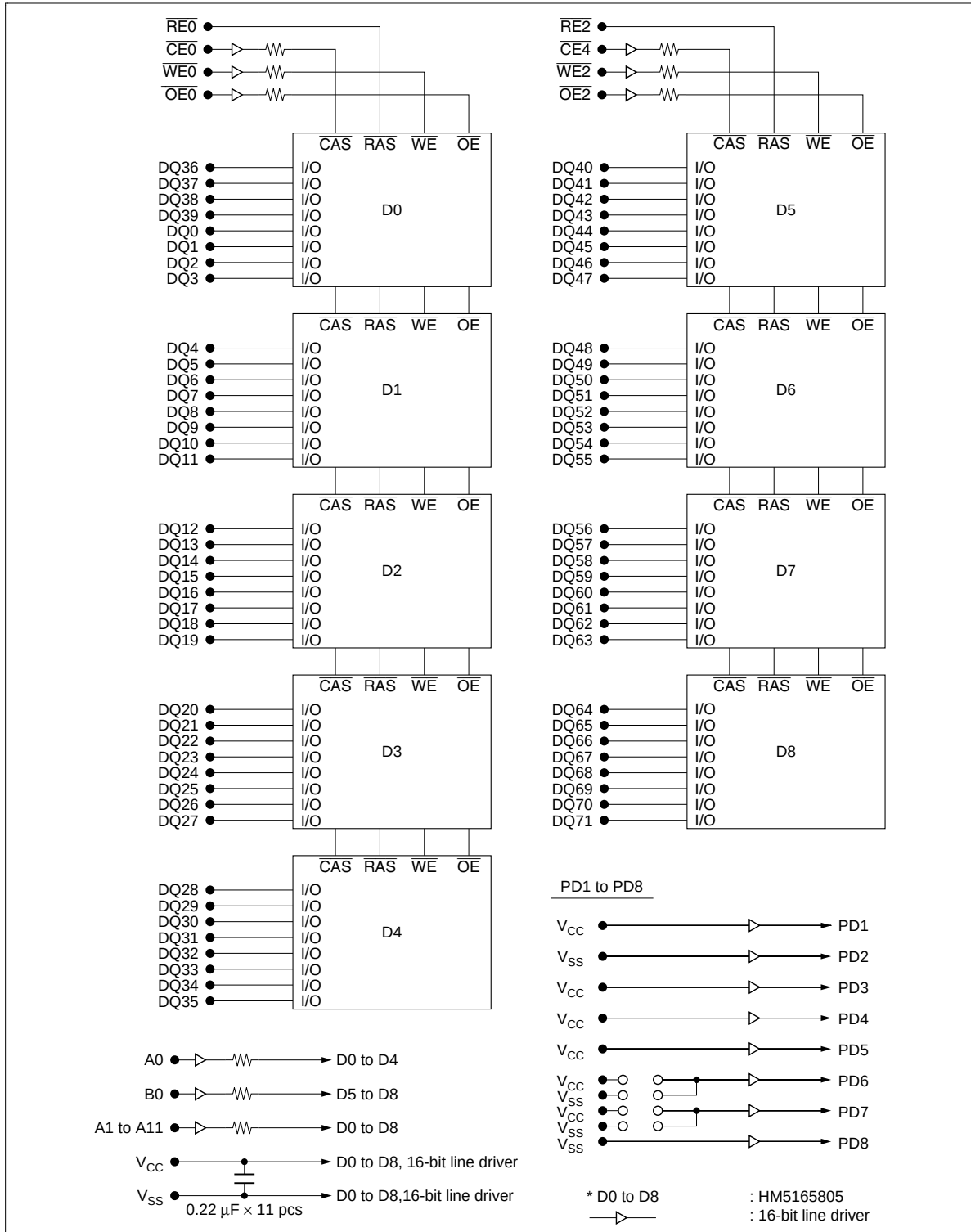
Presence Detect Pin Assignment

Pin name	Pin No.	$\overline{PDE}$ = Low			$\overline{PDE}$ = High
		50 ns	60 ns	70ns	All
PD1	79	1	1	1	High-Z
PD2	163	0	0	0	High-Z
PD3	80	1	1	1	High-Z
PD4	164	1	1	1	High-Z
PD5	81	1	1	1	High-Z
PD6	165	0	1	0	High-Z
PD7	82	0	1	1	High-Z
PD8	166	0	0	0	High-Z

1 : High level (driver output)

0 : Low level (driver output)

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	10	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC} (HB56UW873E-5AR)	3.15	3.3	3.6	V	1, 2
	V_{CC} (HB56UW873E-6A/7A)	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .
 2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V +0.3 V/−0.15 V, V_{SS} = 0 V) (HB56UW873E-5AR)

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HB56UW873E-6A/7A)

		HB56UW873E-A							
		50 ns		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current* ¹ , * ²	I _{CC1}	—	1765	—	1495	—	1315	mA	t _{RC} = min
Standby current	I _{CC2}	—	28	—	28	—	28	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	19	—	19	—	19	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	1765	—	1495	—	1315	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	55	—	55	—	55	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	1540	—	1270	—	1090	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	1360	—	1135	—	1000	mA	t _{HPC} = min
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ V _{CC} + 0.3 V
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ V _{CC} Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{IL}.

3. Address can be changed once or less within one page mode cycle t_{HPC}.

Capacitance

(Ta = 25°C, V_{CC} = 3.3 V +0.3 V/−0.15 V, V_{SS} = 0 V) (HB56UW873E-5AR)

(Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HB56UW873E-6A/7A)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	20	pF	1
Input capacitance (CAS, WE, OE)	C _{I2}	—	20	pF	1
Input capacitance (RAS)	C _{I3}	—	55	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS = V_{IH} to disable Dout.

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AC Characteristics*¹, *², *¹⁷

(Ta = 0 to +70°C, V_{CC} = 3.3 V +0.3 V/-0.15 V, V_{SS} = 0 V) (HB56UW873E-5AR)

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HB56UW873E-6A/7A)

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (50 pF) (Including scope and jig) (HB56UW873E-5AR)
1 TTL gate + C_L (100 pF) (Including scope and jig) (HB56UW873E-6A/7A)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	84	—	104	—	124	—	ns	
RAS precharge time	t _{RP}	30	—	40	—	50	—	ns	
CAS precharge time	t _{CP}	8	—	10	—	13	—	ns	
RAS pulse width	t _{RAS}	50	10000	60	10000	70	10000	ns	
CAS pulse width	t _{CAS}	8	10000	10	10000	13	10000	ns	
Row address setup time	t _{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t _{RAH}	8	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	8	—	10	—	13	—	ns	
RAS to CAS delay time	t _{RCD}	12	32	20	40	20	47	ns	3
RAS to column address delay time	t _{RAD}	10	20	14	25	14	30	ns	4
RAS hold time	t _{RSH}	18	—	20	—	23	—	ns	
CAS hold time	t _{CSH}	40	—	48	—	58	—	ns	21
CAS to RAS precharge time	t _{CRP}	10	—	10	—	10	—	ns	
OE to Din delay time	t _{OED}	18	—	20	—	23	—	ns	5
OE delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	6
CAS delay time from Din	t _{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	7

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Read Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	18	—	20	—	23	ns	9, 10, 16
Access time from address	t_{AA}	—	30	—	35	—	40	ns	9, 11, 16
Access time from $\overline{\text{OE}}$	t_{OEA}	—	18	—	20	—	23	ns	9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	2	—	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	20
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	—	20	ns	13, 20
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	18	—	20	—	20	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	18	—	20	—	23	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	20
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	13	—	15	—	15	ns	13, 20
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	18	—	20	—	20	ns	13
$\overline{\text{WE}}$ to Din delay time	t_{WED}	18	—	20	—	23	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	

Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	8	—	10	—	13	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	18	—	20	—	23	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	10	—	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	13	—	15	—	18	—	ns	

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Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	111	—	154	—	180	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	72	—	83	—	96	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	33	—	39	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	48	—	56	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEh}	13	—	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	5	—	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	0	—	0	—	ns	

EDO Page Mode Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	20	—	25	—	30	—	ns	19
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	15
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	33	—	40	—	45	ns	9, 16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	33	—	40	—	45	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	9
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	8	—	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	8	—	10	—	10	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	28	—	35	—	40	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t_{WPE}	8	—	10	—	10	—	ns	
$\overline{OE}$ precharge time	t_{OEP}	8	—	10	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode read- modify-write cycle time	t_{HPRWC}	57	—	68	—	79	—	ns	
$\overline{\text{WE}}$ delay time from $\overline{\text{CAS}}$ precharge	t_{CPW}	45	—	54	—	62	—	ns	14

Refresh

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	64	ms	4096 cycles

Notes: 1. AC measurements assume $t_f = 2$ ns.

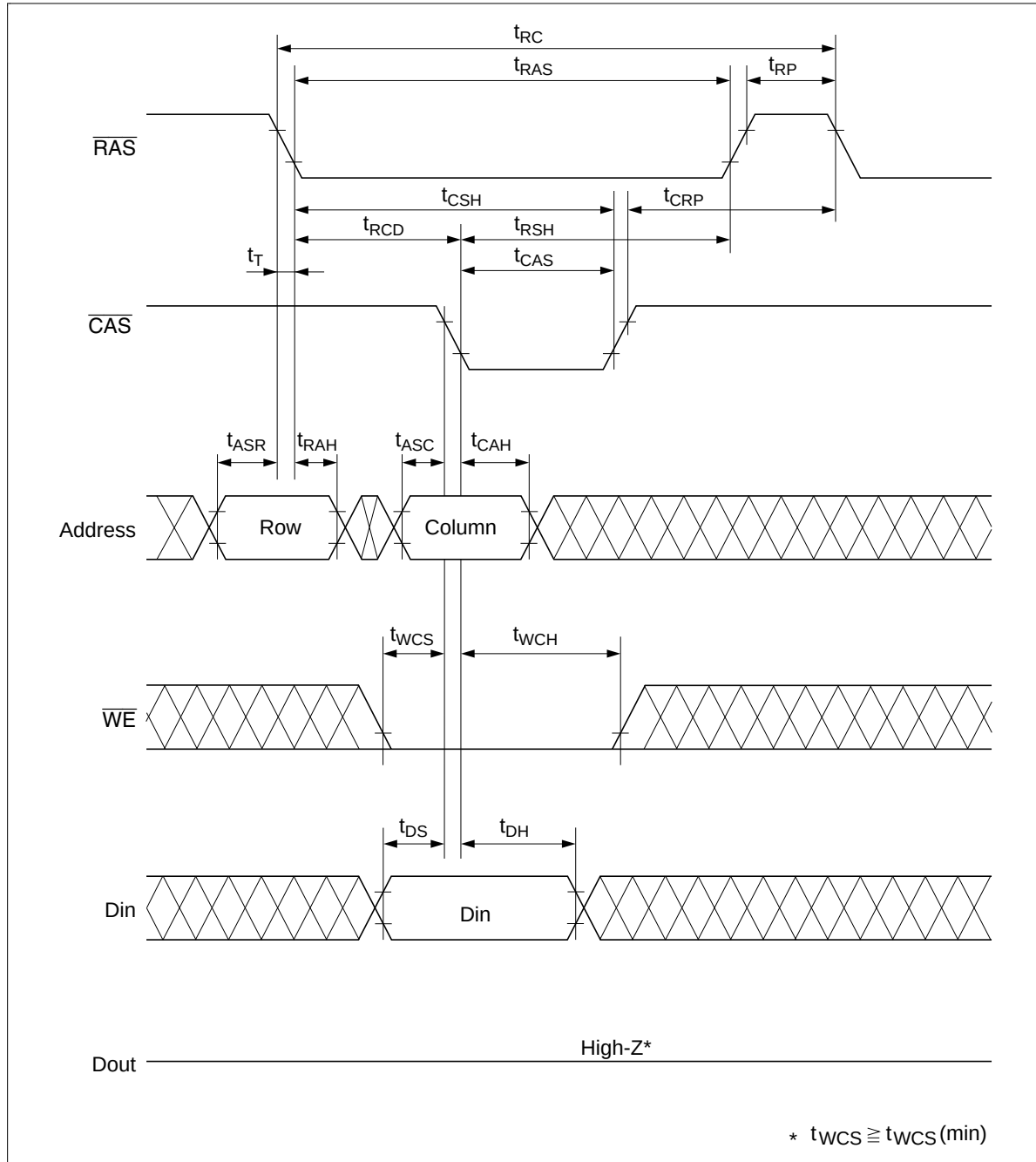
- An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or $\overline{\text{CAS}}$ -before-RAS refresh).
- Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
- Either t_{OED} or t_{CDD} must be satisfied.
- Either t_{DZO} or t_{DZC} must be satisfied.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
- Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 1 TTL loads and 50 pF (HB56UW873E-5AR) and 1 TTL loads and 100 pF (HB56UW873/EJE-6A/7A).
- Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\geq t_{\text{RAD}} + t_{\text{AA}}$ (max).
- Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\leq t_{\text{RAD}} + t_{\text{AA}}$ (max).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
- t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min), or $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPW}} \geq t_{\text{CPW}}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- t_{RASp} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
- Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
- All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
- In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.

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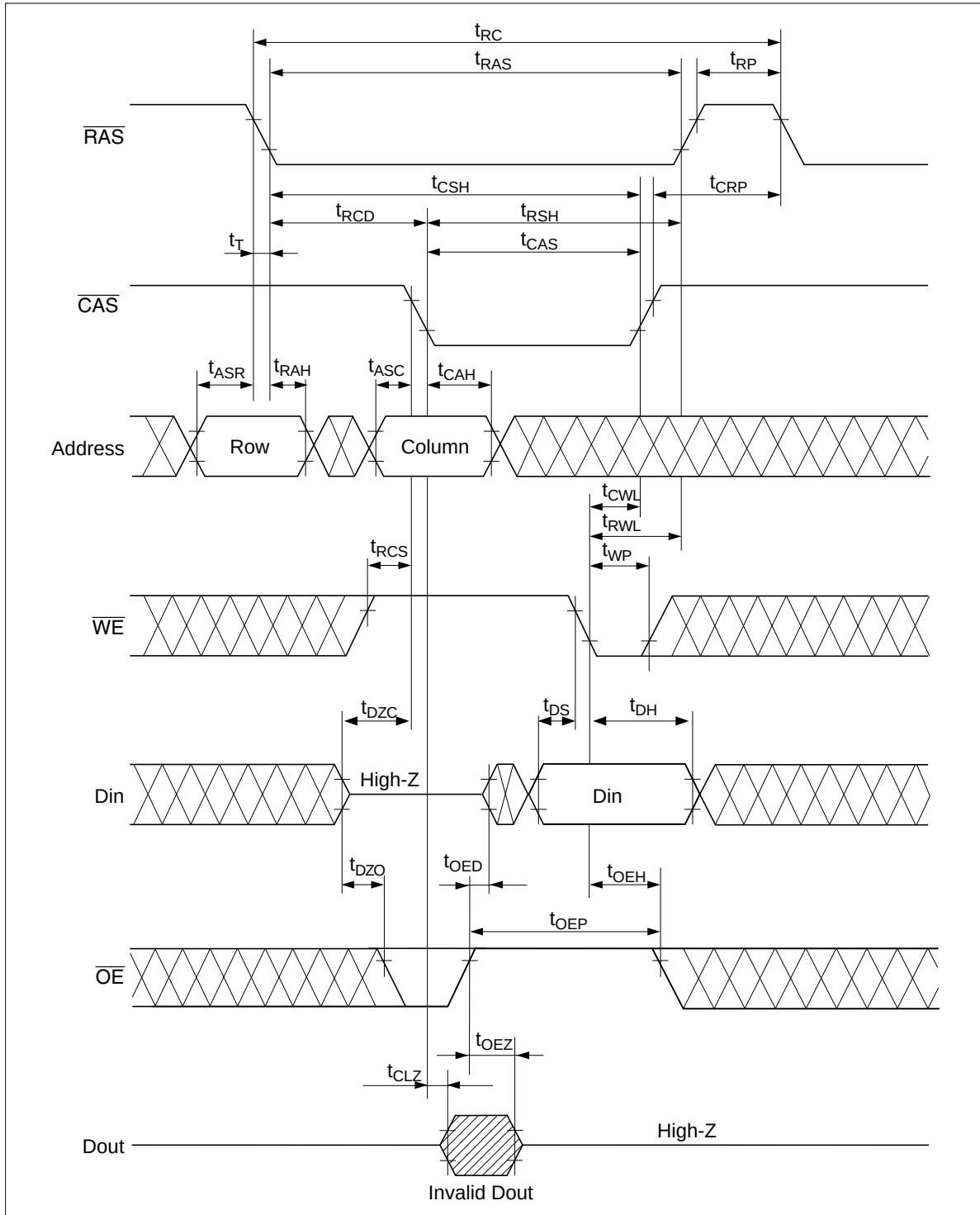
19. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2 t_{\text{r}}$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
20. Data output turns off and becomes high impedance from later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$.
Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF} .
21. t_{CSH} (min) can be achieved when $t_{\text{RCD}} \leq t_{\text{CSH}}$ (min) – t_{CAS} (min).
22. XXX: H or L (H: V_{IH} (min) $\leq V_{\text{IN}} \leq V_{\text{IH}}$ (max), L: V_{IL} (min) $\leq V_{\text{IN}} \leq V_{\text{IL}}$ (max))
/////: Invalid Dout
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

HB56UW873E-A Series

Early Write Cycle

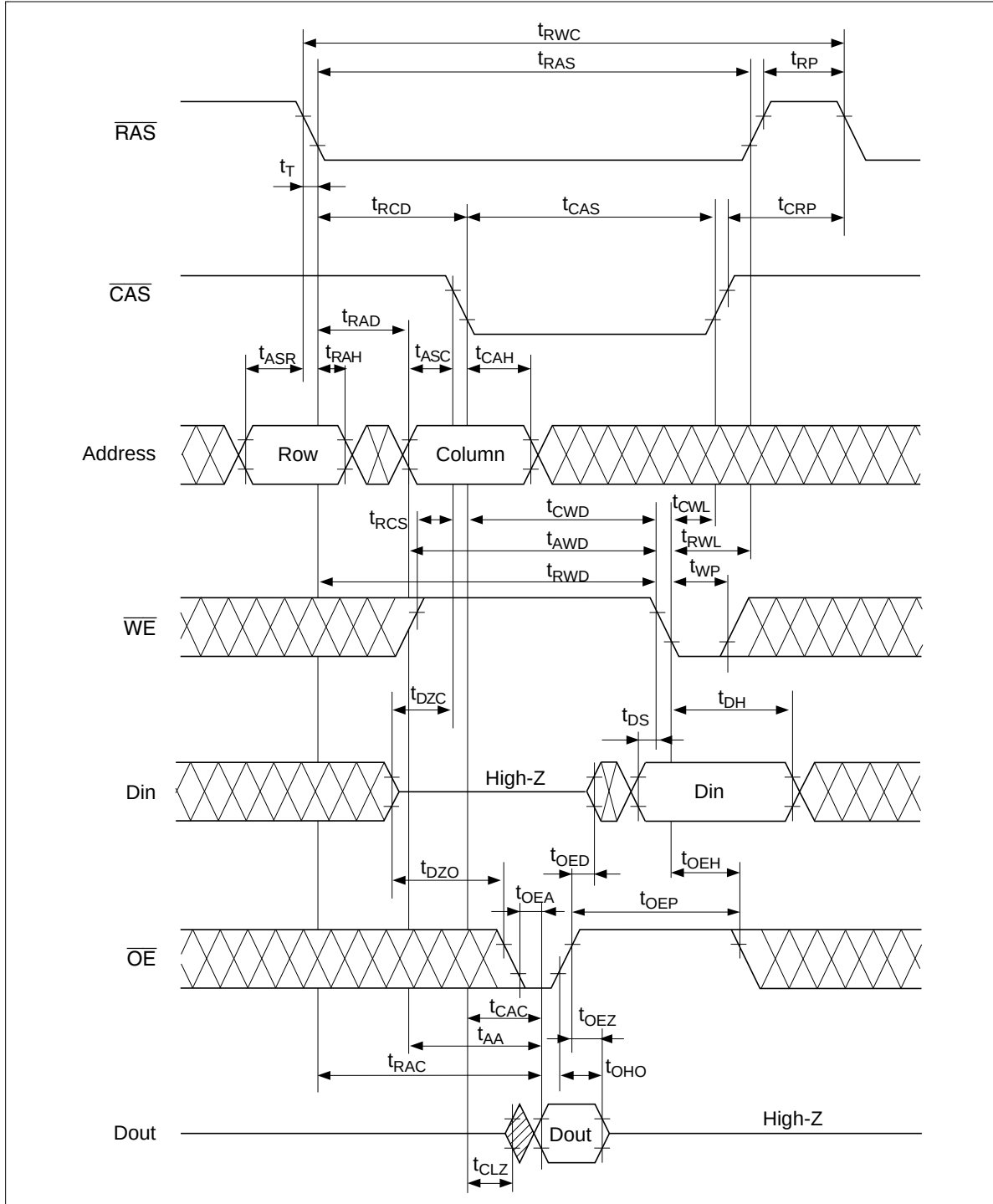


Delayed Write Cycle *18

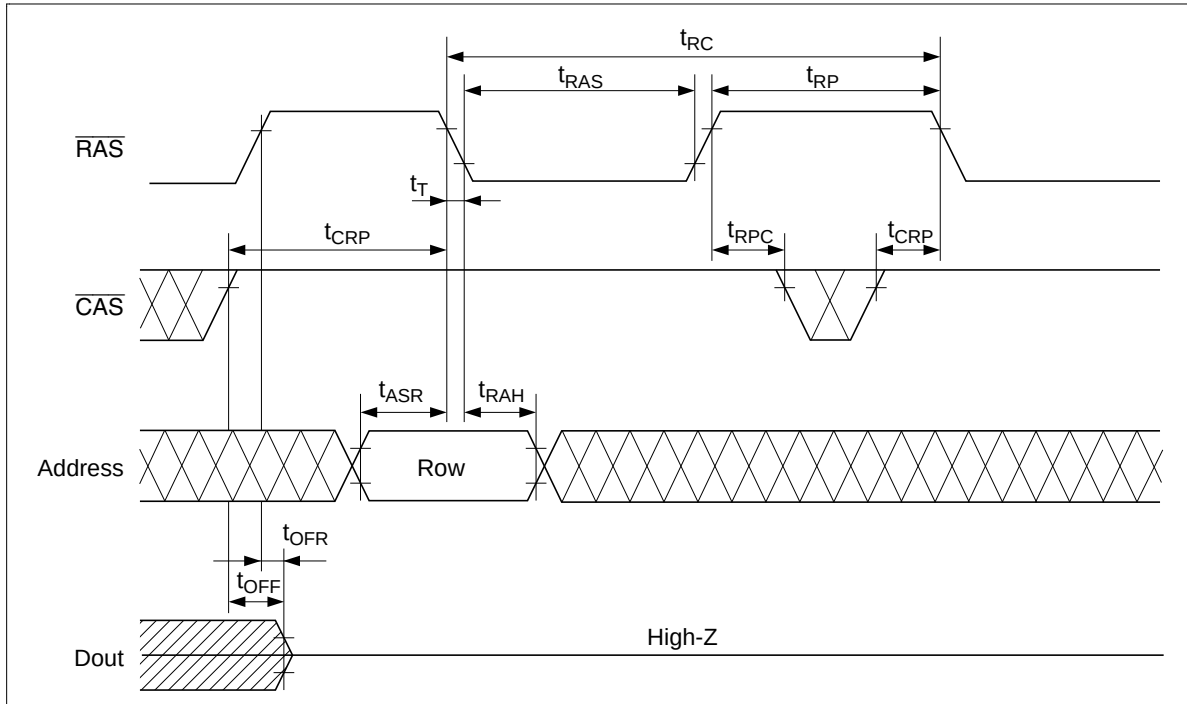


HB56UW873E-A Series

Read-Modify-Write Cycle *18

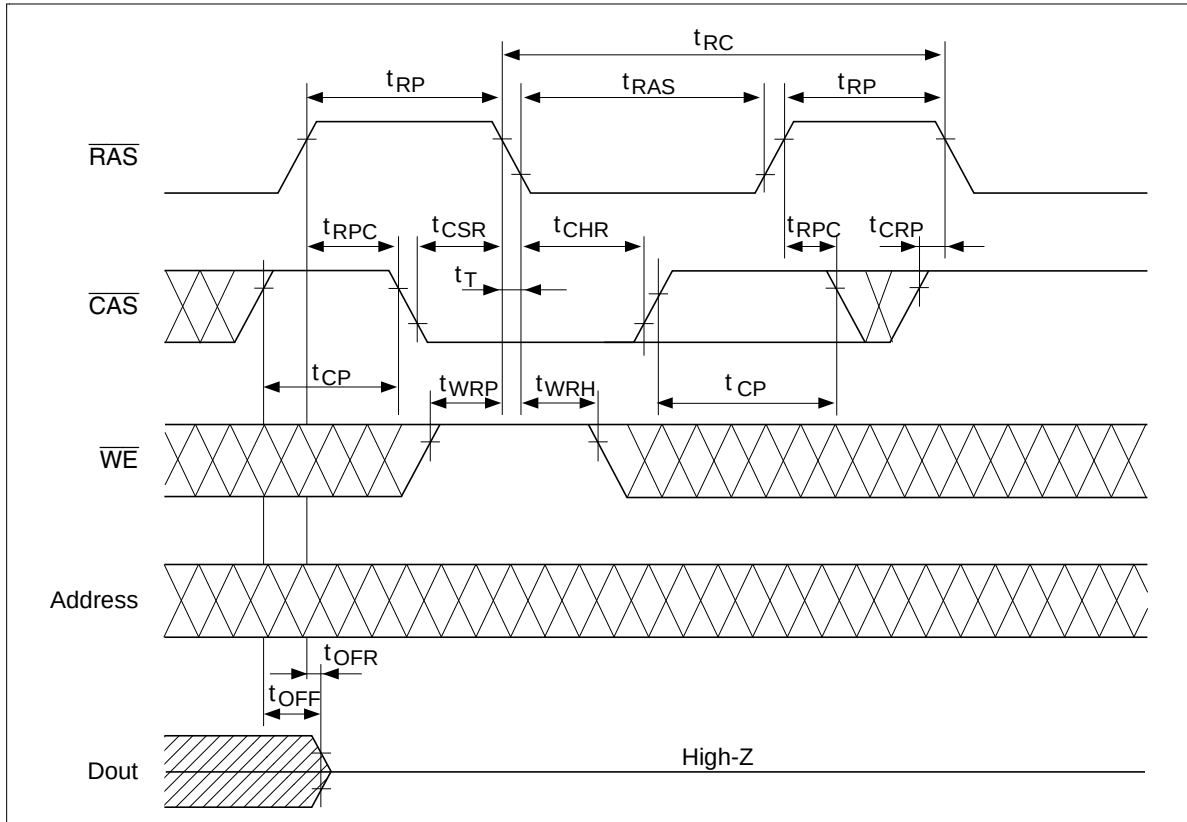


$\overline{\text{RAS}}$ -Only Refresh Cycle

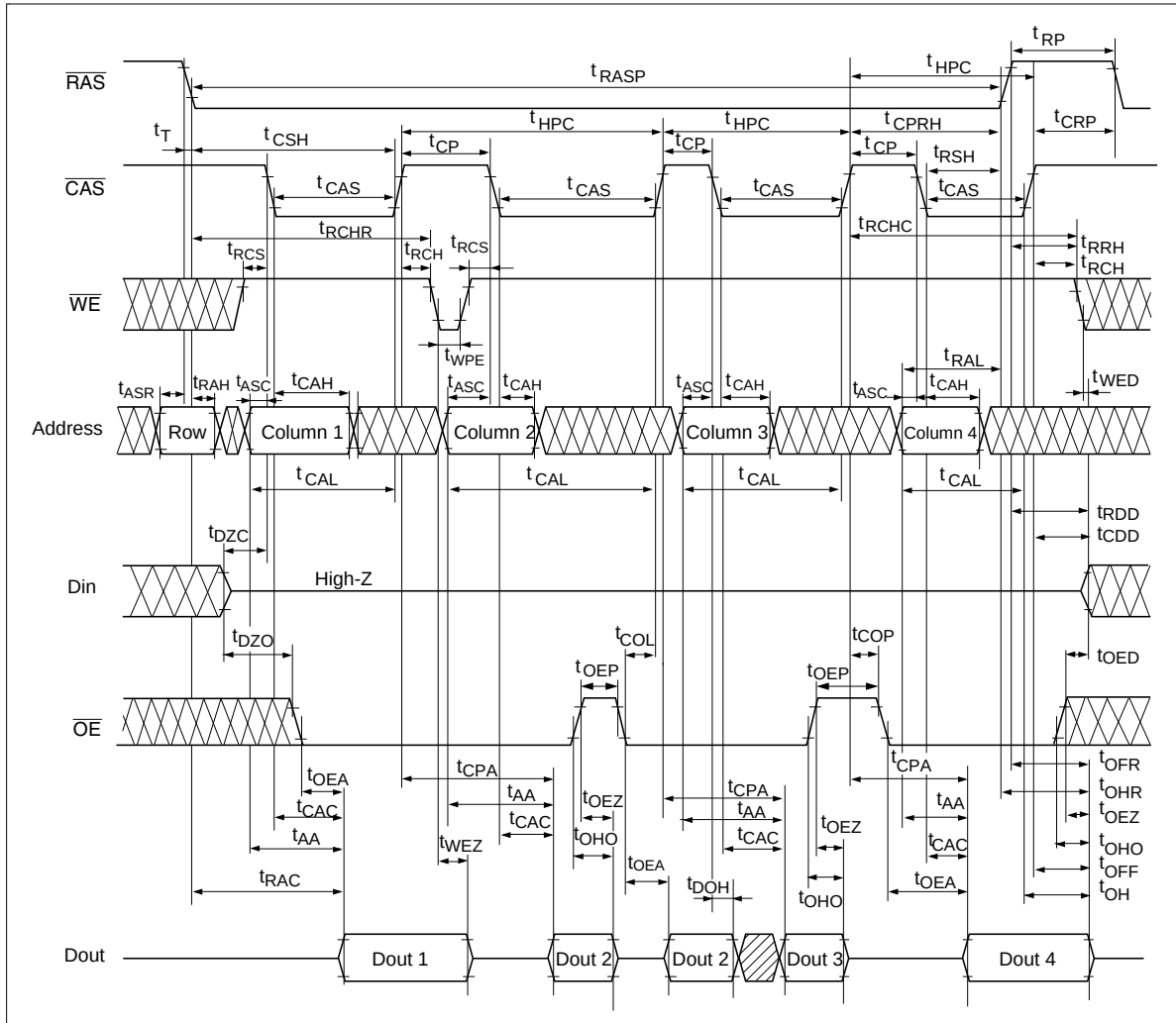


HB56UW873E-A Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

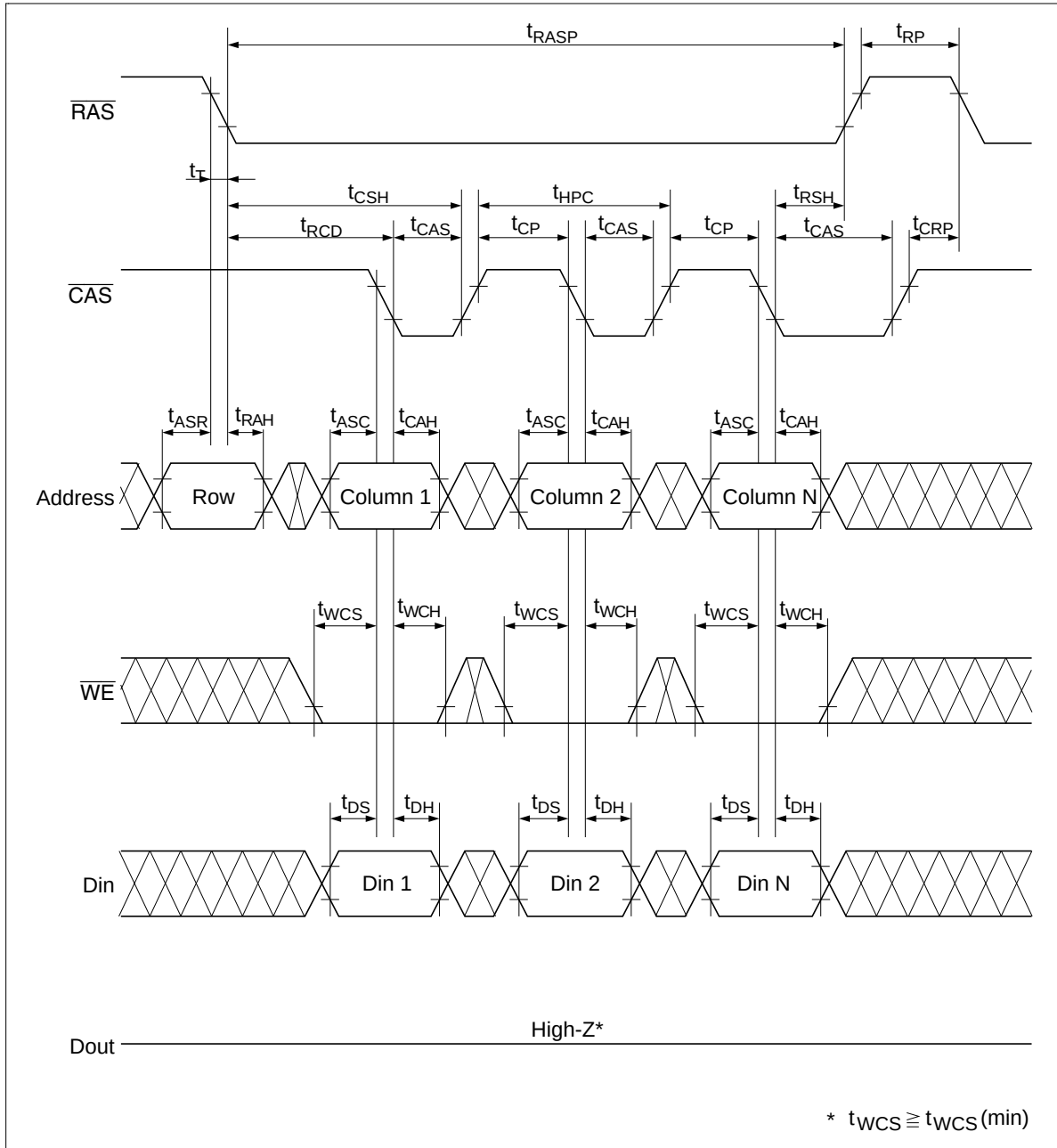


EDO Page Mode Read Cycle

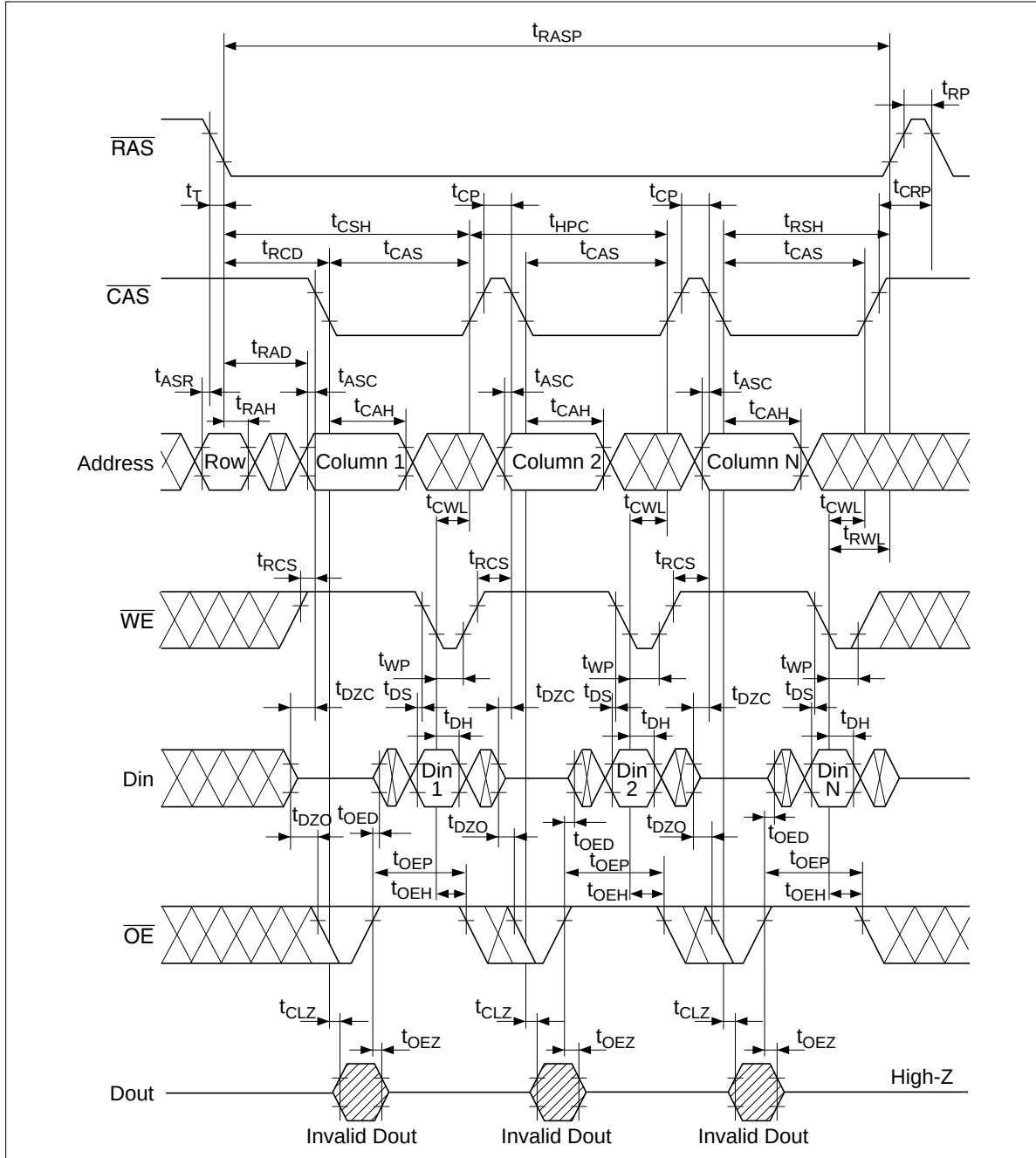


HB56UW873E-A Series

EDO Page Mode Early Write Cycle

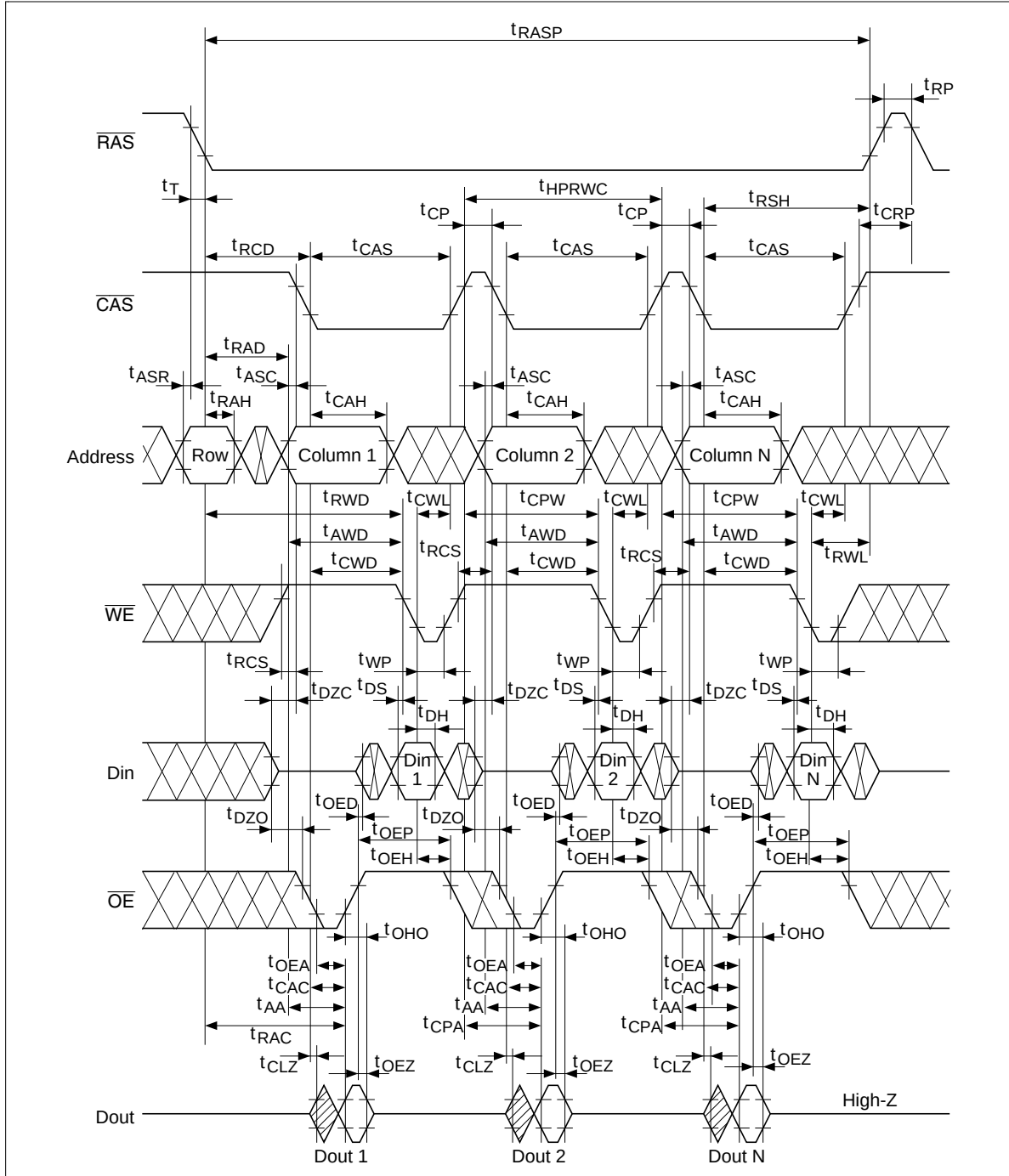


EDO Page Mode Delayed Write Cycle *18

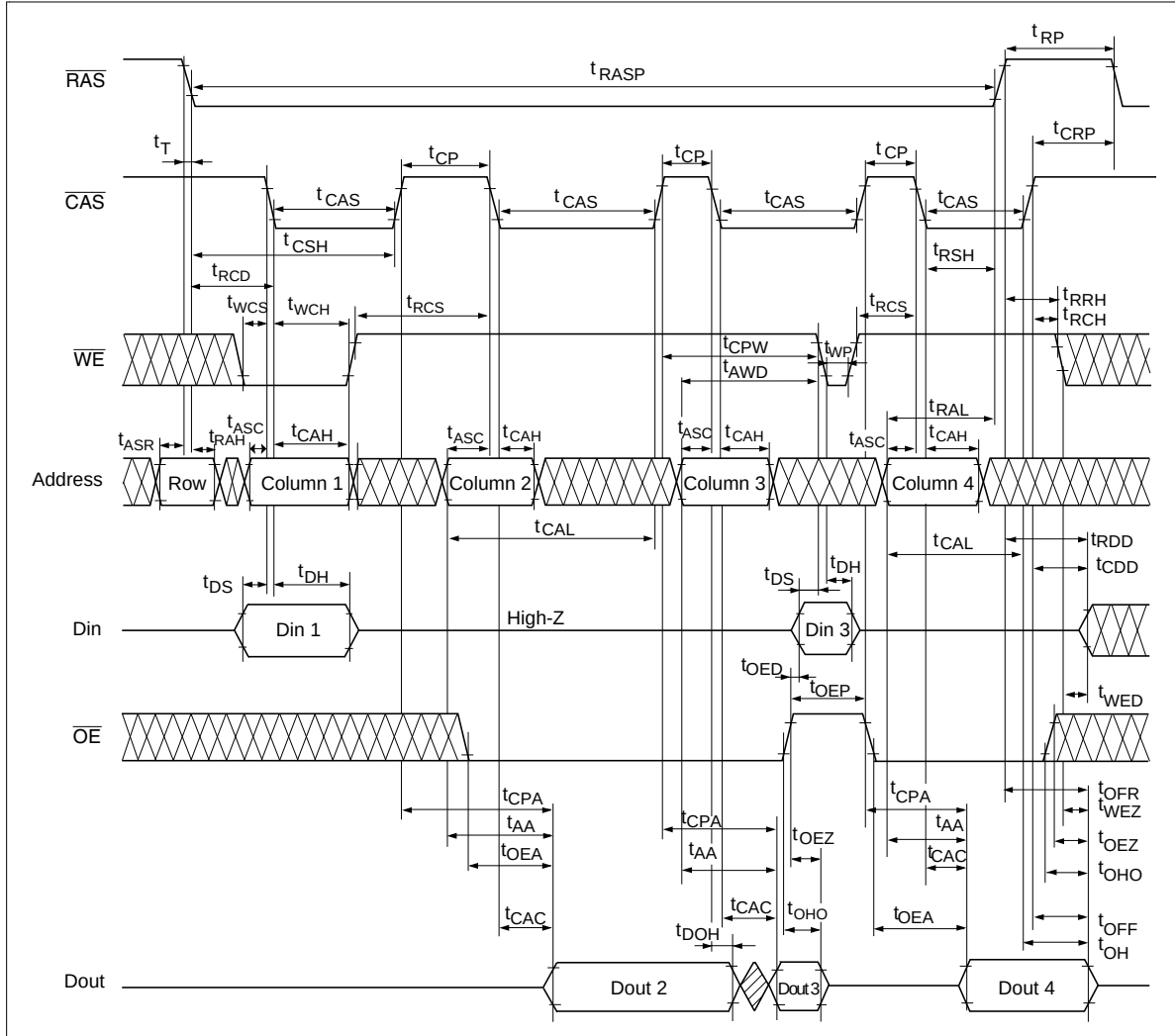


HB56UW873E-A Series

EDO Page Mode Read-Modify-Write Cycle *18

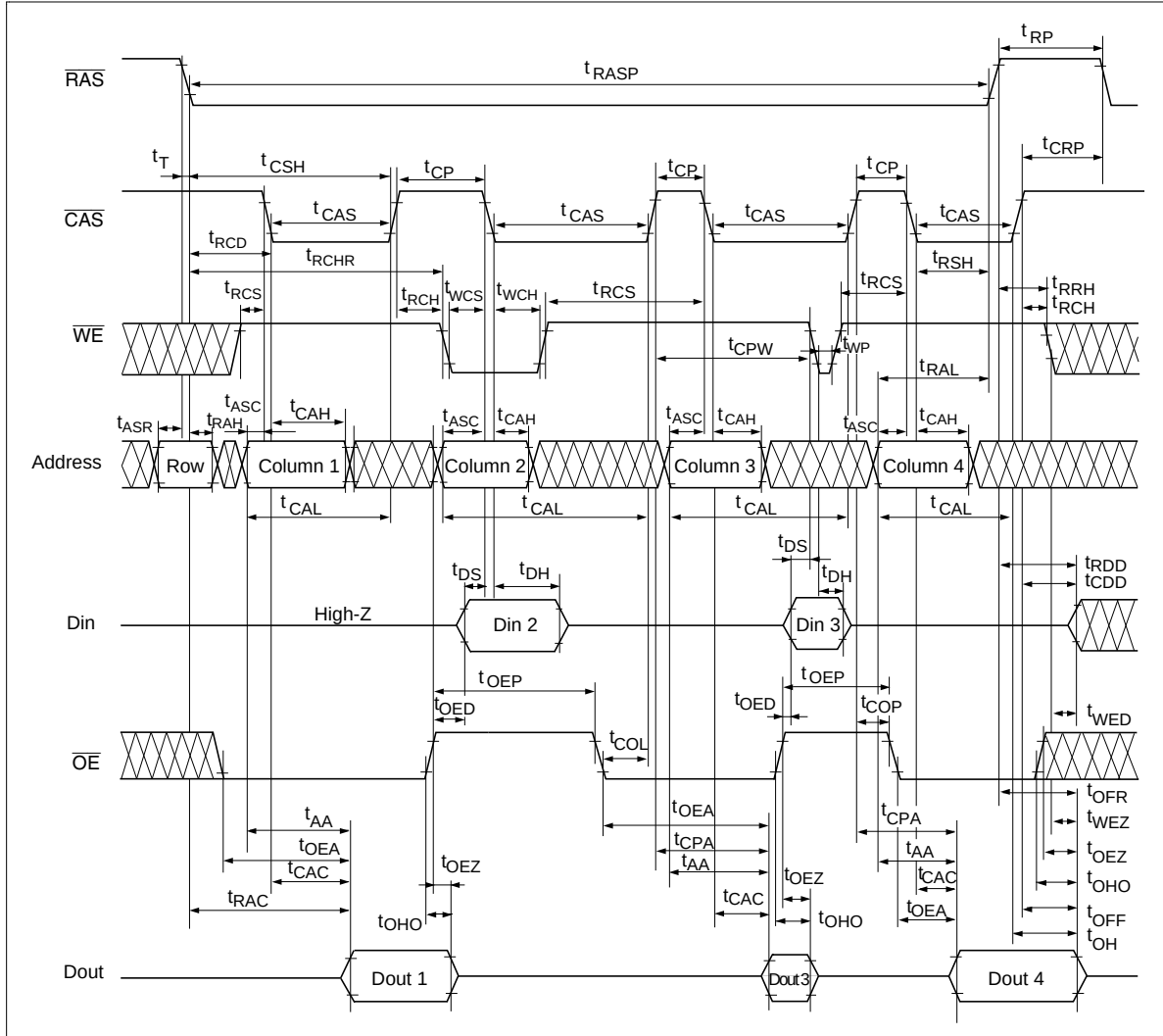


EDO Page Mode Mix Cycle (1) *19



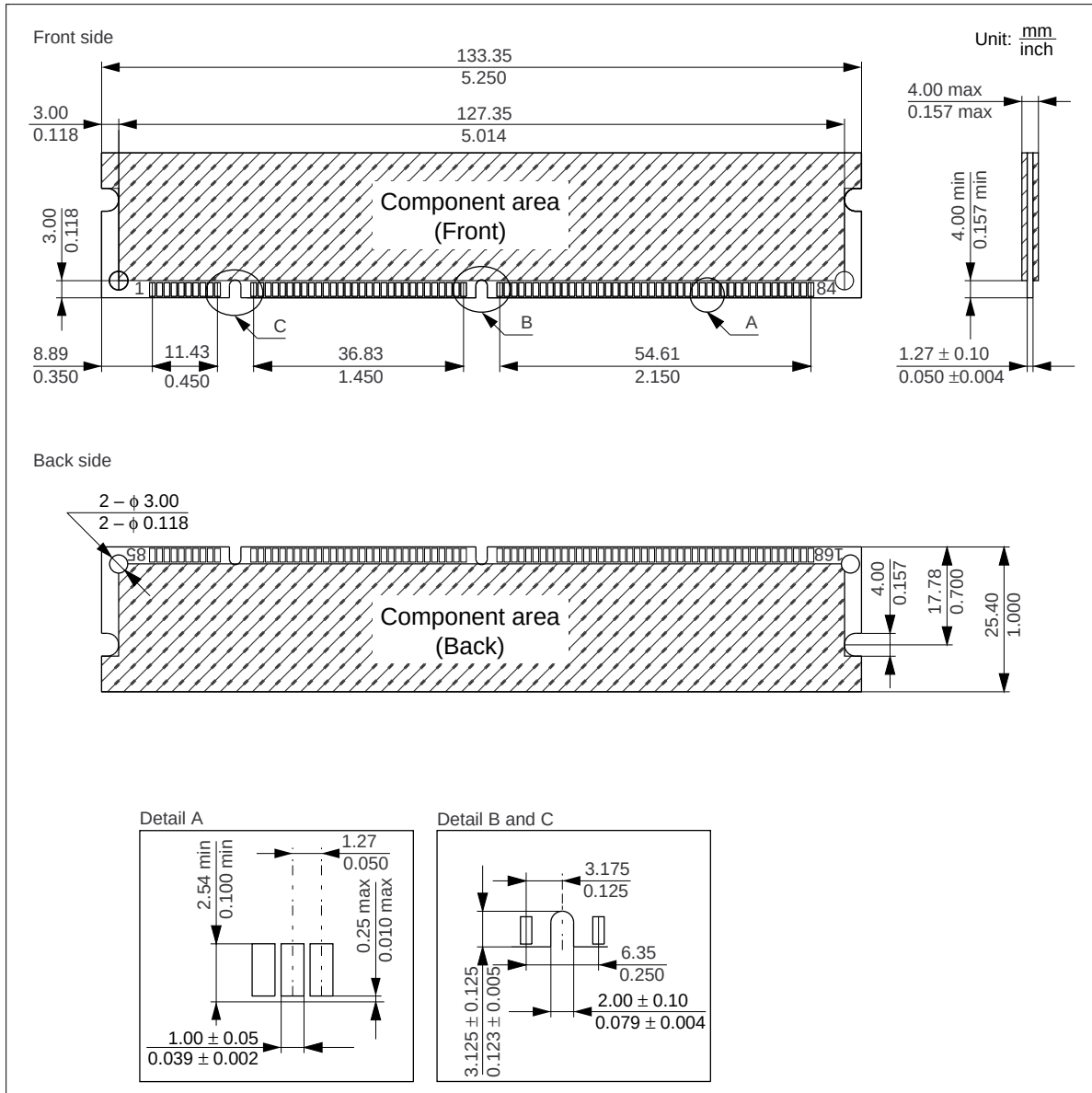
HB56UW873E-A Series

EDO Page Mode Mix Cycle (2) *19



Physical Outline

HB56UW873E-A Series



HB56UW873E-A Series

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HB56UW873E-A Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Sep. 12, 1997	Initial issue (referred to HM5164805A/5165805A Series rev. 1.0)	Y. Saitou	K. Tsuneda
2.0	Nov. 20, 1997	(referred to HM5164805A/5165805A Series rev. 2.0) Addition of HB56UW873E-5AR Series Deletion of driver name 74LVT16244 from Description Recommended DC operating conditions Addition of note 2 Block Diagram 74LVT16244 to 16-bit line driver AC Characteristics t_{RAD} min: 14/15 ns to 10/14/14 ns Timing waveforms Correct errors: EDO page mode mix cycle (1)		