CMOS 8–Bit Microcontrollers

TMP90PM36F/TMP90PM36T

1. Outline and Characteristics

The TMP90PM36 is a system evaluation LSI having a built-in One-Time PROM (16K byte) for TMP90CM36.

A programming and verification for the internal PROM is acheived by using a general EPROM programmer with an adapter socket.

The function of this device is exactly the same as the TMP90CM36 by programming to internal PROM:

Parts No.	ROM	RAM	Package	Adapter Socket No.
TMP90PM36F	OTP 32968 x 8bit	1024 x 8bit	80-FP	Under Development
TMP90PM36T			84-QFJ (PLCC)	

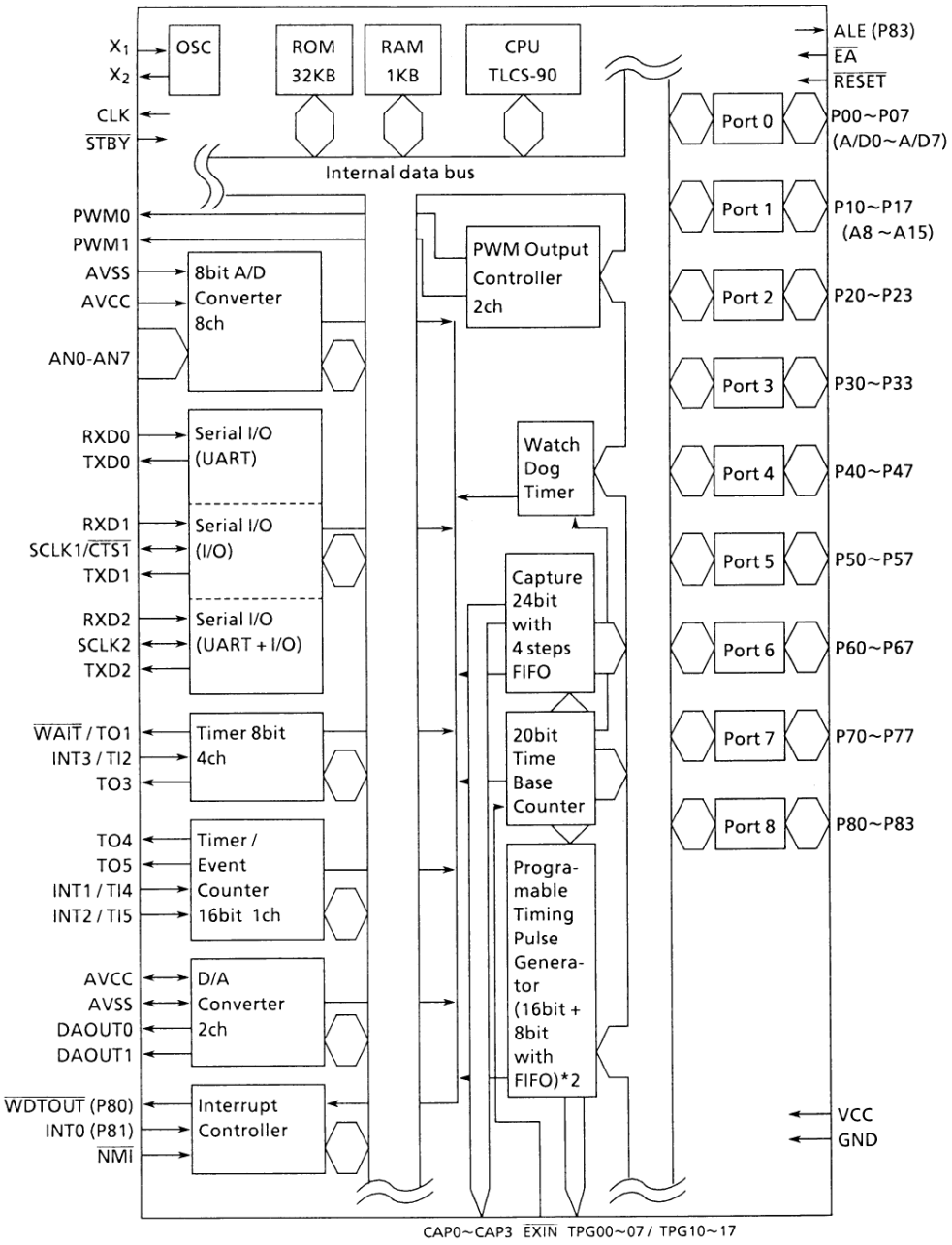


Figure 1. TMP90PM36 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for TMP90PM36, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1 (1) shows pin assignment of the TMP90PM36F.

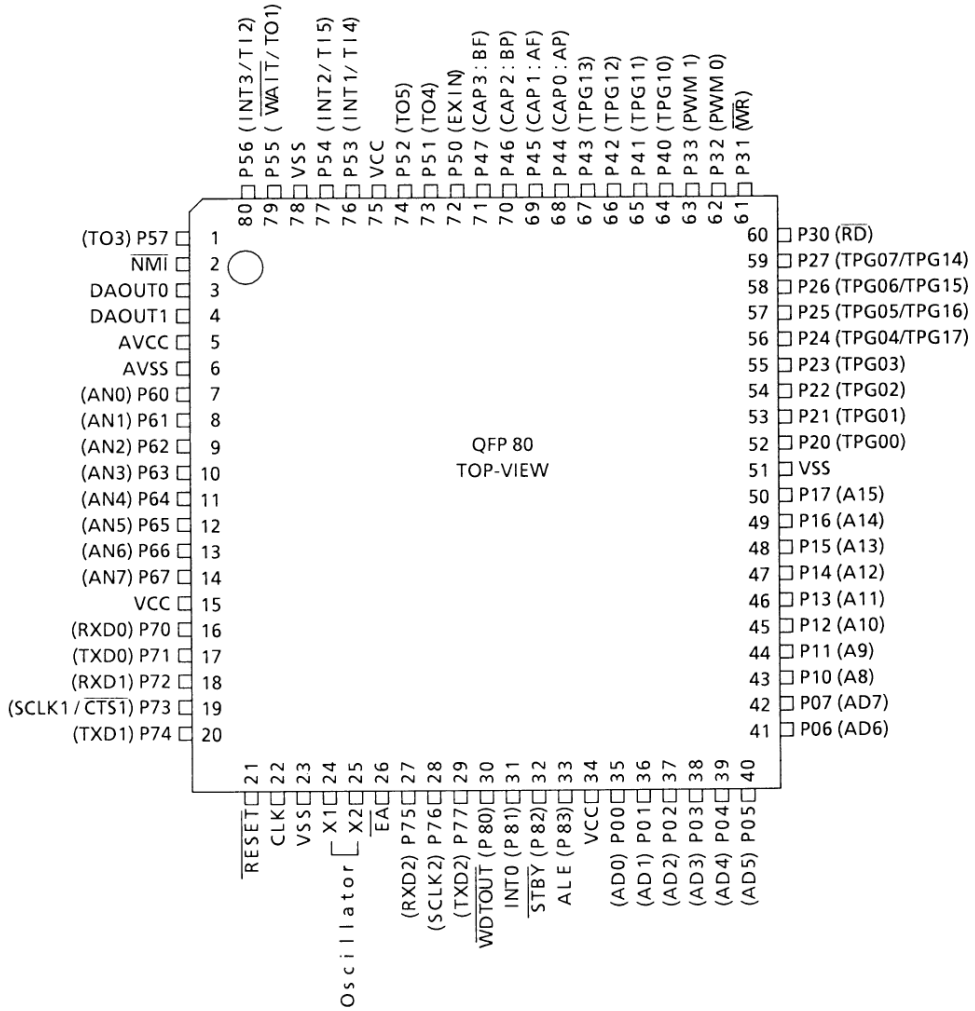


Figure 2.1 (1). Pin Assignments (Flat Package)

Figure 2.1 (2) shows the pin assignment of TMP90PM36.

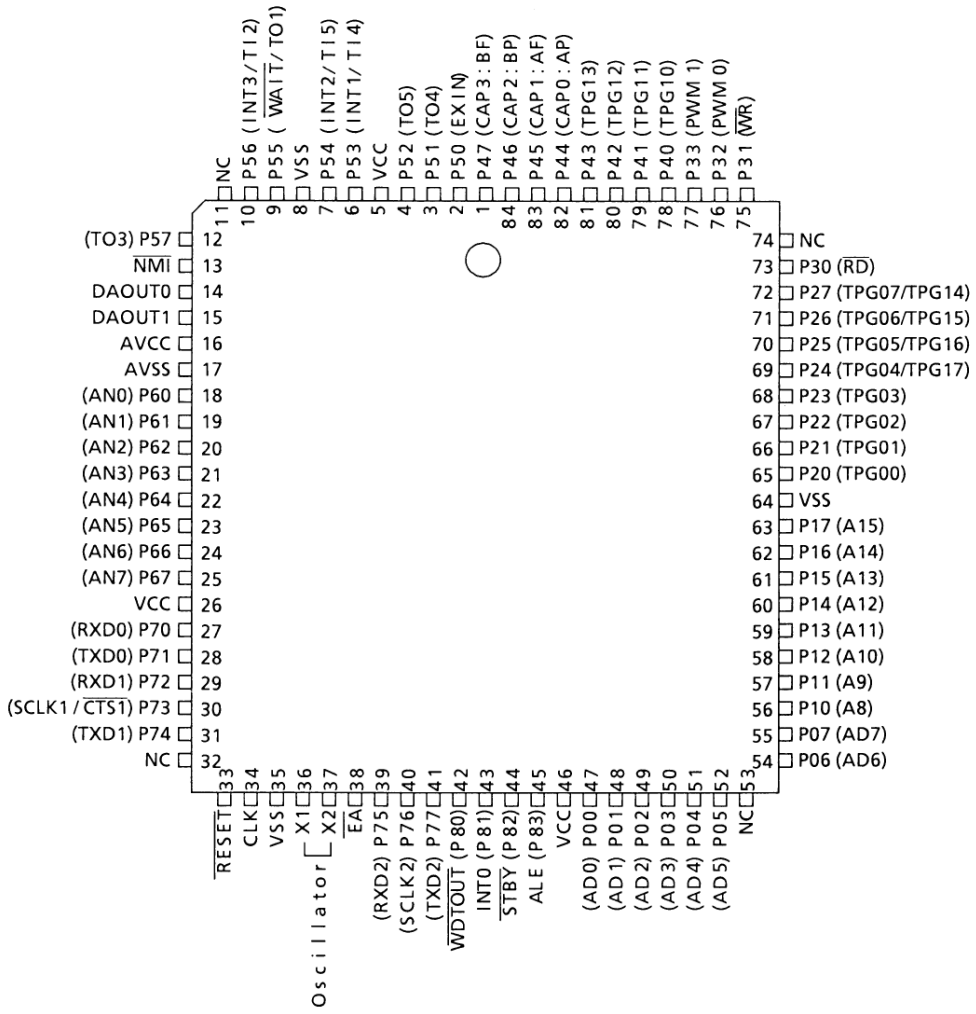


Figure 2.1 (2). Pin Assignments (QFJ (PLCC) Package)

2.2 Pin Names and Functions

The TMP90PM36 has MCU mode and PROM mode.

(1) MCU Mode (The TMP90CM36 is pin compatible).

Table 2.2 (1/4)

Pin name	No. of pins	I/O or tristate	Function
P00~P07	8	I/O	Port 0 : An 8-bit I/O port. Each bit can be set for input or output.
/AD0~AD7		Tristate	Address/data bas : Operates as an 8-bit bi-directional address bus or data bus when using external memory. Operates port when built-in memory used.
P10~P17	8	I/O	Port1: An 8-bit I/O port. Each bit can be set for input or output.
/A8~A15		Output	Address bus: Operates as the 8 upper bits of the address bus when using external memory. Operates port when built-in memory used.
P20~P27 /TPG00~ TPG07 (TPG14~ TPG17)	8	I/O	Port2: An 8-bit I/O port. Each bit can be set for input or output.
		Output Tristate	TPG0 output: Operates of the TPG00~TPG07 output pin. 4 upper bits are shared in TPG14~TPG17. Operates as Reset at once of the 3 state condition. Operates output condition of agreement for output data write and comparator data.
P30	1	Output	Port30: A 1-bit output port.
/$\overline{RD}$			Read: Strobe signal output for reading external memory.
P31	1	Output	Port31: A 1-bit output port.
/$\overline{WR}$			Write: Strobe signal output for writing external memory.
P32, P33	2	I/O	Port32, Port33: A 2-bit I/O port. Each bit can be set for input or output.
/PWM0, PWM1		Output Tristate	Motor control output : PWM0/1 motor control output pin.
P40~P43 /TPG10~ TPG13	4	I/O	Port40~43: A 4-bit I/O port. Each bit can be set for input or output.
		Output Tristate	TPG1output : Operates of the TPG10~TPG13 output pin. TPG14~TPG17 are shared in TPG04~07. Operates as Reset at once of the 3 state condition. Operates output condition of agreement for output data write and comparator data.

Table 2.2 (2/4)

Pin name	No. of pins	I/O or tristate	Function
P44~P47 /CAP0~ CAP3	4	I/O	Port44~47: A 4-bit I/O port. Each bit can be set for input or output.
		Input	Capture input : CAP0~CAP3 input pin.
P50 /EXIN	1	I/O	Port50: A 1-bit I/O port.
		Input	Time base counter to external clock input pin.
P51 /TO4	1	I/O	Port51: A 1-bit I/O port.
		Output	Timer Output4: Timer 4 output pin.
P52 /TO5	1	I/O	Port52: A 1-bit I/O port.
		Output	Timer Output5: Timer 5 output pin.
P53	1	I/O	Port53: A 1-bit I/O port.
/INT1		Input	Interrupt request pin1: A rising/falling edge programmable interrupt request pin.
/TI4		Input	Timer input4: Timer 4 counter input pin.
P54	1	I/O	Port54: A 1-bit I/O port.
/INT2		Input	Interrupt request pin2: A rising edge interrupt request input pin.
/TI5		Input	Timer input5: Timer 5 counter input pin.
P55	1	I/O	Port55: A 1-bit I/O port.
/TO1/$\overline{\text{WAIT}}$		Output / Input	Timer output0/1: Timer 0 or timer 1 output. / Wait: Input pin for connecting a memory or peripheral LSI with delayed access time.
P56	1	I/O	Port56: A 1-bit I/O port.
/TI2		Input	Timer input2/3: Timer 2 or Timer 3 counter input pin.
/INT3		Input	Interrupt request pin3: A rirising edge interrupt request input pin.
P57	1	I/O	Port57: A 1-bit I/O port.
/TO3		Output	Timer Output2/3: Timer 2 or Timer 3 output.
$\overline{\text{NMI}}$	1	Input	Non-maskable Interrupt request pin: A falling edge interrupt request pin (Sctimitt input).
/DAOUT0, DAOUT1	2	Output	D/A Output: D/A converter 0/1 analog current output pin.

Table 2.2 (3/4)

Pin name	No. of pins	I/O or tristate	Function
AVCC	1	Input	Reference Voltage to A/D converter.
AVSS	1	Input	GND pin for A/D converter (0V).
P60~P67	8	Input	Port60~67: An 8-bit input ports.
/AN0~AN7			Analog input: 8 analog inputs to A/D converter.
VCC	2	Input	Power supply pin (+ 5V).
VSS	3	Input	GND pin (0V).
P70	1	I/O	Port70: A 1-bit I/O port.
/RXD0		Input	Serial channel 0 receive data input pin.
P71	1	I/O	Port71: A 1-bit I/O port.
/TXD0		Output	Serial channel 0 send data output pin.
P72	1	I/O	Port72: A 1-bit I/O port.
/RXD1		Input	Serial channel 1 receive data input pin.
P73	1	I/O	Port73: A 1-bit I/O port.
/SCLK1		I/O	Serial clock I/O : External clock for SCLK1 do input or send clock for internal boudrate generator do output when I/O interface mode is condition.
/CTS1		Input	$\overline{\text{CTS1}}$ input pin: Serial data send possible signal (Clear To Send).
P74	1	I/O	Port74: A 1-bit I/O port.
/TXD1		Output	Serial channel 1 send data output pin.
P75	1	I/O	Port75: A 1-bit I/O port.
/RXD2		Input	Serial channel 2 receive data input pin.
P76	1	I/O	Port76: A 1-bit I/O port.
/SCLK2		I/O	Serial clock I/O: External clock for SCLK2 do input or send clock for internal boudrate generator do output when I/O interface mode is condition.
P77	1	I/O	Port77: A 1-bit I/O port.
/TXD2		Output	Serial channel 2 send data output pin.
$\overline{\text{RESET}}$	1	Input	Reset: Reset input pin to initialize the TMP90CM36.

Table 2.2 (4/4)

Pin name	No. of pins	I/O or Tristate	Function
CLK	1	Output	Clock output: Output 1/4 frequency of the clock oscillation. Pulled up during reset.
X1, X2	2	I/O	The crystal oscillator connectopn pin.
$\overline{EA}$	1	Input	External access: Connects to the Vcc pin when the TMP90CM36 built-in ROM is used.
P80	1	Output	Port80: A 1-bit output port.
/$\overline{WDTOUT}$		Output	Wachdog out: Operates $\overline{WDTOUT}$ output pin when watchdog timer register is D1 = 1
P81	1	Input	Port81: A 1-bit input port.
/INT0		Input	Interrupt request pin0: A level/rising edge programmable interrupt request pin.
P82	1	Input	Port82: A 1-bit input port.
/$\overline{STBY}$		Input	Hardware standby input pin (schmitt input).
P83	1	Output	Port83: A 1-bit output port.
/ALE		Output	Address latch enable : The falling edge of this signal is used for latching addresses on AD0-AD7 when accessing external memory.

(2) PROM Mode Pin Functions Pin Disposal

Table 2.2 (2) PROM Mode Name and Function, Pin Disposal

Pin function name	No. of pins	I/O	Function	Pin name (MCU mode)
A3~A0	4	Input	Program memory address input	P23~P20
A7~A4	4	Input		P93~P90
A14~A8	7	Input		P16~P10
A15	1	Input		P17
A16	1	Input		P33
D7~D0	8	I/O	Program memory data input/output	P07~P00
$\overline{CE}$	1	Input	Chip enable input	P32
$\overline{OE}$	1	Input	Output control input	P30
$\overline{PGM}$	1	Input	Program control input	P31
VPP	1	power supply	12.75V/5V (Program power supply)	$\overline{EA}$
VCC	3	power supply	5V	VCC
VSS	3	power supply	0V	VSS
Pin name	No. of pins	I/O	Pin disposal	
P40	1	Input	Be fixed to "L" level (security pin)	
P81	1	Input	Be fixed to "L" level	
$\overline{RESET}$	1	Input	Be fixed to "L" level (PROM mode)	
CLK	1	Input		
ALE	1	Output	Open	
X1	1	Input	Resonator connection pin	
X2	1	Output		
P47~P41	7	Input	Be fixed to "L or H" level	
P57~P50	8	Input	Be fixed to "L or L" level	
$\overline{NMI}$, P82, AVCC	3	Input	Be fixed to "H" level	
DAOUT0, DAOUT1	2	Output	Open	
AVSS	1	Input	Be fixed to "L" level	
P67~P60	8	Input	Be fixed to "L" level	
P77~P70	8	Input	Be fixed to "L or H" level	
$\overline{WDTOUT}$	1	Output	Open	

3. Operation

The TMP90PM36 is the OTP version of the TMP90CM36 that is replaced an internal ROM from Mask ROM to EPROM.

Refer to the TMP90PM36 except for the functions which are not described in this section.

The following is an explanation of the hardware configuration and operation in relation to the TMP90CM36.

The TMP90PM36 has an MCU mode and a PROM mode.

3.1 MCU Mode

(1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status).

In the MCU mode, the operation is the same as that of TMP90CM36.

(2) Memory Map

Figure 3.1 show the memory map of TMP90PM36 and TMP90CM36.

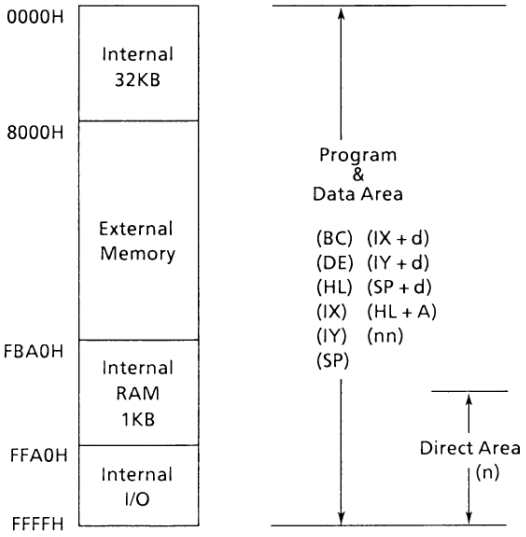


Figure 3.1. TMP90PM36 and TMP90CM36 Memory Map

3.2 PROM Mode

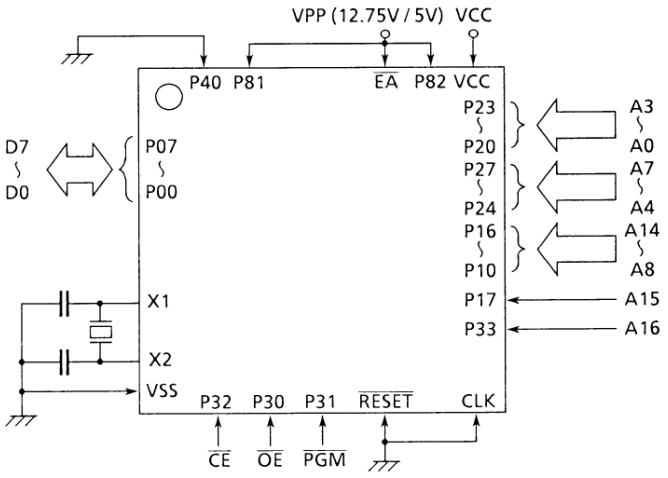
(1) Mode Setting and Function

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the “L” level.

The programming and verification for the internal PROM is acheived by using a general EPROM programmer with the adapter socket. The device selection (ROM Type) should be “TC571000D” with the following conditions.

Size: 1M bit (128K x 8bit), VPP: 12.75V±0.25V, TPW: 0.1ms VCC: 6.25±0.25V

Figure 3.2 shows the setting of pins in PROM mode.



- For other pins, refer to the section on pin function (Table 2.3)
- Use the 10M~16MHz resonator in case of programming and verification by a general EPROM programmer.

Figure 3.2. PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.75V (programming voltage) to the VPP pin when the following pins are set as follows.

(VCC: 6.25V)
($\overline{\text{RESET}}$: "L" level)
(CLK: "L" level)

*These conditions can be obtained by using adapter socket.

After the address and data have been fixed, a data on the Data Bus is programmed when the $\overline{\text{PGM}}$ pin is set to "Low" (0.1ms plus is required).

General programming procedure of an EPROM programmer is as follows.

- Write data to a specified address for 0.1ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

Then, verify the data and increment the address.

The verification for all data is done under the condition of $V_{PP} = V_{CC} = 5V$ after all data were written.

Figure 3.3 shows the programming flowchart.

(3) The Security Bit

The TMP90PM36 has the Security Bit in PROM cell. If the Security Bit is programmed to "0", the content of the PROM is disable to read in PROM mode.

How to program the Security Bit

In the PROM Mode

(1) Connect P40 pin to V_{CC}

(2) Set A0 ~ A16 to "0" respectively

(3) Set the 8-bit data to "FE_H"

(4) Programming Flowchart

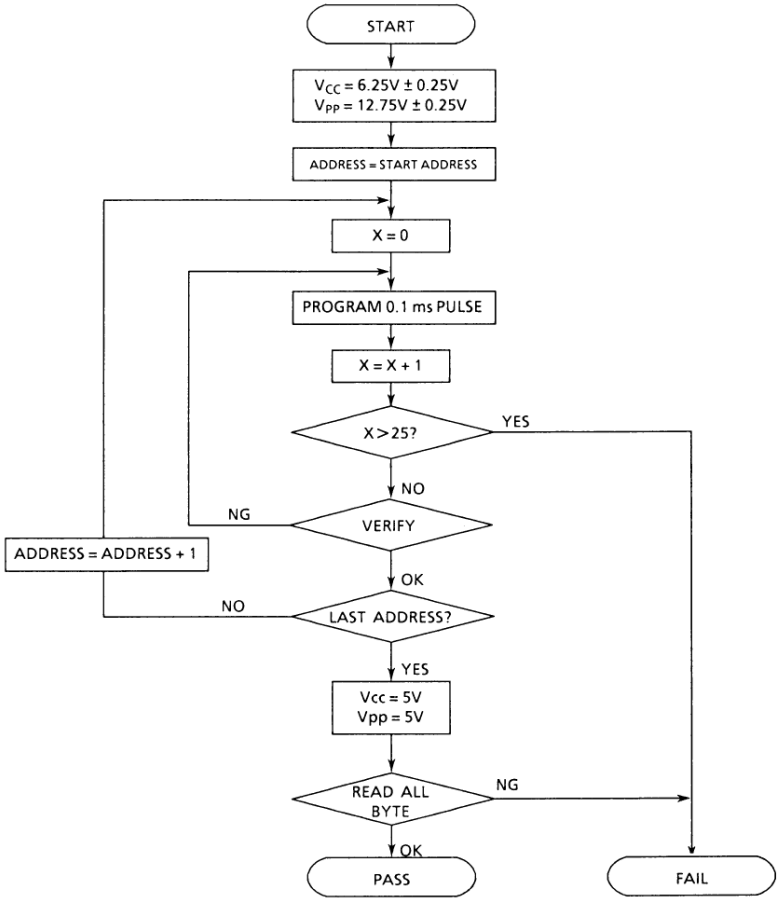


Figure 3.3. Programming Flowchart

4. Electrical Characteristics (Preliminary)

TMP90PM36F/TMP90PM36T

4.1 Absolute Maximum Ratings

Symbol	Item	Rating	Unit
V_{CC}	Power supply voltage	-0.5 ~ + 7	V
V_{IN}	Input voltage	-0.5 ~ V_{CC} + 0.5	V
Σ_{IOL}	Output current (Total)	100	mA
Σ_{IOL}	Output current (Total)	-70	
P_D	Power dissipation (Ta = 85°C)	F 500	mW
		T 600	
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	-65 ~ 150	°C
T_{OPR}	Operating temperature	-40 ~ 85	°C

4.2 DC Characteristics

V_{CC} = 5V ± 10% TA = -20 ~ 70°C (1 ~ 16MHz)
Typical values are for TA = 25°C and Vcc = 5V.

Symbol	Item	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	–
V_{IL1}	P1, P2, P3, P4, P5, P6, P7	-0.3	$0.3V_{CC}$	V	–
V_{IL2}	$\overline{RESET}$, P81 (INT0), P82 ($\overline{STBY}$)	-0.3	$0.25V_{CC}$	V	–
V_{IL3}	$\overline{EA}$	-0.3	0.3	V	–
V_{IL4}	X1	-0.3	$0.2V_{CC}$	V	–
V_{IH}	Input High Voltage (P0)	2.2	V_{CC} + 0.3	V	–
V_{IH1}	P1, P2, P3, P4, P5, P6, P7	$0.7V_{CC}$	V_{CC} + 0.3	V	–
V_{IH2}	$\overline{RESET}$, P81 (INT0), P82 ($\overline{STBY}$)	$0.75V_{CC}$	V_{CC} + 0.3	V	–
V_{IH3}	$\overline{EA}$	V_{CC} -0 .3	V_{CC} + 0.3	V	–
V_{IH4}	X1	$0.8V_{CC}$	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage	–	0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 $0.75V_{CC}$ $0.9V_{CC}$	– – –	V V V	I_{OH} = -400μA I_{OH} = -100μA I_{OH} = -20μA
I_{DAR}	Darlington Drive Current (8 I/O pins max)	-1.0	-3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ Vin ≤ V_{CC}
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
I_{CC}	Operating Current (RUN) Idle	35 (Typ) 1.5 (Typ)	50 5	mA mA	tosc = 16MHz
	STOP (TA = -20 ~ 70°C) STOP (TA = 0 ~ 50°C)	0.2 (Typ)	40 10	μA μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
V_{STOP}	Power Down Voltage (@STOP) (RAM back Up)	2.0	6.0	V	V_{IL2} = $0.2V_{CC}$, V_{IH2} = $0.8V_{CC}$
R_{RST}	$\overline{RESET}$ Pull Up Register	50	150	KΩ	–
CIO	Pin Capacitance	–	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, P81, P82)	0.4	1.0 (Typ)	V	–

4.3 AC Characteristics

V_{CC} = 5V ± 10% TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	Oscillation cycle (= x)	62.5	1000	80	–	62.5	–	ns
t_{CYC}	CLK Period	4x	4x	320	–	250	–	ns
t_{WH}	CLK High width	2x - 40	–	120	–	85	–	ns
t_{WL}	CLK Low width	2x - 40	–	120	–	85	–	ns
t_{AL}	A0 ~ 7 effective address→ALE fall	0.5x - 15	–	25	–	16	–	ns
t_{LA}	ALE fall →A0 ~ 7 hold	0.5x - 15	–	25	–	16	–	ns
t_{LL}	ALE Pulse width	x - 40	–	40	–	23	–	ns
t_{LC}	ALE fall→ $\overline{RD}/\overline{WR}$ fall	0.5x - 30	–	10	–	1	–	ns
t_{CL}	$\overline{RD}/\overline{WR}$ →ALE rise	0.5x - 20	–	20	–	11	–	ns
t_{ACL}	A0 ~ 7 effective address →$\overline{RD}/\overline{WR}$ fall	x - 25	–	55	–	38	–	ns
t_{ACH}	Upper effective address →$\overline{RD}/\overline{WR}$ fall	1.5x - 50	–	70	–	44	–	ns
t_{CA}	$\overline{RD}/\overline{WR}$ fall →Upper address hold	0.5x - 20	–	20	–	11	–	ns
t_{ADL}	A0 ~ 7 effective address →Effective data input	–	3.0x - 35	–	205	–	153	ns
t_{ADH}	Upper effective address →Effective data input	–	3.5x - 55	–	225	–	164	ns
t_{RD}	$\overline{RD}$ fall →Effective data input	–	2.0x - 50	–	110	–	75	ns
t_{RR}	$\overline{RD}$ Pulse width	2.0x - 40	–	120	–	85	–	ns
t_{HR}	$\overline{RD}$ rise →Data hold	0	–	0	–	0	–	ns
t_{RAE}	$\overline{RD}$ rise→ Address enable	x - 15	–	65	–	48	–	ns
t_{WW}	$\overline{WR}$ pulse width	2.0x - 40	–	120	–	85	–	ns
t_{DW}	Effective data→$\overline{WR}$ rise	2.0x - 50	–	110	–	75	–	ns
t_{WD}	$\overline{WR}$ rise→Effective data hold	0.5x - 10	–	30	–	21	–	ns
t_{ACKH}	Upper address→CLK fall	2.5x - 50	–	150	–	106	–	ns
t_{ACKL}	Lower address →CLK fall	2.0x - 50	–	110	–	75	–	ns
t_{CKHA}	CLK fall→Upper address hold	1.5x - 80	–	40	–	13	–	ns
t_{CCK}	$\overline{RD}/\overline{WR}$→CLK fall	x - 25	–	55	–	37	–	ns
t_{CKHC}	CLK fall→$\overline{RD}/\overline{WR}$ rise	x - 60	–	20	–	2	–	ns
t_{DCK}	Valid data CLK fall	x - 50	–	30	–	12	–	ns
t_{CWA}	$\overline{RD}/\overline{WR}$ fall→Valid $\overline{WAIT}$	–	x - 40	–	40	-	22	ns
t_{AWAL}	Lower address →Valid $\overline{WAIT}$	–	2.0x - 70	–	90	-	55	ns
t_{WAH}	CLK fall →Valid $\overline{WAIT}$ hold	0	–	0	–	0	–	ns
t_{AWAH}	Upper address →Valid $\overline{WAIT}$	–	2.5x - 70	-	130	–	86	ns
t_{CPW}	CLK fall →Port Data Output	–	x + 200	-	280	–	262	ns
t_{PRC}	Port Data Input →CLK fall	200	–	200		200	–	ns
t_{CPR}	CLK fall →Port Data hold	100	–	100		100	–	ns

AC Measuring Conditions

- Output level: High 2.2V/Low 0.8V, C_L = 50pF
  (However, CL = 100pF for AD0 ~ 7, A8 ~ 15, ALE, $\overline{RD}$, $\overline{WR}$)
- Input level: High 2.4V/Low 0.45V (AD0 ~ AD7)
  High 0.8V_{CC}/Low 0.2V_{CC} (excluding AD0 ~ AD7)
  High 0.8V_{CC}/Low 0.2V_{CC} (excluding AD0 ~ AD7)

4.4 A/D Conversion Characteristics

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Condition	Min	Max	Unit
V_{REF}	Analog reference voltage	Vcc - 1.5	Vcc	Vcc	V
A_{GND}	Analog reference voltage	Vss	Vss	Vss	
V_{AIN}	Analog input voltage range	Vss	–	Vcc	
IREF	Analog reference voltage power supply current	–	0.5	1.0	mA
Error (Quantize error of ±0.5 LSB not included)	Total error (TA = 25°C, Vcc = V_{REF} = 5.0V)	–	–	1.0	LSB
	Total error	–	–	2.5	

4.5 Timer/Counter Input Clock (TI2, TI4)

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Item	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock cycle	8x + 100	–	740	–	600	–	ns
t_{VCKL}	Low clock pulse width	4x + 40	–	360	–	290	–	ns
t_{VCKH}	High clock pulse width	4x + 40	–	360	–	290	–	ns

4.6 Interrupt Operation

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Item	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	INT0 Low level pulse width 	4x	–	320	–	250	–	ns
t_{INTAH}	INT0 High level pulse width 	4x	–	320	–	250	–	ns
t_{INTBL}	INT1, INT2 Low level pulse width 	8x + 100	–	740	–	600	–	ns
t_{INTBH}	INT1, INT2 High level pulse width 	8x + 100	–	740	–	600	–	ns

4.7 D/A Conversion Characteristics (VCC = 5V, VSS = AVSS = 0V)

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Item	Min	Typ	Max	Unit
–	Analysis ability	–	–	8	Bits
–	Absoluteness accuracy (VCC = AVCC = 5V)	–	–	1.0	%
t_{SU}	Establishment time	–	–	3	μs
R_O	Output resistance	1	2	4	kΩ
V_{AVSS}	Analog power supply voltage	–	0	–	V
V_{DAVREF}	Analog power supply voltage	4	–	V_{CC}	V
I_{DAVREF}	Reference power supply input current	0	2.5	5	mA

4.8 Serial Channel SIO1 Timing - I/O Interface Mode
(1) SCLK1 Input Mode

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Item	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK1 cycle	16x	–	1.28	–	1	–	μs
t_{OSS}	Output data →Rising edge of SCLK	t_{SCY}/2 - 5x - 50	–	190	–	137	–	ns
t_{OHS}	SCLK1 rising edge→Output data hold	5x - 100	–	300	–	212	–	ns
t_{HSR}	SCLK1 rising edge→Input data hold	0	–	0	–	0	–	ns
t_{SRD}	SCLK1 rising edge→ Effective data input	–	t_{SCY} - 5x - 100	–	780	–	587	ns

(2) SCLK1 Output Mode

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16x	8192x	1.28	655.4	1	512	μs
t_{OSS}	Output data setup→SCLK rising edge	t_{SCY} - 2x - 50	–	970	–	725	–	ns
t_{OHS}	SCLK rising edge→Output data hold	2x - 80	–	80	–	45	–	ns
t_{HSR}	SCLK rising edge→Input data hold	0	–	0	–	0	–	ns
t_{SRD}	SCLK rising edge→ Effective data input	–	t_{SCY} - 2x - 150	–	970	–	725	ns

4.9 Serial Channel SIO2 Timing

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Condition	16MHz Clock		Variable		Unit
			Min	Max	Min	Max	
t_{SCR}	Serial port clock cycle time	Internal	500	16000	8x	256x	ns
		External	1000	–	600	–	
t_{SCL}	SCLK2 Low width	Internal	200	300	4x - 50	4x + 50	ns
		External	980	1020	16x - 20	16x + 20	
t_{SCH}	SCLK2 High width	Internal	200	300	4x - 50	4x + 50	ns
		External	980	1020	16x - 20	16x + 20	
t_{SKDO}	SCLK2 → TXD2 (Output data) delay time	Internal	112.5	–	x + 50	–	ns
		External	475	–	6x + 100	–	
t_{SRD}	SCLK2 Rising edge to input data valid	Internal	377.5	–	7x - 60	–	ns
		External	1150	–	20x - 100	–	
t_{HSR}	Input data hold after SCLK2 rising edge	Internal	162.5	–	x - 100	–	ns
		External	475	–	6x + 100	–	

4.10 Read Operation (PROM mode)

DC Characteristic, AC Characteristic

TA = -20 ~ 70°C V_{CC} = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} read voltage	–	4.5	5.5	V
V_{IH1}	Input high voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	0.7 x V_{CC}	V + 0.3	V
V_{IL1}	Input low voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	-0.3	0.3 x V_{CC}	V
t_{ACC}	Address to output delay	C_L = 50pF	2.25TCYC + α	–	ns

TCYC = 250ns (16MHz Clock)
α = 100ns

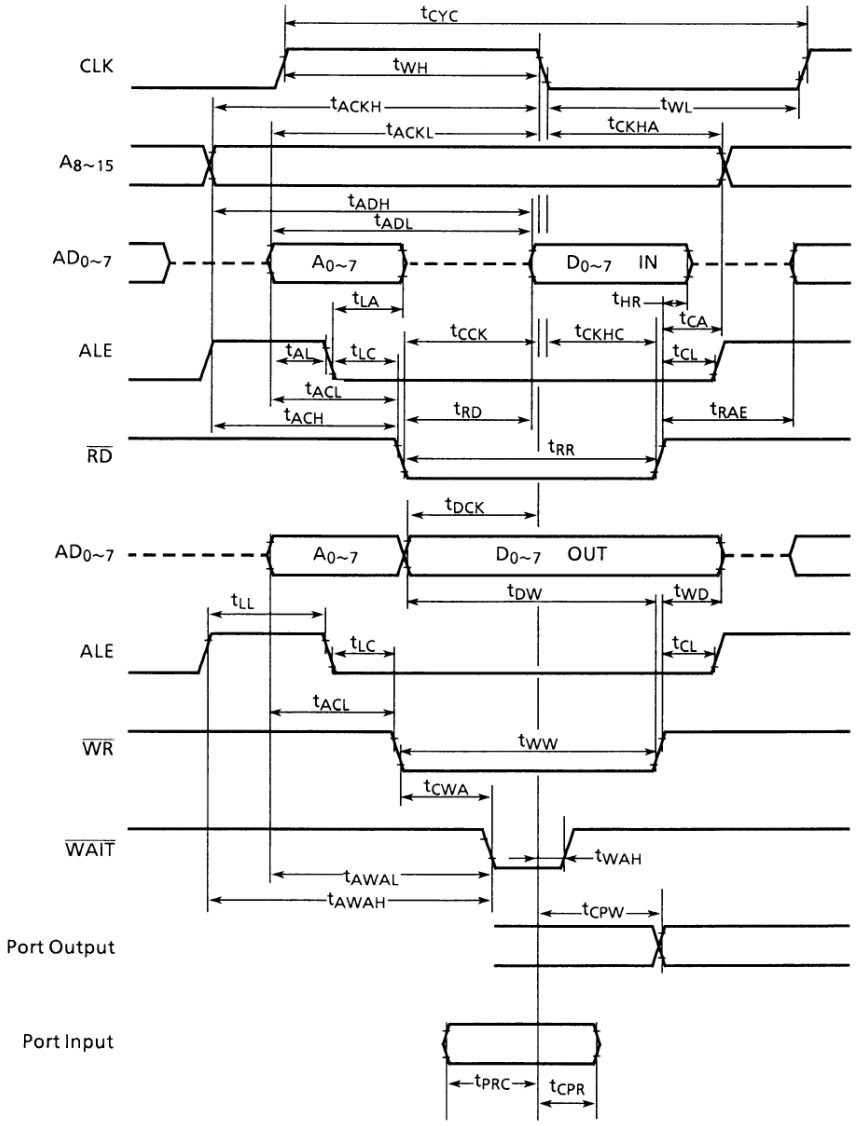
4.11 Read Operation (PROM mode)

DC Characteristic, AC Characteristic

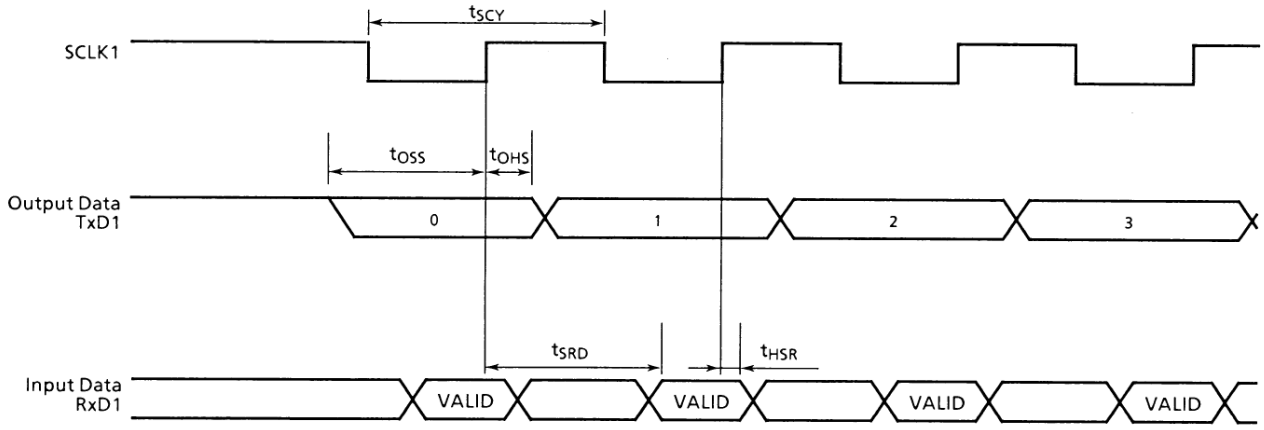
TA = 25±5°C V_{CC} = 6.25V ± 0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programming Algorithm	–	12.50	12.75	13.00	V
V_{IH}	Input high voltage (D0 ~ D7)	–	0.2V_{CC} + 1.1		V_{CC} + 0.3	V
V_{IL}	Input low voltage (D0 ~ D7)	–	-0.3		0.2V_{CC} - 0.1	V
V_{PP}	Input high voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	0.7V_{CC}		V_{CC} + 0.3	V
V_{IH}	Input low voltage (A0 ~ A15, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	-0.3		0.3V_{CC}	V
V_{IL}	V_{CC} supply current	t_{OSC} = 12.75MHz	–		50	mA
V_{IL}	V_{PP} supply current	V_{PP} = 13.00V	–		50	mA
t_{PW}	CE program pulse width	C_L = 50pF	0.095	0.1	0.105	ms

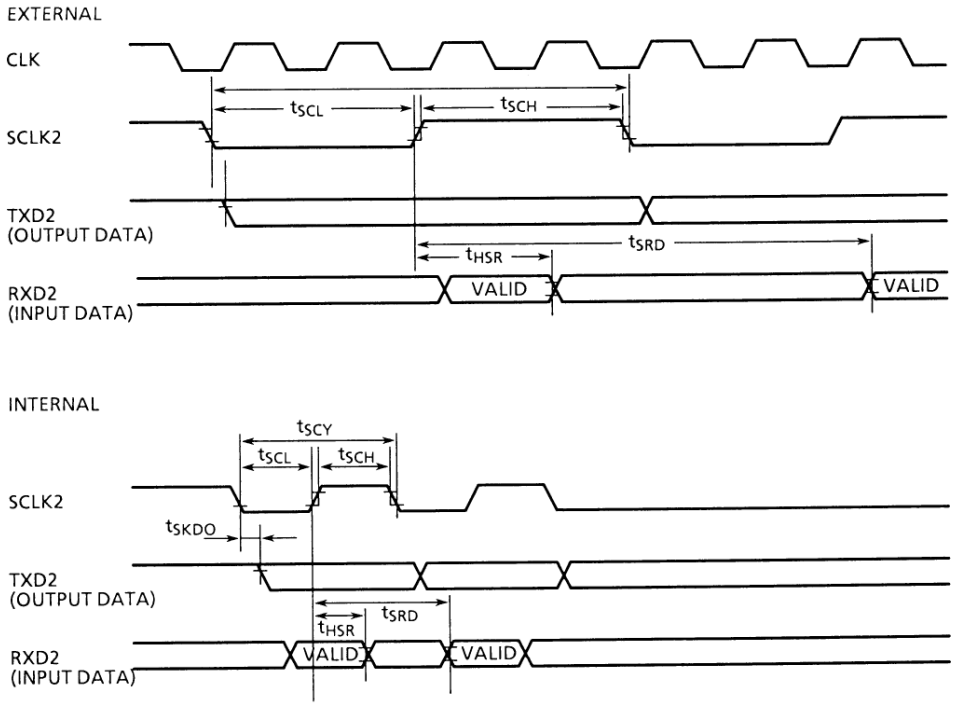
4.12 Timing Chart



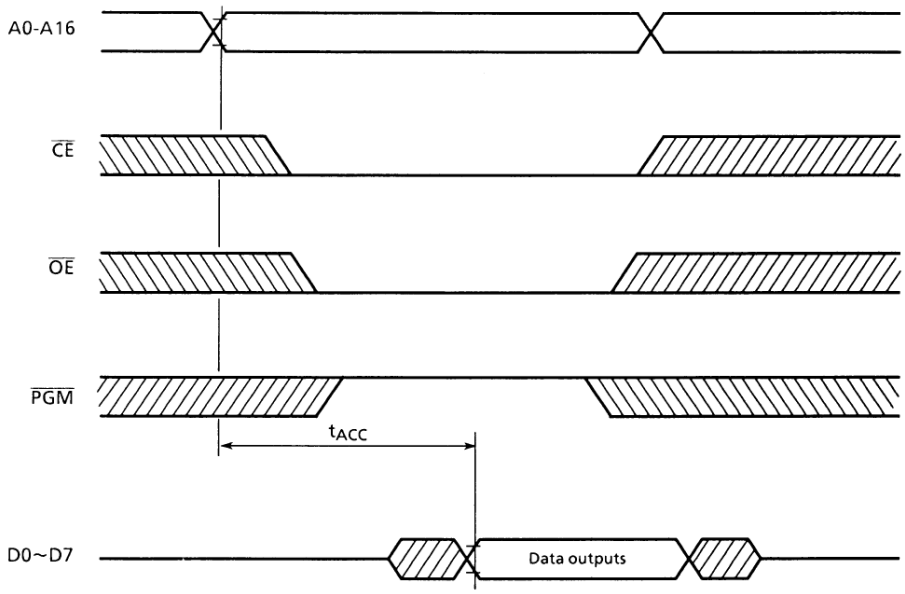
4.13 Serial Channel SIO1 I/O Interface Mode Timing Chart



4.14 Serial Channel SIO2 Timing Chart

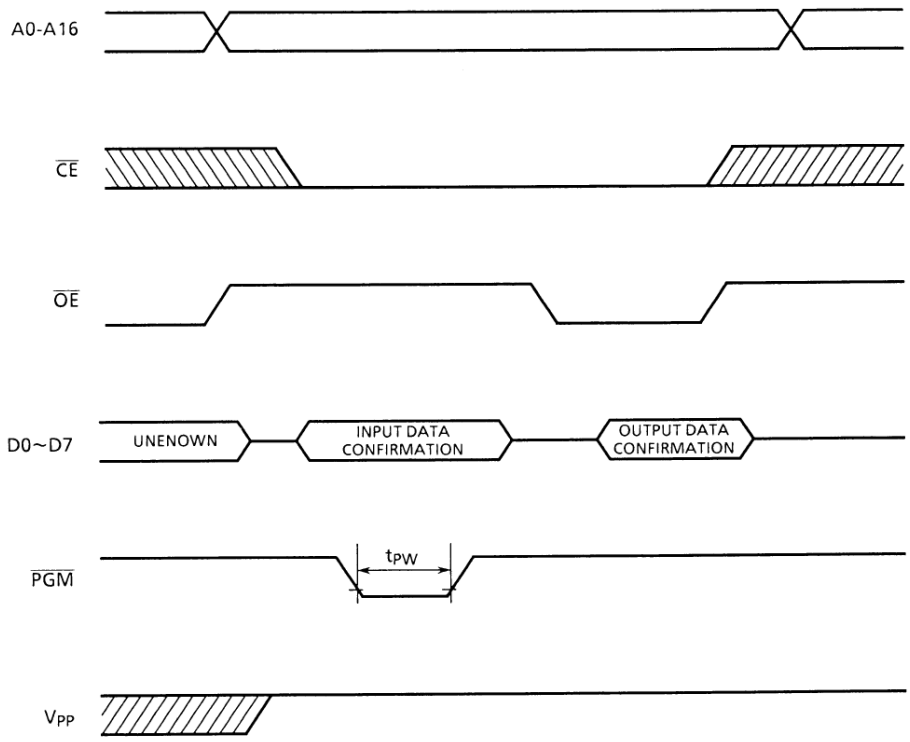


4.15 Read Operation Timing Chart (PROM mode)



4.16 Program OperationTiming Chart (PROM mode)

High Speed Program Formula



Note 1. Force V_{PP} (12.75V) power supply and V_{CC} power supply at the same time, or V_{PP} (12.75V) power supply later than V_{CC} power supply. And interrupt V_{PP} (12.75V) power supply and V_{CC} power supply at the same time, or V_{PP} (12.75V) power supply before V_{CC} power supply.

2. Please attend to drawing and rising in the programming (mode) in 12.75V to the V_{PP} as there is some possibility that you give "DAMAGE" to the devices.

3. Don't force more than 14V (voltage) including over shoot to the V_{PP} pin in the programming as maximum rating of V_{PP} pin is 14V (voltage).